IO LINK/BREAKOUT BOARD

TMDS64DC01EVM/TMDS243DC01EVM

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REV	A
VER	1.0

Designed for TI by Mistral Solutions Pvt Ltd

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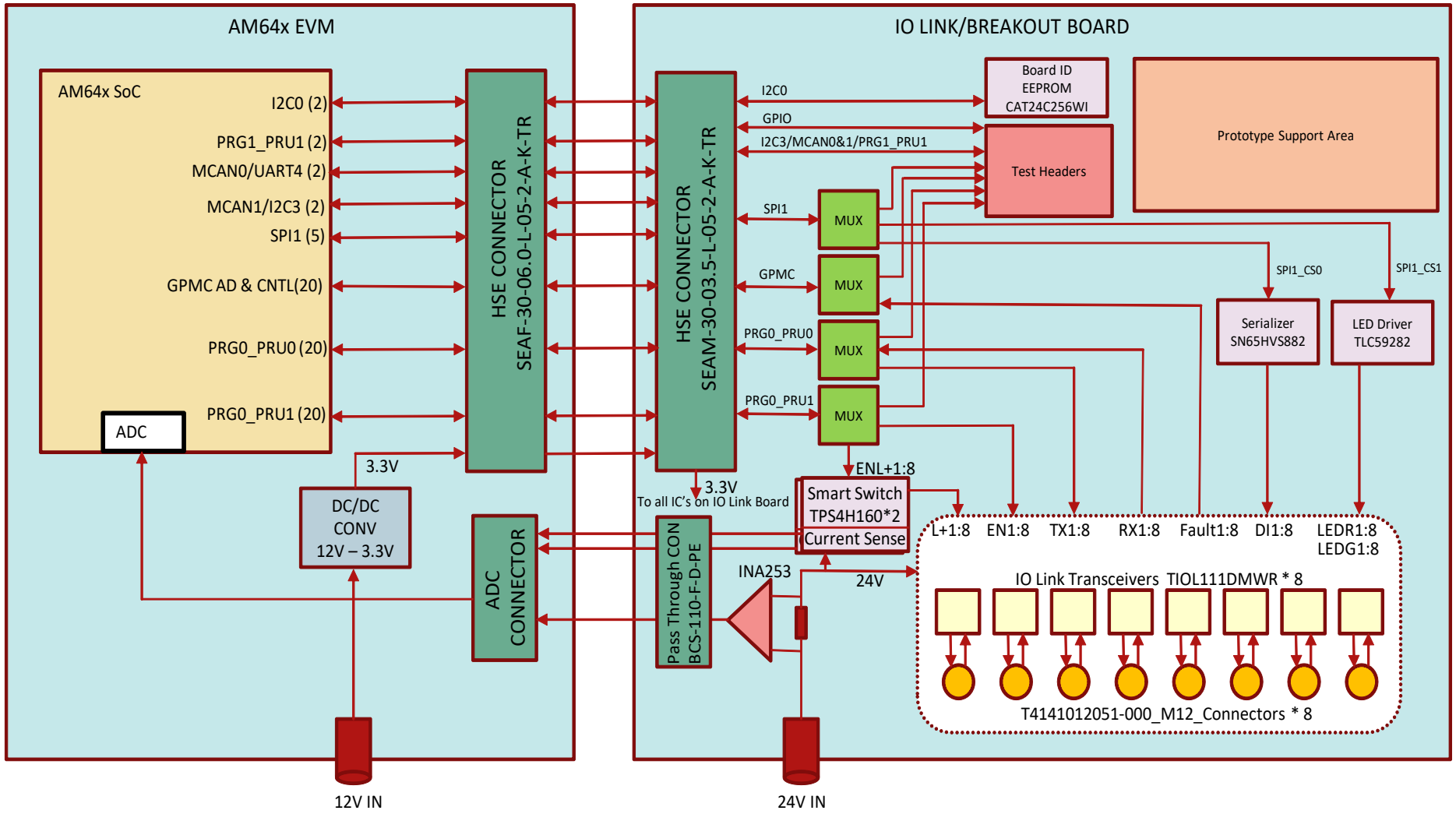
REVISION HISTORY

REV #	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
A	0.1	09-06-2021	Schmeatic Imported from REV E1	Mistral Design Team	RAKESH RAJDEV	AJIT MB
A	1.0	09-06-2021	Added Diode at Base of transistor for Voltage Spike Protection on TX line of IO Link PHY Changed Resistors R78 R79 R84 R85 R90 R91 R96 R97 to 240E Baselined	Mistral Design Team	RAKESH RAJDEV	AJIT MB

BLOCK DIAGRAM



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Title	BLOCK DIAGRAM	
Size: C	Variant Name = PROC102A(002) TMDS243DC01EVM	Rev: E1
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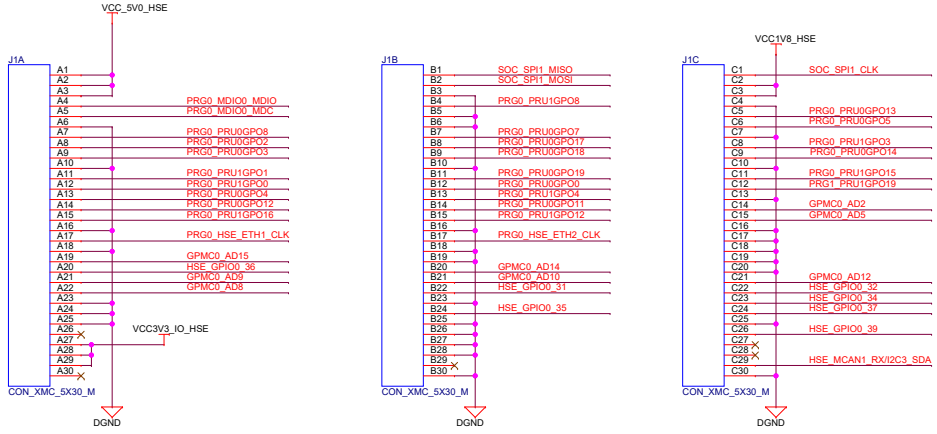
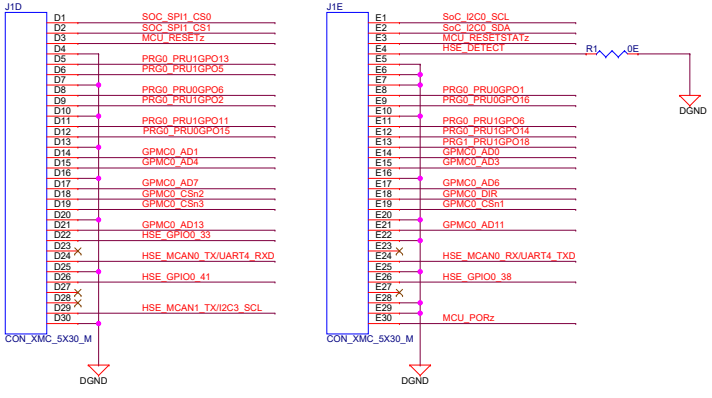
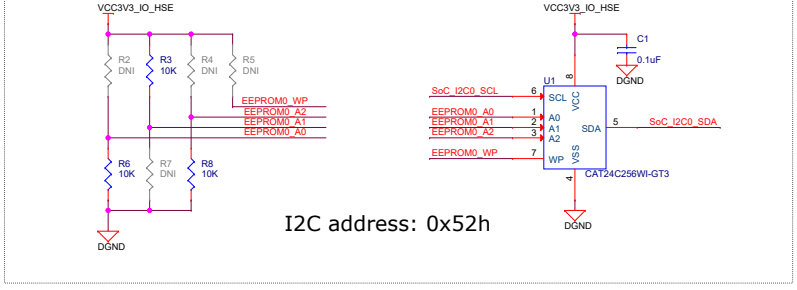
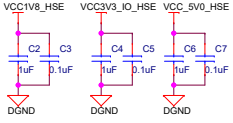
HSE CONNECTOR









Off Page Connections

PRG0_PRU0GPO0 — PRG0_PRU0GPO0
PRG0_PRU0GPO1 — PRG0_PRU0GPO1
PRG0_PRU0GPO2 — PRG0_PRU0GPO2
PRG0_PRU0GPO3 — PRG0_PRU0GPO3
PRG0_PRU0GPO4 — PRG0_PRU0GPO4
PRG0_PRU0GPO5 — PRG0_PRU0GPO5
PRG0_PRU0GPO6 — PRG0_PRU0GPO6
PRG0_PRU0GPO7 — PRG0_PRU0GPO7
PRG0_PRU0GPO8 — PRG0_PRU0GPO8

PRG0_PRU0GPO11 — PRG0_PRU0GPO11
PRG0_PRU0GPO12 — PRG0_PRU0GPO12
PRG0_PRU0GPO13 — PRG0_PRU0GPO13
PRG0_PRU0GPO14 — PRG0_PRU0GPO14
PRG0_PRU0GPO15 — PRG0_PRU0GPO15
PRG0_PRU0GPO16 — PRG0_PRU0GPO16
PRG0_PRU0GPO17 — PRG0_PRU0GPO17
PRG0_PRU0GPO18 — PRG0_PRU0GPO18
PRG0_PRU0GPO19 — PRG0_PRU0GPO19

PRG0_PRU1GPO0 — PRG0_PRU1GPO0
PRG0_PRU1GPO1 — PRG0_PRU1GPO1
PRG0_PRU1GPO2 — PRG0_PRU1GPO2
PRG0_PRU1GPO3 — PRG0_PRU1GPO3
PRG0_PRU1GPO4 — PRG0_PRU1GPO4
PRG0_PRU1GPO5 — PRG0_PRU1GPO5
PRG0_PRU1GPO6 — PRG0_PRU1GPO6

PRG0_PRU1GPO8 — PRG0_PRU1GPO8
PRG0_PRU1GPO11 — PRG0_PRU1GPO11
PRG0_PRU1GPO12 — PRG0_PRU1GPO12
PRG0_PRU1GPO13 — PRG0_PRU1GPO13
PRG0_PRU1GPO14 — PRG0_PRU1GPO14
PRG0_PRU1GPO15 — PRG0_PRU1GPO15
PRG0_PRU1GPO16 — PRG0_PRU1GPO16

GPMC0_AD0 — GPMC0_AD0
GPMC0_AD1 — GPMC0_AD1
GPMC0_AD2 — GPMC0_AD2
GPMC0_AD3 — GPMC0_AD3
GPMC0_AD4 — GPMC0_AD4
GPMC0_AD5 — GPMC0_AD5
GPMC0_AD6 — GPMC0_AD6
GPMC0_AD7 — GPMC0_AD7
GPMC0_AD8 — GPMC0_AD8
GPMC0_AD9 — GPMC0_AD9
GPMC0_AD10 — GPMC0_AD10
GPMC0_AD11 — GPMC0_AD11
GPMC0_AD12 — GPMC0_AD12
GPMC0_AD13 — GPMC0_AD13
GPMC0_AD14 — GPMC0_AD14
GPMC0_AD15 — GPMC0_AD15

GPMC0_CSn2 — GPMC0_CSn2
GPMC0_CSn3 — GPMC0_CSn3
GPMC0_CSn1 — GPMC0_CSn1
GPMC0_DIR — GPMC0_DIR

HSE_GPIO0_31 — HSE_GPIO0_31
HSE_GPIO0_32 — HSE_GPIO0_32
HSE_GPIO0_33 — HSE_GPIO0_33
HSE_GPIO0_34 — HSE_GPIO0_34
HSE_GPIO0_35 — HSE_GPIO0_35
HSE_GPIO0_36 — HSE_GPIO0_36
HSE_GPIO0_37 — HSE_GPIO0_37
HSE_GPIO0_38 — HSE_GPIO0_38
HSE_GPIO0_39 — HSE_GPIO0_39
HSE_GPIO0_41 — HSE_GPIO0_41

PRG0_MDIO0_MDIO — PRG0_MDIO0_MDIO
PRG0_MDIO0_MDC — PRG0_MDIO0_MDC

HSE_MCAN0_TX/UART4_RXD — HSE_MCAN0_TX/UART4_RXD
HSE_MCAN0_RX/UART4_TXD — HSE_MCAN0_RX/UART4_TXD
HSE_MCAN1_TX/I2C3_SCL — HSE_MCAN1_TX/I2C3_SCL
HSE_MCAN1_RX/I2C3_SDA — HSE_MCAN1_RX/I2C3_SDA

SOC_SPI1_MISO — SOC_SPI1_MISO
SOC_SPI1_CLK — SOC_SPI1_CLK
SOC_SPI1_CS0 — SOC_SPI1_CS0
SOC_SPI1_CS1 — SOC_SPI1_CS1
SOC_SPI1_MOSI — SOC_SPI1_MOSI
MCU_RESETz — MCU_RESETz
MCU_RESETSTATz — MCU_RESETSTATz
MCU_PORz — MCU_PORz
PRG0_HSE_ETH2_CLK — PRG0_HSE_ETH2_CLK
PRG0_HSE_ETH1_CLK — PRG0_HSE_ETH1_CLK
PRG1_PRU1GPO19 — PRG1_PRU1GPO19
PRG1_PRU1GPO18 — PRG1_PRU1GPO18

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Size	Variant Name = PROC102A(002) TMDS243DC01EVM	Rev
C		E1
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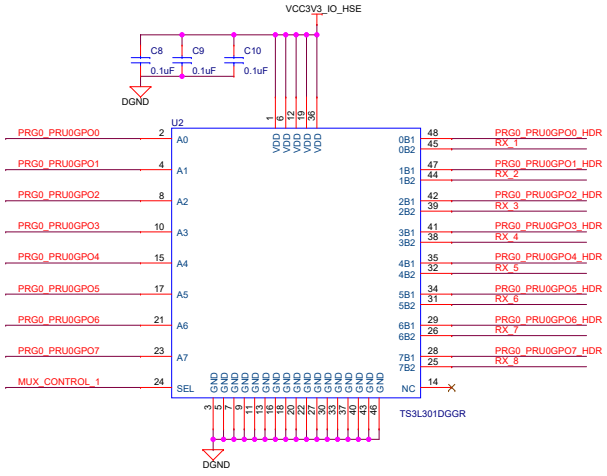
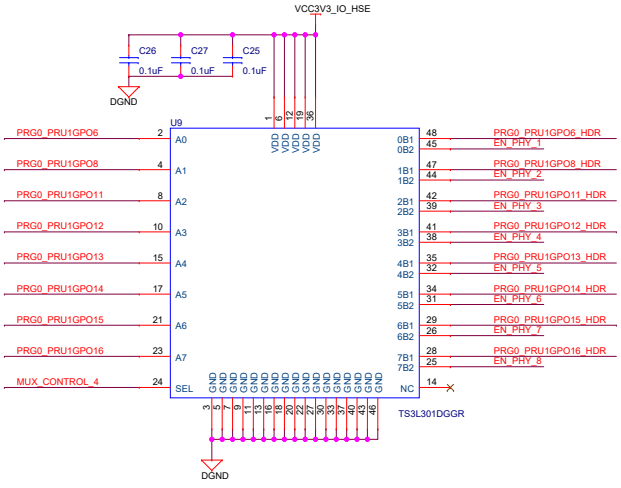
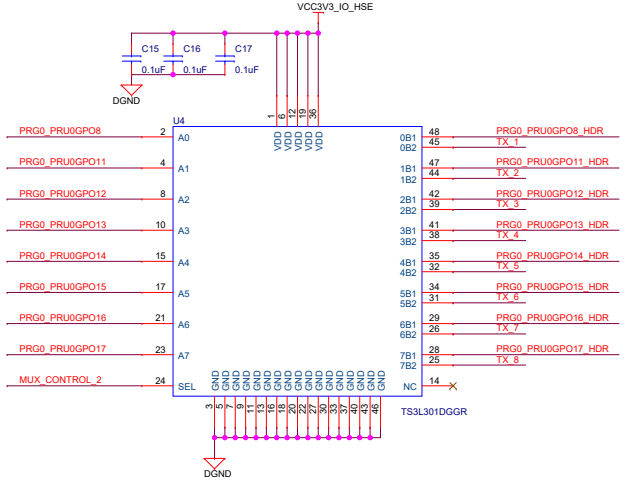
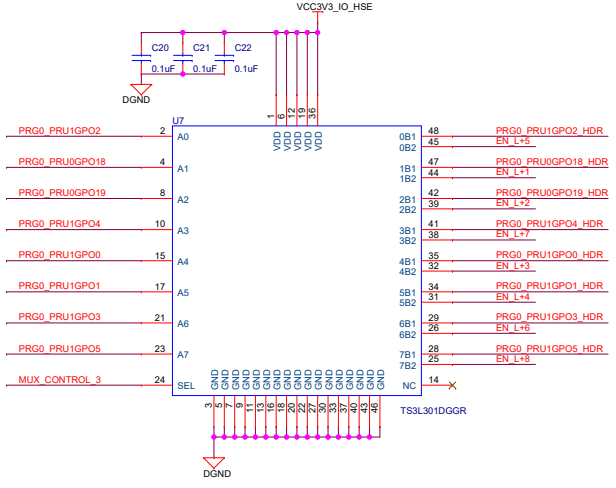
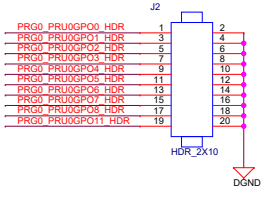
PRG SIGNALS

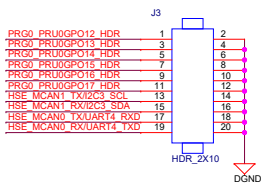


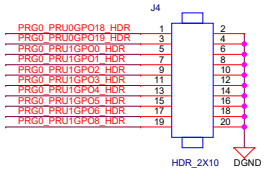


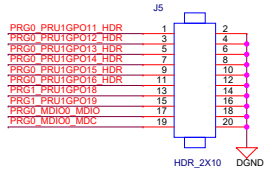












Off Page Connections

PRG0_PRU0GPO0 PRG0_PRU0GPO1 PRG0_PRU0GPO2 PRG0_PRU0GPO3 PRG0_PRU0GPO4 PRG0_PRU0GPO5 PRG0_PRU0GPO6 PRG0_PRU0GPO7

PRG0_PRU0GPO8 PRG0_PRU0GPO11 PRG0_PRU0GPO12 PRG0_PRU0GPO13 PRG0_PRU0GPO14 PRG0_PRU0GPO15 PRG0_PRU0GPO16 PRG0_PRU0GPO17

PRG0_PRU0GPO18 PRG0_PRU0GPO19 PRG0_PRU1GPO0 PRG0_PRU1GPO1 PRG0_PRU1GPO2 PRG0_PRU1GPO3 PRG0_PRU1GPO4 PRG0_PRU1GPO5

PRG0_PRU1GPO6 PRG0_PRU1GPO8 PRG0_PRU1GPO11 PRG0_PRU1GPO12 PRG0_PRU1GPO13 PRG0_PRU1GPO14 PRG0_PRU1GPO15 PRG0_PRU1GPO16

PRG0_MDIO0_MDIO PRG0_MDIO0_MDC PRG1_PRU1GPO18 PRG1_PRU1GPO19

HSE_MCAN1_RX/I2C3_SDA HSE_MCAN1_TX/I2C3_SCL HSE_MCAN0_TX/UART4_RXD HSE_MCAN0_RX/UART4_TXD

RX_1 RX_2 RX_3 RX_4 RX_5 RX_6 RX_7 RX_8

TX_1 TX_2 TX_3 TX_4 TX_5 TX_6 TX_7 TX_8

EN_L+1 EN_L+2 EN_L+3 EN_L+4 EN_L+5 EN_L+6 EN_L+7 EN_L+8

EN_PHY_1 EN_PHY_2 EN_PHY_3 EN_PHY_4 EN_PHY_5 EN_PHY_6 EN_PHY_7 EN_PHY_8

MUX_CONTROL_1 MUX_CONTROL_2 MUX_CONTROL_3 MUX_CONTROL_4

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Size C	Variant Name = PROC102A(002) TMDS243DC01EVM	Rev E1
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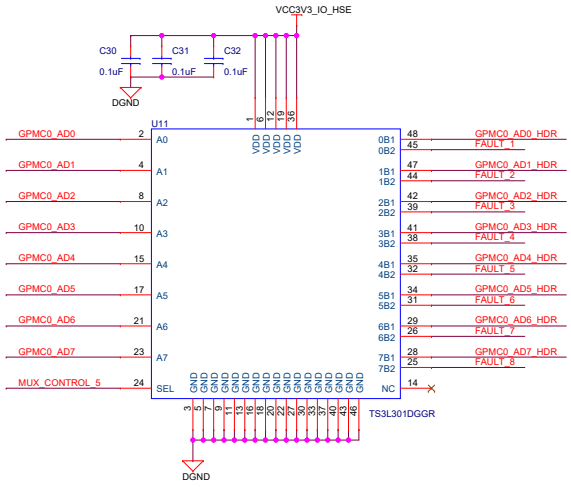
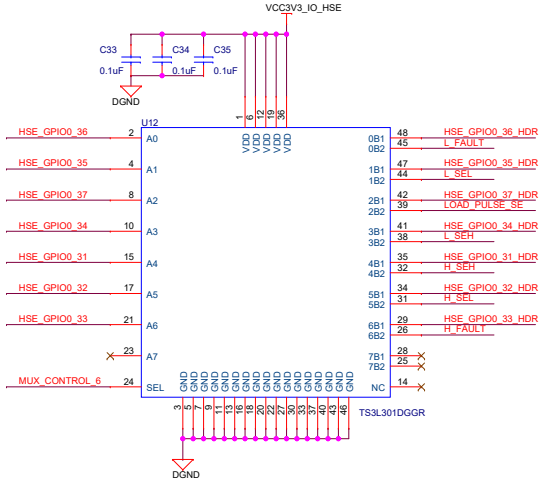
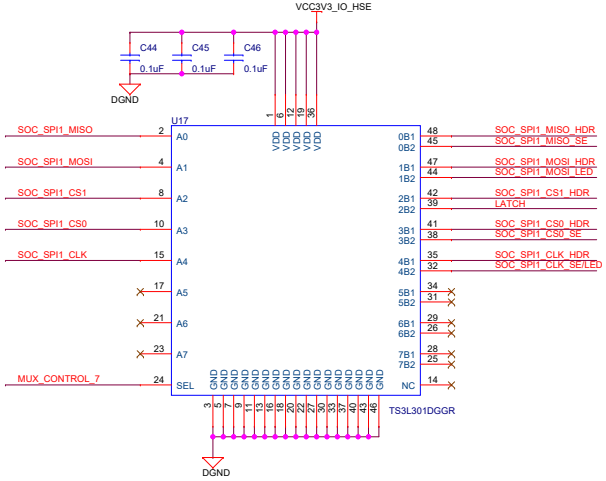
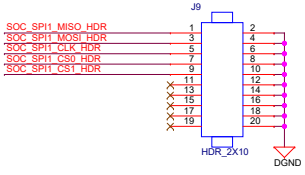
GPMC SIGNALS

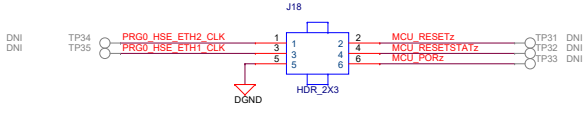


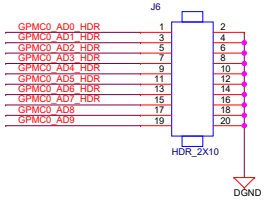


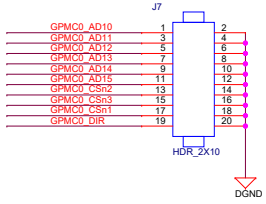
PERIPHERAL_COMMUNICATION_SIGNALS

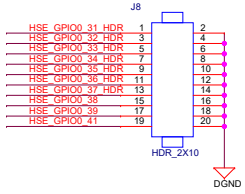












Off Page Connections

GPMC0_AD0 GPMC0_AD1 GPMC0_AD2 GPMC0_AD3 GPMC0_AD4 GPMC0_AD5 GPMC0_AD6 GPMC0_AD7 GPMC0_AD8 GPMC0_AD9 GPMC0_AD10 GPMC0_AD11 GPMC0_AD12 GPMC0_AD13 GPMC0_AD14 GPMC0_AD15

GPMC0_CSn2 GPMC0_CSn3 GPMC0_CSn1 GPMC0_DIR

FAULT_1 FAULT_2 FAULT_3 FAULT_4 FAULT_5 FAULT_6 FAULT_7 FAULT_8

MUX_CONTROL_5 MUX_CONTROL_6 MUX_CONTROL_7

LOAD_PULSE_SE H_SEH H_SEL H_FAULT L_SEH L_SEL L_FAULT

SOC_SPI1_MOSI SOC_SPI1_MISO SOC_SPI1_CLK SOC_SPI1_CS0 SOC_SPI1_CS1

SOC_SPI1_MISO_SE SOC_SPI1_CS0_SE LOAD_PULSE_SE LATCH SOC_SPI1_MOSI_LED SOC_SPI1_CLK_SE/LED

HSE_GPIO0_31 HSE_GPIO0_32 HSE_GPIO0_33 HSE_GPIO0_34 HSE_GPIO0_35 HSE_GPIO0_36 HSE_GPIO0_37 HSE_GPIO0_38 HSE_GPIO0_39 HSE_GPIO0_41

PRG0_HSE_ETH1_CLK PRG0_HSE_ETH2_CLK MCU_RESETz MCU_RESETSTATz MCU_PORz

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Title	GPMC & PERIPHERAL COMMUNICATION SIGNALS	
Size: C	Variant Name = PROC102A(002) TMDS243DC01EVM	Rev: E1
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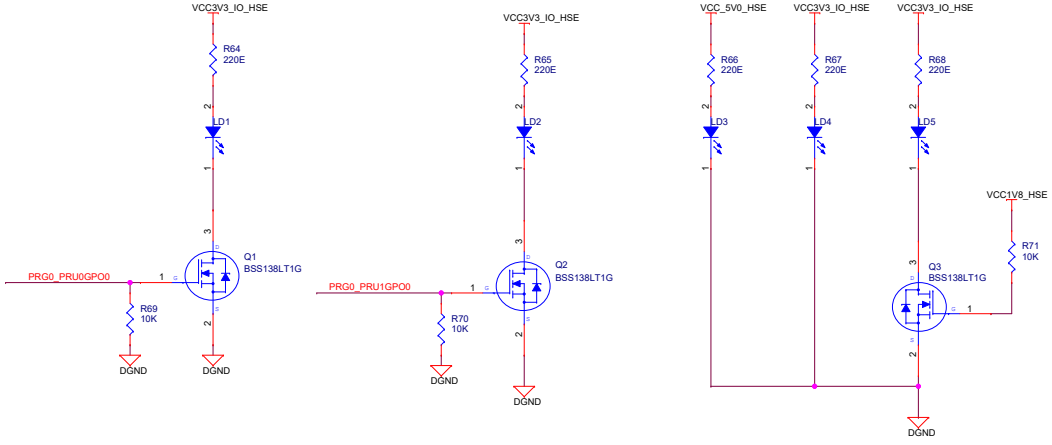
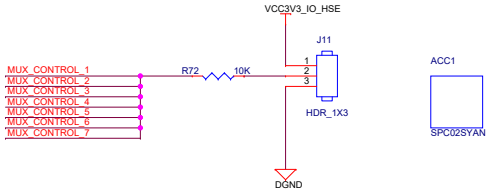
LED'S

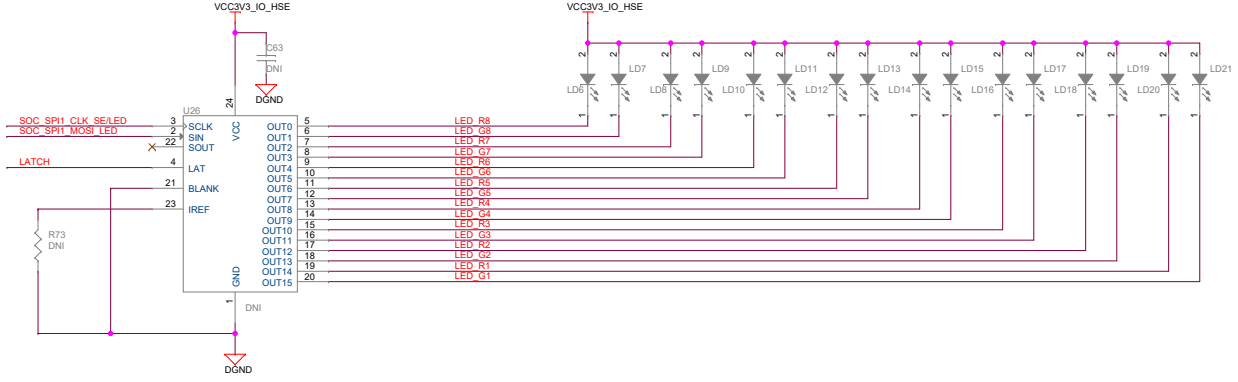
PRG0 & POWER_LED



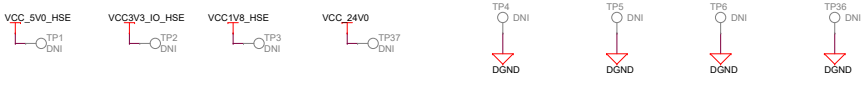
MUX SELECTION



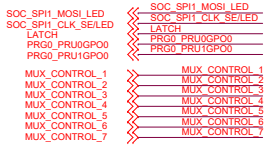
SEL	INPUT/OUTPUT An	FUNCTION	
L	nB1	An=nB1	HEADER SIDE IS ACTIVATED
H	nB2	An=nB2	IO LINK IS ACTIVATED



Test Points



Off Page Connections



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Title	LED	
Size: C	Variant Name = PROC102A(002) TMDS243DC01EVM	Rev: E1
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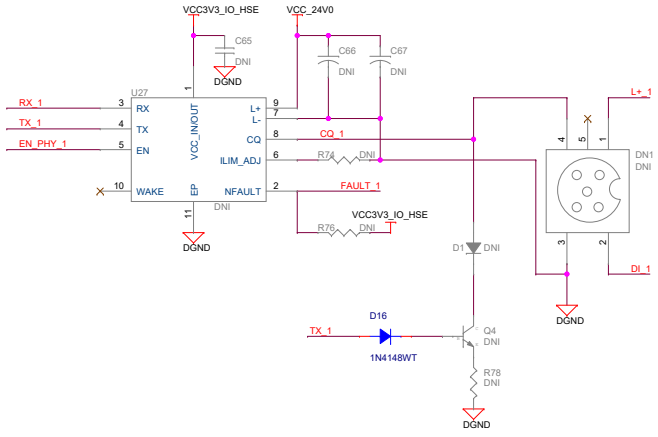
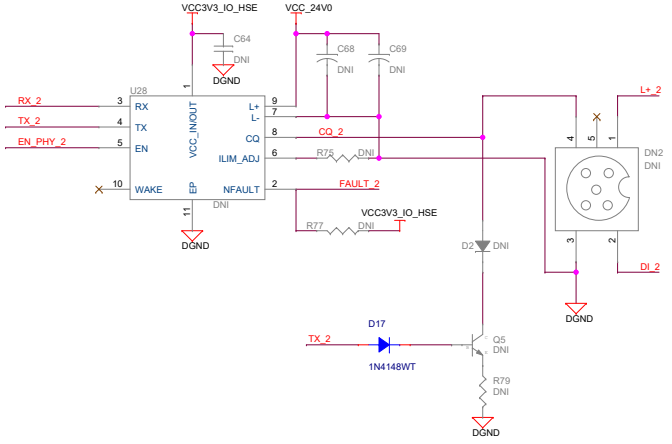
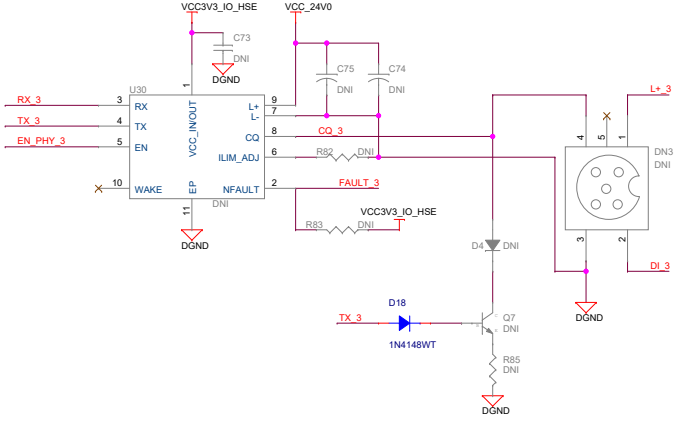
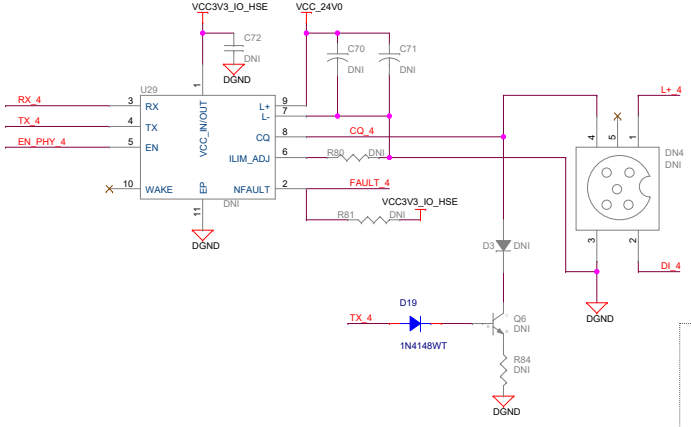
IO LINK TRANCIEVER[1:4]









Off Page Connections

RX_1 RX_2 RX_3 RX_4 TX_1 TX_2 TX_3 TX_4 DI_1 DI_2 DI_3 DI_4 FAULT_1 FAULT_2 FAULT_3 FAULT_4 L+_4 L+_3 L+_1 L+_2 EN_PHY_1 EN_PHY_2 EN_PHY_3 EN_PHY_4

Test Points

TX_1 TX_2 TX_3 TX_4 TP7 TP10 TP13 TP16 RX_1 RX_2 RX_3 RX_4 TP8 TP11 TP14 TP17 EN_PHY_1 EN_PHY_2 EN_PHY_3 EN_PHY_4 TP9 TP12 TP15 TP18

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Size	Variant Name = PROC102A(002) TMDS243DC01EVM	Rev
C		E1
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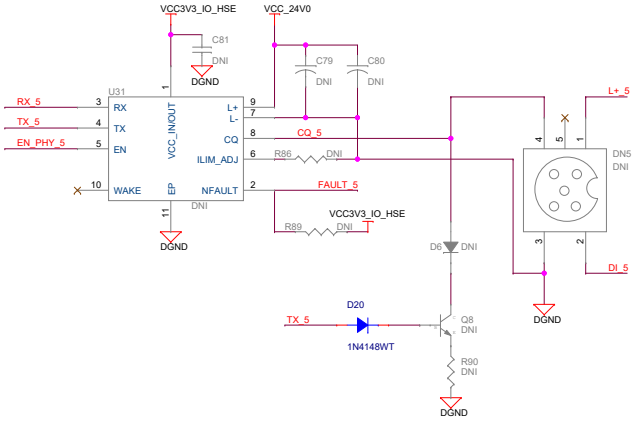
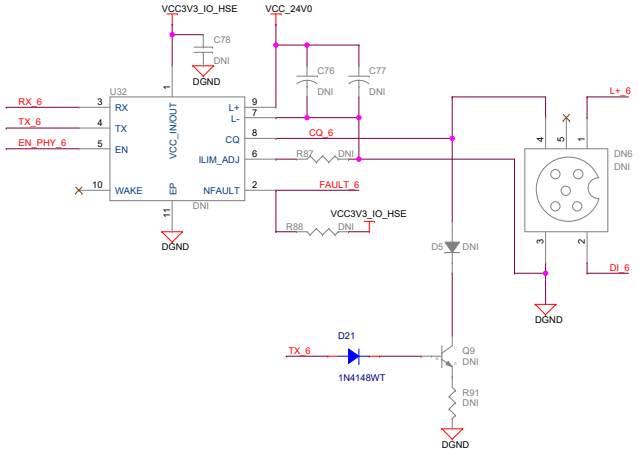
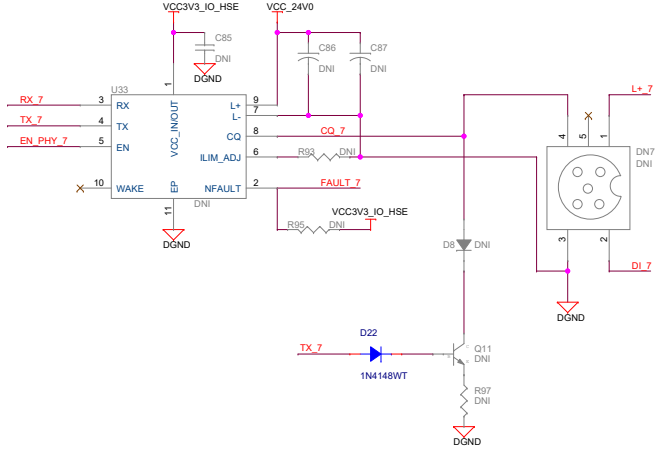
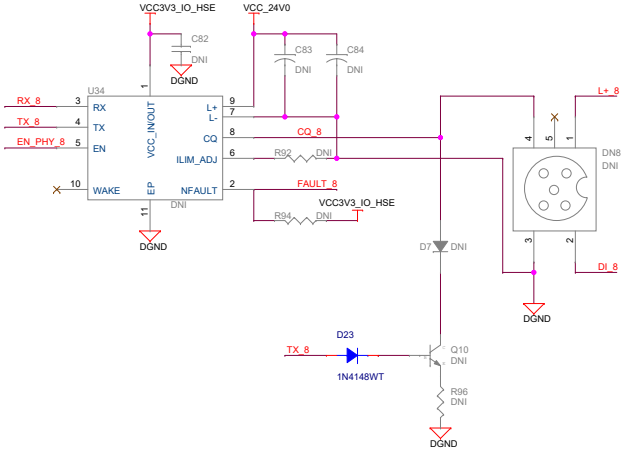
IO LINK TRANCIEVER[5:8]









Off Page Connections

RX_5 RX_5
RX_6 RX_6
RX_7 RX_7
RX_8 RX_8

FAULT_5 FAULT_5
FAULT_6 FAULT_6
FAULT_7 FAULT_7
FAULT_8 FAULT_8

TX_5 TX_5
TX_6 TX_6
TX_7 TX_7
TX_8 TX_8
EN_PHY_5 EN_PHY_5
EN_PHY_6 EN_PHY_6
EN_PHY_7 EN_PHY_7
EN_PHY_8 EN_PHY_8
DI_5 DI_5
DI_6 DI_6
DI_7 DI_7
DI_8 DI_8
L+_8 L+_8
L+_7 L+_7
L+_5 L+_5
L+_6 L+_6

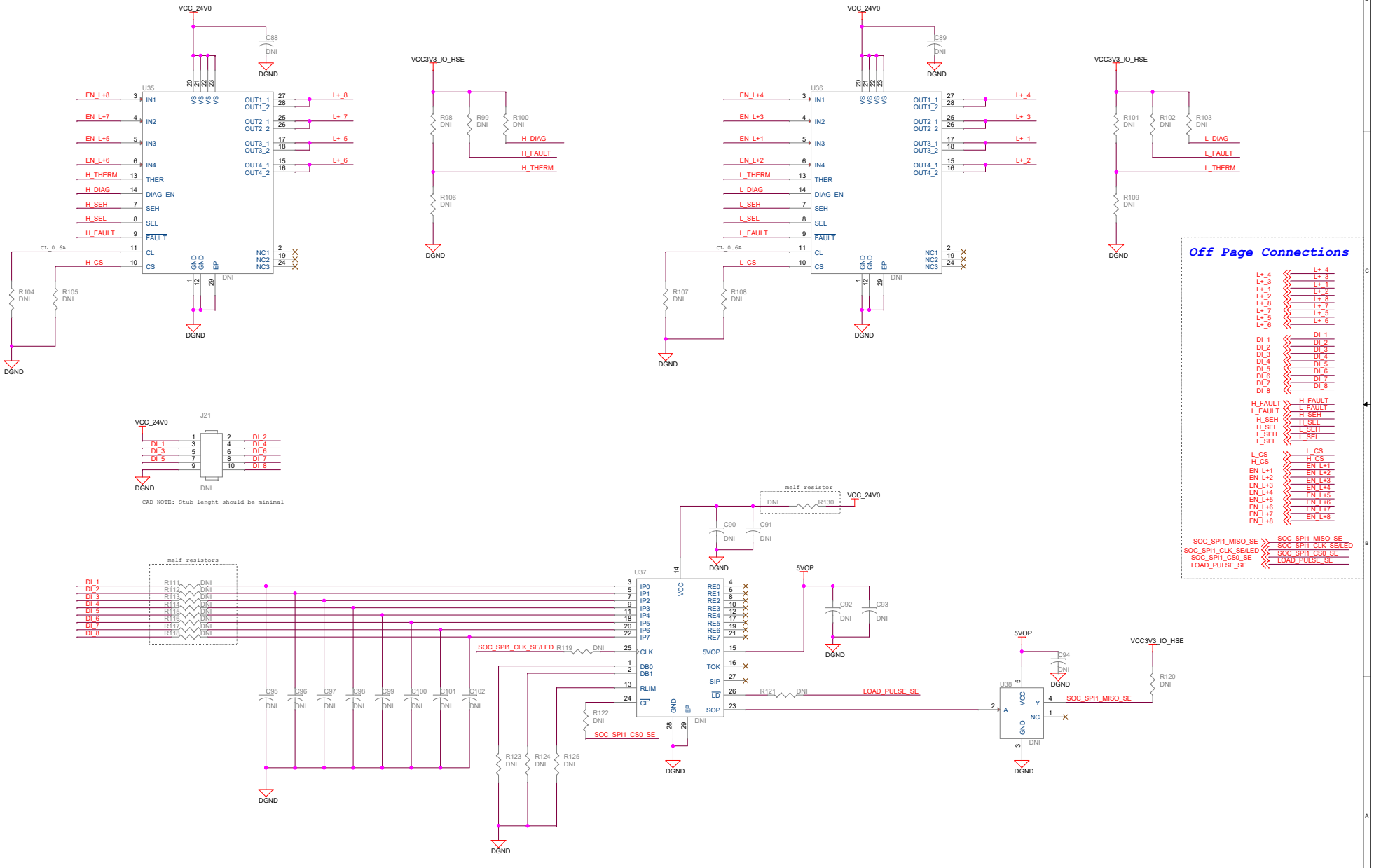
Test Points

TX_5 TP19 RX_5 TP20 EN_PHY_5 TP21
TX_6 TP22 RX_6 TP23 EN_PHY_6 TP24
TX_7 TP25 RX_7 TP26 EN_PHY_7 TP27
TX_8 TP28 RX_8 TP29 EN_PHY_8 TP30

Designed for TI by Mistral Solutions Pvt Ltd

Title	IO LINK TRANCIEVER[5:8]	
Size C	Variant Name = PROC102A(002) TMDS243DC01EVM	Rev E1
Date: Wednesday, June 09, 2021	Sheet 9 of 12	

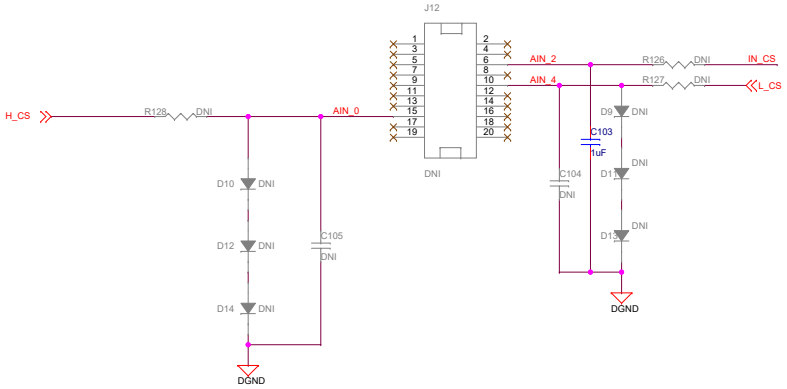
SMART SWITCH

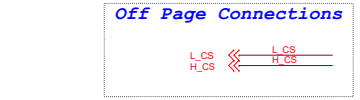


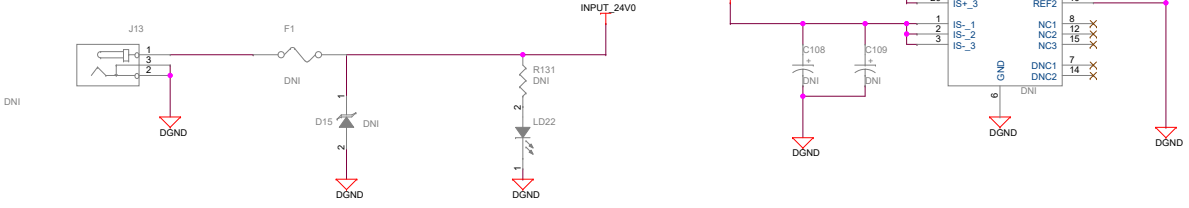
Designed for TI by Mistral Solutions Pvt Ltd

Title	SMART SWITCH	
Size	Variant Name = PROC102A(002) TMDS243DC01EVM	Rev
C		E1
Date:	Wednesday, September 29, 2021	Sheet 10 of 12

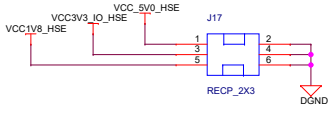
POWER AND ADC SECTION







POWER SUPPLY_HEADER



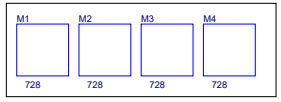
CAD NOTE: PLACE THIS HEADER NEAR PROTOTYPE SUPPORT AREA

Designed for TI by Mistral Solutions Pvt Ltd

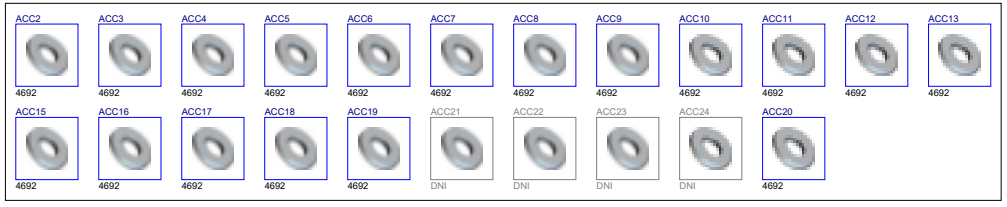
Title	POWER AND ADC SECTION	
Size	Variant Name = PROC102A(002) TMDS243DC01EVM	Rev
C		E1
Date:	Wednesday, September 29, 2021	Sheet 11 of 12

HARDWARE SCHEMATICS

RUBBER FEET



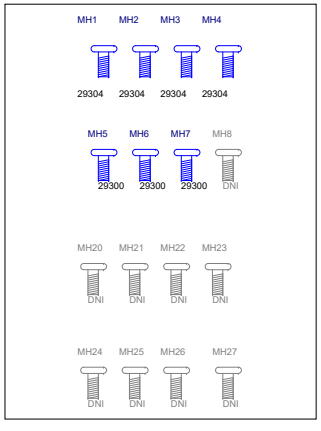
WASHER's



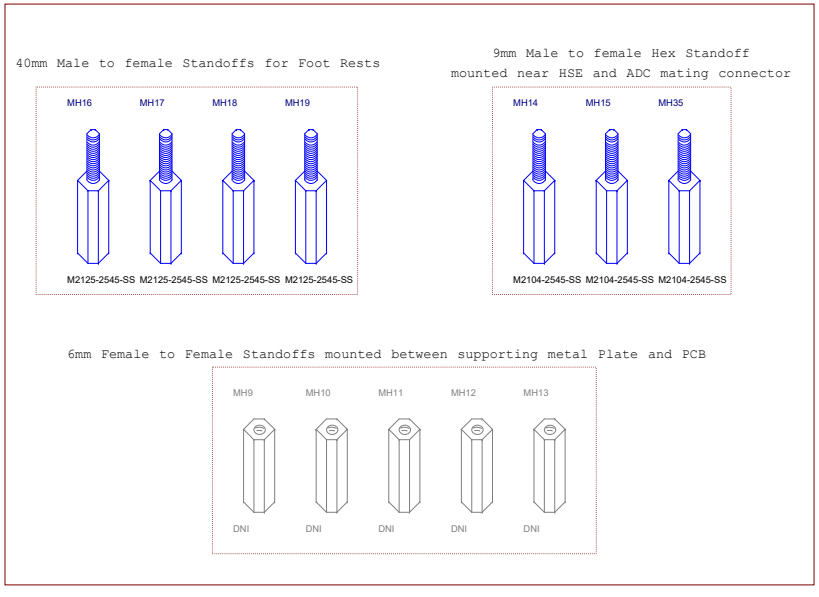
ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

SCREWS



STANDOFFs



LABELS

Board Serial No.

LBL1
PCB LABEL
DNI

ORDERABLE PART NO

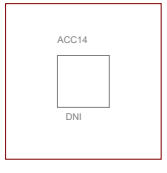
LBL2
PCB LABEL
DNI

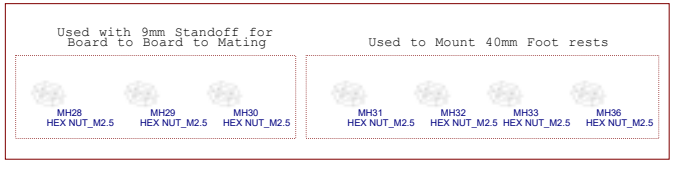
Assembly Revision

LBL3
PCB LABEL
DNI

Orderable part number	
Variant	**Label Text**
001	TMDS64DC01EVM
002	TMDS243DC01EVM

Metal Plate for supporting IO Link M12 Connector





BARE PCB

PROC102
PROC102

Assembled PCB

FIDUCIALS

FID1 DNI
FID2 DNI
FID3 DNI

LOGOs

PCB LOGO DNI
For Evaluation only; not FCC approved for resale

LOGOs

PCB LOGO DNI
Texas Intruments

PCB LOGO DNI
WEEE Mark

PCB LOGO DNI
CE Mark

Designed for TI by Mistral Solutions Pvt Ltd

Title	HARDWARE SCHEMATIC	
Size	Variant Name = PROC102A(002) TMDS243DC01EVM	Rev
C		E1
Date:	Wednesday, September 29, 2021	Sheet 12 of 12