



ABSTRACT

This is a guide for hardware designers creating PCB systems based on the AM263x and AM263Px family of MCU devices. This document serves to integrate device-specific schematic and PCB layout recommendations and hardware design examples from the various AM263x and AM263Px evaluation modules (EVM) such as the LP-AM263 Launchpad™ and TMDSCNCD263P controlCard, with the [AM263x Sitara™ Microcontroller Data Sheet](#), [AM263Px Sitara™ Microcontroller Data Sheet](#), [AM263x Sitara™ Microcontroller Technical Reference Manual](#), [AM263Px Sitara™ Microcontroller Technical Reference Manual](#) and other collateral documents and tools, as shown in [Section 13](#).

Table of Contents

1 Introduction	2
1.1 Acronyms.....	4
2 Power	5
2.1 Discrete DC-DC Power Solution.....	5
2.2 Integrated PMIC Power Solution.....	7
2.3 Power Decoupling and Filtering	8
2.4 Power Consumption.....	12
2.5 Power Distribution Network.....	12
2.6 e-Fuse Power.....	18
3 Clocking	19
3.1 Crystal and Oscillator Input Options.....	19
3.2 Output Clock Generation.....	21
3.3 Crystal Selection and Shunt Capacitance.....	21
3.4 Crystal Placement and Routing.....	21
4 Resets	21
5 Bootstrapping	23
5.1 SOP Signal Implementation.....	23
5.2 OSPI/QSPI Memory Implementation.....	25
5.3 ROM OSPI/QSPI Boot Requirements.....	29
6 JTAG Emulators and Trace	29
7 Multiplexed Peripherals	30
8 Digital Peripherals	31
8.1 General Digital Peripheral Routing Guidelines.....	31
9 Analog Peripherals	31
9.1 General Analog Peripheral Routing Guidelines.....	31
10 Layer Stackup	32
10.1 Key Stackup Features.....	33
11 Vias	34
12 BGA Power Fan-Out and Decoupling Placement	34
12.1 Ground Return.....	35
12.2 1.2 V Core Digital Power.....	36
12.3 3.3 V Digital and Analog Power.....	38
12.4 1.8 V Digital and Analog Power.....	41
13 References	44
Revision History	44

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1 Introduction

The AM263x and AM263Px devices are single, dual or quad-core Arm® Cortex®-R5F based MCUs in the Sitara™ MCU family intended for the industrial and automotive motion control environments. A typical AM263x or AM263Px-based design with a discrete power solution is shown in [Figure 1-1](#). This diagram is excerpted from the AM263x Launchpad (LP-AM263) system block diagram. A typical AM263x- or AM263Px-based design with a PMIC (Power Management Integrated Circuit) based power solution is shown in [Figure 1-2](#). This diagram is excerpted from the AM263Px controlCard (TMDSCNCD263P) system block diagram. As can be seen below, the AM263x and AM263Px devices offer designers a wide range of digital connectivity, control and analog sensor feedback options with multiple power solutions supported.

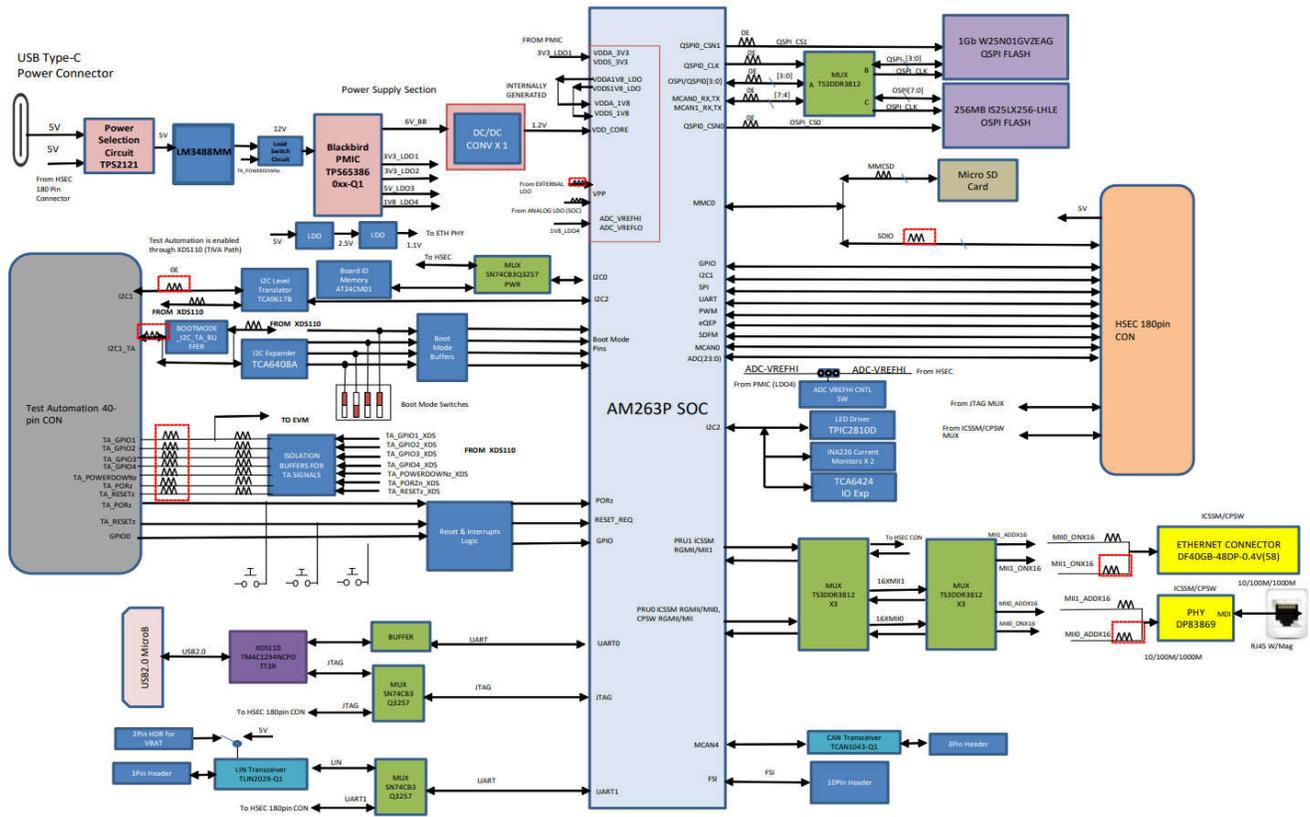


Figure 1-2. Typical AM263x or AM263Px System Block Diagram with PMIC Power (Based on TMDSCNCD263P controlCard Design)

This document should be referenced along with the other key AM263x and AM263Px collateral references. These include:

- The [AM263x Sitara™ Microcontroller Data Sheet \[1111\]](#) and [AM263Px Sitara™ Microcontroller Data Sheet \[4444\]](#) are the primary resources for all device pinout and pin-level multiplexing options.
- The SYSCONFIG [12] pinmux planning tool should be utilizing when starting a new AM263x or AM263Px pinout and driver utilization.
- The [AM263x Sitara™ Microcontroller Technical Reference Manual \[2222\]](#) and [AM263Px Sitara™ Microcontroller Technical Reference Manual \[5555\]](#) document detail each core and peripheral subsystem from a conceptual, usage and programming model perspective.
- The AM263x MCU-SDK [16] ties the data sheet and technical reference manual together with core and peripheral software usage examples.

1.1 Acronyms

Table 1-1. Acronyms Used in This Document

Acronym	Description
EVM	Evaluation Module. Referencing TI PCB assemblies such as the AM263x controlCard (TMDSCNCD263) or AM263x LaunchPad (LP-AM263)
PDN	Power Distribution Network. The active and passive components providing regulated power to a load such as the AM263x MCU power pins.
EMI	Electromagnetic Interference
PI	Power Integrity
SI	Signal Integrity
BOM	Bill of Materials

2 Power

2.1 Discrete DC-DC Power Solution

The AM263x Launchpad and AM263x controlCard EVM designs both integrate a set of buck-converter, DC-DC regulators that may be useful as a reference power solution for some systems. This solution consists of a pair of TPS62913 buck-converter regulators for AM263x MCU core, system digital and analog I/O power, and a set of TPS74801 LDO for powering paired industrial Ethernet PHY.

Current and transient requirements of the DC-DC closed-loop and passive power plane and decoupling network are taken from the power consumption and transient loading tables: [Table 2-3](#) and [Table 2-4](#). Many DC-DC regulators can be matched to fit within these requirements and the maximum power consumption.

It is also recommended to use the power-good generation circuits available on these and similar DC-DC regulators to drive the power on reset (PORz) into the AM263x.

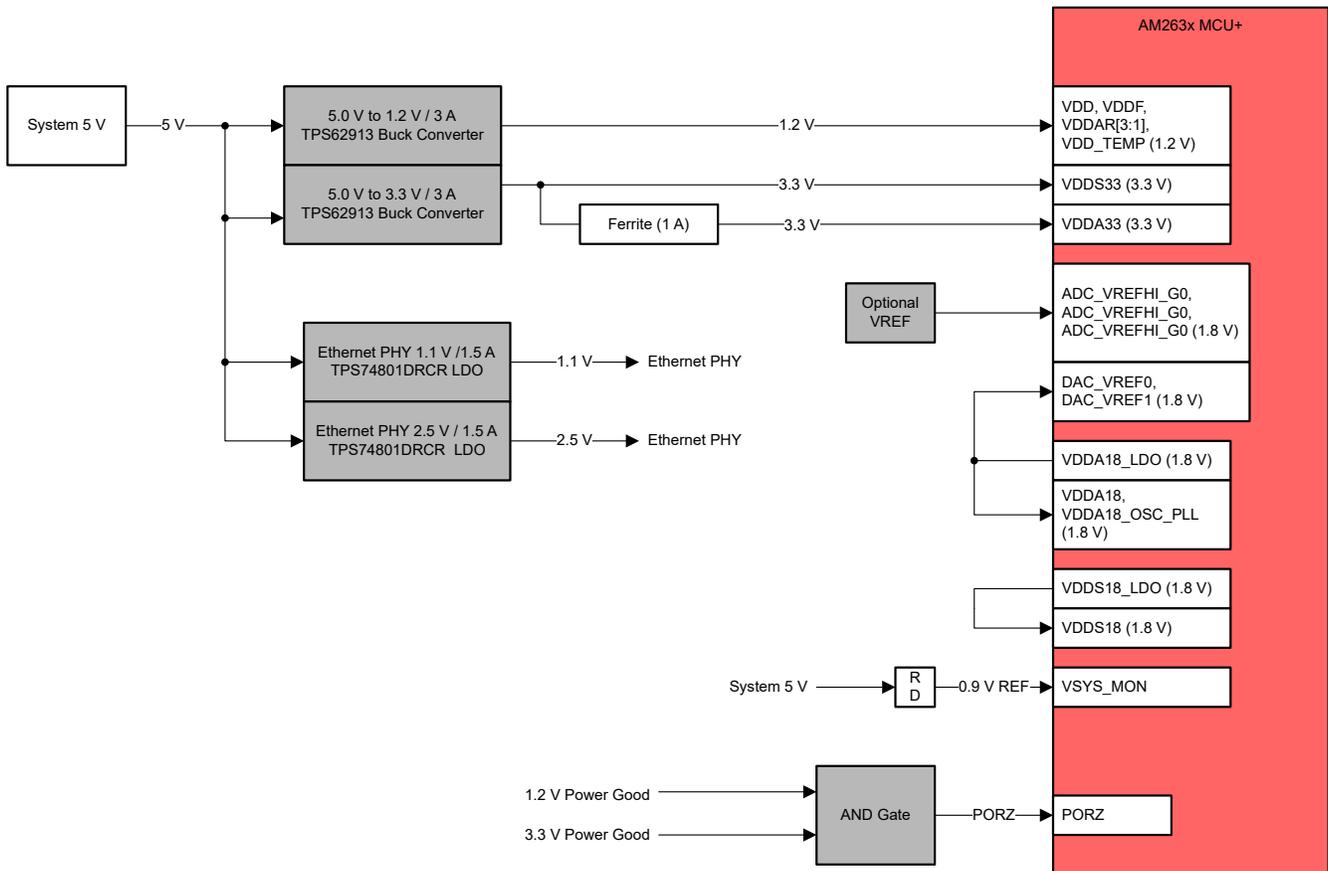


Figure 2-1. AM263x DC-DC Regulator Example Solution

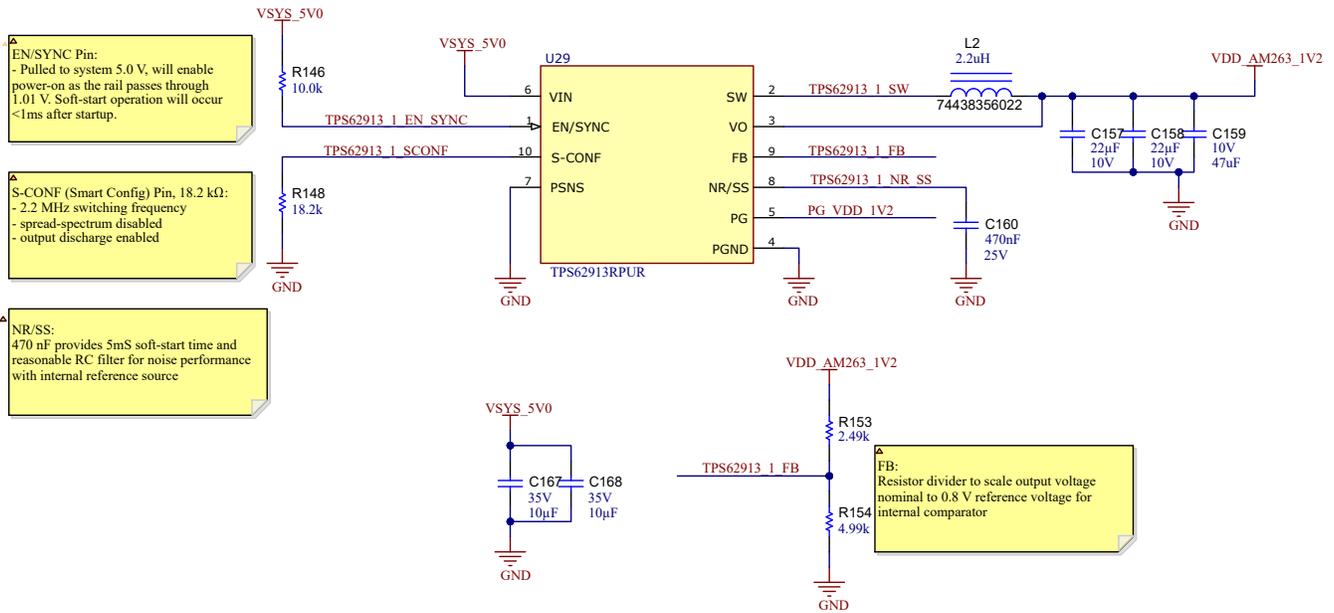


Figure 2-2. AM263x LP-AM263 Schematic Excerpt 1.2 V Core Power Implementation

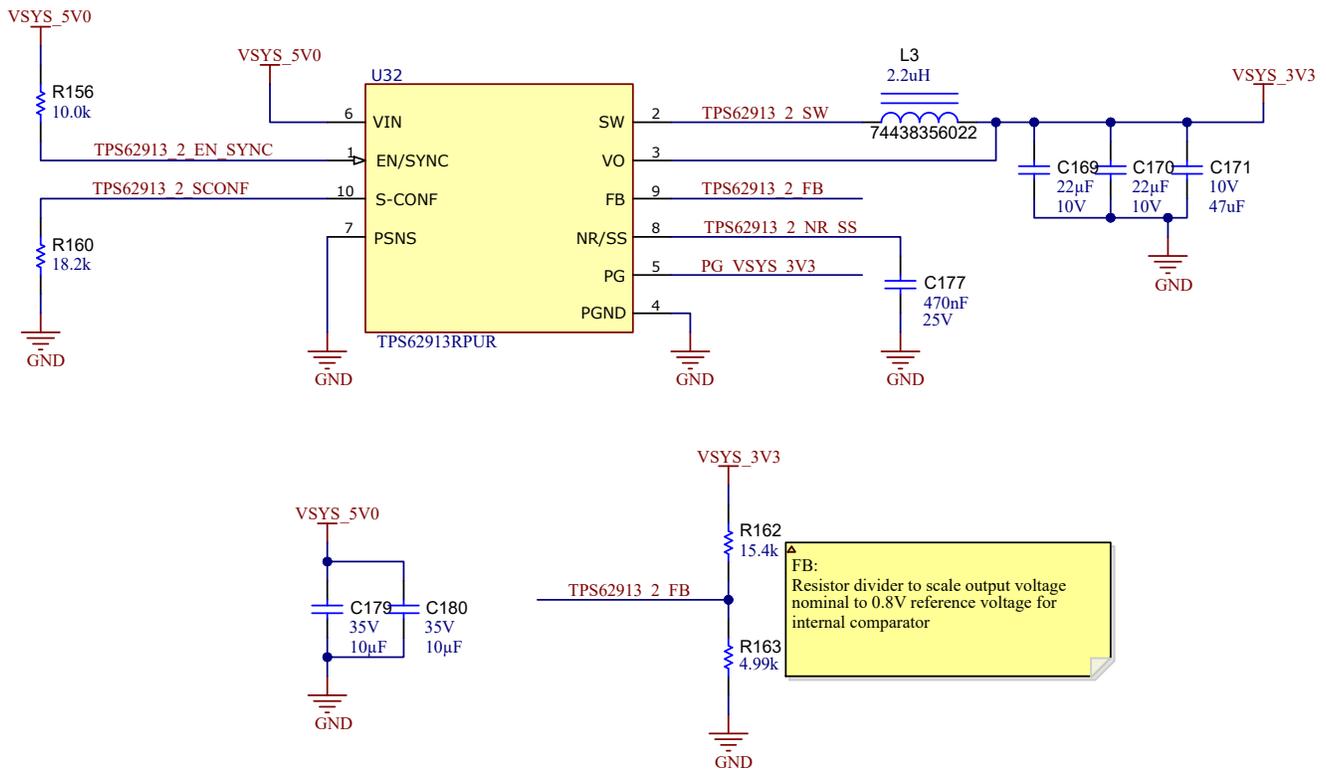


Figure 2-3. AM263x LP-AM263 Schematic Excerpt 3.3 V System Digital/Analog I/O Power Implementation

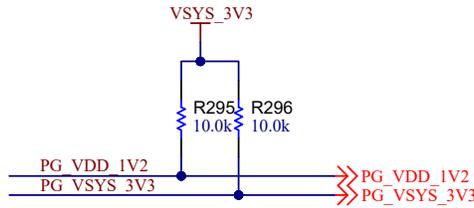
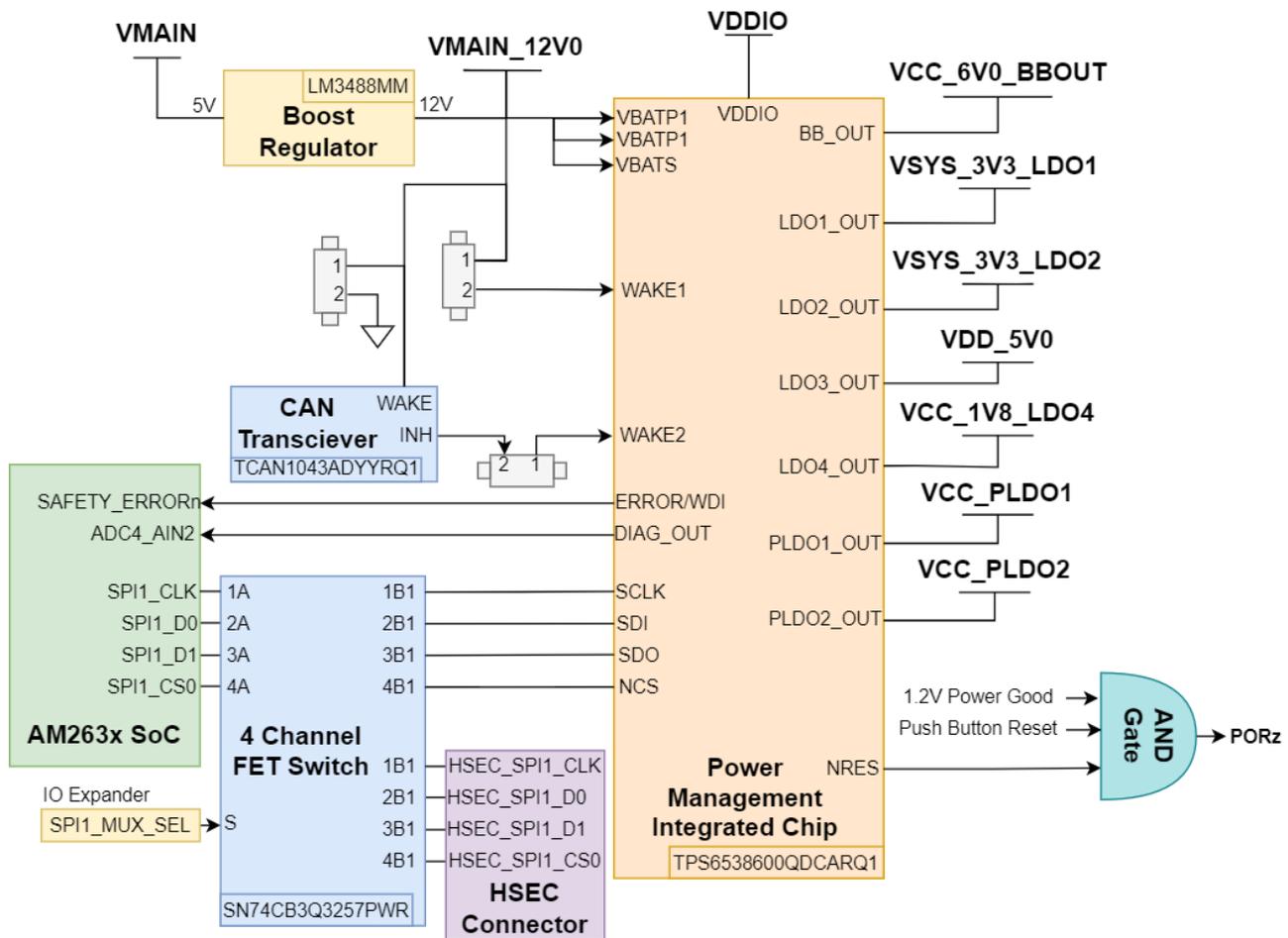


Figure 2-4. AM263x LP-AM263 Schematic Excerpt – Power Good Implementation (see PORz Reset Implementation as well)

2.2 Integrated PMIC Power Solution

The AM263Px controlCard EVM design makes use of a Multirail Power Supply for Microcontrollers in Safety- Relevant Applications (TPS6538600QDCARQ1). The PMIC integrates multiple supply rails to power the MCU, CAN, and other on-board peripherals.

The NRES output of the PMIC should be used to help drive the PORz reset input to the AM263x or AM263Px device to ensure the power on sequencing of the power rails is complete before releasing the MCU from reset.



2.3 Power Decoupling and Filtering

Table 2-1 describes the initial BGA decoupling and power filtering required for the AM263x and AM263Px. These were based on the initial simulation feedback of the Control Card EVM PCB and AM263x package with the transient use-cases shown in Table 2-3.

The decoupling network presented in the below sections and in the AM263x EVM schematics and layouts are reasonable starting points for any AM263x or AM263Px PCB design. However, due to specific PCB routing differences and the resulting plane capacitance and decoupling mounting inductances and other parasitics, it is highly recommended that designers simulate and measure their specific power distribution network performance. Simulations and measurements should ideally be done with target application software active, and intended operating environment conditions applied to the system.

The AM263Px Sensor Package has additional set of ADC reference voltages, ADC_VREFHI_G3 and ADC_VREFLO_G3, which are shown in Figure 2-10

Table 2-1. AM263x and AM263Px Recommended Decoupling per Power Net

Device Supply	Quantity	Comment	Part Number	Manufacturer
VDD_CORE	2	2.2 μ F, 6.3 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0603	GCM188R70J225KE22D	Murata
	3	0.22 μ F, 16 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	Murata
	16	0.01 μ F, 50 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0402	CGA2B3X7R1H103K050BB	TDK
VNWA	1	0.22 μ F, 16 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	Murata
	1	0.01 μ F, 50 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0402	CGA2B3X7R1H103K050BB	Murata
VDD_F	1	0.22 μ F, 16 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	TDK
	1	0.01 μ F, 50 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0402	CGA2B3X7R1H103K050BB	TDK
VDDAR_CORE	1	2.2 μ F, 6.3 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0603	GCM188R70J225KE22D	Murata
	2	0.22 μ F, 16 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	Murata
	1	Ferrite Bead, 120 Ω @ 100 MHz, 2 A, 0603	742792625	Wurth
	3	0.01 μ F, 50 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0402	CGA2B3X7R1H103K050BB	TDK
VDDA18_LDO VDDA18 VDDA18_OSC_PLL VDDA18_TEMP	1	3.3 μ F, 10 V, \pm 10%, X5R, 0603	GRM188R61A335KE15D	Murata
	4	0.1 μ F, 6.3 V, \pm 10%, X7R, 0402	GRM155R70J104KA01D	Murata
VDDS18_LDO VDDS18	1	3.3 μ F, 10 V, \pm 10%, X5R, 0603	GRM188R61A335KE15D	Murata
	4	0.1 μ F, 6.3 V, \pm 10%, X7R, 0402	GRM155R70J104KA01D	Murata
VDDS33	3	2.2 μ F, 6.3 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0603	GCM188R70J225KE22D	Murata
	4	0.22 μ F, 16 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	Murata
	1	Ferrite Bead, 120 Ω @ 100 MHz, 2 A, 0603	742792625	Wurth
	7	0.01 μ F, 50 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0402	CGA2B3X7R1H103K050BB	TDK
VDDA33	1	2.2 μ F, 6.3 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0603	GCM188R70J225KE22D	Murata
	2	0.22 μ F, 16 V, \pm 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	Murata

Table 2-1. AM263x and AM263Px Recommended Decoupling per Power Net (continued)

Device Supply	Quantity	Comment	Part Number	Manufacturer
	1	Ferrite Bead, 120 Ω @ 100 MHz, 2 A, 0603	742792625	Wurth
	3	0.01 μF, 50 V, ± 10%, X7R, AEC-Q200 Grade 1, 0402	CGA2B3X7R1H103K050BB	TDK

VDD 1V2 Core Digital

VDDAR[3:1] 1V2 SRAM Array

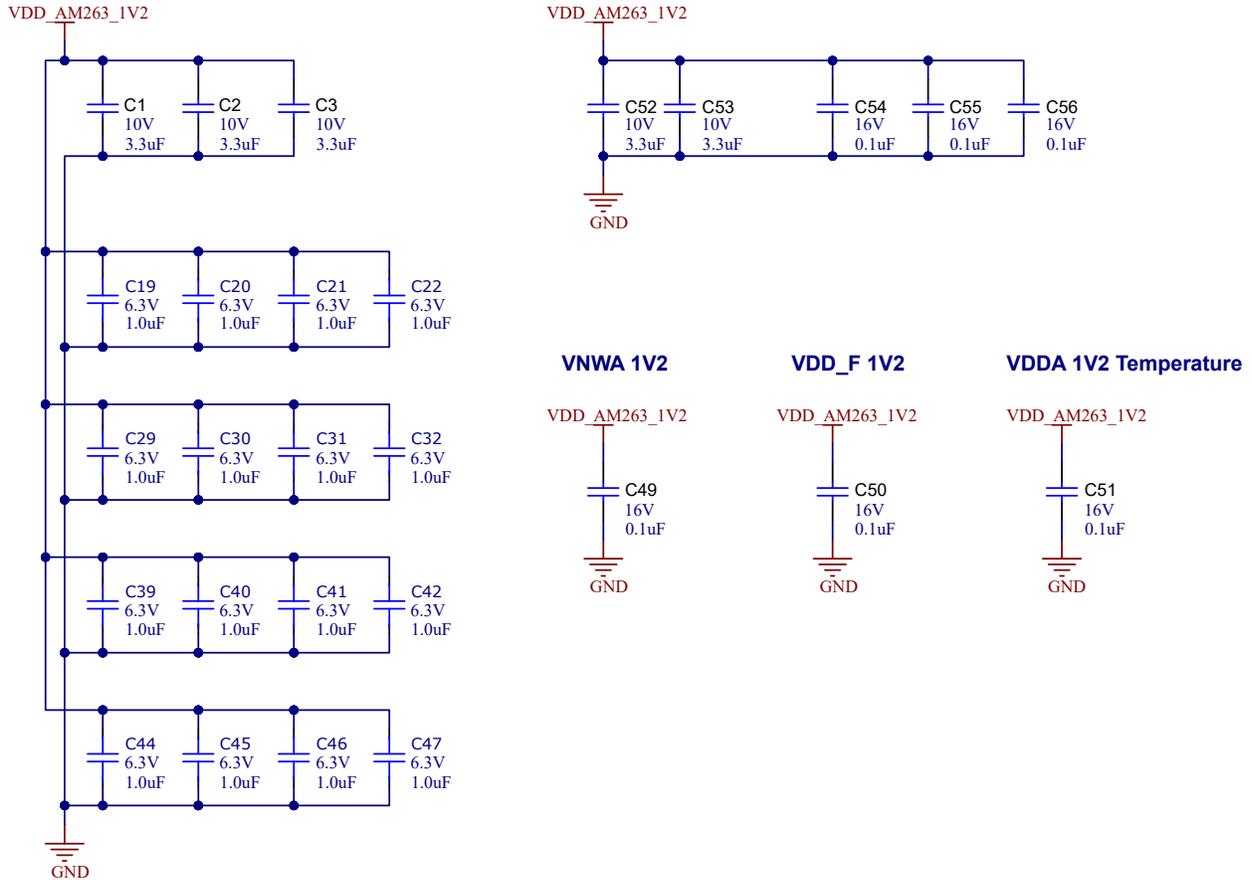
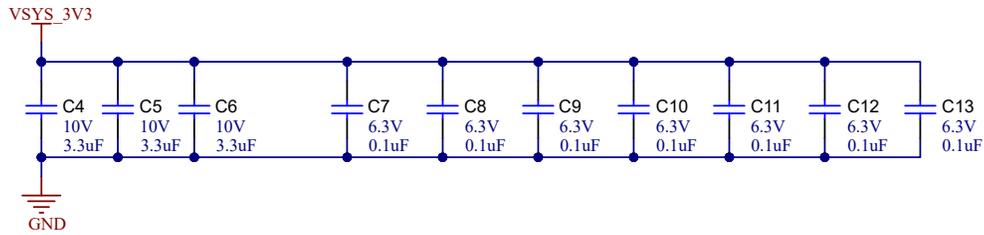


Figure 2-6. AM263x LaunchPad Excerpt – 1.2 V Power Decoupling Schematic

VDDS 3V3 Digital



VDDA 3V3 Analog

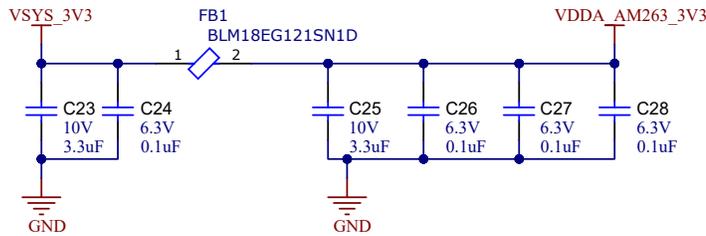
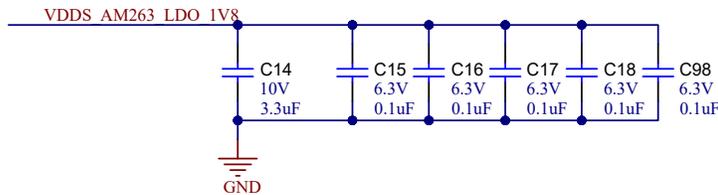


Figure 2-7. AM263x LaunchPad Excerpt – 3.3 V Digital I/O and Analog I/O Decoupling and Filtering Schematic

VDDS 1V8 Digital



VDDA 1V8 Analog

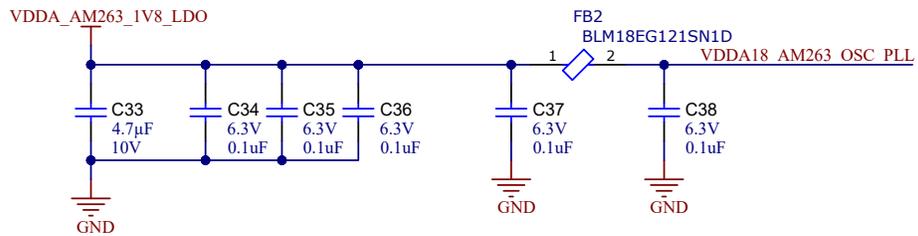


Figure 2-8. AM263x LaunchPad Excerpt – 1.8 V Digital I/O and Analog I/O Decoupling and Filtering Schematic

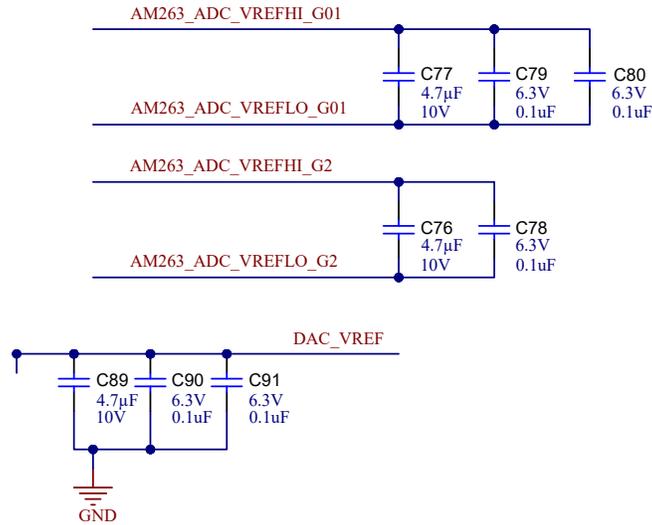


Figure 2-9. AM263x LaunchPad Excerpt – ADC and DAC VREF Decoupling Schematic

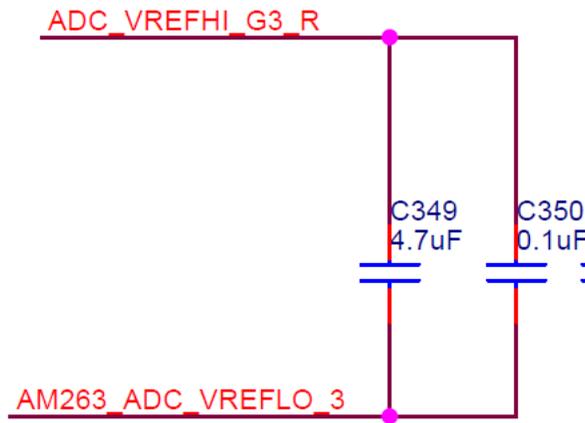


Figure 2-10. AM263Px controlCard Excerpt – additional VREFHI_G3 and VREFLO_G3 connections

2.4 Power Consumption

This section outlines the latest estimates of the AM263x and AM263Px power consumption on a per device power net basis. These values may change as more power modeling and characterization is performed. This data can be used to scale peak DC-DC conversion power margin, perform IR drop analysis of the PCB layout, and help with thermal loading analysis.

These estimates are based on initial power simulations of the device when operating at 150°C junction temperature. For the latest characterized, peak power numbers, see the [AM263x Sitara™ Microcontroller Data Sheet](#) or [AM263Px Sitara™ Microcontroller Data Sheet](#).

Also, a use-case based power estimation tool (PET) is provided for both the AM263x and AM263Px MCUs. These tools can help further bound the peak power based on specific core and peripheral utilization duty-cycle.

Table 2-2. AM263x and AM263Px Estimated Peak Power Consumption at 150°C Junction Temperature

Device Supply	Nominal V	Peak mA AM263	Peak mA AM263P	Comment
VDD, VDDAR[3:1]	1.2	2500	2800	Digital core power
VDDS33	3.3	200	200	3.3 V digital I/O power
VDDA33	3.3	100	200	3.3 V analog I/O power

2.5 Power Distribution Network

This section outlines the latest estimates of the AM263x and AM263Px transient current requirements on a per net basis. These values may change as more power modeling and characterization is performed.

These transient use-case values were used to constrain the PDN design of the AM263x and AM263Px EVMs (controlCards and LaunchPads) by creating a set of minimum/maximum operating frequency and PDN impedance (Z_{max}) target limits. These limits were based on the magnitude and slew-rate of simulated transient current use-cases. The use-cases were used to estimate the PDN bandwidth needed to adequately decouple the resulting transient event. Additional z-parameter simulation of the EVM PDN was used to verify that the power plane design and decoupling placement and component values could then meet these limits. This is summarized in [Figure 2-11](#).

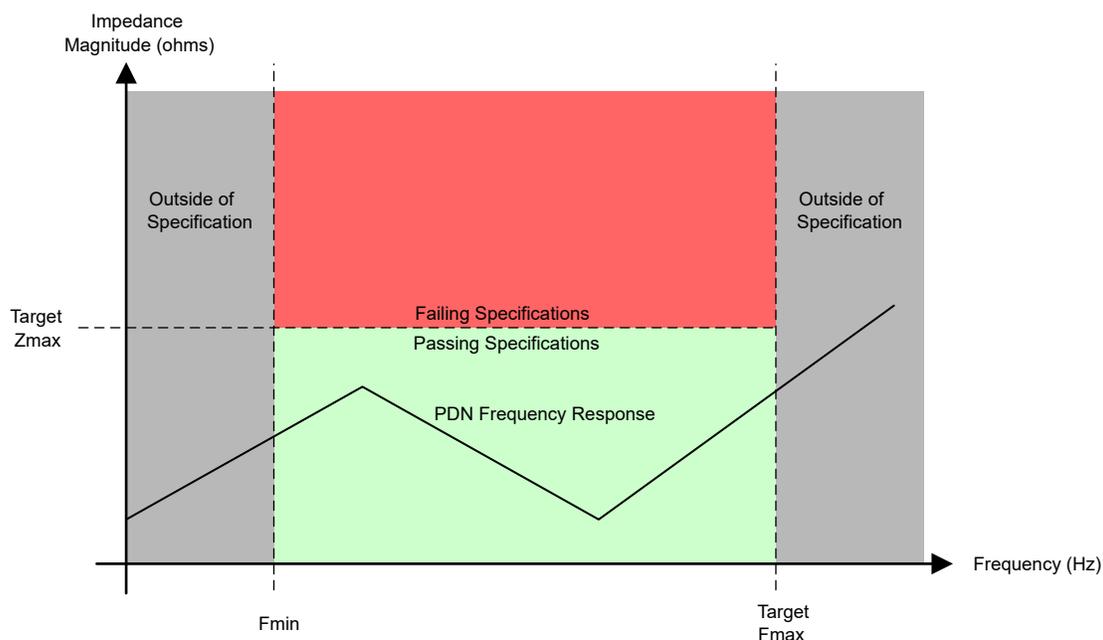


Figure 2-11. AM263x PDN Requirements – Example Diagram

Table 2-3. AM263x and AM263Px Transient Current Model – Use-case Conditions

Transient Case	Net Name	Nominal Voltage (V)	DC IR Budget (%)	AC Ripple Budget (%)	Idle Current (mA)	Peak Current (mA)	Idle to Peak Slew Rate (ns)	Comment
VDD BASELINE1	VDD	1.2	2.5	2.5	0	2402	2.5	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle.
VDD XTAL_PLL1	VDD	1.2	2.5	2.5	42	875	10	XTAL to PLL turn-on transient
VDD WFI1	VDD	1.2	2.5	2.5	750	1117	12.5	4x R5F WFI event transient
VDDS33 BASELINE1	VDDS33	3.3	2.5	2.5	0	84	2.5	Baseline, simple transient model assuming 0 to peak transition in a single R5F clock cycle
VDDA33 BASELINE1	VDDA33	3.3	2.5	2.5	0	34	2.5	Baseline, simple transient model assuming 0 to peak transition in a single R5F clock cycle
VDDS18LDO BASELINE1	VDDS18LDO	1.8	2.5	2.5	0	01	2.5	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle
VDDA18LDO BASELINE1	VDDA18LDO	1.8	2.5	2.5	0	66	2.5	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle

Table 2-4. AM263x and AM263Px Transient Current Model – Resulting PDN Requirements

Transient Case	Net Name	Fmax (MHz)	Current Step (mA)	PCB DC Tolerance (mV)	PCB AC Tolerance (mV)	PCB Target DC IR (mΩ)	PCB Target AC Zmax (mΩ)	Comment
VDD BASELINE1	VDD	200	2402	30	30	12	12	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle.
VDD XTAL_PLL1	VDD	50	833	30	30	36	36	XTAL to PLL turn-on transient
VDD WFI1	VDD	40	367	30	30	82	82	4x RF5 WFI event transient
VDDS33 BASELINE1	VDDS33	200	84	83	83	982	982	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle
VDDA33 BASELINE1	VDDA33	200	34	83	83	2419	2419	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle
VDDS18LDO BASELINE1	VDDS18LDO	200	1	45	45	45	45	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle
VDDA18LDO BASELINE1	VDDA18LDO	200	66	45	45	682	682	Baseline, simple transient model assuming 0 to peak transition in minimal 1 R5F clock cycle

2.5.1 Simulations

The following simulated PDN z-parameter performance was extracted from the AM263x LaunchPad and controlCard layouts using Ansys SI wave. Wide-band s-parameter models of each of the selected capacitors were taken from the manufacturer. Simulations capture only 25°C (room temperature) PCB and capacitor model performance.

2.5.1.1 Core Digital Power 1.2 V

Z11 simulations were performed on the 1.2 V core digital power net of the LP-AM263 LaunchPad EVM to verify transient power margin. The simulation domain included the:

- AM263x BGA (UI) 1.2 V digital and GND return fan-out
- Internal PCB 1.2 V and GND return planes
- Decoupling placed on the 1.2 V power net,
- U29 buck regulator output LC filter up to switch node

These simulations were done iteratively with multiple capacitor BOM changes made between each iteration. Each iteration was characterized primarily by the maximum and minimum frequency bandwidth below Z_{target} (see above sections) and the BOM selection changed to maximize bandwidth and maximum Z_{target} margin. Only the initial and final chosen BOM iterations are shown in [Figure 2-12](#) and [Figure 2-13](#).

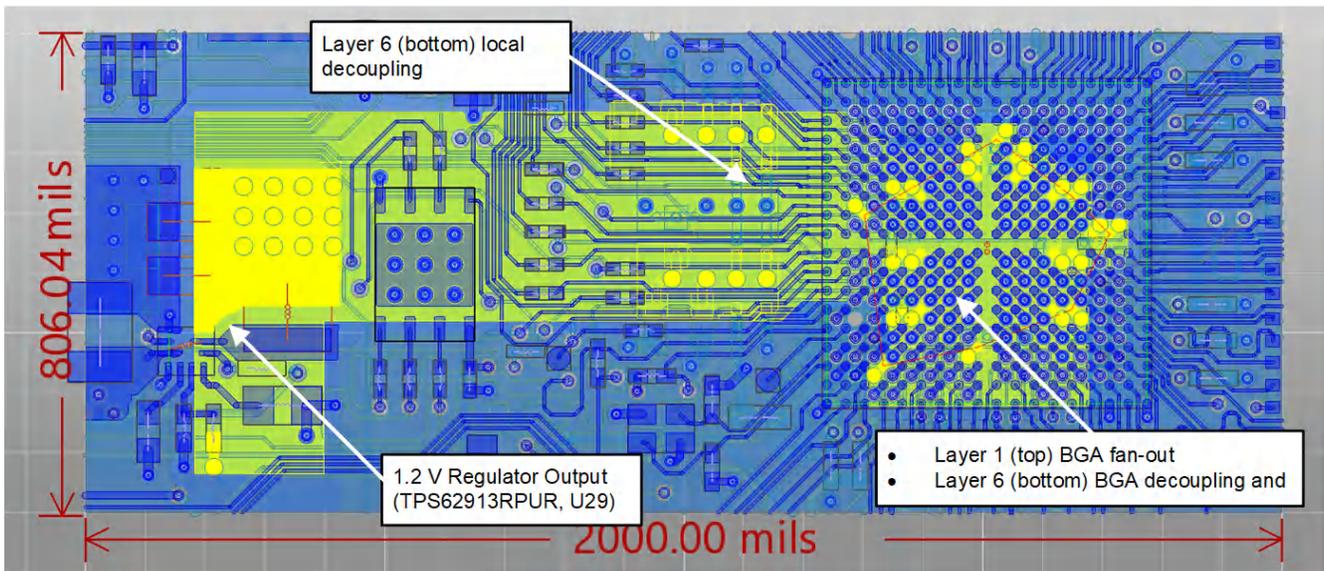


Figure 2-12. AM263x LaunchPad PDN Simulations – 1.2 V Core Power Simulation Domain

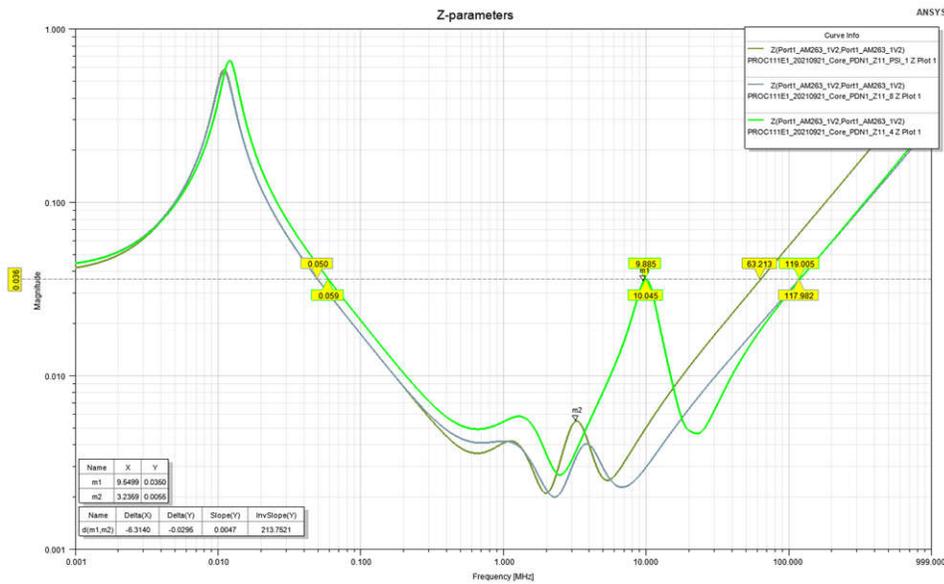


Figure 2-13. AM263x LaunchPad PDN Simulations – 1.2 V Core Power Simulated Z11

- AM263x LaunchPad PDN Simulations – 1.2 V Core Power Simulated Z11
 - This resulted in the marker (m2) point of 5.5 mΩ
 - Ztarget requirement of 36mOhm maintained from 50 KHz to 63 MHz
 - Major difference in BOM was replacing all 0.1 μF BGA and local decoupling capacitors with 1.0 μF capacitors this entirely removed the 10 MHz resonant point in the PDN impedance spectrum
- PROC111E1_20210921 Initial simulations
 - Major resonance at 10 MHz eliminated almost all margin against 36 mΩ Ztarget requirement

2.5.1.2 Digital/Analog I/O Power 3.3 V

Z11 simulations were performed on the 3.3 V digital and analog power net of the controlCard EVM to verify transient power margin. The simulation domain included the:

- AM263x BGA (U1) 3.3V power and ground return BGA and fan-out
- Internal power and ground return routing layers
- Regulator output

Initial runs of these simulations showed that no BOM changes were needed to meet the maximum and minimum frequency bandwidth below Ztarget (see above sections). Only the initial simulation with the final chosen BOM iterations are shown below.

The simulations were divided between the VDDS33 digital 3.3 V plane and decoupling network and the VDDA33 analog 3.3 V traces and decoupling local to the design. The F dividing line between these simulations is the FL18 ferrite bead element was used to separate these two decoupling performance simulations.

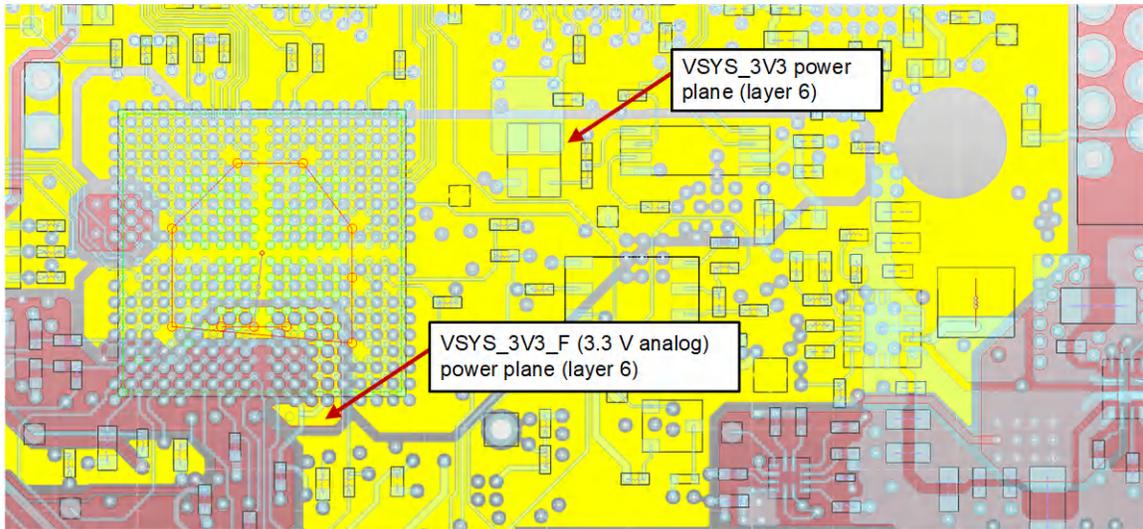


Figure 2-14. AM263x LaunchPad PDN Simulations – 3.3 V Digital/Analog I/O Power Simulation Domain (A)

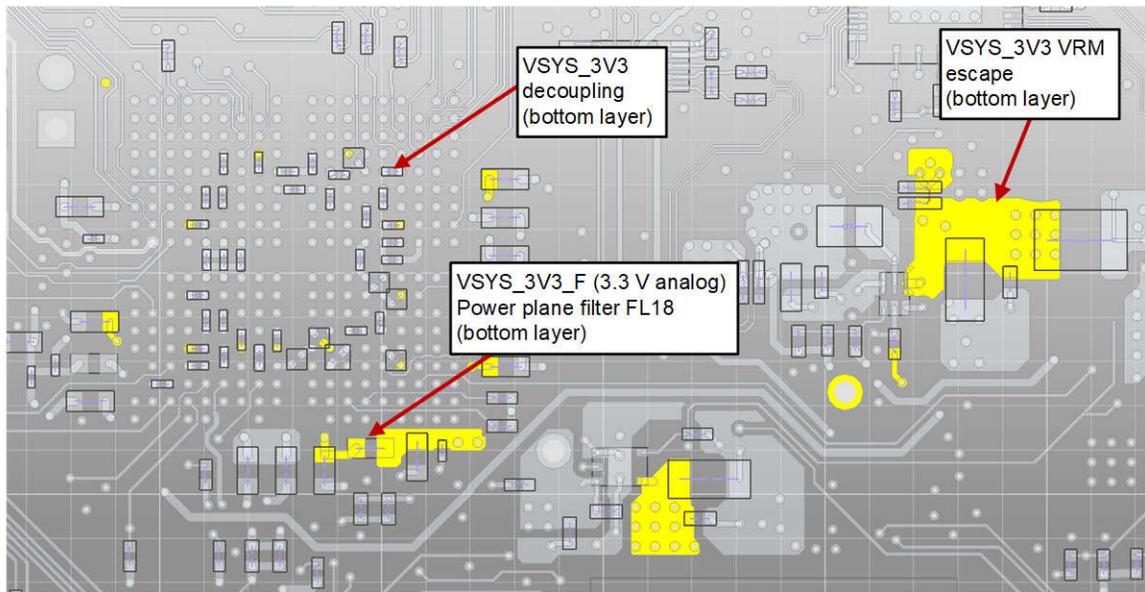


Figure 2-15. AM263x LaunchPad PDN Simulations – 3.3 V Digital/Analog I/O Power Simulation Domain (layer 8, bottom)

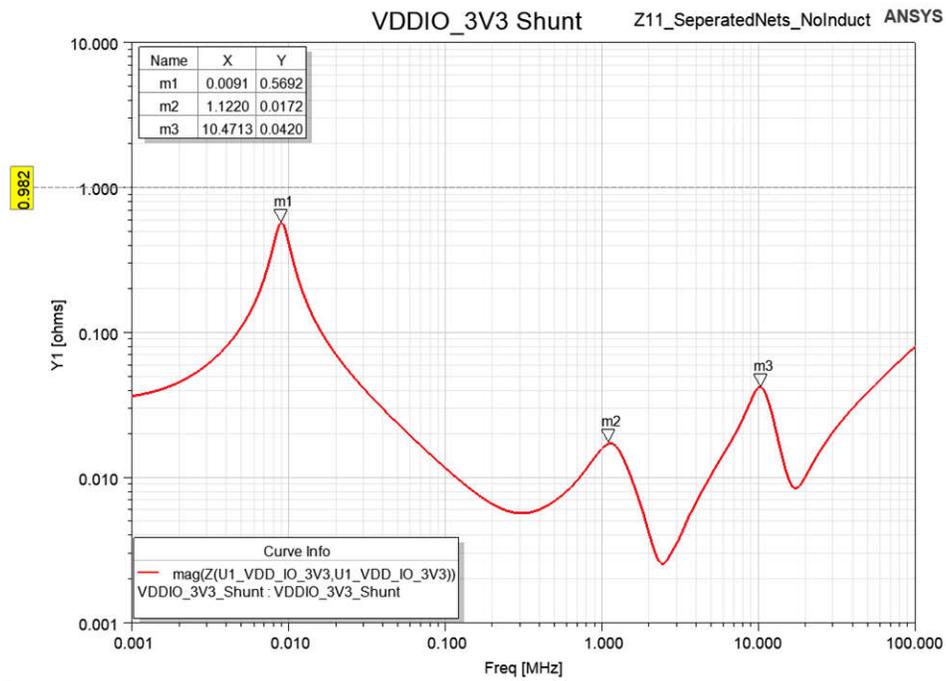


Figure 2-16. AM263x LaunchPad PDN Simulations – 3.3 V Digital I/O Power Simulated Z11

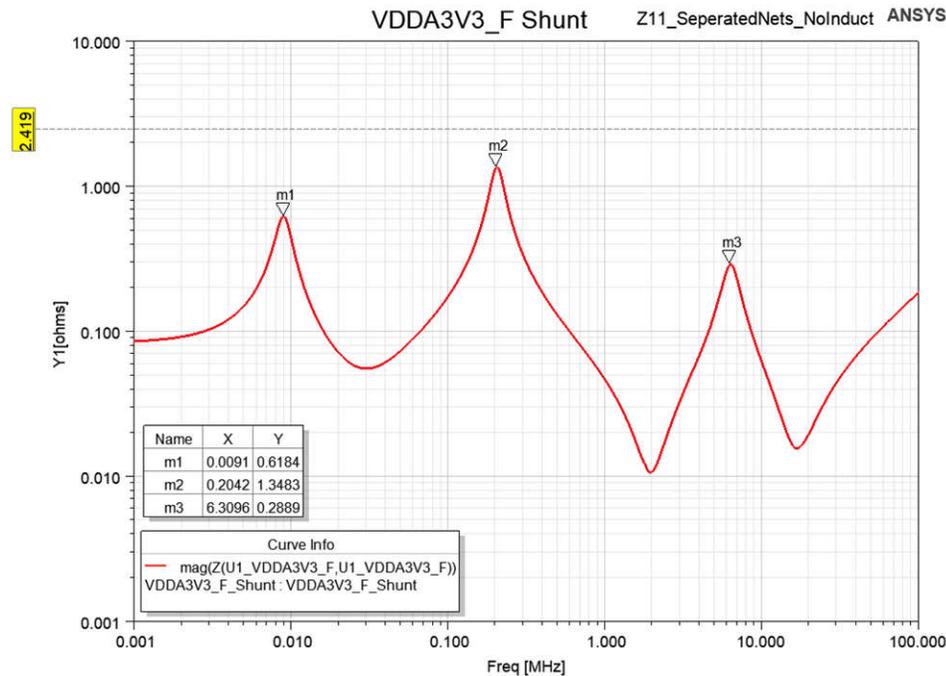


Figure 2-17. AM263x LaunchPad PDN Simulations – 3.3 V Analog I/O Power Simulated Z11

2.6 e-Fuse Power

The AM263x and AM263Px one-time programmable, e-Fuse memory can be utilized for storing customer cryptographic keys and other information specific to individual devices. These e-Fuse memory locations can only be programmed when the target device VPP, e-Fuse power pin, is powered by a 1.7 V nominal output voltage, 100 mA peak current supply. This 1.7V VPP power supply can be onboard or off-board. The specific placement of the VPP supply and implementation depend on how the e-Fuse memory will be utilized by the designer. The implementation should follow the diagram shown in [Figure 2-18](#)

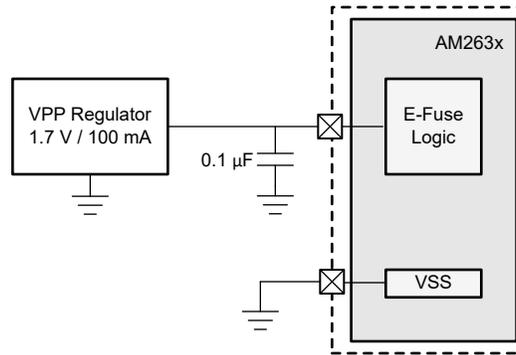


Figure 2-18. AM263x and AM263Px e-Fuse VPP Power Implementation Example

The AM263Px has the option to source VPP internally using the ANALDO. The ANALDO must be overwritten to provide 1.7V during e-Fuse programming, then reverted back to normal operation.

The e-Fuse programming typically follows one or both of the following scenarios:

- **Factory programming** – e-Fuse memory programmed during post assembly test of the AM263x system.
- **Field programming** – e-Fuse memory is programmed after the device has left the factory and is installed in the end-equipment.

If the factory programming scenario is all that is required for a product, then it is typically preferable for the VPP power supply to be implemented off-board since this reduces the number of supplies required to be placed on the PCB assembly. The VPP supply would only be used during this programming sequence, so keeping it on the board would not be an efficient use of PCB floor plan area, BOM cost or test time.

However, if the e-Fuse memory must be programmed outside the factory environment, the VPP power must either be supplied from an onboard component or from an attached accessory board that can supply this power as needed.

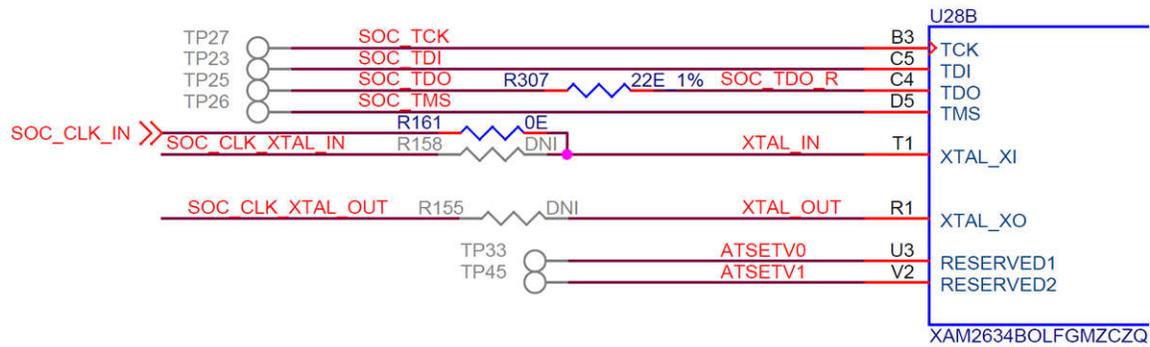
In the case of the TMDSCNCD263 controlCard evaluation module design, the VPP supply was left on the board to enable convenient e-fuse programming by customers experimenting with this process. On the controlCard the TLV75801PDRVR LDO, U66, was used to drop down the 3.3 V system I/O voltage to the VPP 1.7 V. Additionally, the GPIO expander, U50 was used to toggle the VPP_LDO_EN pin to enable/disable the LDO in the required sequence for e-Fuse programming.

For the full VPP electrical requirements and e-Fuse programming sequence, see the *VPP Specifications for One-Time Programmable (OTP) eFuses* section in the [AM263x Sitara™ Microcontroller Data Sheet](#) or [AM263Px Sitara™ Microcontroller Data Sheet](#).

3 Cloning

3.1 Crystal and Oscillator Input Options

The AM263x and AM263Px XTAL_XI and XTAL_XO (pins T1 and R1) clock input can be sourced from either an attached crystal or a single-ended oscillator output. The attached crystal should be a fundamental mode crystal operating at 25 MHz. If operating from a single-ended oscillator output, the XTAL_XI pin should be connected to the oscillator and the XTAL_XO pin must be left floating, unconnected on the PCB. In oscillator input mode, the XTAL_XI pin can be tied to either a 1.8 V square-wave or sinewave oscillator. For full crystal and oscillator input requirements, see the [AM263x Sitara™ Microcontroller Data Sheet](#) or [AM263Px Sitara™ Microcontroller Data Sheet](#).



SOC Clock

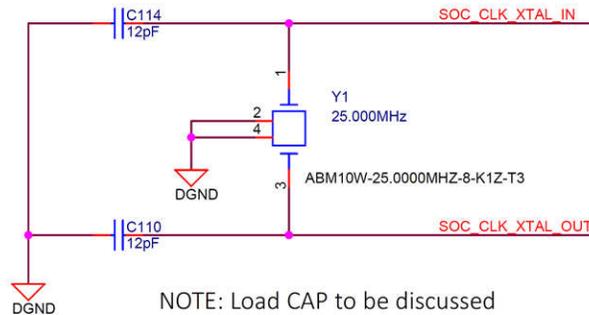


Figure 3-1. Excerpt From AM263x Control Card Schematics (for full crystal and oscillator input requirements)

In the case of the AM263x Control Card, an onboard ABM10W-25.0000MHZ-8-K1Z-T3 25 MHz crystal provides crystal mode clocking. Alternatively, an LMK1C1104PWR clock distributor circuit and SN74LV1T34 buffer provide the 1.8 V square-wave clock to the XTAL_XI pin. The LMK1C1104PWR is also used to provide a clock source to the onboard Ethernet PHY as well.

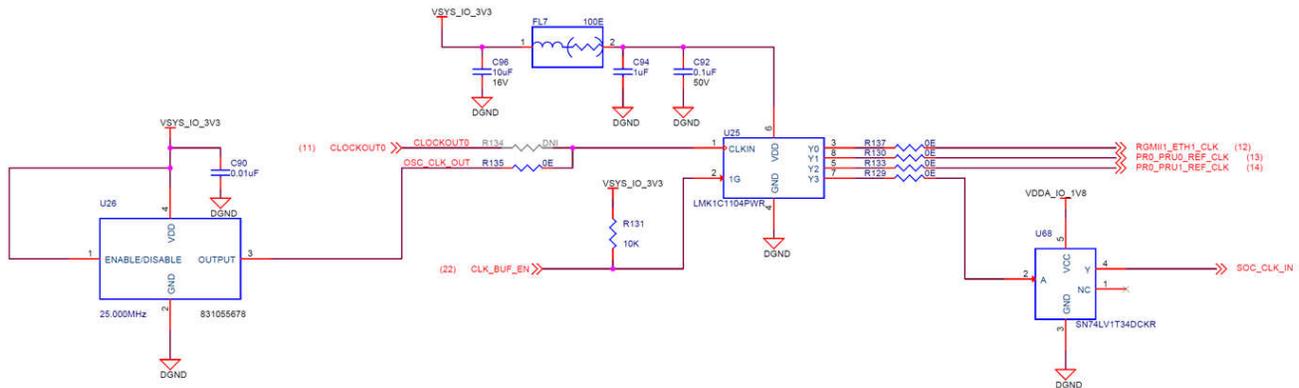


Figure 3-2. Excerpt From AM263x controlCard Schematics - Oscillator Clock Source and Clock Distributor

3.2 Output Clock Generation

The AM263x and AM263Px devices include two output clock sources, CLKOUT0 (pin M2) and CLKOUT1 (pin B16). These are intended to be used to clock attached peripheral IC such as Industrial/Automotive Ethernet PHY. This can save on BOM cost and additional IC placement and routing space. The AM263x and AM263Px Launchpads include an optional path for the CLKOUT0 (pin M2) signal to clock the onboard DP83869HMRGZT Ethernet PHY.



Figure 3-3. Excerpt From AM263x LaunchPad Layout – CLKOUT0 and EXT_REFCLK0 Output

3.3 Crystal Selection and Shunt Capacitance

In crystal operating mode, the AM263x or AM263Px can be interfaced to a wide variety of compatible crystals. Based on PCB parasitic capacitance and crystal selected, the additional load capacitance needs to be modified to achieve the best start-up stability and frequency accuracy.

For full crystal loading tolerances, see the [AM263x Sitara™ Microcontroller Data Sheet](#) or [AM263Px Sitara™ Microcontroller Data Sheet](#).

3.4 Crystal Placement and Routing

Crystal oscillator input should be placed as close as possible to the AM263x or AM263Px XTAL_XI/XO with minimal length traces between crystal and MCU pads. A ground ring shorted to the local VSS plane should be placed adjacent and between the XTAL_XI and XTAL_XO traces to help prevent coupling from adjacent signals onto the clock higher impedance crystal input paths.

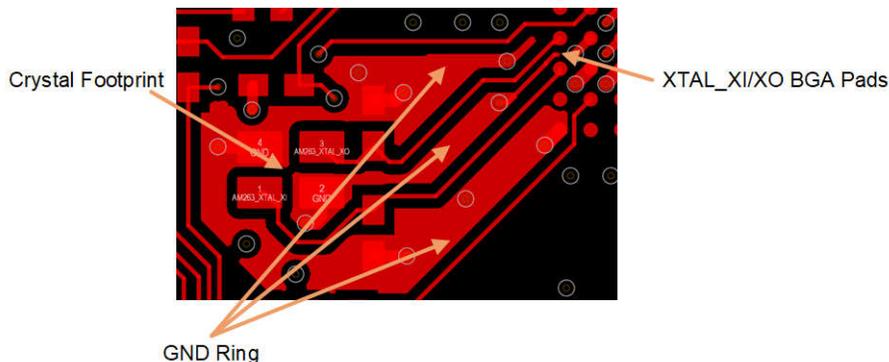


Figure 3-4. Excerpt From AM263x Launchpad Layout - Crystal Layout and Ground Ring Structure

4 Resets

The AM263x and AM263Px MCUs have two hardware reset sources:

- PORZ: Power on reset (logic low enable) signal, pin R2
 - Should be driven from the power-good circuits of the associated VDD 1.2 V core and VDDS33 3.3 V I/O regulators
 - For a valid reset the PORZ signal must transition from logic low to logic high only after the VDD 1.2V core and VDDS33 3.3V I/O regulators are stable, and at their nominal values. For power-on-reset timing requirements, see the device-specific data sheet.

- WARMRSTN: Warm reset (logic low enable) input and reset status output signal, pin C3
 - The power-on the default configuration sets this pin as open-drain output, which outputs the reset status of the device.
 - When the device enters reset, this signal is driven logic low.
 - When the device is fully out of reset, this signal is driven logic high.

The PORZ is intended to be kept at logic low at initial startup of the system. Once each regulator sourcing the AM263x or AM263Px power pins has been verified to be operating at nominal output voltage, then the PORZ signal can be brought up to logic high. This action will start the MCU boot ROM execution, beginning with sampling of the SOP pins. The AM263x Launchpad implementation utilizes a single SN74LVC1G11 AND gate which takes in as input the open-drain output power-good signals from the onboard DC-DC regulators and an optional push-button reset switch. A weak pull-down resistor is recommended on the PORZ signal to keep the signal at logic low before startup of the system. PORZ should be forced low if either VDD 1.2 V or VDDS33 3.3 V rail power goes below the nominal operating range.

For a full description of the power-on and power-off reset sequencing requirements, see the [AM263x Sitara™ Microcontroller Data Sheet](#) or [AM263Px Sitara™ Microcontroller Data Sheet](#).

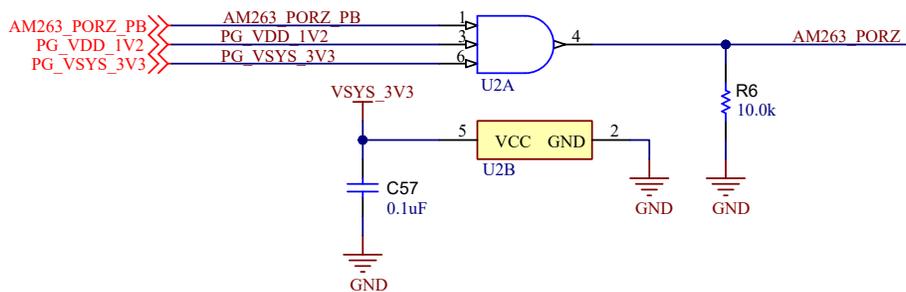


Figure 4-1. Excerpt From AM263x Launchpad Schematic – PORZ Generation

The WARMRSTN pin is a multi-purpose software reset input and hardware reset status pin. In the power-on-default configuration, this pin is configured as an open-drain output and requires an external pull-up resistor to VDDS33 3.3 V I/O voltage rail. In this mode, WARMRSTN can be used as an MCU reset indicator and can be used to drive reset input for attached peripheral IC such as Ethernet PHY and memories.

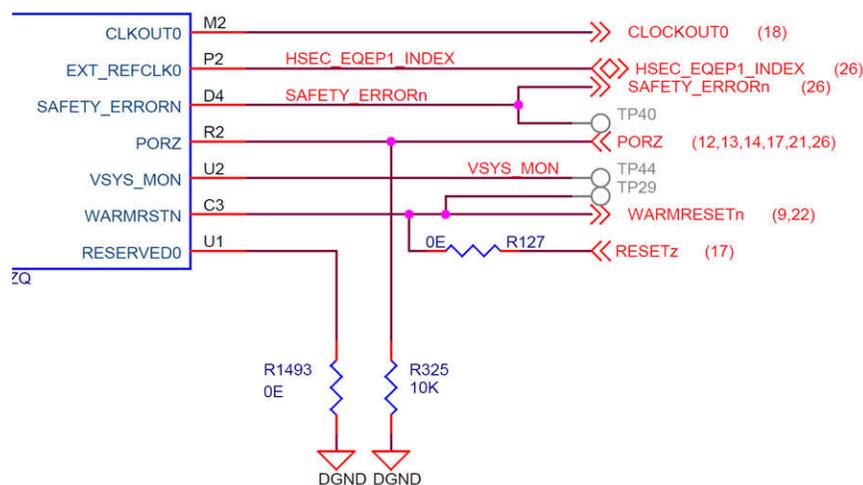


Figure 4-2. Excerpt From AM263x Control Card Schematic – PORZ and WARMRSTN Pinout

WARMRSTN can also be configured by software as software reset. Additional software reset sources are also available on the AM263x and AM263Px devices. For more information on reset functionality, see the [Reset](#) chapter in the [AM263x Sitara™ Microcontroller Technical Reference Manual](#) or [AM263Px Sitara™ Microcontroller Technical Reference Manual](#).

Because of the default open-drain configuration of this pin, if both the reset status output mode and the software reset input mode is needed in a design, it is recommended that open-drain buffers be used to drive the optional reset input status. In the case of the AM263x Control Card, a SN74LVC1G07 open-drain buffer is used to optionally drive the push-button WARMRSTN without conflicting with the reset status output which is used to reset the Ethernet PHY onboard during initial board power-on.

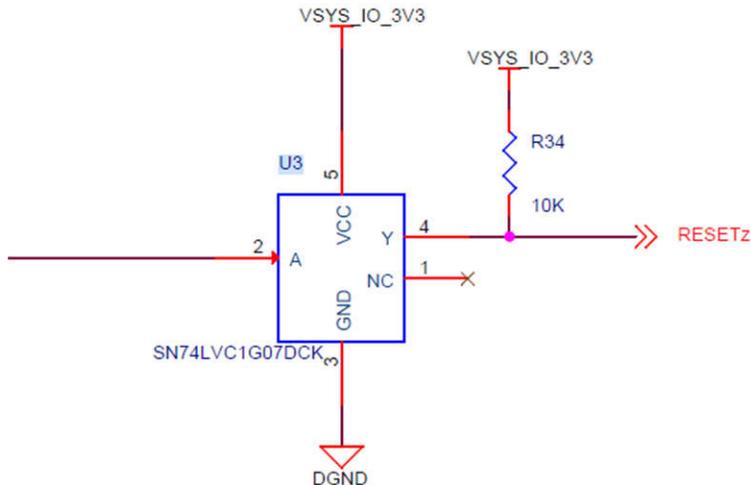


Figure 4-3. Excerpt From AM263x Control Card Schematic – WARMRESETN Push-Button Open-Drain Driver

5 Bootstrapping

The start-on-power (SOP) signals are used to latch in the selected boot mode into the AM263x or AM263Px device. During the PORZ rising edge (low to high logic transition) the SOP[3:0] signals are sampled. The resulting 4 bits are used to branch the boot ROM into the selected boot mode. Not all combinations are supported. For a full description of the SOP pin states and supported boot modes, see the [AM263x Sitara™ Microcontroller Technical Reference Manual](#) or [AM263x Sitara™ Microcontroller Technical Reference Manual Addendum](#).

5.1 SOP Signal Implementation

Each SOP bootmode selection signal is multiplexed with a subset of OSPI/QSPI and SPI peripheral functional mode signals. For all signal descriptions, see the *Signal Description* tables in the [AM263x Sitara™ Microcontroller Data Sheet](#) and [AM263Px Sitara™ Microcontroller Data Sheet](#). The SOP signal descriptions are excerpted in [Figure 5-1](#).

Table 5-1. SOP and Functional Mode Signal Mapping

AM263x/AM263Px Pin Number	Primary Pinmux Signal	SOP Mode Signal
N1	OSPI0/QSPI0_D0	SOP[0]
N4	OSPI0/QSPI_D1	SOP[1]
A11	SPI0_CLK	SOP[2]
C10	SPI0_D0	SOP[3]

Because of this SOP/functional-mode multiplexing additional care must be taken in schematic and layout to ensure that the SOP mode selection resistors, jumpers or switch paths are routed in such a way that the SOP mode branches do not present inductive stubs to the functional mode signal paths. Failing to take care of this may result in non-functional OSPI/QSPI or SPI interfaces.

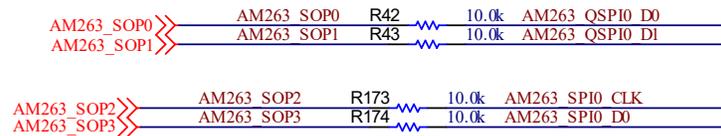


Figure 5-1. Excerpt From AM263x Launchpad Schematic – SOP[3:0] Functional and SOP Paths

In the AM263x and AM263Px Control Card and Launchpad designs this SOP mode isolation is accomplished by including a 10KΩ resistor in the SOP signal path. The resistor is placed such as one pad is as close to the AM263x BGA pad and in-line with the functional mode path. This creates a layout where the additional stub length necessary to breakout the SOP path will only minimally impact the functional mode operation of the signals, as shown in [Figure 5-2](#) and [Figure 5-3](#).

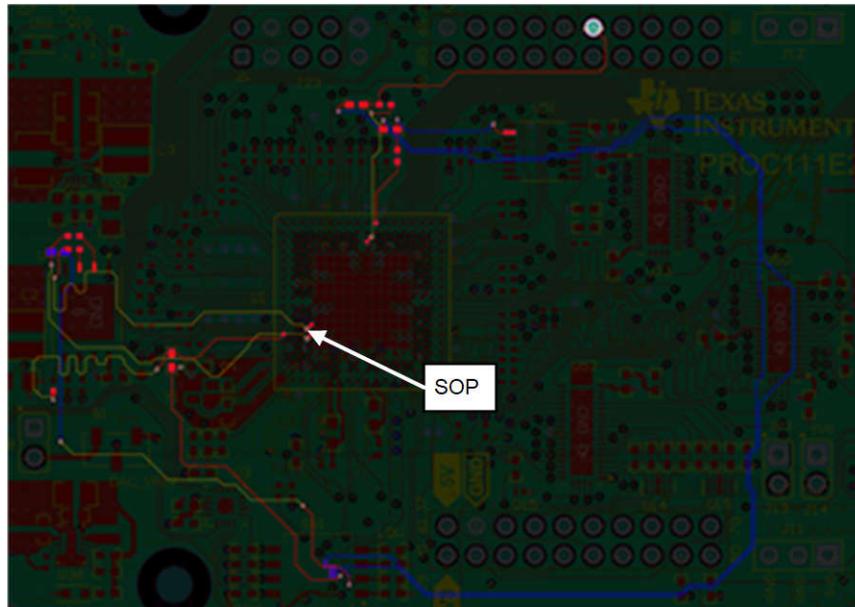


Figure 5-2. Excerpt From AM263x Launchpad Layout – All SOP[3:0] Functional and SOP Paths

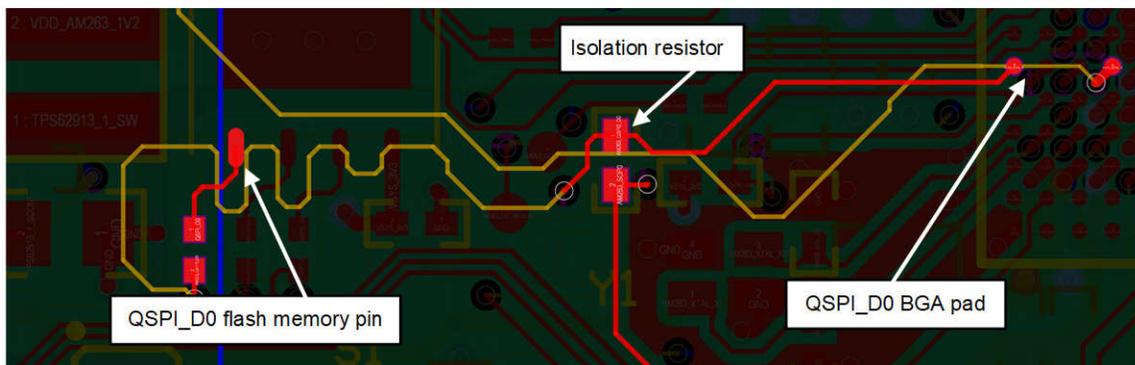


Figure 5-3. Excerpt From AM263x Launchpad Layout – Highlighting SOP0/QSPI_D0 Path and SOP Isolation Resistor

5.2 OSPI/QSPI Memory Implementation

The OSPI Flash memory interface is the primary bootloader memory location for the AM263P MCU and the QSPI Flash memory interface is the primary bootloader memory location for the AM263x MCU. For a full description of boot ROM execution, including OSPI and QSPI boot information, see the [AM263x Sitara™ Microcontroller Technical Reference Manual](#) and [AM263Px Sitara™ Microcontroller Technical Reference Manual](#). The excerpt from [Figure 5-4](#) shows the implementation of the QSPI NOR flash interface from the LP-AM263 LaunchPad design. The excerpt from [Figure 5-5](#) shows the implementation of the OSPI NOR flash interface on the TMDSCNCD263P AM263Px controlCard design.

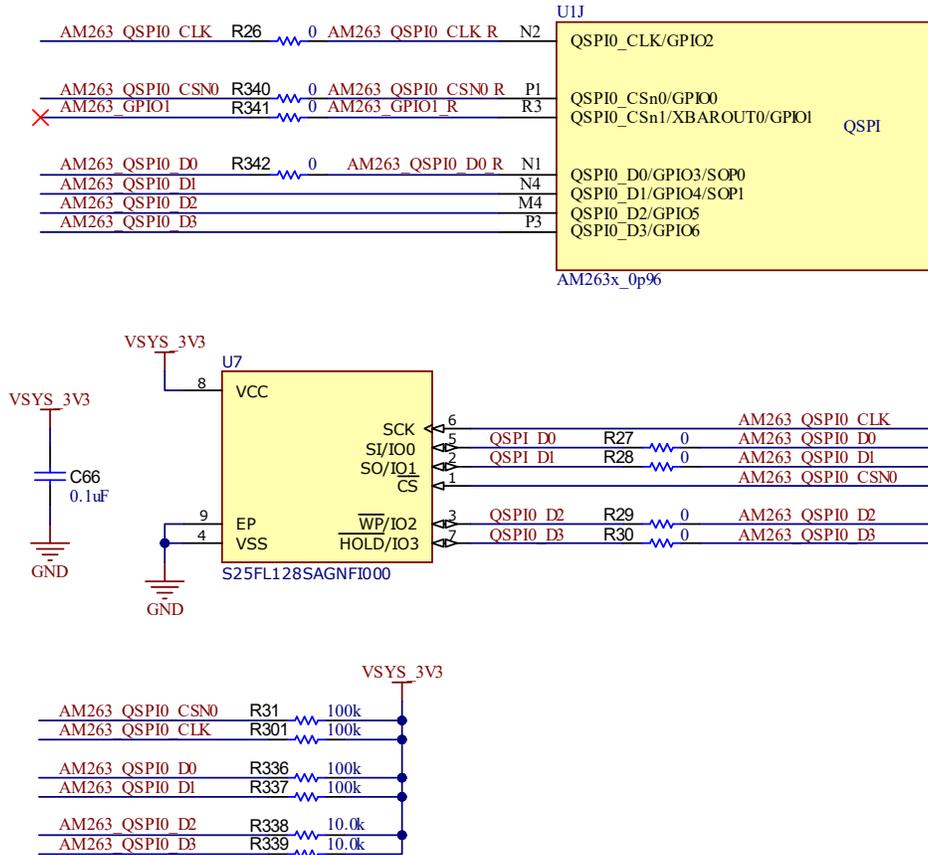


Figure 5-4. Example AM263x QSPI Controller and NOR Flash Memory Schematic

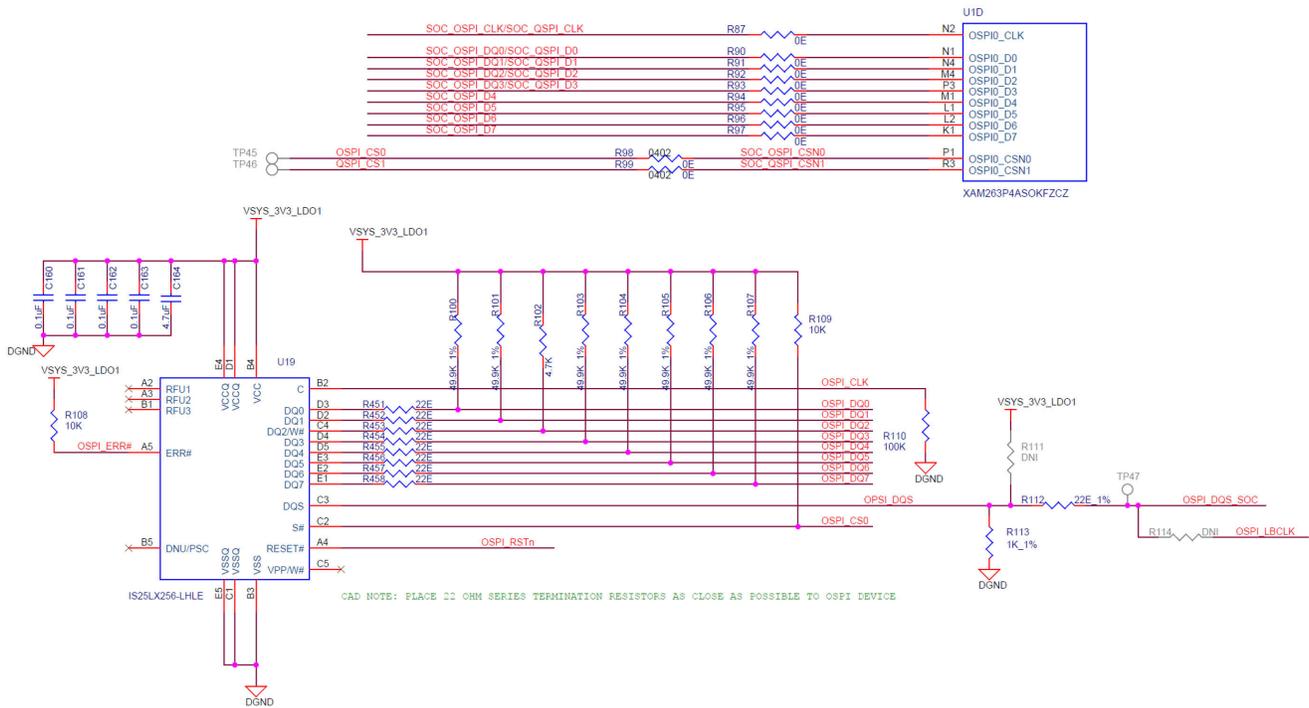


Figure 5-5. Example AM263Px OSPI Controller and NOR Flash Memory Schematic

To control OSPI/QSPI bus transition overshoot and undershoot, include the following series termination resistors close to the OSPI/QSPI memory pins and the AM263x or AM263Px BGA.

- Series termination at the AM263x or AM263Px MCU, transmit side of QSPI0_CLK, and QSPI0_CS[1:0]
- Series termination at OSPI/QSPI memory side of OSPI0_D[7:0] or QSPI0_D[3:0]

For recommended series termination resistor placement, see [Figure 5-7](#).

The OSPI_D[7:1] and QSPI_D[3:1] bits of the interface are used as a read interface, so series termination at the memory side of the bus are used. OSPI/QSPI_D0 may benefit from termination at both the MCU side and the OSPI/QSPI memory side of the bus since is used as both a single-mode write and part of single-mode and octal/quad-mode reads. However, placement of additional termination on both sides of this bus may be difficult to achieve from a PCB floor-planning perspective. The termination scheme presented here should be used as a minimum recommendation. For more details on termination requirements, see [Section 8](#).

Pull resistors are also necessary on the OSPI/QSPI clock, chip-select and data lines. Include the following pull resistors on the QSPI signals. Different QSPI memory may have different pull-up/down requirements depending on the specific memory and application requirements. These pull resistor recommendations are based on the implementation of the S25FL128x memory used on the LP-AM263 design. To confirm all pin memory configuration details, see the device-specific QSPI Flash memory data sheet.

- QSPI_CLK, QSPI_CS[1:0], and QSPI_D[1:0] - include 100kohm pull-up to VDD33 IO supply
- QSPI_D[2] - 10 kohm pull-up to VDD33 IO supply. This disables write-protect mode on the S25FL128 flash memories.
- QSPI_D[3] - 10 kohm pull-up to VDD33 IO supply. This disables hold mode on the S25FL128 flash memories

Include the following pull resistors on the OSPI signals. Different OSPI memory may have different pull-up/down requirements depending on the specific memory and application requirements. These pull resistor recommendations are based on the implementation of the IS25LX256x memory used on the TMDSCNCD263P design. To confirm all pin memory configuration details, see the device specific OSPI Flash memory data sheet.

- OSPI_CLK - include 100kohm pull-down to GND
- OSPI_CS - 10kohm pull-up to VDD33 IO supply
- OSPI_DQS - 1k pull-down to GND

- OSPI_D[2] - 4.7kohm pull-up to VDDS33 IO supply. This disables write-protect mode on the IS25LX256 flash memories
- OSPI_D[1:0] and OSPI_D[7:3] - 49.9kohm pull-up to VDDS33 IO supply

Stronger pull-up resistors are used to disable write-protect and hold modes by default. Weaker pull-up resistors are used to keep the lines at valid logic levels between transactions. Pull resistors should be placed close to the OSPI/QSPI memory pins to prevent any additional routing stubs from being formed.

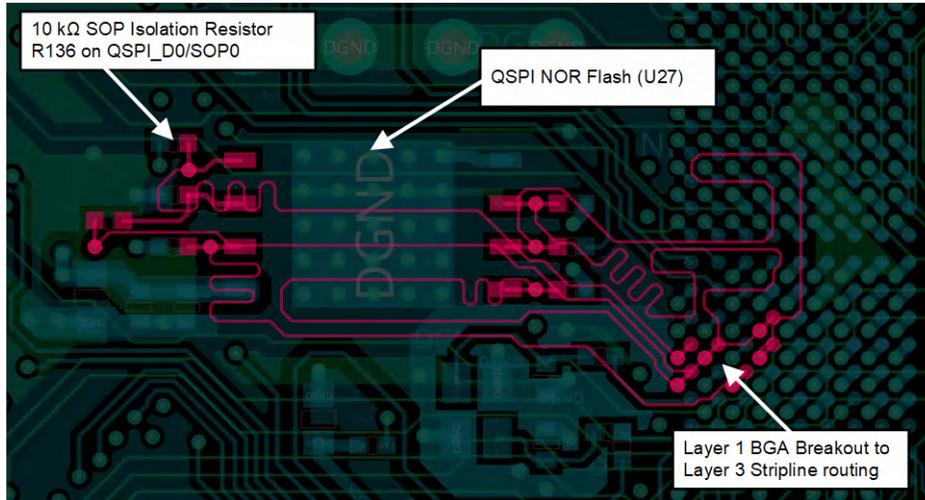


Figure 5-6. Excerpt From LP-AM263 Launchpad Layout – Highlighting SOP0/QSPI_D0 Path and SOP Isolation Resistor

Additional routing guidelines for the QSPI memory interface are provided in [Figure 5-7](#) and [Table 5-2](#). These should be used as maximum routing delay and skew match limits. The QSPI memory should be placed close to the AM263x or AM263Px BGA footprint as possible. This allows for routing that maximizes the delay margins and skew margins and minimizes transmission-line effects.

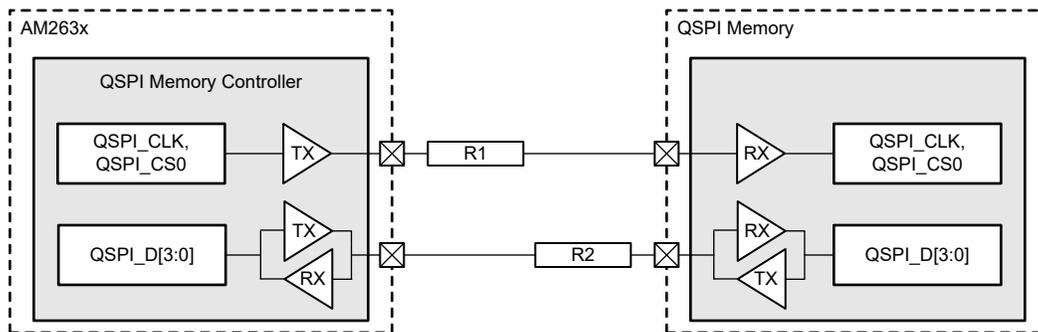


Figure 5-7. AM263x or AM263Px QSPI - Routing Rules Diagram

Additional routing guidelines for the OSPI memory interface are provided in [Figure 5-8](#) and [Table 5-3](#). These should be used as maximum routing delay and skew match limits. The OSPI memory should be placed close to the AM263Px BGA footprint as possible. This allows for routing that maximizes the delay margins and skew margins and minimizes transmission-line effects.

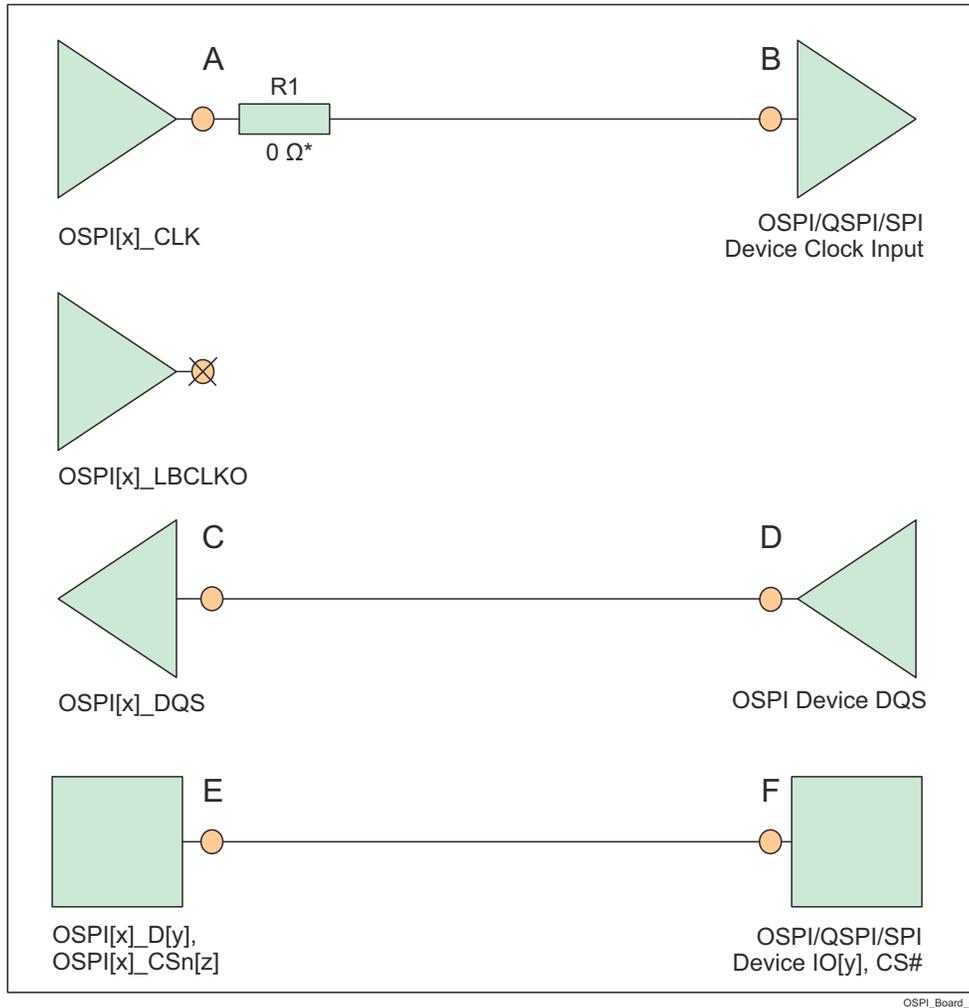


Figure 5-8. AM263Px OSPI - Routing Rules Diagram

Table 5-2. AM263x and AM263Px QSPI – Recommended Routing Rules

Spec No.	Specification	Value	Unit
1	QSPI_CLK, QSPI_CS0, QSPI_D[3:0] maximum delay	450	ps
2	QSPI_CLK to QSPI_D[3:0] maximum skew	50	ps
3	Approximate maximum routing distances	3214	mils
4	Approximate maximum routing skew	357	mils
5	A series termination resistor (R1 in diagram above) should be placed close to the QSPI_CLK transmit pin of the AM263x to control rise-time and reflections of the clock line.	Variable, 0 to 40	Ω
6	A series termination resistor (R2 in diagram above) should be placed close to the QSPI data pins of the attached memory to control rise-time and reflections of the data lines.	Variable, 0 to 40	Ω

Table 5-3. AM263Px OSPI – Recommended Routing Rules

Spec No.	Specification	Value	Unit
1	OSPI_CLK, OSPI_CS0, OSPI_D[7:0] maximum delay	450	ps
2	OSPI_CLK to OSPI_D[7:0] and OSPI_CS _n maximum skew	60	ps
3	OSPI_CLK to OSPI_DQS maximum skew	30	ps
4	Approximate maximum routing distances	3214	mils
5	OSPI_CLK to OSPI_D[7:0] and OSPI_CS _n approximate maximum routing skew	429	mils
6	OSPI_CLK to OSPI_DQS approximate maximum routing skew	214	mils
7	A series termination resistor (R1 in diagram above) should be placed close to the OSPI_CLK transmit pin of the AM263Px to control rise-time and reflections of the clock line.	Variable, 0 to 40	Ω
8	Series termination resistor should be placed close to the OSPI data pins of the attached memory and the AM263Px device to control rise-time and reflections of the data lines.	Variable, 0 to 40	Ω

Note

Approximate routing distances are computed assuming a typical 140 ps/inch propagation delay in 50-Ω FR4 Microstrip or Stripline transmission lines. A 2D field solver or appropriate closed-form approximate impedance model should be used to find more exact propagation delay for your specific stackup and routing.

5.3 ROM OSPI/QSPI Boot Requirements

For more information concerning QSPI flash memory compatibility and boot requirements, see the [AM263x QSPI Flash Selection Guide](#).

Note

The S25FL128SAGNFI000 devices from Infineon were utilized on the AM263x controlCard and LaunchPad EVM and the IS25LX256-LHLE device from ISSI was utilized on the AM263Px controlCard.

6 JTAG Emulators and Trace

The AM263x and AM263Px MCUs support multiple different classes of JTAG emulators with or without additional ARM Trace capture capabilities.

For out of box convenience the LP-AM263, LP-AM263P, TMDSCNCD263, and TMDSCNCD263P EVM designs implement an onboard XDS110 emulator with JTAG and auxiliary UART-USB bridge is implemented with a TI TM4C MCU and high-voltage isolation. However, for actual custom systems, a simpler JTAG/Trace debug header should be implemented. This allows for external JTAG and Trace pods to be attached to the system as needed during development. The header can then be removed entirely or depopulated for full production of the system to save cost.

One popular, JTAG and Trace implementation is the MIPI industry standard MIPI-60 shown in [13]. This is based on the Samtec QSH-030-01-L-D-A. This implementation is compatible with TI XDS560v2 JTAG/Trace pods as well as other third-party JTAG/Trace pods. Additional, TI JTAG debugger connections can be found in [14].

8 Digital Peripherals

8.1 General Digital Peripheral Routing Guidelines

The following general routing recommendations should be followed throughout an AM263x or AM263Px PCB design. The 45nm LVCMOS process I/O can produce relatively fast edge-rates. Without transmission-line effects planned for, this can result in severe overshoot/undershoot even with relatively short traces on the PCB. These uncontrolled level transitions can damage associated components by presenting attached I/O with over/under-voltage conditions. Additionally, these uncontrolled transitions can radiate excessively which creates cross-talk and EMI compliance problems.

To mitigate these problems:

- Route all digital I/O as controlled impedance transmission-lines (Microstrip/Stripline)
- Place series termination near each AM263x or AM263Px transmit pin and attached transmit pins of associated IC
 - The values and performance of these termination resistors should be validated during wake-up of new PCB hardware.
 - In some cases, these termination resistors may not be required, but they should only be removed or eliminated from the design after testing
- Route with solid ground return planes on adjacent layers
- Route with ground return rings surrounding constantly switching signals (clocks, EPWM)
- Route with ground return rings surrounding sensitive analog signals (ADC/DAC channels, VREF)

For additional guidance on peripheral routing please reference [High-speed Interface Layout Guidelines](#).

9 Analog Peripherals

9.1 General Analog Peripheral Routing Guidelines

The following general routing recommendations should be followed throughout the analog portions of an AM263x or AM263Px PCB design. Analog signals are especially sensitive to cross talk and requiring clean signal return paths for maximizing signal integrity.

To mitigate these problems:

- Isolate all analog signals as much as possible with ground isolation between the analog trace and any adjacent trace
- Route analog signals with solid ground return layers on adjacent layers
- Avoid routing analog signals near high speed or current signals
 - When impossible to totally avoid high speed or current signals, cross the traces perpendicularly to avoid as much cross-talk as possible
- Adding signal amplifier and filter networks can promote signal integrity

For the SAR ADCs on AM263x and AM263Px, reference the *Choosing an Acquisition Window Duration* section of the [AM263Px Sitara™ Microcontroller Technical Reference Manual](#) and [AM263Px Sitara™ Microcontroller Technical Reference Manual Addendum](#) for additional guidance.

9.1.1 Resolver ADC Routing Guidelines

The AM263Px Sensor package includes two Resolver to Digital Converter (RDC) peripherals. A resolver is a type of rotary electrical transformer used for measuring degrees of rotation which is typically attached to an electrical motor. A typical resolver consists of a rotary transformer (exciter winding) and two windings separated by 90 degrees on the stator. An excitation sinusoidal signal is applied to the excitation coil of the resolver and the motor's rotation causes modulated sine and cosine outputs on the sine and cosine sense coils of the resolver. The angle of the modulated sine and cosine signals is directly related to the mechanical angle of the rotor compared to the stator and the speed of the motor rotation.

The AM263Px RDCs generate an excitation signal as a PWM which is routed through an excitation amplifier before being applied to the exciter winding on the motor resolver. The resolver sine and cosine outputs are then routed back into the RDC analog inputs, where the RDC IP converts and interprets the signals to determine motor angle and rotational speed. Figure 9-1 shows an example block diagram of a resolver based solution with an AM263P device.

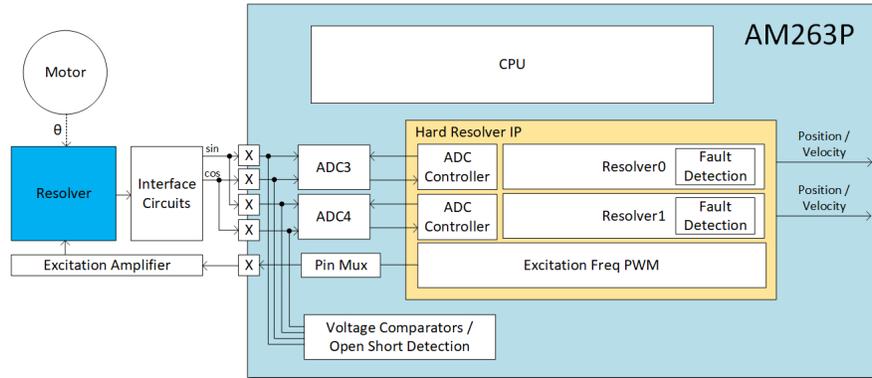


Figure 9-1. AM263P Resolver ADC System

The excitation PWM signals from the AM263Px support up to 20KHz and should follow the same guidelines for PCB routing as other similar frequency digital signals. For guidance on routing digital signals, see [General Digital Peripheral Routing Guidelines](#).

The Excitation Amplifier is used to convert the excitation PWM signals to sine waves as inputs to the motor resolver. These signals and the sine and cosine signals output from the resolver to the RDC inputs of the AM263Px should follow the same guidelines for PCB routing as other analog signals. For guidance on routing analog signals, see [General Analog Peripheral Routing Guidelines](#).

10 Layer Stackup

The AM263x and AM263Px MCUs are packaged in a ZCZ0324A 324 ball, 0.8mm pitch, 18 x 18 full NFBGA array [1][4]. The larger pitch on this package allows for a low layer count power and full signal fan-out. In the case of the LP-AM263 EVM, a 6-layer stackup design was able to fully route all power and signal pins across the device for the LaunchPad form-factor of boards.

Lower layer count stackup are likely possible, especially when considering partial signal fan-out designs. However, these have not yet been explored by TI at this time. The LP-AM263 LaunchPad EVM represents the most optimized stackup example at this time, so the LaunchPad is referenced in this section.

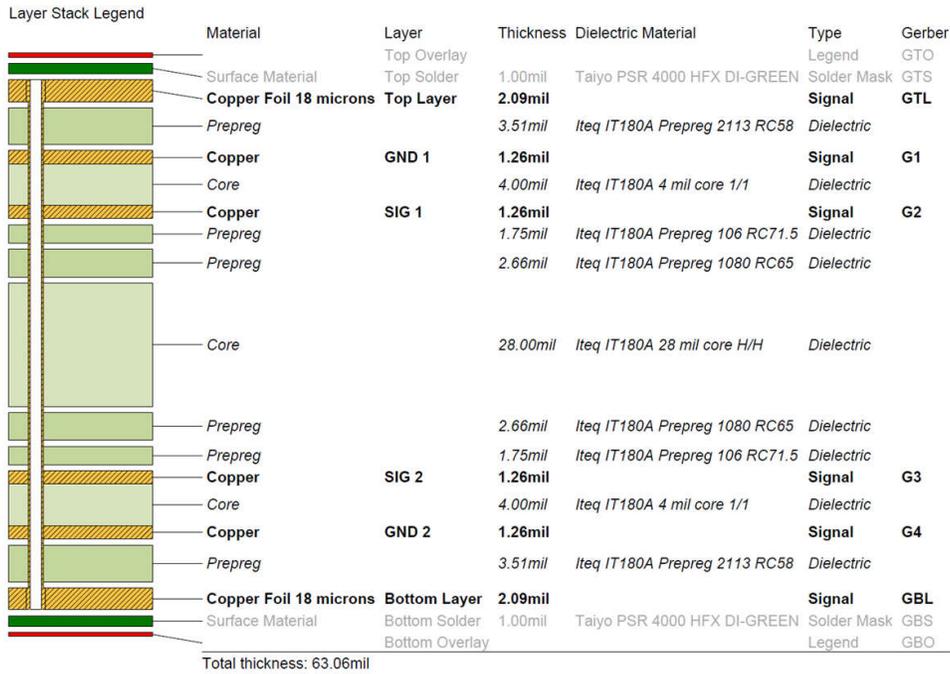


Figure 10-1. LP-AM263 Stackup

10.1 Key Stackup Features

- Standard 62 mil total thickness
- 4, optionally controlled impedance routing layers on L1, L3, L4 and L6.
- All signal and power layers all have adjacent ground reference for controlled impedance planning and EMI performance
- The use of a thicker, 28 mil center core layer, relative to the 4 mil, L2-L3 and L4-L5 dielectric layers, allows for L3 and L4 copper layers to be used as controlled impedance, embedded Microstrip or Stripline routing layers internally due to the low broad-side coupling between L3 and L4.
- Minimal dielectric thickness between L4 power and L5 GND return layers for best plane capacitance performance, aiding power integrity and EMI.
- Example fan-out with all through-hole via layer transitions – no micro-via or via-in-pad necessary.

Table 10-1. LP-AM263 Layer Utilization

Layer Number	Comment
Copper 1 (Top)	Top layer mounting and signal routing
Copper 2	Ground return plane
Copper 3	Embedded Microstrip/Stripline signal routing and power routing
Copper 4	Embedded Microstrip/Stripline and power routing
Copper 5	Ground return plane
Copper 6 (Bottom)	Bottom layer mounting and signal routing

Table 10-2. Controlled Impedance Planning Options

Layer Number	Reference Layer Number	Structure Name ⁽¹⁾	Trace Width (mils)	Trace Separation (mils)	Target Impedance (Ω)	Calculated Impedance (Ω)	Notes
L1	L2	Coated Microstrip	5.300	0.000	50.000	50.140	
L1	L2	Edge Coupled Coated Microstrip	4.200	5.000	90.000	89.830	L1, USB differential
L1	L2	Edge Coupled Coated Microstrip	4.000	7.700	100.000	99.840	

Table 10-2. Controlled Impedance Planning Options (continued)

Layer Number	Reference Layer Number	Structure Name ⁽¹⁾	Trace Width (mils)	Trace Separation (mils)	Target Impedance (Ω)	Calculated Impedance (Ω)	Notes
L1	L2	Edge Coupled Coated Microstrip	4.100	6.800	120.000	120.030	
L3	L3	Offset Stripline	4.750	0.000	50.000	49.960	
L3	L2	Edge Coupled Offset Stripline	4.000	6.000	90.000	90.040	L3, USB differential
L3	L2	Edge Coupled Offset Stripline	3.500	8.100	100.000	99.880	
L3	L2	Edge Coupled Offset Stripline	4.000	12.000	100.000	100.160	
L6	L5	Coated Microstrip	5.300	0.000	50.000	50.140	
L6	L5	Edge Coupled Coated Microstrip	4.200	5.000	90.000	89.830	
L6	L5	Edge Coupled Coated Microstrip	4.000	7.700	100.000	99.840	
L6	L4	Edge Coupled Coated Microstrip	4.100	6.800	120.000	120.030	

(1) All impedance calculated using Polar 2D field solver on given copper and dielectric thicknesses, widths and dissipation constants.

11 Vias

The AM263x and AM263Px EVMs show different examples of via construction for BGA fan-out and overall board routing. The AM263x LaunchPad is an example of PTH via only construction. The AM263x controlCard made use of via-in-pad with PTH via construction. The via-in-pad construction was used to provide minimal decoupling capacitor mounting distances from the BGA. This resulted in a more optimal power distribution network at the cost of additional fabrication cycle time per PCB.

Table 11-1. AM263x EVM Via Types

EVM	Via Type	Via Diameter (mils)	Via Drill (mils)
AM263x and AM263Px LaunchPads	PTH	18.000	8.000
AM263x and AM263Px controlCards	PTH	18.000	8.000
	PTH via-in-pad	18.000	8.000

12 BGA Power Fan-Out and Decoupling Placement

45 nm CMOS technology allows for faster core and SRAM clock rates, and faster edge rates for LVCMOS I/O buffers. Therefore, in comparison with previous MCU process nodes, careful power and ground return placement is critical to achieving best power integrity, signal integrity and EMI performance with AM263x and AM263Px designs.

It is recommended that designers follow a similar power distribution layout as implemented in the AM263x and AM263Px EVM PCB designs to achieve good power integrity results across all operating conditions and EMI testing conditions.

The TMDSCNCD263 controlCard EVM represents the most optimized and scrutinized power distribution layout example so far and so the controlCard is referenced in this section.

12.1 Ground Return

All available ground return BGA must be utilized to create the best possible electrical and thermal connection between the AM263x or AM263Px package and the attached PCB. Maximizing VSS BGA usage is critical from signal integrity, EMI/EMC and thermal perspectives.

Unless a separate top package heatsink is used in the design, the VSS BGA (and VDDCORE to a lesser extent) are the only heat sinking thermal connection for the BGA package. For required, thermal performance, AM263x or AM263Px PCB designs must adhere to following thermal via design requirements.

- A minimum of 49 VSS vias in the center of the BGA must be shorted to PCB ground return planes. However, if possible, and for best thermal performance, all VSS BGA should be connected to PCB ground return planes
- Solid ground return planes shall be used directly under the BGA on as many layers as possible.
- Solid ground return, or the widest possible traces shall be used on the top or bottom mounting layer for VSS BGA pad connection
- VSS via drills shall use largest possible drill diameter. This will maximize surface area of the via, providing lowest thermal resistance.
- VSS vias should be conductively filled, if possible.

All of these thermal via requirements must be balanced against the necessary power and signal fan-out of the design.

The AM263x and AM263Px devices contain both analog and digital ground return pins. Both analog and digital ground return pins should be shorted to a common set of ground return planes on the PCB for best noise and EMI performance as this creates the lowest possible impedance path for all return currents to follow. It is not recommended to separate these two return paths as this typically ends up with lower performance return paths for both digital and analog signal paths.

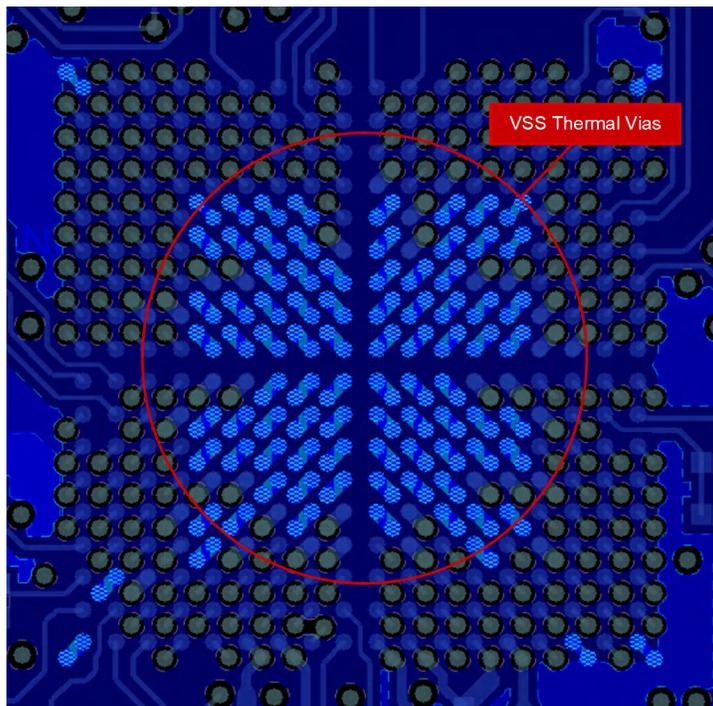


Figure 12-1. AM263x controlCARD Excerpt – Ground Return Via Under AM263x BGA Layer 1 and Layer

2

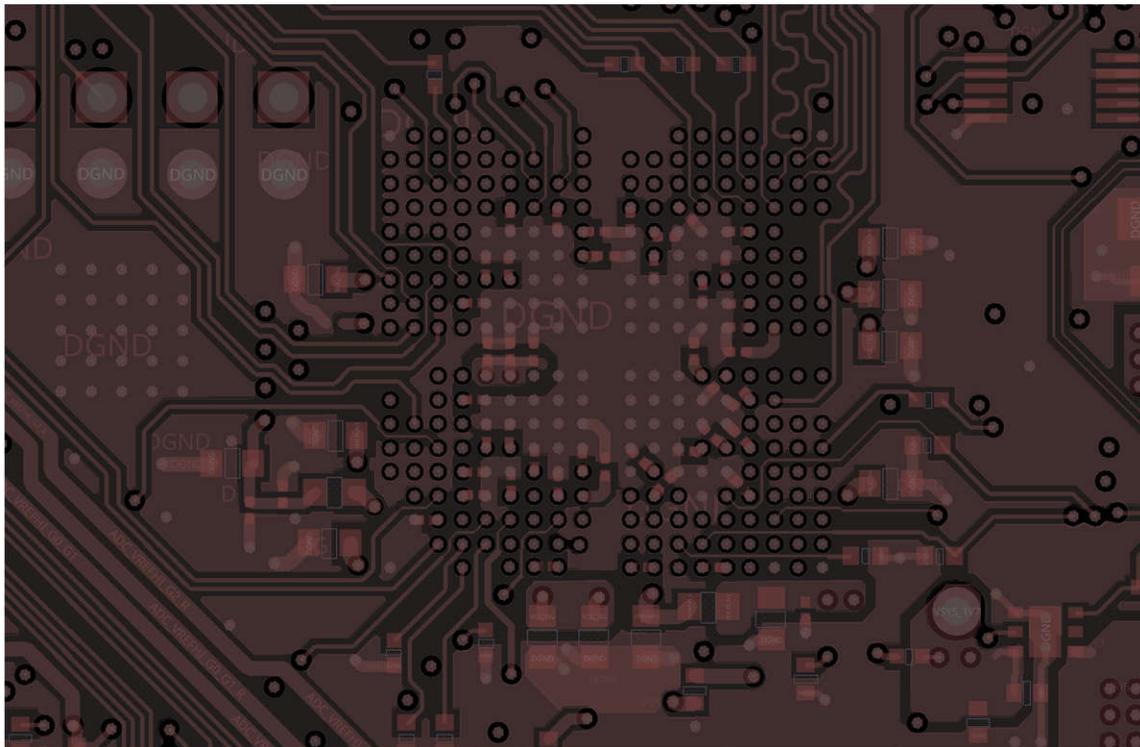


Figure 12-2. AM263x controlCARD Excerpt – Ground Return Vias Under AM263x BGA Layer 10

12.2 1.2 V Core Digital Power

This section summarizes the main elements of the 1.2 V core digital power routing of the AM263x controlCARD EVM (TMDSCNCD263) from the 1.2 V buck-converter (TPS62913RPUR, U65) through the board power planes and ending in at the BGA bulk and per pin decoupling capacitor array.

12.2.1 Key Layout Considerations

- AM263x or AM263Px should be co-located with the 1.2 V core digital regulator to allow for minimal IR drop from the regulator to the BGA power pins.
- Wide 15 mil traces should be used for all power and ground return via fan-out.
- A dedicated power layer, with tightly coupled ground return reference plane should be used for best transient performance and EMI coupling
- A wide power plane entry into the center of the BGA 1.2 V power pin areas should be used for minimal IR drop and best transient performance
- Larger packaged, lower-frequency, bulk capacitance should be placed adjacent to the BGA with vias directly to power plane paths
- Smaller packaged, higher-frequency decoupling capacitance should be placed directly on BGA fan-out vias with as small of a dog-bone to power and ground return vias as possible

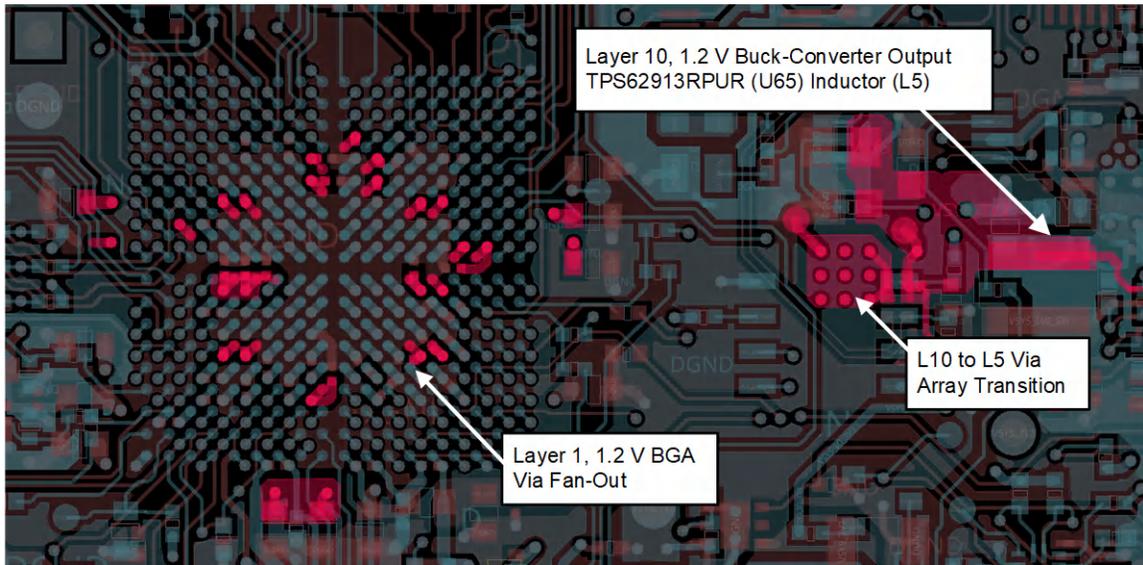


Figure 12-3. AM263x controlCARD Excerpt – 1.2 V Core Power Output, Power Plane Vias and BGA Vias

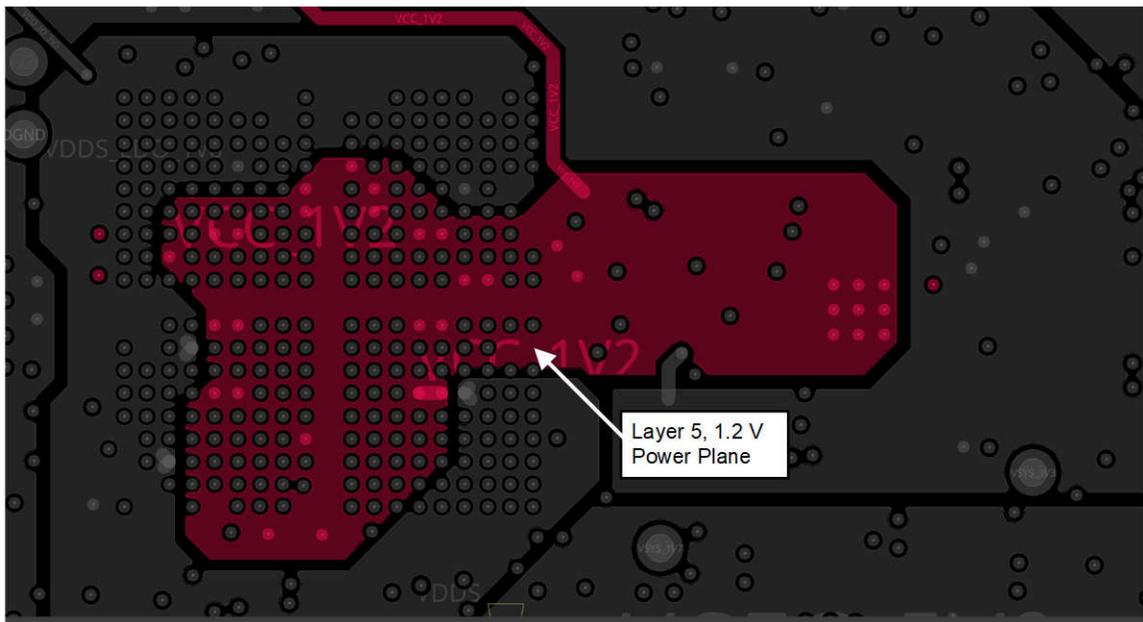


Figure 12-4. AM263x controlCARD Excerpt – 1.2 V Core Power Plane, Layer 5

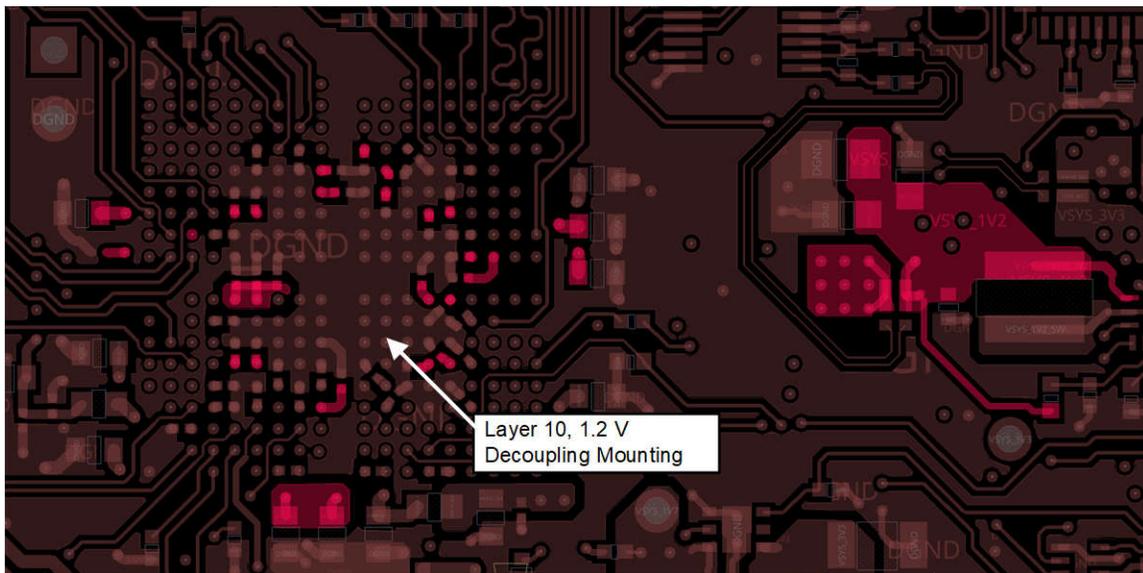


Figure 12-5. AM263x controlCARD Excerpt – 1.2 V Core Power Decoupling Mounting, Layer 10

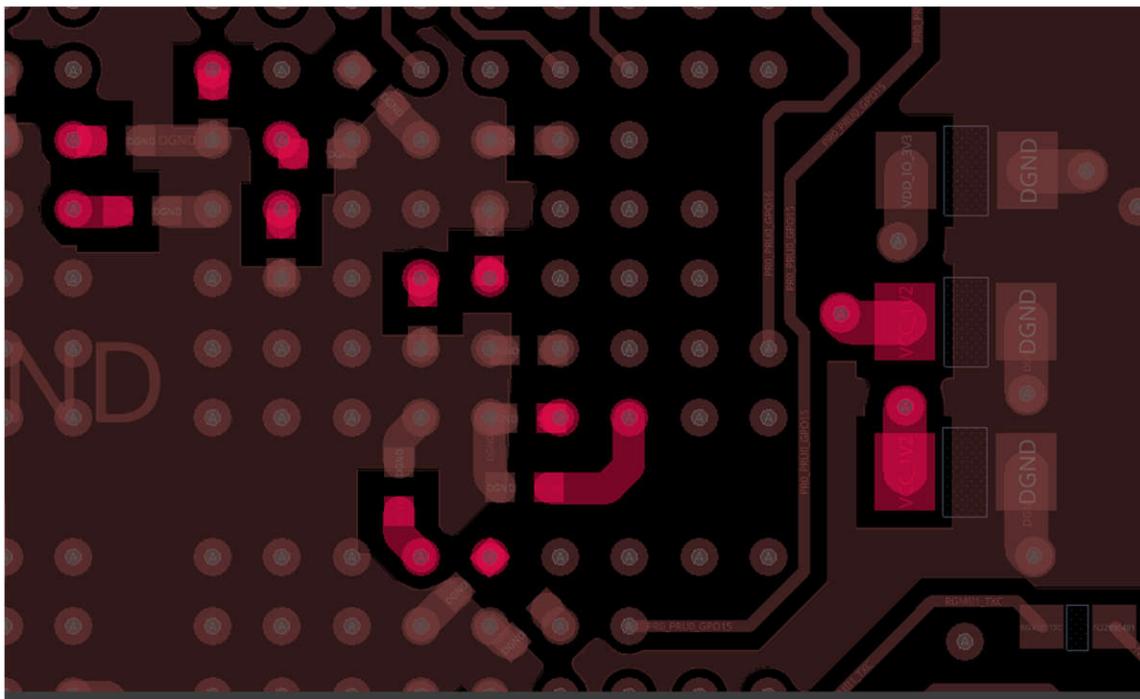


Figure 12-6. AM263x controlCARD Excerpt – 1.2 V Core Power Decoupling Mounting, Layer 10

12.3 3.3 V Digital and Analog Power

This section summarizes the main elements of the 3.3 V digital I/O and analog I/O power routing of the AM263x controlCARD EVM (TMDSCNCD263) from the 3.3 V buck-converter (TPS62913RPUR, U30) through the board power planes and ending in at the BGA bulk and per pin decoupling capacitor array.

A common buck-converter supplies power for all of the AM263x digital I/O, analog I/O and the rest of the controlCard 3.3 V loads. This is common in most designs where all 3.3 V digital level I/O share a common power supply.

Additional filtering for the local AM263x 3.3 V analog power net is done through the LC filter of ferrite-bead FL13 and associated capacitors. This is used to create a low-IR drop low-pass filter that attenuates the higher frequency switching harmonics of the TPS62913RPUR regulator.

12.3.1 Key Layout Considerations

- Wide 15 mil traces should be used for all power and ground return via fan-out.
- 3.3 V I/O power tends to be shared across multiple devices in the system, recommend routing with very wide power planes across the PCB to minimize IR drops to all components including the AM263x or AM263Px
- A tightly coupled, adjacent ground return reference plane should be used for best transient performance and EMI coupling
- A wide power plane entry that covers the BGA 3.3 V power pin areas should be used for minimal IR drop and best transient performance
- Larger packaged, lower-frequency, bulk capacitance should be placed adjacent to MCU BGA with vias directly to power plane paths
- Smaller packaged, higher-frequency decoupling capacitance should be placed directly on BGA fan-out vias with as small of a dog-bone to power and ground return vias as possible

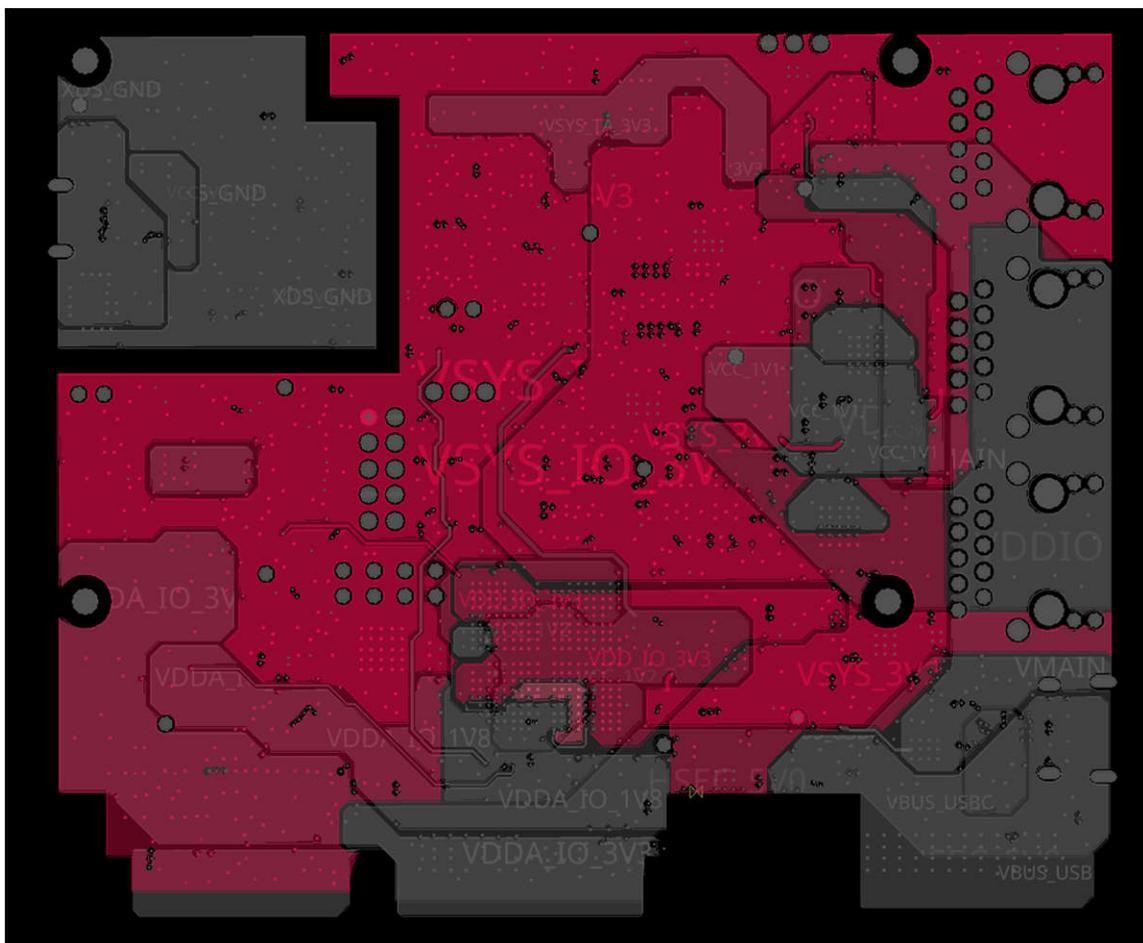


Figure 12-7. AM263x controlCARD Excerpt – 3.3 V Digital and Analog Power Planes on Layer 5 and Layer 6

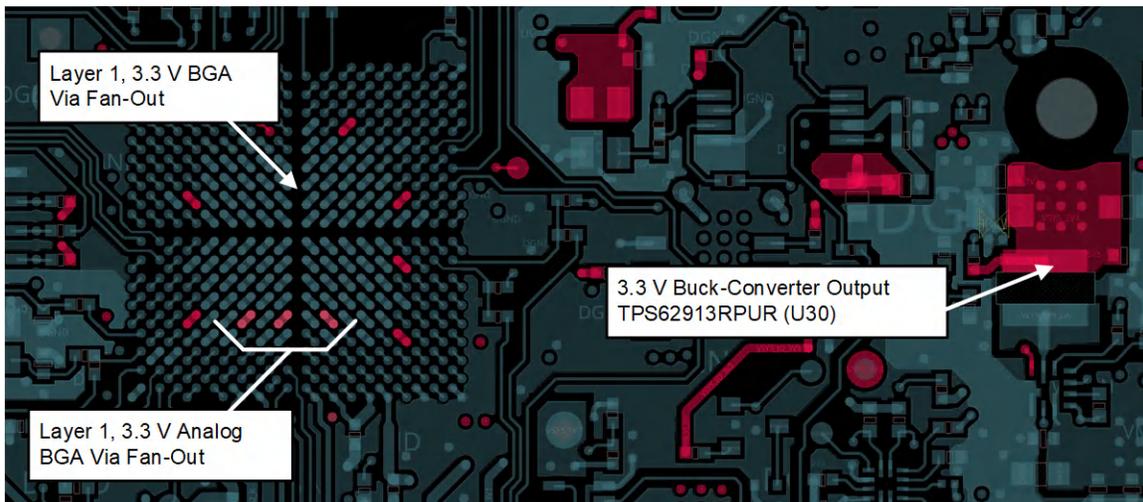


Figure 12-8. AM263x controlCARD Excerpt – 3.3 V Digital I/O and Analog I/O BGA Pinout and Regulator Output

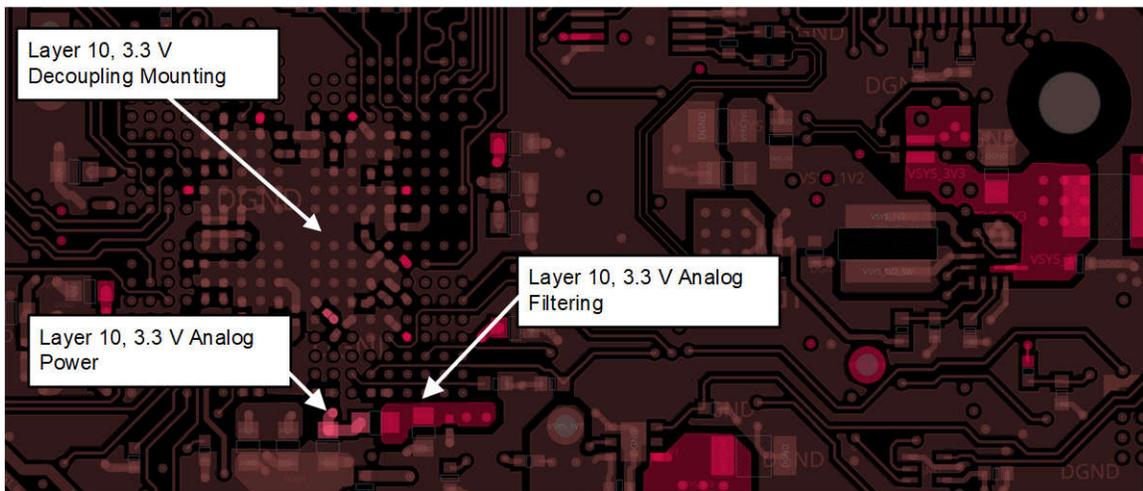


Figure 12-9. AM263x controlCARD Excerpt – Common 3.3 V Plane Transition Vias

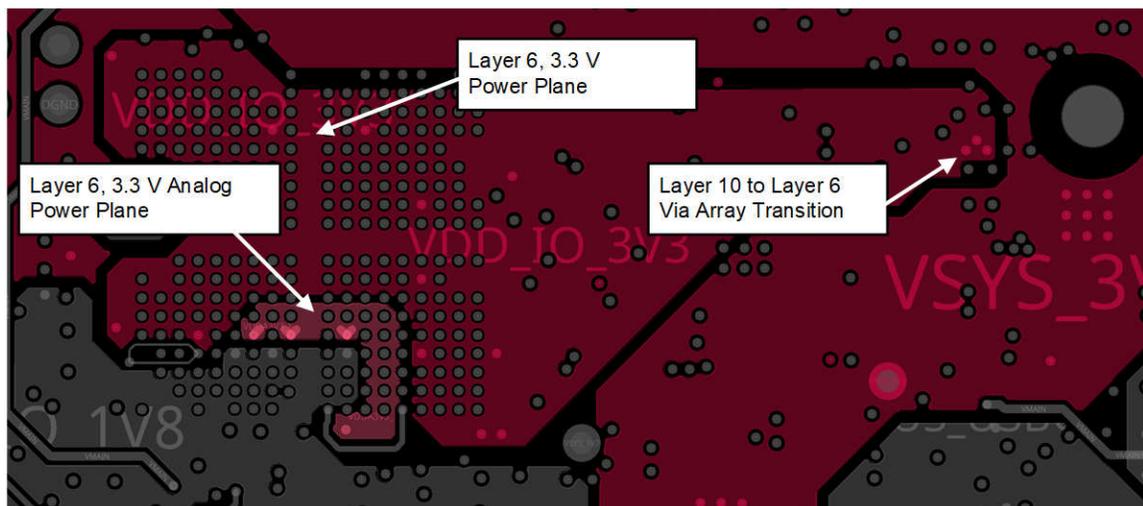


Figure 12-10. AM263x controlCARD Excerpt – 3.3 V Digital and Analog Planes Layer 6

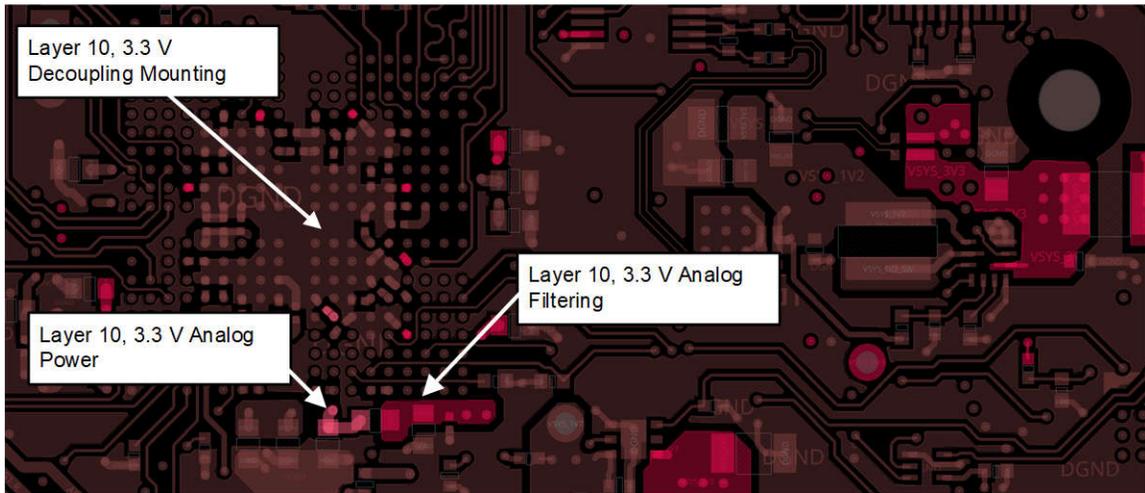


Figure 12-11. AM263x controlCARD Excerpt – 3.3 V Digital and Analog Power Decoupling Mounting, Layer 10

12.4 1.8 V Digital and Analog Power

This section summarizes the main elements of the 1.8 V digital I/O and analog I/O power routing of the AM263x controlCARD EVM (TMDSCNCD263). Both 1.8 V power nets are generated from on-chip LDO which are in turn supplied by either the 3.3 V digital or 3.3 V analog power nets from the PCB.

Additional filtering for the local AM263x 1.8 V PLL power net is done through the LC filter of ferrite-bead FL12 and associated capacitors. This is used to create an additional low-IR drop low-pass filter that will attenuate any high frequency noise present on the 1.8 V LDO analog output.

12.4.1 Key Layout Considerations

- Wide, minimum 15 mil traces, should be used for all power and ground return via fan-out.
- 1.8 V digital and analog is generated from on-chip LDO and so is highly localized to the BGA pinout
- A tightly coupled, adjacent ground return reference plane should be used for best transient performance and EMI coupling
- Smaller power planes or wider traces should be used for minimal IR drop and best transient routing across the associated BGA pins
- Smaller packaged, higher-frequency decoupling capacitance should be placed directly on BGA fan-out vias with as small of a dog-bone to power and ground return vias as possible

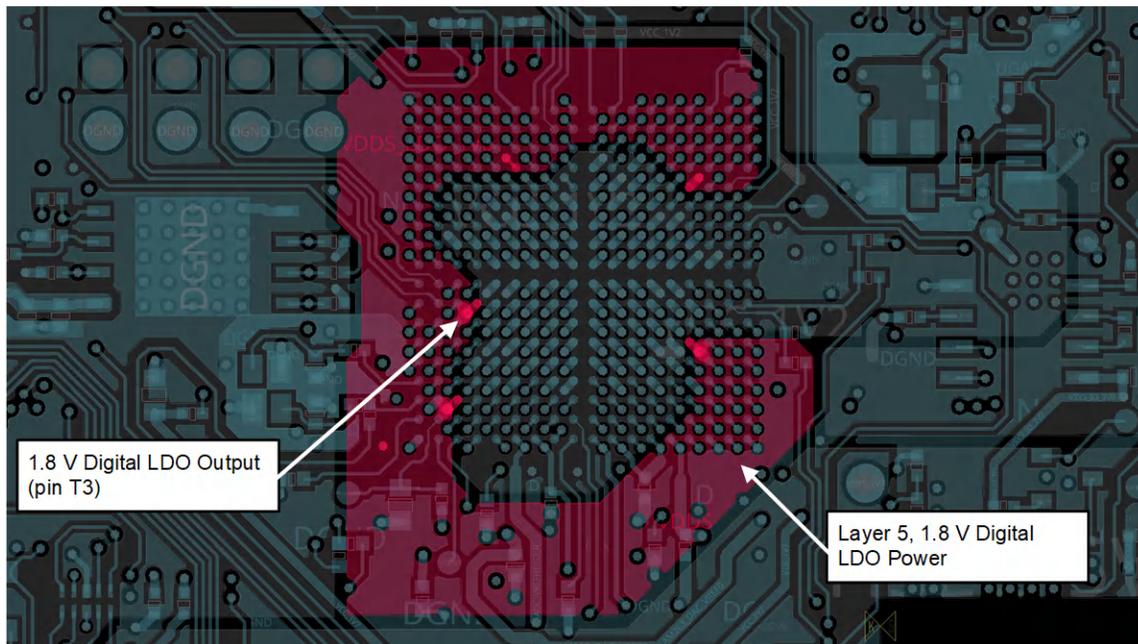


Figure 12-12. AM263x controlCARD Excerpt – 1.8 V Digital Power Via Fan-Out and Plane Routing Layer 6

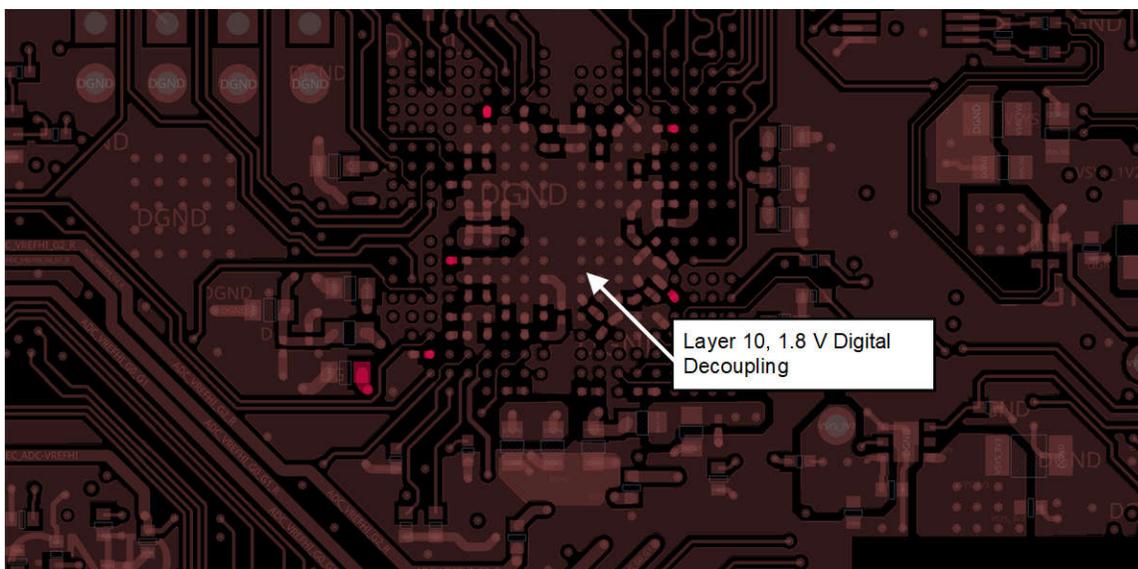


Figure 12-13. AM263x controlCARD Excerpt – 1.8 V Digital Power Decoupling on Layer 10

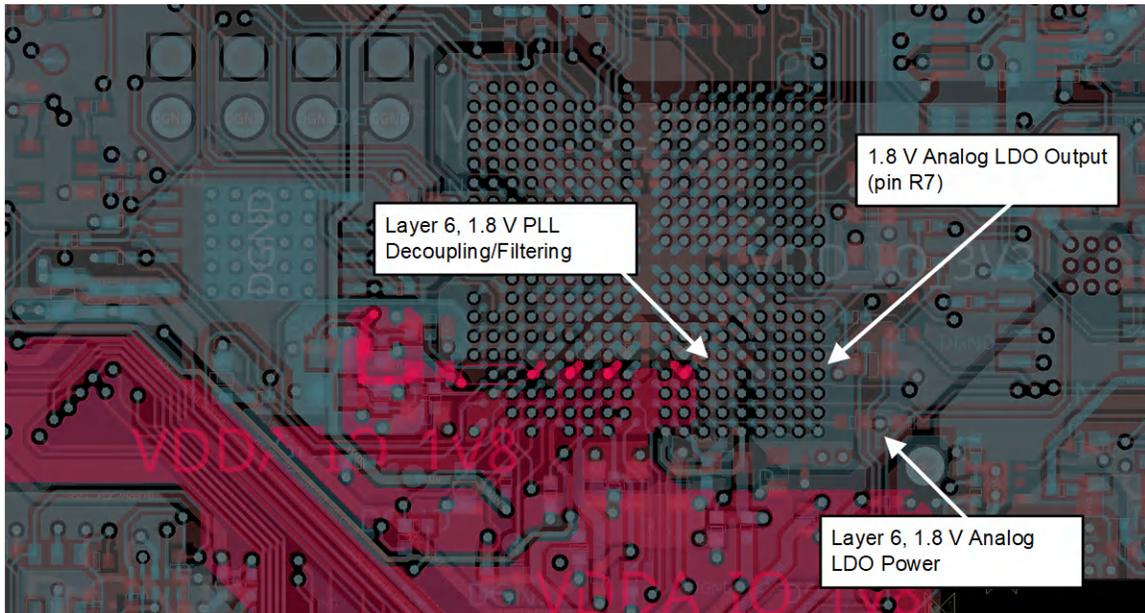


Figure 12-14. AM263x controlCARD Excerpt – 1.8 V Analog Power Via Fan-Out and Plane Routing Layer 6

Note

Figure 2-13 shows an example of a suboptimal routing between the FL12 filter output and the BGA pads. Ideally the output of the FL12 filter should be routed as a wide trace or small plane, and not smaller traces as was done on this initial revision of the controlCard EVM.

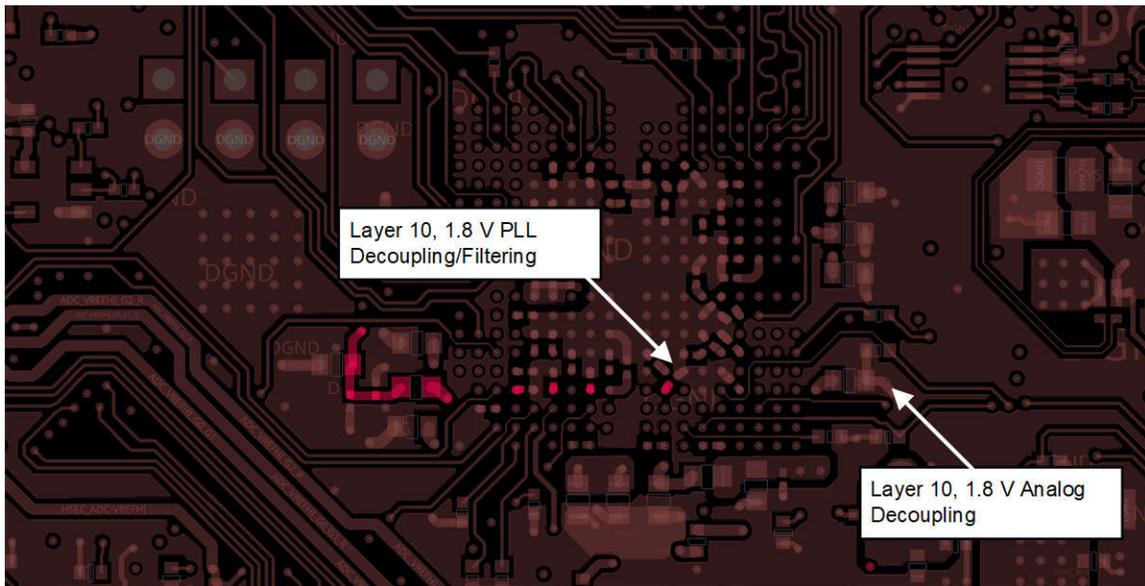


Figure 12-15. AM263x controlCARD Excerpt – 1.8 V Analog Power Decoupling on Layer 10

13 References

1. Texas Instruments: [AM263x Sitara™ Microcontroller Data Sheet](#)
2. Texas Instruments: [AM263x Sitara™ Microcontroller Technical Reference Manual](#)
3. Texas Instruments: [AM263x Sitara™ Microcontroller Technical Reference Manual Addendum](#)
4. Texas Instruments: [AM263Px Sitara™ Microcontroller Data Sheet](#)
5. Texas Instruments: [AM263Px Sitara™ Microcontroller Technical Reference Manual](#)
6. Texas Instruments: [AM263Px Sitara™ Microcontroller Technical Reference Manual Addendum](#)
7. AM263x Control Card EVM Design: <https://www.ti.com/tool/TMDSCNCD263>
8. AM263x Launchpad EVM Design: <https://www.ti.com/tool/LP-AM263>
9. AM263Px Control Card EVM Design: <https://www.ti.com/tool/TMDSCNCD263P>
10. AM263Px Launchpad EVM Design: <https://www.ti.com/tool/LP-AM263P>
11. Texas Instruments: [High-speed Interface Layout Guidelines](#)
12. Texas Instruments System Configuration Tool (SYSCONFIG): <https://www.ti.com/tool/SYSCONFIG>
13. MIPI Alliance Recommendation for Debug and Trace Connectors: <https://www.mipi.org/sites/default/files/MIPI-Alliance-Recommendation-Debug-Trace-Connectors.pdf>
14. JTAG Connectors and Pinout: https://software-dl.ti.com/ccs/esd/documents/xdsdebugprobes/emu_jtag_connectors.html
15. Texas Instruments: [AM263x QSPI Flash Selection Guide](#)
16. AM263x MCU Software Development Kit: [MCU-PLUS-SDK-AM263X](#)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2023) to Revision B (November 2023)	Page
• Added AM263Px throughout the document.....	1
• Introduction: added example system block diagram showing PMIC based power solution.....	2
• Integrated PMIC Power Solution: updating to reference TMDSCNCD263P PMIC solution.....	7
• Power Decoupling and Filtering: added schematic example for ADC_VREFHI_G3 and ADC_VREFLO_G3 on AM263Px Sensor package.....	8
• e-Fuse Power: updated to include AM263Px internally sourcing VPP.....	18
• SOP Signal Implementation: Added AM263P Bootmodes.....	23
• OSPI/QSPI Memory Implementation: added AM263Px and OSPI information.....	25
• Added Analog Peripherals section.....	31

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