ADS981x 18-Bit, 2-MSPS/Ch, Dual, Simultaneous-Sampling ADC With Integrated Analog Front-End

1 Features

- 8-channel, 18-bit ADC with analog front-end:
  - Dual, simultaneous sampling: 4 × 1 channels
  - Constant 1-MΩ input impedance front-end
- Programmable analog input ranges:
  - ±12 V, ±10 V, ±7 V, ±5 V, ±3.5 V, and ±2.5 V
  - Single-ended and differential inputs
  - ±12-V common-mode voltage range
  - Input overvoltage protection: Up to ±18 V
- User-selectable analog input bandwidth:
  - 21 kHz and 400 kHz
- Integrated low-drift precision references
  - ADC reference: 4.096 V
  - 2.5-V reference output for external circuits
- Excellent AC and DC performance at full-throughput:
  - DNL: ±0.3 LSB, INL: ±1.5 LSB
  - SNR: 92.2 dB, THD: –112 dB
- Power supply:
  - Analog and digital: 5 V and 1.8 V
  - Digital interface: 1.2 V to 1.8 V
- Temperature range: –40°C to +125°C

2 Applications

- Semiconductor tests
- Battery tests
- Data acquisition (DAQ)

3 Description

The ADS981x is an 8-channel data acquisition (DAQ) system based on a dual, simultaneous-sampling, 18-bit successive approximation register (SAR) analog-to-digital converter (ADC). The ADS981x features a complete analog front-end for each channel with an input clamp protection circuit, 1-MΩ input impedance, and a programmable gain amplifier (PGA) with user-selectable bandwidth options. The high input impedance allows direct connection with sensors and transformers, thus eliminating the need for external driver circuits. The ADS981x can be configured to accept unipolar or bipolar inputs with up to a ±12-V common-mode voltage.

The device also features a 4.096-V reference for the ADC and a 2.5-V reference output for use with external circuits. A digital interface supporting 1.2-V to 1.8-V operation enables the ADS981x to be used without external voltage level translators.

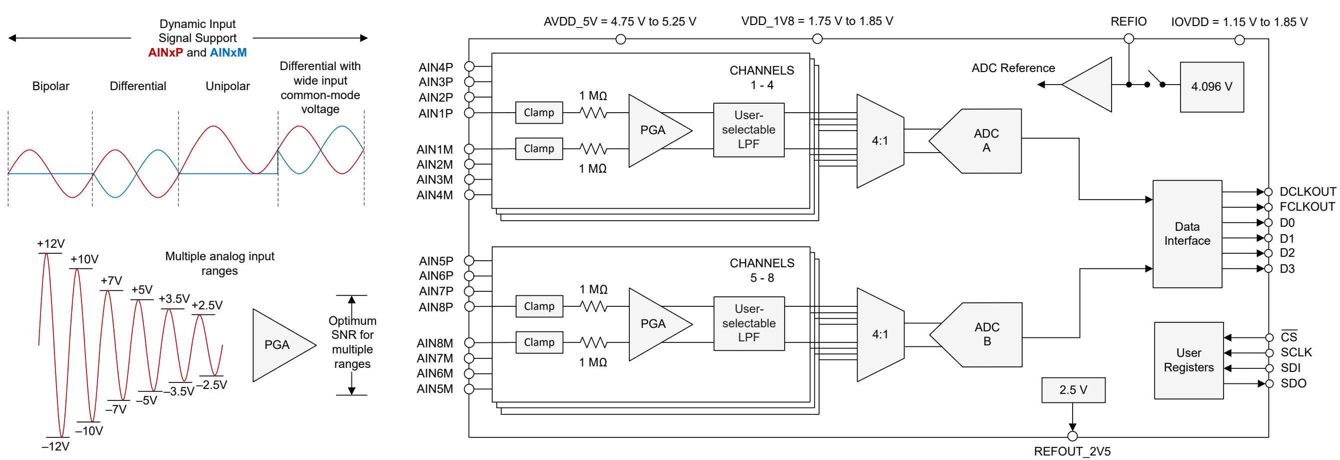
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADS981x	RSH (VQFN, 56)	7 mm × 7 mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER	SPEED	TOTAL POWER
ADS9817	2 MSPS/channel	232 mW
ADS9815	1 MSPS/channel	160 mW



Device Block Diagram

Table of Contents

4 Pin Configuration and Functions

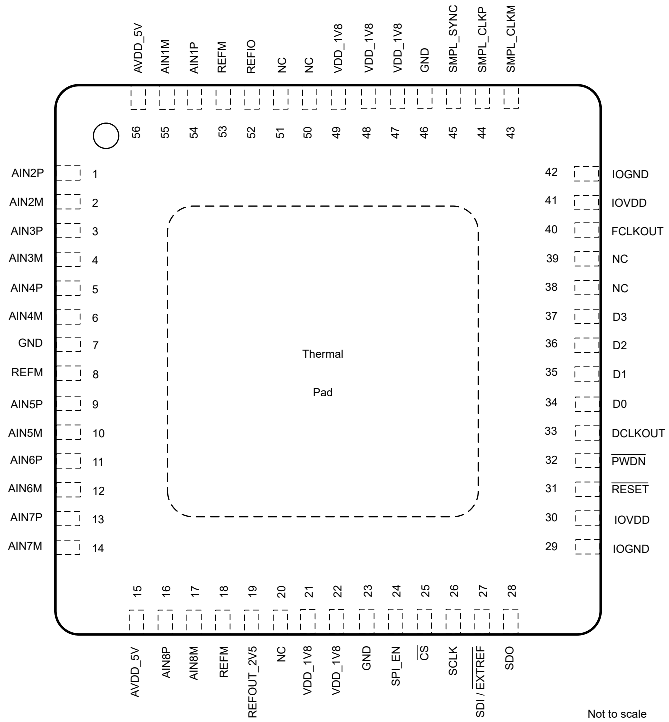


Figure 4-1. RSH Package, 56-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
AIN1M	55	AI	Analog input channel 1, negative input.
AIN1P	54	AI	Analog input channel 1, positive input.
AIN2M	2	AI	Analog input channel 2, negative input.
AIN2P	1	AI	Analog input channel 2, positive input.
AIN3M	4	AI	Analog input channel 3, negative input.
AIN3P	3	AI	Analog input channel 3, positive input.
AIN4M	6	AI	Analog input channel 4, negative input.
AIN4P	5	AI	Analog input channel 4, positive input.
AIN5M	10	AI	Analog input channel 5, negative input.
AIN5P	9	AI	Analog input channel 5, positive input.
AIN6M	12	AI	Analog input channel 6, negative input.
AIN6P	11	AI	Analog input channel 6, positive input.
AIN7M	14	AI	Analog input channel 7, negative input.
AIN7P	13	AI	Analog input channel 7, positive input.
AIN8M	17	AI	Analog input channel 8, negative input.
AIN8P	16	AI	Analog input channel 8, positive input.
AVDD_5V	15, 56	P	5-V analog supply. Connect 1-µF and 0.1-µF decoupling capacitors to GND.
$\overline{CS}$	25	DI	Chip-select input for SPI interface configuration; active low. This pin has an internal 100-kΩ pullup resistor to IOVDD.
D0	34	DO	Serial output data lane 0.
D1	35	DO	Serial data output lane 1.

Table 4-1. Pin Functions (continued)

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
D2	36	DO	Serial data output lane 2.
D3	37	DO	Serial data output lane 3.
DCLKOUT	33	DO	Clock output for data interface.
FCLKOUT	40	DO	Frame synchronization output for data interface.
GND	7, 23, 29, 42, 46	P	Ground.
IOVDD	30, 41	P	Digital I/O supply for data interface. Connect 1-µF and 0.1-µF decoupling capacitor to GND.
NC	20, 38, 39, 50, 51	—	Not connected. No external connection.
$\overline{\text{PWDN}}$	32	DI	Power-down control; active low. $\overline{\text{PWDN}}$ has an internal 100-kΩ pullup resistor to the digital interface supply.
REFIO	52	AI/AO	REFIO acts as an internal reference output when the internal reference is enabled. REFIO functions as an input pin for the external reference when the internal reference is disabled. Connect a 10-µF decoupling capacitor to the REFM pins.
REFM	8, 18, 53	AI	Reference ground potential. Connect to GND.
REFOUT_2V5	19	AO	2.5-V reference output. Connect a decoupling 10-µF capacitor to the REFM pins.
$\overline{\text{RESET}}$	31	DI	Reset input for the device; active low. $\overline{\text{RESET}}$ has an internal 100-kΩ pullup resistor to the digital interface supply.
SCLK	26	DI	Serial clock input for the configuration interface. $\overline{\text{SCLK}}$ has an internal 100-kΩ pulldown resistor to the digital interface ground.
SDI	27	DI	SDI is a multifunction logic input; pin function is determined by the SPI_EN pin. SDI has an internal 100-kΩ pulldown resistor to GND. SPI_EN = 0b: SDI is the logic input to select between the internal or external reference. Connect SDI to GND for the external reference. Connect SDI to IOVDD for the internal reference. SPI_EN = 1b: Serial data input for the configuration interface.
SDO	28	DO	Serial data output for the configuration interface.
SMPL_CLKP	44	DI	Single-ended ADC sampling clock input. SMPL_CLKP is the positive input for the differential sampling clock input to the ADC.
SMPL_CLKM	43	DI	Connect SMPL_CLKM to GND for a single-ended ADC sampling clock input. SMPL_CLKM is the negative input for the differential sampling clock input to the ADC.
SMPL_SYNC	45	DI	Synchronization input. See the *Sample Synchronization* section on how to use the SMPL_SYNC pin.
SPI_EN	24	DI	Logic input to enable the SPI interface configuration ($\overline{\text{CS}}$, SCLK, SDI, and SDO). SPI_EN has an internal 100-kΩ pullup resistor to the digital interface supply.
VDD_1V8	21, 22, 47, 48, 49	P	1.8-V power-supply. Connect 1-µF and 0.1-µF decoupling capacitors to GND.
Thermal pad	—	P	Exposed thermal pad; connect to GND.

(1) I = input, O = output, I/O = input or output, G = ground, and P = power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
AVDD_5V to GND	–0.3	6	V
VDD_1V8 to GND	–0.3	2.1	V
IOVDD to GND	–0.3	2.1	V
AINxP and AINxM to GND	–18	18	V
REFIO to REFM	REFM – 0.3	AVDD_5V + 0.3	V
REFM to GND	GND – 0.3	GND + 0.3	V
Digital inputs to GND	GND – 0.3	2.1	V
Input current to any pin except supply pins[(2)]	–10	10	mA
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Pin current must be limited to 10 mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD_5V	Analog power supply	AVDD_5V to GND, 5 V	4.75	5	5.25	V
VDD_1V8	Analog power supply	VDD_1V8 to GND, 1.8 V	1.75	1.8	1.85	V
IOVDD	Digital interface power supply	IOVDD to GND	1.15	1.8	1.85	V
REFERENCE VOLTAGE						
V_{REF}	Reference voltage to the ADC	External reference	4.092	4.096	4.100	V
ANALOG INPUTS						
V_{FSR}	Full-scale input range	RANGE_CHx = 0010b	–2.5		2.5	V
		RANGE_CHx = 0001b	–3.5		3.5	
		RANGE_CHx = 0000b	–5		5	
		RANGE_CHx = 0011b	–7		7	
		RANGE_CHx = 0100b	–10		10	
		RANGE_CHx = 0101b	–12		12	
AINxP	Operating input voltage, positive input		–17		17	V
AINxM	Operating input voltage, negative input		–17		17	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	125	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		ADS981x RSH (VQFN) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	6.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

at AVDD_5V = 4.75 V to 5.25 V, VDD_1V8 = 1.75 V to 1.85 V, IOVDD = 1.15 V to 1.85 V, V_{REF} = 4.096 V (internal or external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
R_{IN}	Input impedance	All input ranges	0.85	1	1.15	MΩ
	Input impedance thermal drift	All input ranges		10	25	ppm/°C
	Input capacitance			10		pF
ANALOG INPUT FILTER						
$BW_{(-3\ dB)}$	Analog input LPF bandwidth –3 dB	Low-bandwidth filter, all input ranges		21		kHz
		Wide-bandwidth filter, input range = ±2.5 V		182		
		Wide-bandwidth filter, input range = ±3.5 V		240		
		Wide-bandwidth filter, input range = ±5 V		320		
		Wide-bandwidth filter, input range = ±7 V		400		
		Wide-bandwidth filter, input range = ±10 V		385		
		Wide-bandwidth filter, input range = ±12 V		375		
DC PERFORMANCE						
	Resolution	No missing codes	18			Bits
DNL	Differential nonlinearity	Wide-CM enabled and disabled, all ranges	–0.99	±0.5	0.99	LSB
INL	Integral nonlinearity	Wide-CM enabled and disabled, all ranges, T_A = 0°C to 70°C	–4	±1.5	4	LSB
		Wide-CM enabled and disabled, all ranges, T_A = –40°C to 125°C	–4.5	±1.5	4.5	LSB
	Offset error	Wide-CM disabled, RANGE = ±2.5 V	–175	±90	175	LSB
		Wide-CM enabled, RANGE = ±2.5 V		±120		
		Wide-CM disabled, RANGE = ±3.5 V	–100	±60	100	
		Wide-CM enabled, RANGE = ±3.5 V		±80		
		Wide-CM disabled, RANGE = ±5 V	–50	±10	50	
		Wide-CM enabled, RANGE = ±5 V		±60		
		Wide-CM enabled, RANGE = ±7 V	–100	±35	100	
		Wide-CM enabled, RANGE = ±10 V	–50	±10	50	
		Wide-CM enabled, RANGE = ±12 V	–75	±15	75	
	Offset error matching	Wide-CM disabled, RANGE = ±2.5 V	0	300	512	LSB
		Wide-CM enabled, RANGE = ±2.5 V	0	450	750	
		Wide-CM disabled, RANGE = ±3.5 V	0	150	256	
		Wide-CM enabled, RANGE = ±3.5 V	0	300	512	
		Wide-CM disabled, RANGE = ±5 V	0	25	64	
		Wide-CM enabled, RANGE = ±5 V	0	175	296	
		Wide-CM enabled, RANGE = ±7 V	0	100	200	
		Wide-CM enabled, RANGE = ±10 V	0	25	64	
		Wide-CM enabled, RANGE = ±12 V	0	35	96	
	Offset error thermal drift	Wide-CM enabled and disabled, all ranges		0.5	1.5	ppm/°C
	Gain error	Wide-CM disabled, RANGE = ±2.5 V, ±3.5 V, and ±5 V	–130	±48	130	LSB
		Wide-CM enabled, RANGE = ±2.5 V, ±3.5 V, and ±5 V		±100		
		Wide-CM enabled, RANGE = ±7V, ±10 V, ±12 V	–130	±48	130	

5.5 Electrical Characteristics (continued)

at AVDD_5V = 4.75 V to 5.25 V, VDD_1V8 = 1.75 V to 1.85 V, IOVDD = 1.15 V to 1.85 V, V_{REF} = 4.096 V (internal or external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Gain error matching	Wide-CM disabled, RANGE = ±2.5 V, ±3.5 V, and ±5 V	0	±96	200	LSB
		Wide-CM enabled, RANGE = ±2.5 V, ±3.5 V, and ±5 V	0	±200	600	
		Wide-CM enabled, RANGE = ±7V, ±10 V, ±12 V	0	±96	200	
	Gain error thermal drift	Wide-CM enabled and disabled, all ranges		0.7	3	ppm/°C
AC PERFORMANCE						
SNR	Signal-to-noise ratio	Low-noise filter, f_{IN} = 2 kHz, range = ±2.5 V	86.7	89.5		dBFS
		Low-noise filter, f_{IN} = 2 kHz, range = ±3.5 V	87.8	90.5		
		Low-noise filter, f_{IN} = 2 kHz, range = ±5 V	88.5	91.4		
		Low-noise filter, f_{IN} = 2 kHz, range = ±7 V	89.3	91.3		
		Low-noise filter, f_{IN} = 2 kHz, range = ±10 V	89.9	91.8		
		Low-noise filter, f_{IN} = 2 kHz, range = ±12 V	90	92		
		Wide-bandwidth filter, f_{IN} = 2 kHz, range = ±2.5 V	79	82.5		
		Wide-bandwidth filter, f_{IN} = 2 kHz, range = ±3.5 V	80	83.5		
		Wide-bandwidth filter, f_{IN} = 2 kHz, range = ±5 V	80.5	84.5		
		Wide-bandwidth filter, f_{IN} = 2 kHz, range = ±7 V	81.5	83.5		
		Wide-bandwidth filter, f_{IN} = 2 kHz, range = ±10 V	83	85		
		Wide-bandwidth filter, f_{IN} = 2 kHz, range = ±12 V	83.5	85.5		
SINAD	Signal-to-noise + distortion ratio	Low-noise filter, f_{IN} = 2 kHz, range = ±2.5 V	85.7	88.9		dB
		Low-noise filter, f_{IN} = 2 kHz, range = ±3.5 V	86.7	89.9		
		Low-noise filter, f_{IN} = 2 kHz, range = ±5 V	87.3	90.7		
		Low-noise filter, f_{IN} = 2 kHz, range = ±7 V	88.0	90.6		
		Low-noise filter, f_{IN} = 2 kHz, range = ±10 V	88.5	91.1		
		Low-noise filter, f_{IN} = 2 kHz, range = ±12 V	88.6	91.3		
		Wide-bandwidth filter, f_{IN} = 2 kHz, range = ±2.5 V	78.6	82.2		
		Wide-bandwidth filter, f_{IN} = 2 kHz, range = ±3.5 V	79.5	83.2		
		Wide-bandwidth filter, f_{IN} = 2 kHz, range = ±5 V	80.0	84.2		
		Wide-bandwidth filter, f_{IN} = 2 kHz, range = ±7 V	80.9	83.2		
		Wide-bandwidth filter, f_{IN} = 2 kHz, range = ±10 V	82.3	84.7		
		Wide-bandwidth filter, f_{IN} = 2 kHz, range = ±12 V	82.8	85.1		
THD	Total harmonic distortion	Low-noise filter, f_{IN} = 2 kHz, all ranges		–113		dB
		Wide-bandwidth filter, f_{IN} = 2 kHz, all ranges		–113		
SFDR	Spurious-free dynamic range	f_{IN} = 2 kHz		113		dB

5.5 Electrical Characteristics (continued)

at AVDD_5V = 4.75 V to 5.25 V, VDD_1V8 = 1.75 V to 1.85 V, IOVDD = 1.15 V to 1.85 V, V_{REF} = 4.096 V (internal or external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	CMRR	at dc		–70		dB
	Isolation crosstalk	at dc		–100		dB
INTERNAL REFERENCE						
V_{REF} (1)	Voltage on REFIO pin (configured as output)	1-µF capacitor on REFIO pin, T_A = 25°C	4.092	4.096	4.1	V
	Reference temperature drift			10	25	ppm/°C
DIGITAL INPUTS						
V_{IL}	Input low logic level		–0.3		0.3 IOVDD	V
V_{IH}	Input high logic level		0.7 IOVDD		IOVDD	V
	Input current		–1	0.1	1	µA
	Input capacitance			6		pF
LVDS SAMPLING CLOCK INPUT						
V_{TH}	High-level input voltage				100	mV
V_{TL}	Low-level input voltage		–100			mV
V_{ICM}	Input common-mode voltage		0.3	1.2	1.4	V
DIGITAL OUTPUTS						
V_{OL}	Output low logic level	I_{OL} = 500 µA sink	0		0.2 IOVDD	V
V_{OH}	Output high logic level	I_{OH} = 500 µA source	0.8 IOVDD		IOVDD	V
POWER SUPPLY						
	Total power dissipation	Maximum throughput		232	304	mW
I_{AVDD_5V}	Supply current from AVDD_5V	Maximum throughput, internal reference		26	32	mA
		Power-down		0.2	2	
I_{VDD_1V8}	Supply current from VDD_1V8	Maximum throughput, internal reference		50	70	mA
		Power-down		0.2	8	
I_{IOVDD}	Supply current from IOVDD	Maximum throughput		7	10	mA
		Power-down		0.1	2	

(1) Does not include the variation in voltage resulting from solder shift effects.

5.6 Timing Requirements

at AVDD_5V = 4.75 V to 5.25 V, VDD_1V8 = 1.75 V to 1.85 V, IOVDD = 1.15 V to 1.85 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = -40°C to +125°C; typical values at T_A = 25°C

		MIN	MAX	UNIT
CONVERSION CYCLE				
f_{SMPL_CLK}	Sampling frequency	3.6	8	MHz
t_{SMPL_CLK}	Sampling time interval	1 / f_{SMPL_CLK}		ns
$t_{PL\_SMPL\_CLK}$	SMPL_CLK low time	0.45 t_{SMPL_CLK}	0.55 t_{SMPL_CLK}	ns
$t_{PH\_SMPL\_CLK}$	SMPL_CLK high time	0.45 t_{SMPL_CLK}	0.55 t_{SMPL_CLK}	ns
SPI INTERFACE TIMINGS (CONFIGURATION INTERFACE)				
f_{SCLK}	Maximum SCLK frequency		20	MHz
t_{PH_CK}	SCLK high time	0.48	0.52	t_{CLK}
t_{PL_CK}	SCLK low time	0.48	0.52	t_{CLK}
t_{hi_CS}	Pulse duration: $\overline{CS}$ high	220		ns
t_{d_CSCK}	Delay time: $\overline{CS}$ falling to the first SCLK capture edge	20		ns
t_{su_CKDI}	Setup time: SDI data valid to the SCLK rising edge	10		ns
t_{ht_CKDI}	Hold time: SCLK rising edge to data valid on SDI	5		ns
t_{D_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising	5		ns
CMOS DATA INTERFACE				
t_{su_SS}	Setup time: SMPL_SYNC rising edge to SMPL_CLK falling edge	10		ns
t_{ht_SS}	Hold time: SMPL_CLK falling edge to SMPL_SYNC high	10		ns

5.7 Switching Characteristics

at AVDD_5V = 4.75 V to 5.25 V, VDD_1V8 = 1.75 V to 1.85 V, IOVDD = 1.15 V to 1.85 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = -40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
RESET					
t_{PU}	Power-up time for device			25	ms
SPI INTERFACE TIMINGS (CONFIGURATION INTERFACE)					
t_{den_CKDO}	Delay time: 8th SCLK rising edge to data enable			22	ns
t_{dz_CKDO}	Delay time: 24th SCLK rising edge to SDO going Hi-Z			50	ns
t_{d_CKDO}	Delay time: SCLK falling edge to corresponding data valid on SDO			16	ns
t_{ht_CKDO}	Delay time: SCLK falling edge to previous data valid on SDO		2		ns
CMOS DATA INTERFACE					
t_{DCLK}	Data clock output	DDR mode	10		ns
		SDR mode	20		
	Clock duty cycle		45	55	%
$t_{off\_DCLKDO\_r}$	Time offset: DCLK rising to corresponding data valid	DDR mode	t_{DCLK} / 4 – 1.5	t_{DCLK} / 4 + 1.5	ns
$t_{off\_DCLKDO\_f}$	Time offset: DCLK falling to corresponding data valid	DDR mode	t_{DCLK} / 4 – 1.5	t_{DCLK} / 4 + 1.5	ns
t_{d_DCLKDO}	Time delay: DCLK rising to corresponding data valid	SDR mode	–1	1	ns
$t_{d\_SYNC\_FCLK}$	Time delay: SMPL_CLK falling edge with SYNC signal to corresponding FCLKOUT rising edge		3	4	t_{SMPL_CLK}

5.8 Timing Diagrams

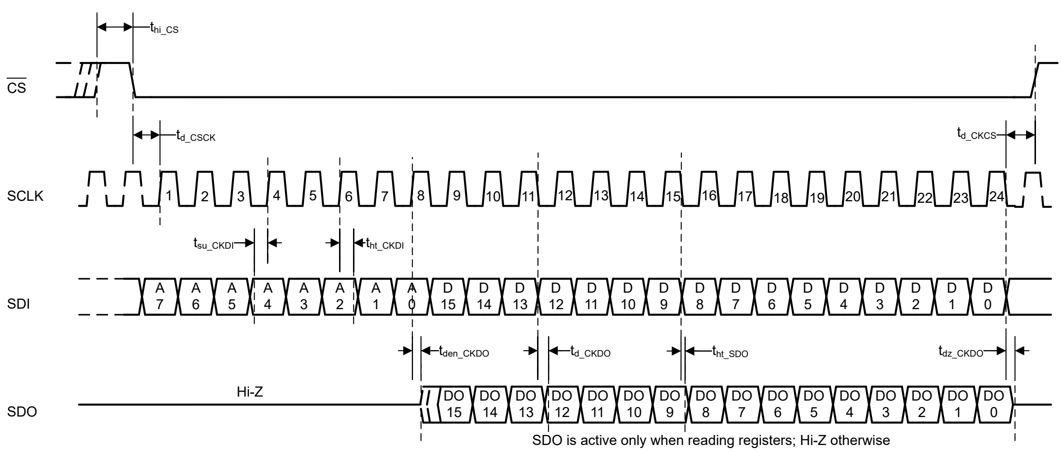


Figure 5-1. SPI Configuration Interface

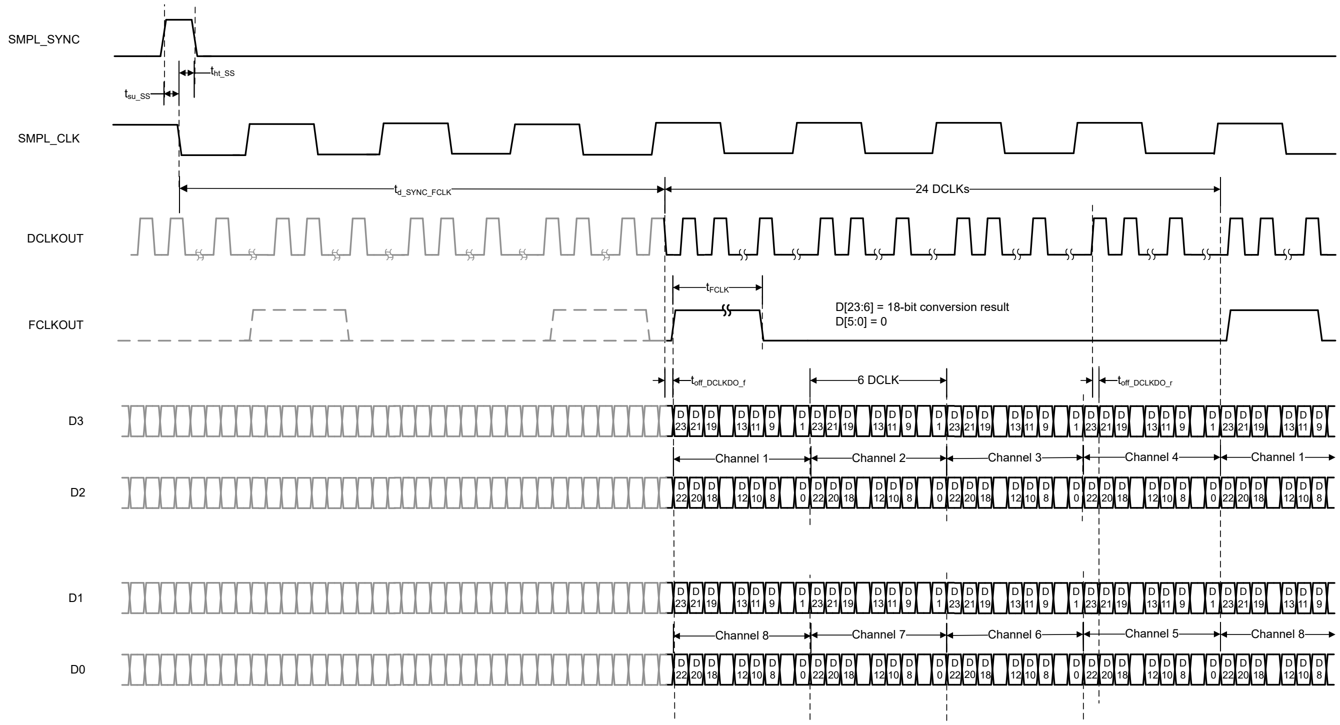


Figure 5-2. 4-SDO DDR CMOS Data Interface

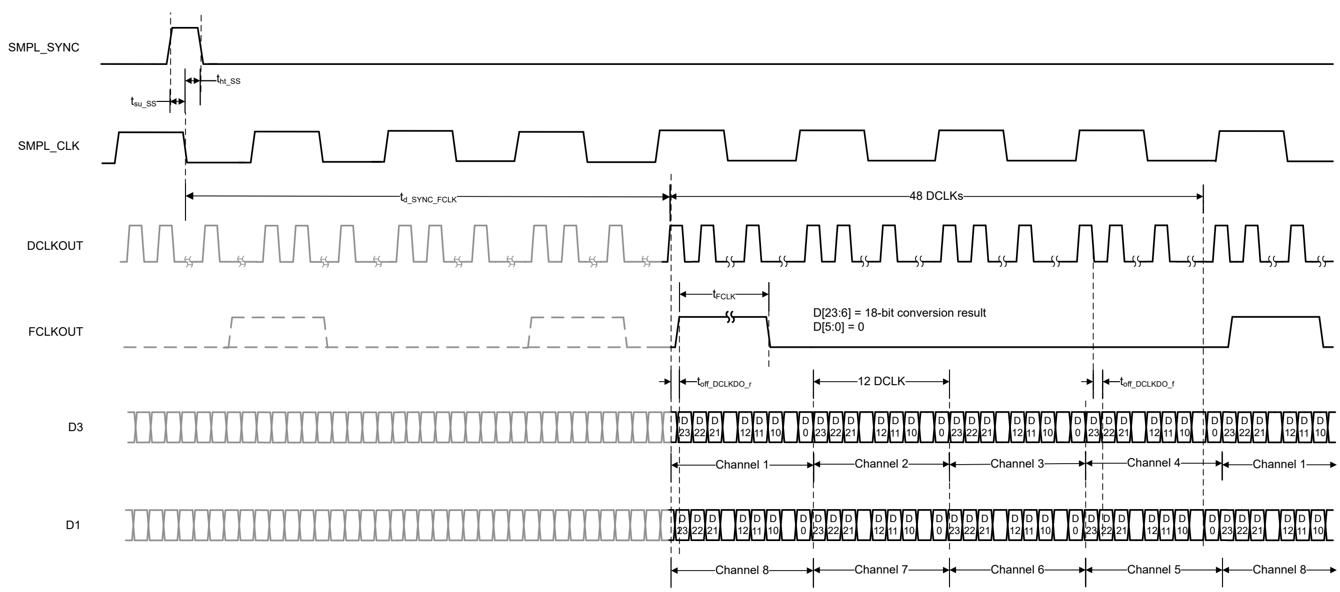


Figure 5-3. 2-SDO DDR CMOS Data Interface

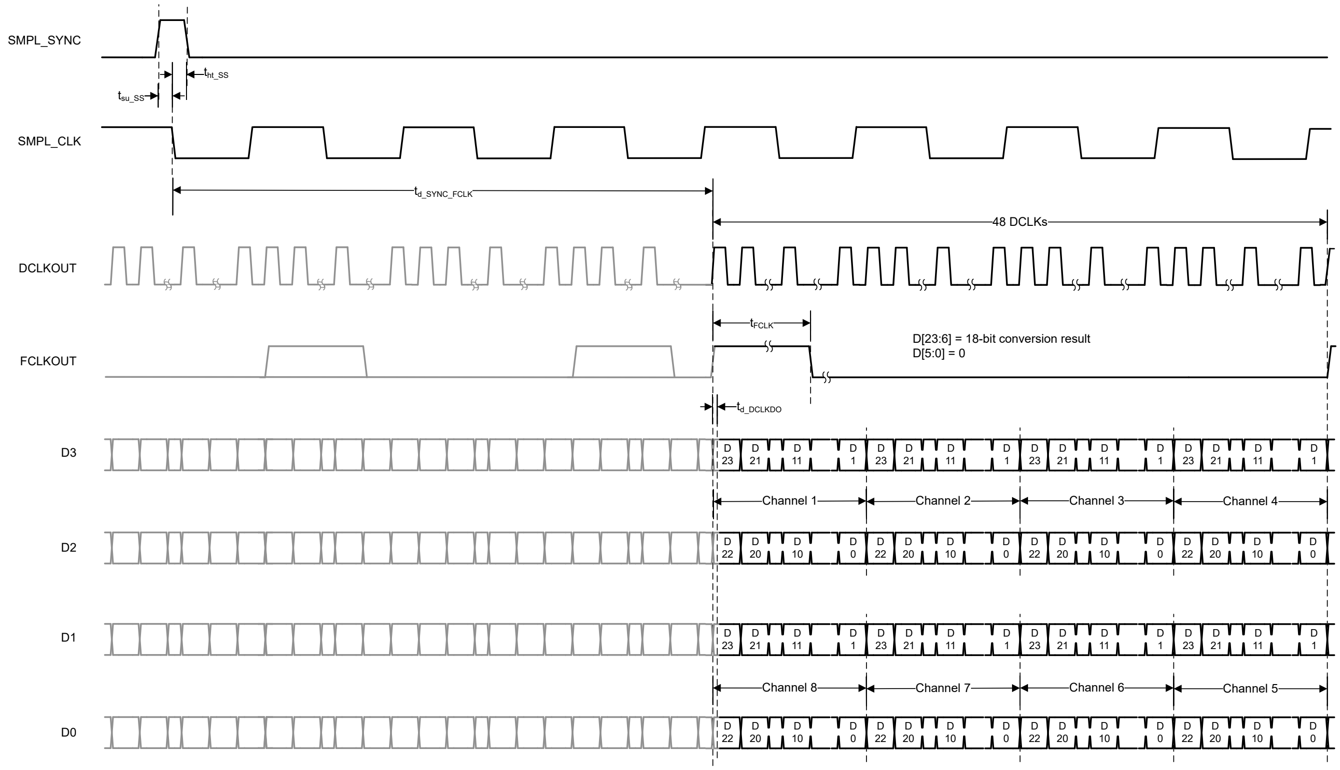


Figure 5-4. 4-SDO SDR CMOS Data Interface

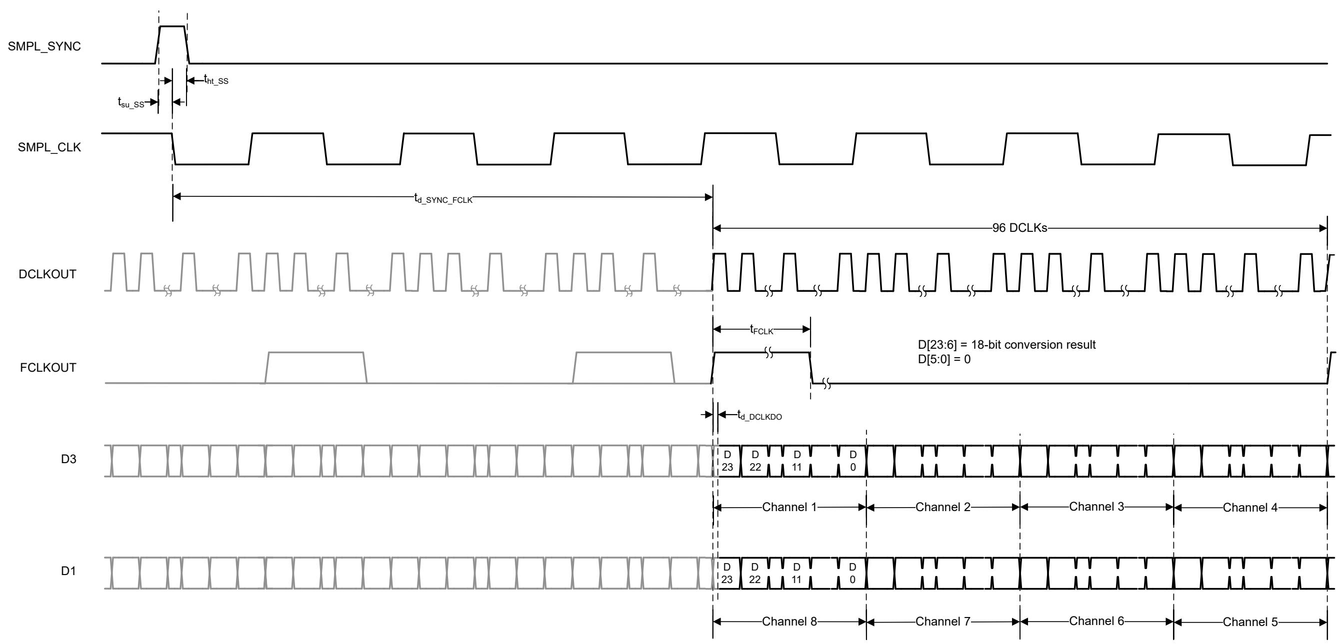
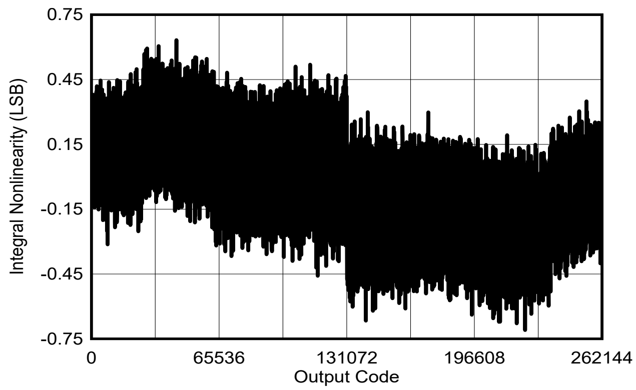


Figure 5-5. 2-SDO SDR CMOS Data Interface

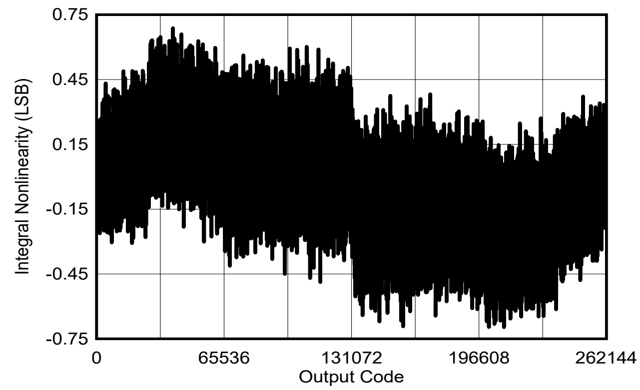
5.9 Typical Characteristics

at T_A = 25°C, AVDD_5V = 5 V, VDD_1V8 = 1.8 V, internal VREF = 4.096 V, ±5-V analog input range, and maximum throughput (unless otherwise noted)



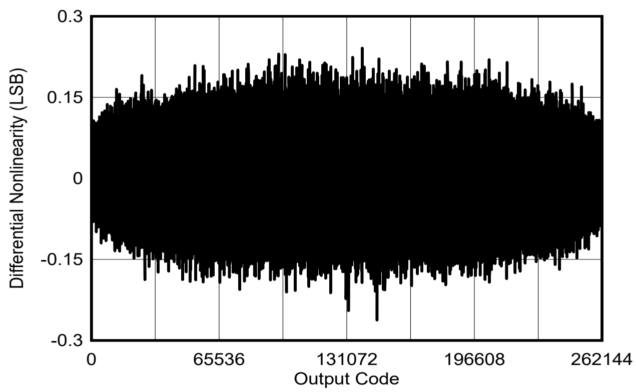
Typical INL = ±0.75 LSB

Figure 5-6. Typical INL With Low-Bandwidth LPF



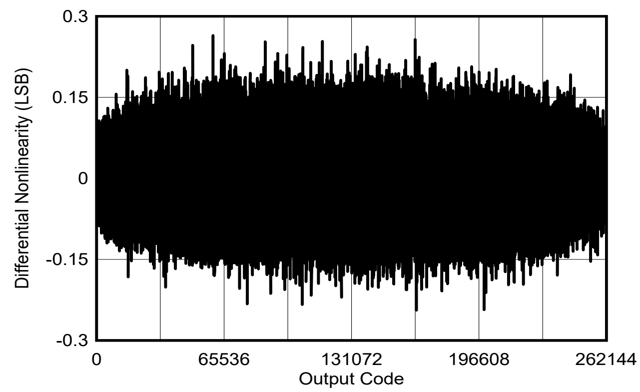
Typical INL = ±0.75 LSB

Figure 5-7. Typical INL With Wide-Bandwidth LPF



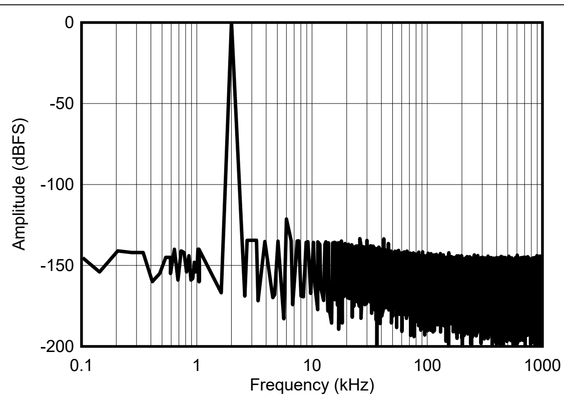
Typical DNL = ±0.2 LSB

Figure 5-8. Typical DNL With Low-Noise LPF



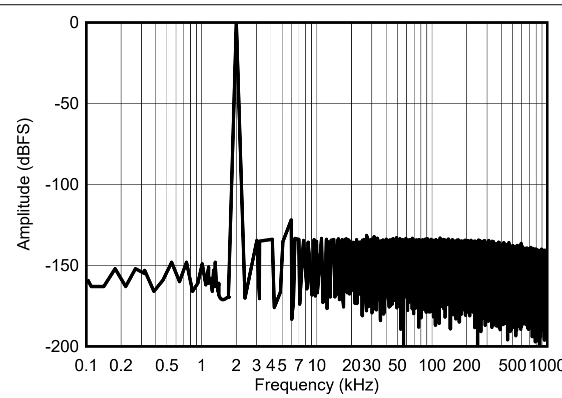
Typical DNL = ±0.25 LSB

Figure 5-9. Typical DNL With Wide-Bandwidth LPF



SNR = 91.5 dBFS, THD = –113 dB at f_{IN} = 2 kHz

Figure 5-10. Typical FFT With Low-Bandwidth LPF, RANGE = ±5 V

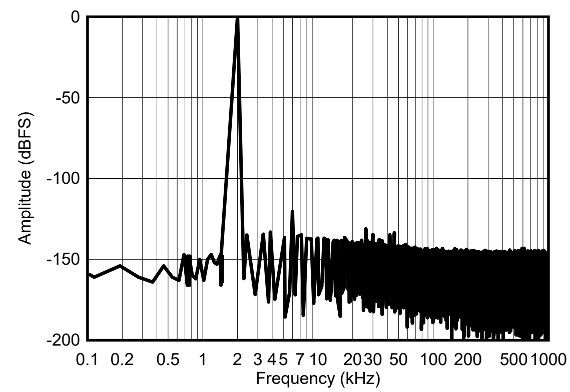


SNR = 83.7 dBFS, THD = –113 dB at f_{IN} = 2 kHz

Figure 5-11. Typical FFT With Wide-Bandwidth LPF, RANGE = ±5 V

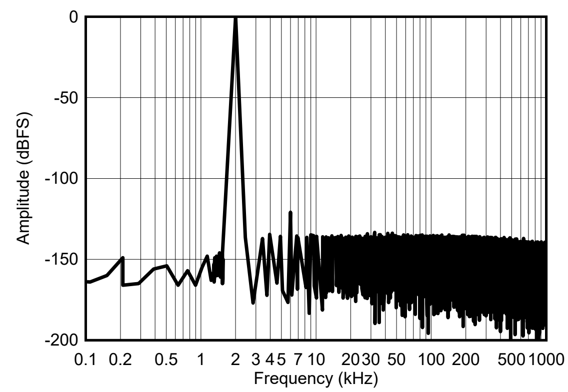
5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD_5V = 5 V, VDD_1V8 = 1.8 V, internal VREF = 4.096 V, ±5-V analog input range, and maximum throughput (unless otherwise noted)



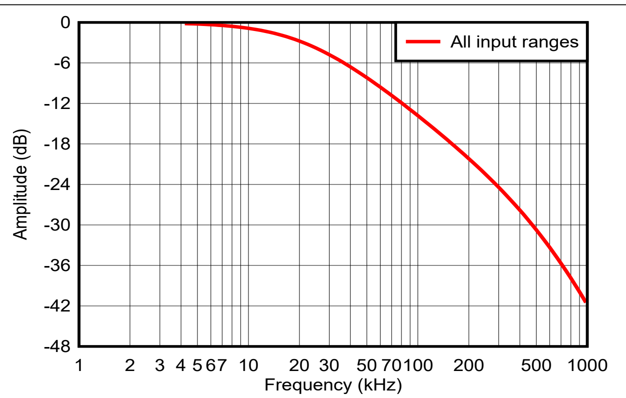
SNR = 92.1 dBFS, THD = –113 dB at f_{IN} = 2 kHz

Figure 5-12. Typical FFT With Low-Bandwidth LPF, RANGE = ±10 V



SNR = 85.5 dBFS, THD = –113 dB at f_{IN} = 2 kHz

Figure 5-13. Typical FFT With Wide-Bandwidth LPF, RANGE = ±10 V



Typical bandwidth (–3 dB) = 21.2 kHz

Figure 5-14. Low-Bandwidth LPF Frequency Response Across Input Ranges

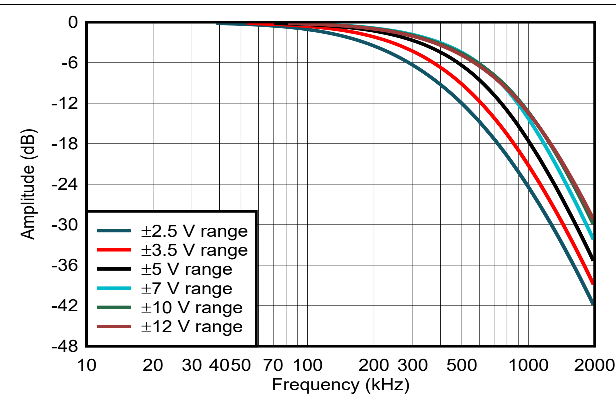


Figure 5-15. Wide-Bandwidth LPF Frequency Response Across Input Ranges

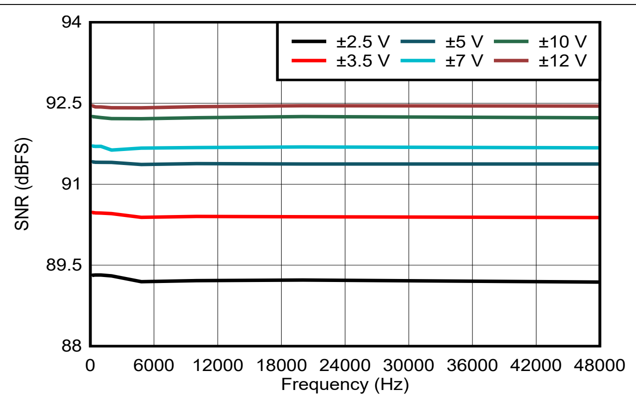


Figure 5-16. SNR vs Input Signal Frequency Across Input Ranges With Low-Bandwidth LPF

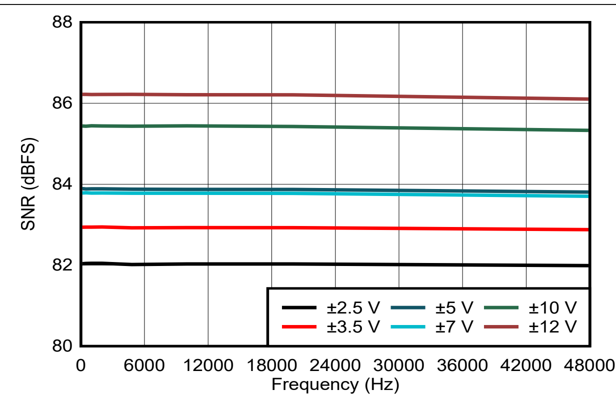


Figure 5-17. SNR vs Input Signal Frequency Across Input Ranges With Wide-Bandwidth LPF

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD_5V = 5 V, VDD_1V8 = 1.8 V, internal VREF = 4.096 V, ±5-V analog input range, and maximum throughput (unless otherwise noted)

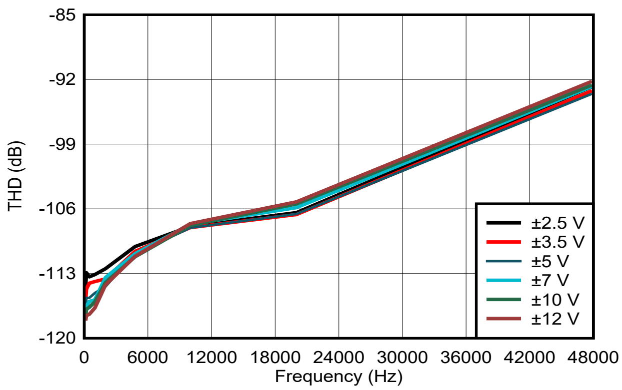


Figure 5-18. THD vs Input Signal Frequency Across Input Ranges With Low-Bandwidth LPF

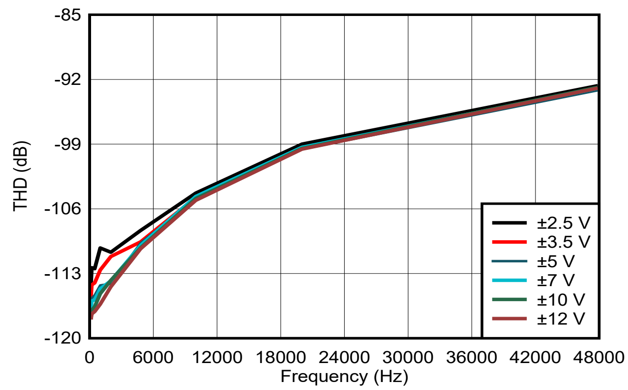


Figure 5-19. THD vs Input Signal Frequency Across Input Ranges With Wide-Bandwidth LPF

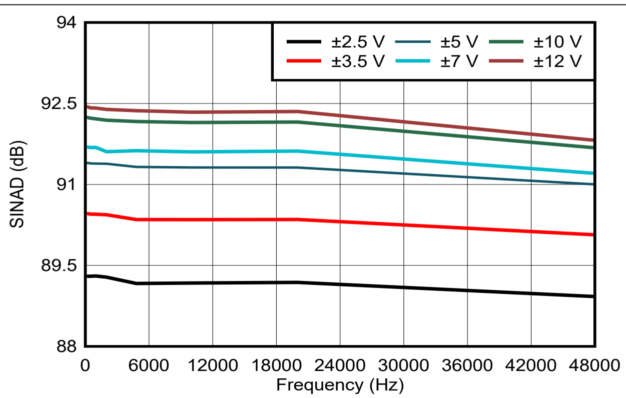


Figure 5-20. SINAD vs Input Signal Frequency Across Input Ranges With Low-Bandwidth LPF

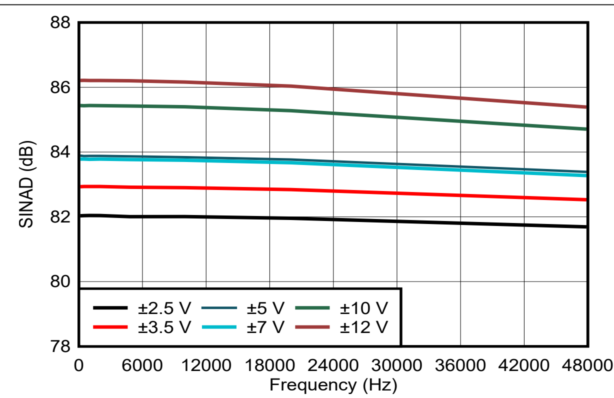


Figure 5-21. SINAD vs Input Signal Frequency Across Input Ranges With Wide-Bandwidth LPF

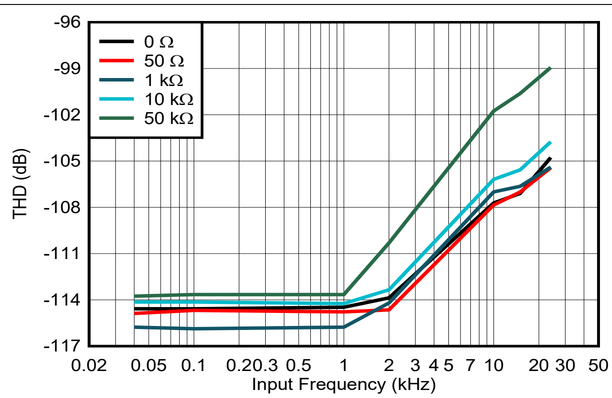


Figure 5-22. THD vs Input Frequency, Low-BW Mode, RANGE = ±5 V, ADS9817

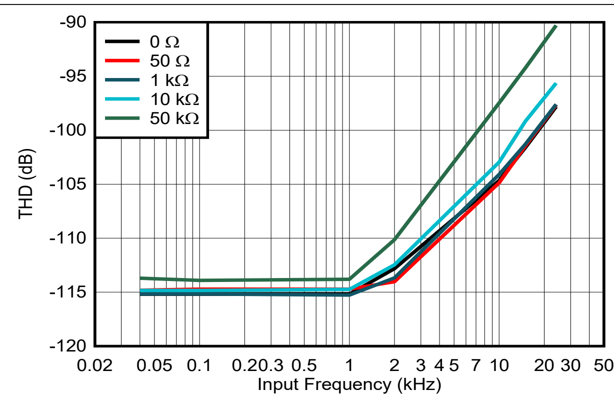


Figure 5-23. THD vs Input Frequency, High-BW Mode, RANGE = ±5 V, ADS9817

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD_5V = 5 V, VDD_1V8 = 1.8 V, internal VREF = 4.096 V, ±5-V analog input range, and maximum throughput (unless otherwise noted)

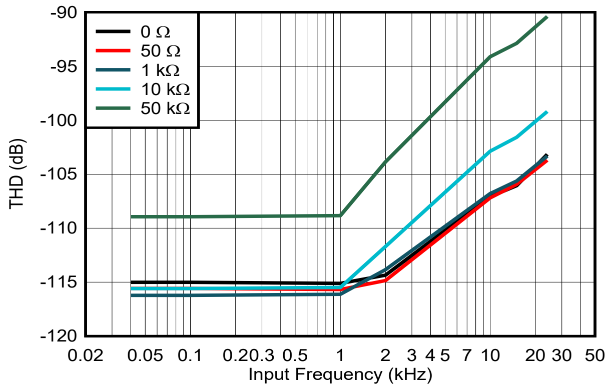


Figure 5-24. THD vs Input Frequency, Low-BW Mode, RANGE = ±10 V, ADS9817

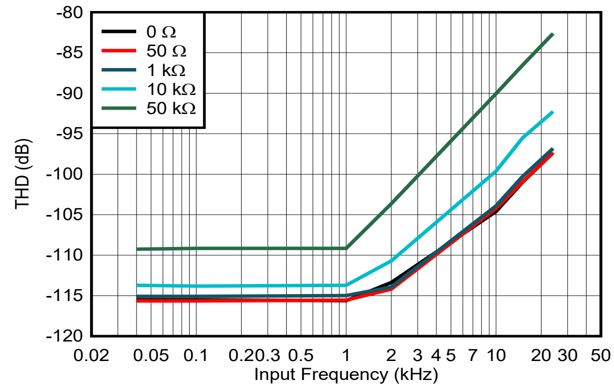


Figure 5-25. THD vs Input Frequency, High-BW Mode, RANGE = ±10 V, ADS9817

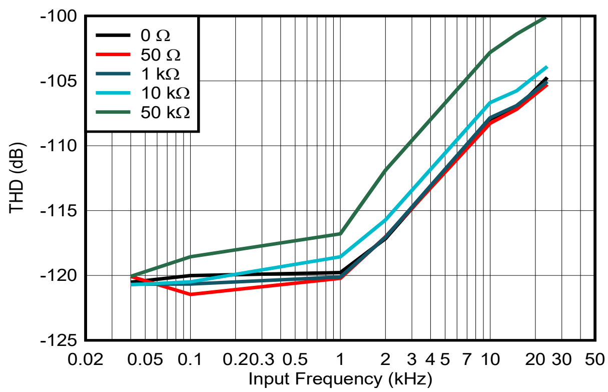


Figure 5-26. THD vs Input Frequency, Low-BW Mode, RANGE = ±5 V, ADS9815

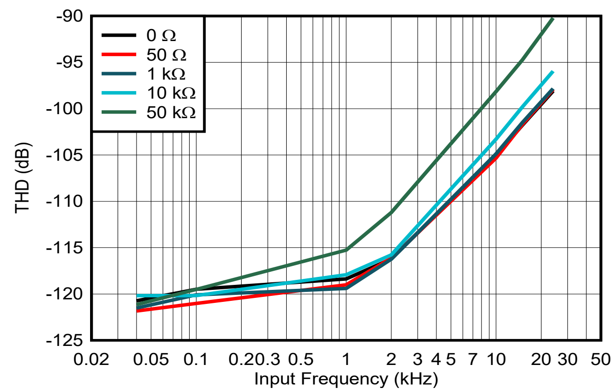


Figure 5-27. THD vs Input Frequency, High-BW Mode, RANGE = ±5 V, ADS9815

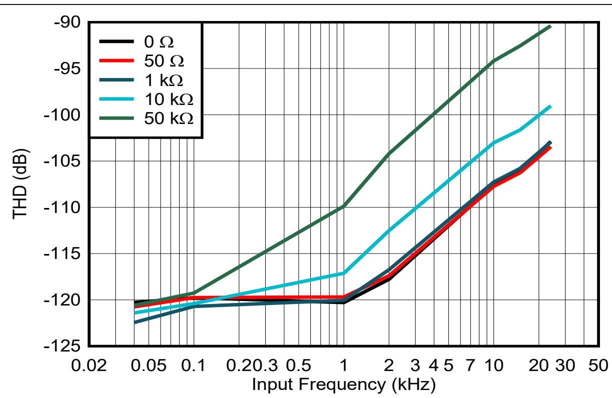


Figure 5-28. THD vs Input Frequency, Low-BW Mode, RANGE = ±10 V, ADS9815

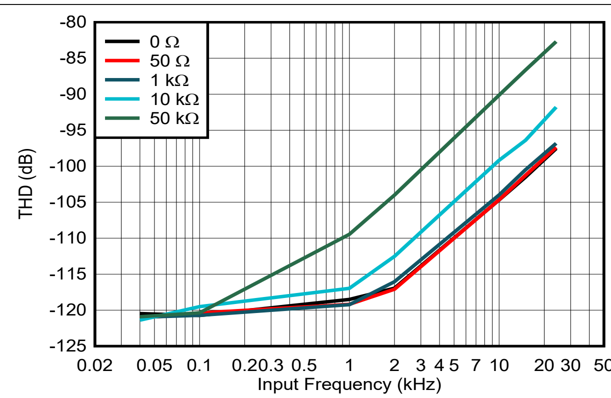


Figure 5-29. THD vs Input Frequency, High-BW Mode, RANGE = ±10 V, ADS9815

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD_5V = 5 V, VDD_1V8 = 1.8 V, internal VREF = 4.096 V, ±5-V analog input range, and maximum throughput (unless otherwise noted)

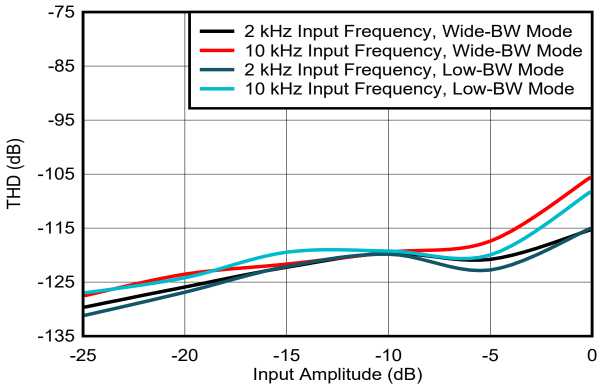
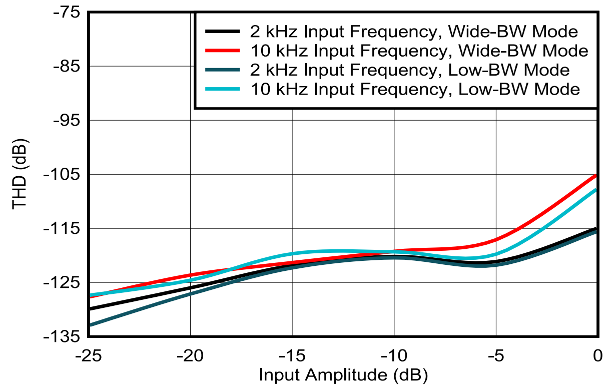


Figure 5-30. THD vs Input Amplitude, RANGE = ±5 V



Input level = 0 dB; R_{IN} = 0 Ω, 50 Ω, 1 kΩ, 10 kΩ, 50 kΩ, f_{IN} = 40 Hz, 110 Hz, 1 kHz, 2 kHz, 10 kHz, 15 kHz, 24 kHz

Figure 5-31. THD vs Input Amplitude, RANGE = ±10 V

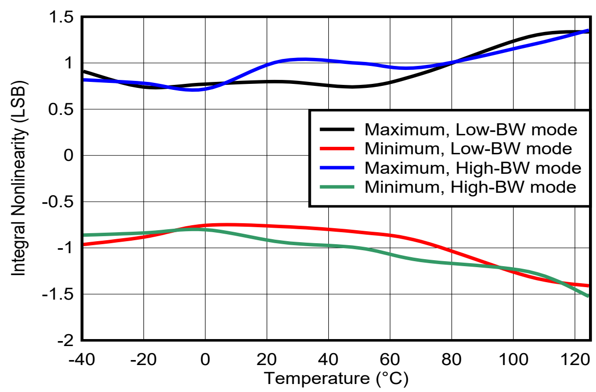


Figure 5-32. INL vs Temperature

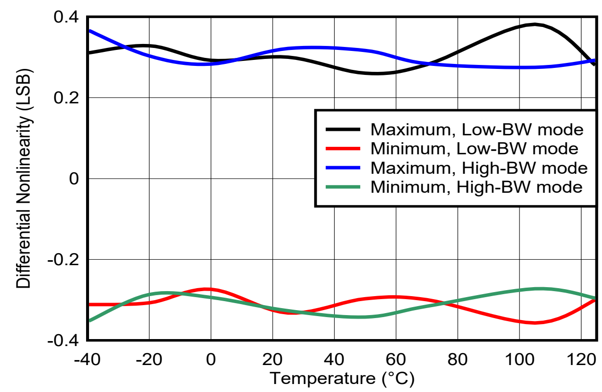


Figure 5-33. DNL vs Temperature

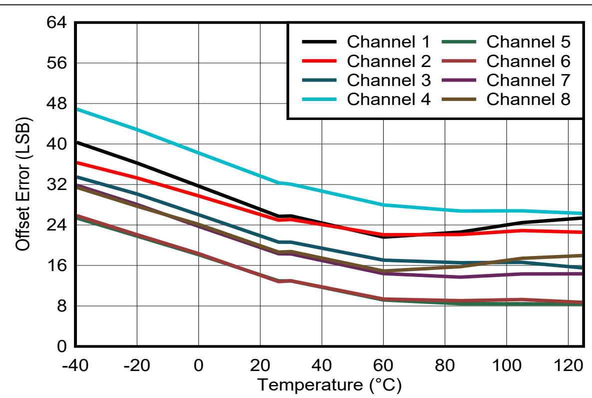


Figure 5-34. Offset Error vs Temperature, RANGE = ±5 V

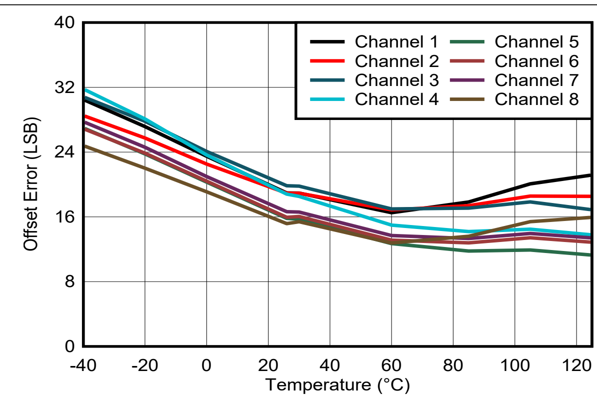


Figure 5-35. Offset Error vs Temperature, RANGE = ±10 V

5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD_5V = 5 V, VDD_1V8 = 1.8 V, internal VREF = 4.096 V, ±5-V analog input range, and maximum throughput (unless otherwise noted)

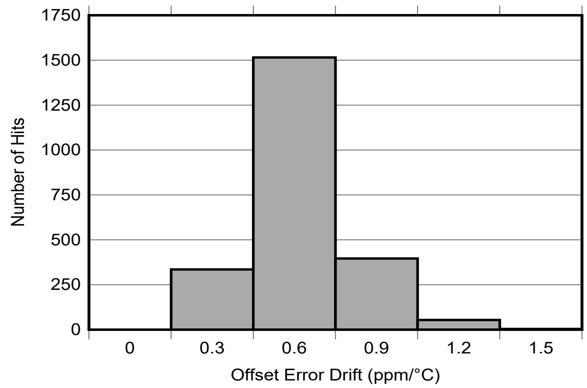


Figure 5-36. Offset Error Drift Histogram

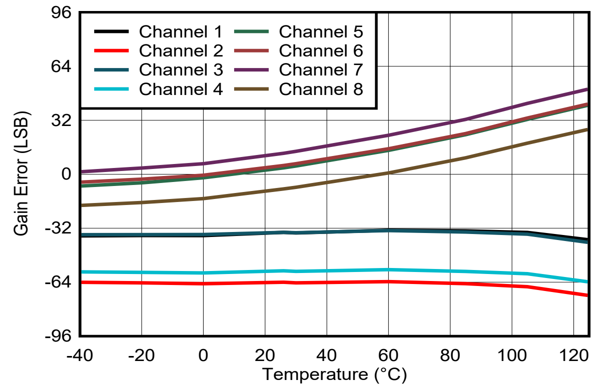


Figure 5-37. Gain Error vs Temperature, RANGE = ±5 V

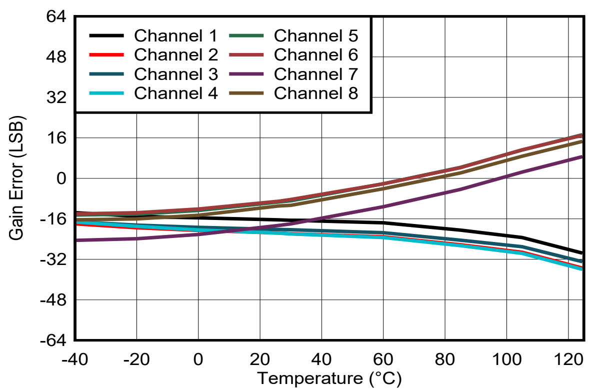


Figure 5-38. Gain Error vs Temperature, RANGE = ±10 V

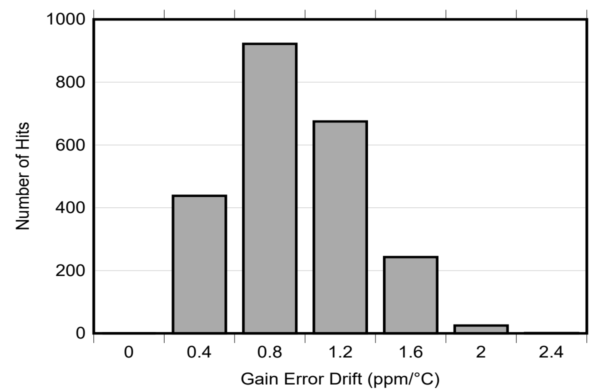
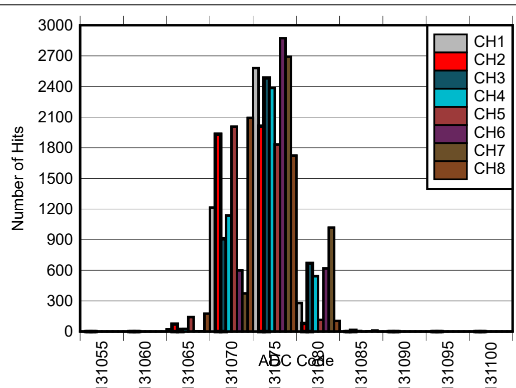
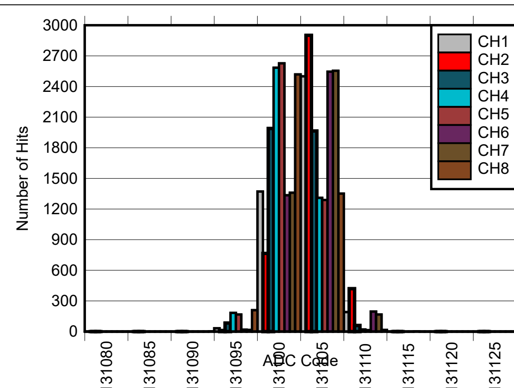


Figure 5-39. Gain Error Drift Histogram



Mean = 131073.8 LSB, standard deviation = 2.45 LSB, number of hits = 4096

Figure 5-40. DC Histogram of Codes for AINxP = AINxM = GND, Low-BW Mode, RANGE = ±5 V

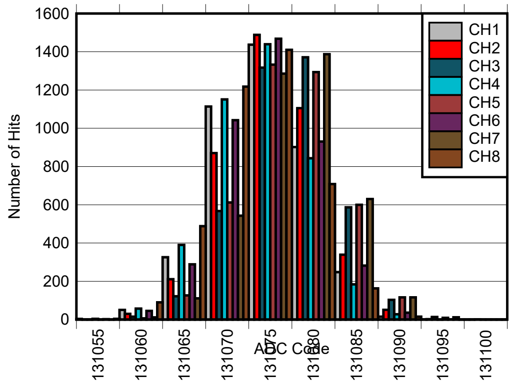


Mean = 131103.5 LSB, standard deviation = 2.49 LSB, number of hits = 4096

Figure 5-41. DC Histogram of Codes for V_{IN} = 1 mV, Low-BW Mode, RANGE = ±5 V

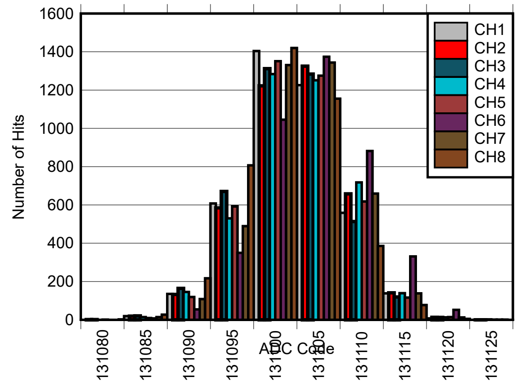
5.9 Typical Characteristics (continued)

at T_A = 25°C, AVDD_5V = 5 V, VDD_1V8 = 1.8 V, internal VREF = 4.096 V, ±5-V analog input range, and maximum throughput (unless otherwise noted)



Mean = 131074.4 LSB, standard deviation = 5.47 LSB, number of hits = 4096

Figure 5-42. DC Histogram of Codes for AINxP = AINxM = GND, Wide-BW Mode, RANGE = ±5 V



Mean = 131102.3 LSB, standard deviation = 5.68 LSB, number of hits = 4096

Figure 5-43. DC Histogram of Codes for V_{IN} = 1 mV, Wide-BW Mode, RANGE = ±5 V

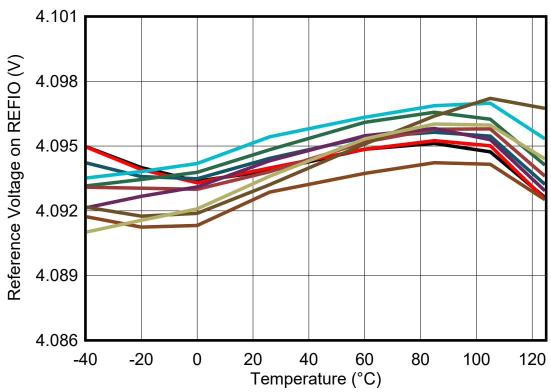


Figure 5-44. REFIO vs Temperature

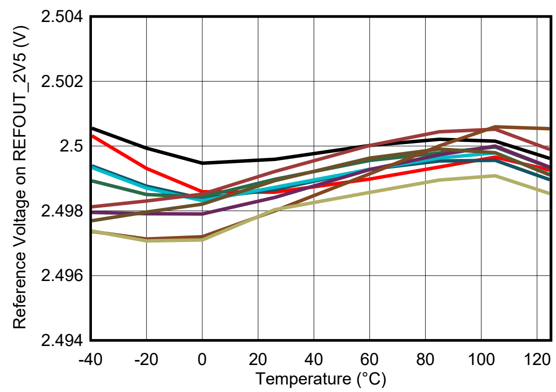


Figure 5-45. REFOUT_2V5 vs Temperature

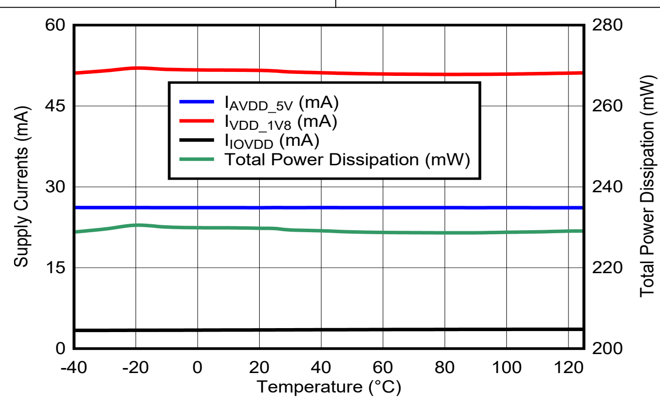


Figure 5-46. Supply Currents and Total Power Dissipation vs Temperature

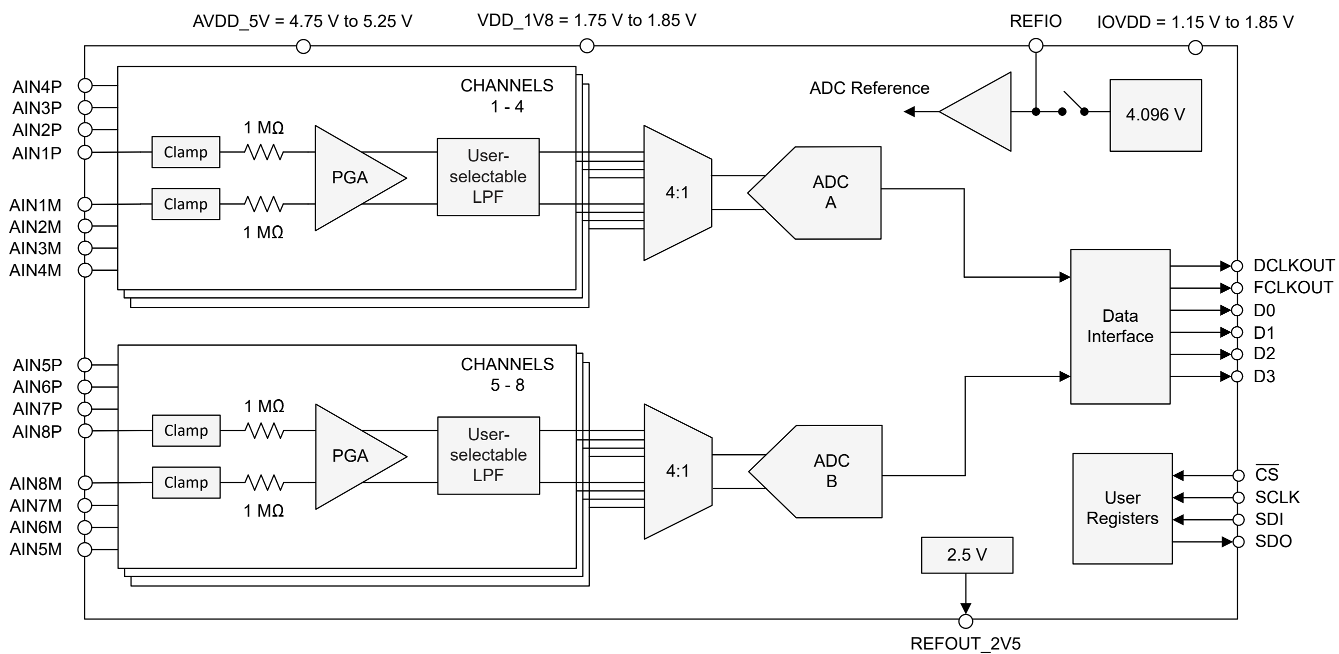
6 Detailed Description

6.1 Overview

The ADS981x is an 18-bit data acquisition (DAQ) system with eight-channel analog inputs that can be configured as either single-ended or differential. Each analog input channel consists of an input clamp protection circuit, and a programmable gain amplifier (PGA) with user-selectable bandwidth options. The input signals are digitized using an 18-bit analog-to-digital converter (ADC), based on the successive approximation register (SAR) architecture. This overall system can achieve a maximum throughput of 2 MSPS/channel for all channels. The device features a 4.096-V internal reference with a fast-settling buffer.

The device operates from 5-V and 1.8-V analog supplies and can accommodate true bipolar input signals. The input clamp protection circuitry can tolerate voltages up to ±18 V. The device offers a constant 1-MΩ resistive input impedance irrespective of the sampling frequency or the selected input range. The ADS981x offers a simplified end solution without requiring external high-voltage bipolar supplies and complicated driver circuits.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Analog Inputs

The ADS981x incorporates dual, simultaneous-sampling, 18-bit successive approximation register (SAR) analog-to-digital converters (ADCs). Each ADC is connected to four analog input channels through a multiplexer. The device has a total of eight analog input pairs. The ADC digitizes the voltage difference between the analog input pairs AINxP – AINxM. Figure 6-1 shows the simplified circuit schematic for each analog input channel, including the input clamp protection circuit, PGA, low-pass filter, multiplexer, high-speed ADC driver, and a precision 18-bit SAR ADC.

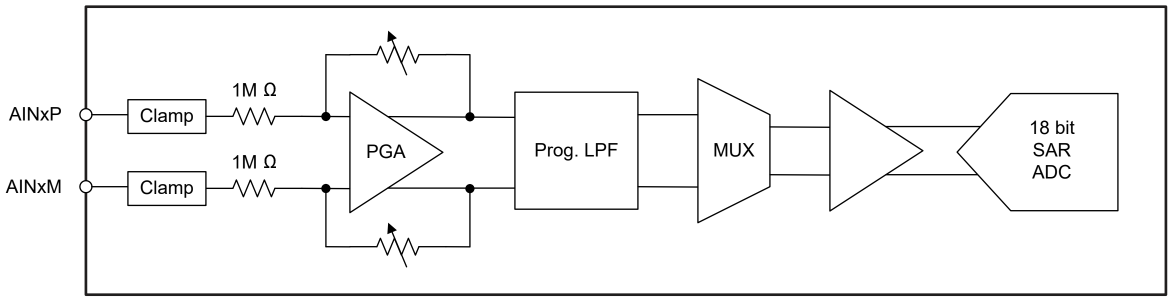


Figure 6-1. Front-End Circuit Schematic for the Selected Analog Input Channel

6.3.1.1 Input Clamp Protection Circuit

The ADS981x features an internal clamp protection circuit on each of the eight analog input channels, see Figure 6-1. The input clamp protection circuit allows each analog input to swing up to a maximum voltage of ±18 V. Beyond an input voltage of ±18 V, the input clamp circuit turns on and still operates from the single 5-V supply. Figure 6-2 shows a typical current versus voltage characteristic curve for the input clamp.

For input voltages above the clamp threshold, make sure that the input current never exceeds ±10 mA. A resistor placed in series with the analog inputs is an effective way to limit the input current. In addition to limiting the input current, the series resistor can also provide an antialiasing, low-pass filter (LPF) when coupled with a capacitor. Matching the external source impedance on the AINxP and AINxM pins cancels any additional offset error.

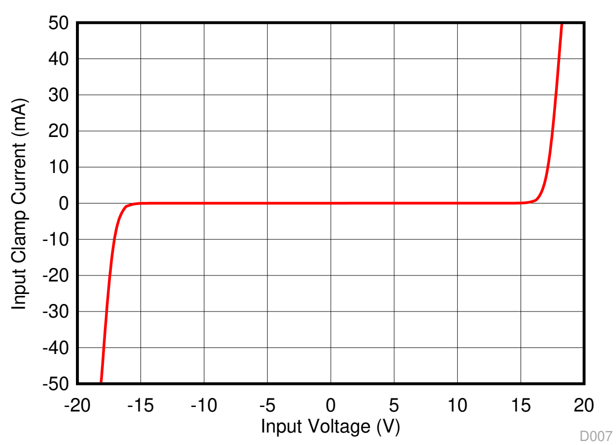


Figure 6-2. Input Protection Clamp Profile, Input Clamp Current vs Source Voltage

6.3.1.2 Programmable Gain Amplifier (PGA)

The ADS981x features a PGA at every analog input channel. The PGA supports single-ended and differential inputs with a bipolar signal swing. Table 6-1 lists the supported analog input ranges. The analog input range can be configured independently for each channel by using the RANGE_CHx register fields in address 0xC2 and address 0xC3.

Table 6-1. Analog Input Ranges

DIFFERENTIAL INPUTS	SINGLE-ENDED INPUTS	RANGE_CHx CONFIGURATION
±12 V	±12 V	5
±10 V	±10 V	4
±7 V	±7 V	3
±5 V	±5 V	0
±3.5 V	±3.5 V	1
±2.5 V	±2.5 V	2

Each analog input channel features an antialiasing, low-pass filter (LPF) at the output of the PGA. Table 6-2 lists the various programmable LPF options available in the ADS981x corresponding to the analog input range. Figure 5-14 and Figure 5-15 illustrate the frequency responses for low-bandwidth and wide-bandwidth LPF configurations. The analog input bandwidth for the eight analog input channels can be can be selected using the ANA_BW[7:0] bits in address 0xC0 of register bank 1.

Table 6-2. Low-Pass Filter Corner Frequency

LPF	ANALOG INPUT RANGE	CORNER FREQUENCY (–3 dB)
Low-bandwidth	All input ranges	21.2 kHz
Wide-bandwidth	±12 V	375 kHz
	±10 V	385 kHz
	±7 V	400 kHz
	±5 V	320 kHz
	±3.5 V	240 kHz
	±2.5 V	185 kHz

6.3.1.3 Wide-Common-Mode Voltage Rejection Circuit

The ADS981x features a common-mode (CM) rejection circuit at the analog inputs that supports CM voltages up to ±12 V. The CM voltage for differential inputs is given by Equation 1. On power-up or after reset, the common-mode voltage range for the analog input channels is ±12 V (WIDE_CM_EN1 = 0b). Voltage at the analog inputs, in all cases, must be within the *Absolute Maximum Ratings*.

$$\text{Common mode voltage} = \frac{(\text{Voltage on AINP}) + (\text{Voltage on AINM})}{2} \quad (1)$$

As described in Table 6-3, the CM voltage rejection circuit can be optimized for various CM voltages for differential inputs.

Table 6-3. Wide Common-Mode Configuration for Differential Inputs

<table>
<tr><th rowspan="2">COMMON-MODE (CM) RANGE</th><th rowspan="2">CM_CTRL_EN</th><th colspan="2">ADC A (ANALOG INPUT CHANNELS 1–4)</th><th colspan="2">ADC B (ANALOG INPUT CHANNELS 5–8)</th></tr>
<tr><th>CM_EN_ADC_A</th><th>CM_RNG_ADC_A [1:0]</th><th>CM_EN_ADC_B</th><th>CM_RNG_ADC_B [1:0]</th></tr>
<tr><td>CM ≤ ±1 V</td><td rowspan="4">1</td><td>0</td><td>Don't care</td><td>0</td><td>Don't care</td></tr>
<tr><td>CM ≤ ±RANGE / 2</td><td rowspan="3">1</td><td>0</td><td rowspan="3">1</td><td>0</td></tr>
<tr><td>CM ≤ ±6 V</td><td>2</td><td>2</td></tr>
<tr><td>CM ≤ ±12 V</td><td>1</td><td>1</td></tr>
</table>

The CM voltage rejection circuit must be configured depending on the analog input range of the PGA when using single-ended inputs as well. Table 6-4 lists the recommended configuration for single-ended inputs for various analog input voltage ranges.

Table 6-4. Wide Common-Mode Configuration for Single-Ended Inputs

PGA ANALOG INPUT RANGE	CM_CTRL_EN	ADC A (ANALOG INPUT CHANNELS 1–4)		ADC B (ANALOG INPUT CHANNELS 5–8)	
		CM_EN_ADC_A	CM_RNG_ADC_A [1:0]	CM_EN_ADC_B	CM_RNG_ADC_B [1:0]
±2.5 V, ±3.5 V, and ±5 V	1	0	Don't care	0	Don't care
±7 V, ±10 V, and ±12 V		1	0	1	0

6.3.1.4 Gain Error Calibration

The ADS981x features calibration logic to minimize gain error from the analog inputs. Enable gain error calibration for minimum gain error. Gain error calibration can be enabled by configuring the GE_CAL_EN1 (address = 0xD), GE_CAL_EN2, GE_CAL_EN3 (address = 0x33), and GE_CAL_EN4 (address = 0x34).

If gain error calibration is not enabled as shown in Table 6-5, the full-scale analog input ranges are increased by a factor of 1.024.

Table 6-5. Analog Input Ranges vs Gain-Error Calibration

RANGE_CHx CONFIGURATION	ANALOG INPUT RANGE WITH CALIBRATION	ANALOG INPUT RANGE WITHOUT CALIBRATION
5	±12 V	±12.288 V
4	±10 V	±10.24 V
3	±7 V	±7.168 V
0	±5 V	±5.12 V
1	±3.5 V	±3.584 V
2	±2.5 V	±2.56 V

6.3.2 ADC Transfer Function

The ADS981x outputs 18 bits of conversion data in either straight-binary or binary two's-complement formats. The format for the output codes is the same across all analog channels. The format for the output codes can be selected using the DATA_FORMAT field in address 0xD in register bank 1. Figure 6-3 and Table 6-6 show the transfer characteristics for the ADS981x. The LSB size depends on the analog input range selected, gain-error calibration, and system gain error calibration as shown in Equation 2.

$$LSB = \frac{Analog\ input\ range}{2^{18}} \times \left(1 + G \times 0.024\right) \quad (2)$$

where:

- G is 0 when gain-error calibration is enabled, otherwise G is1; see the *Gain Error Calibration* section

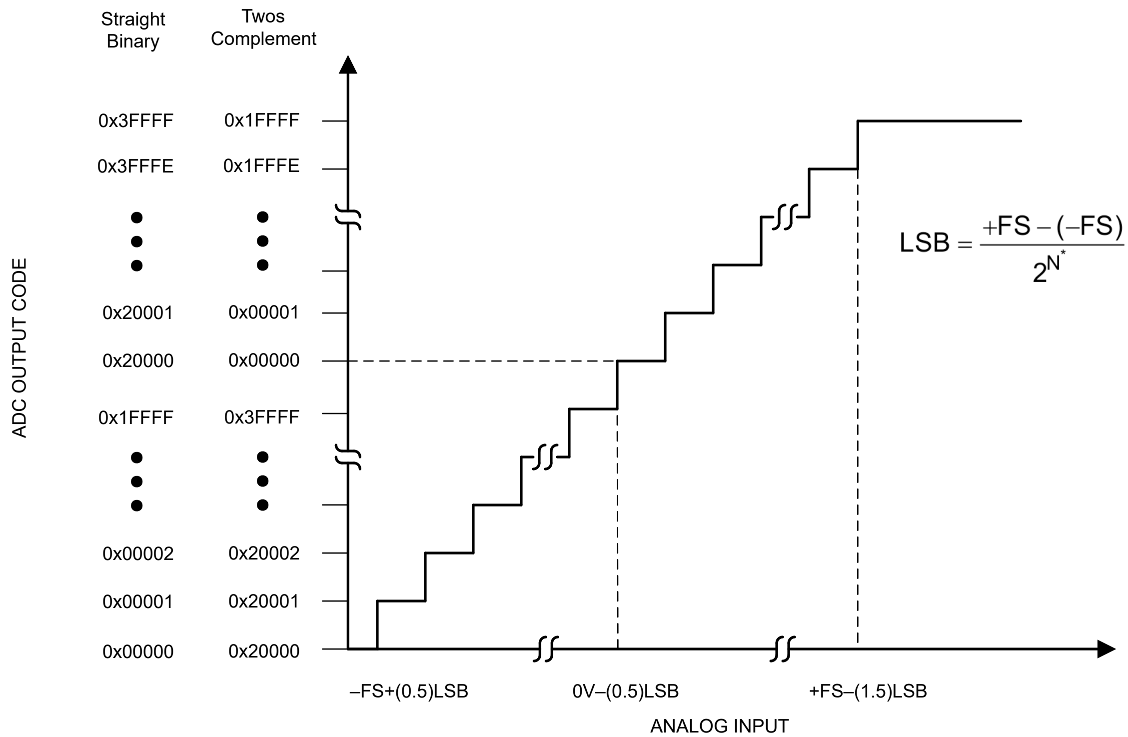


Figure 6-3. Transfer Characteristics

Table 6-6. ADC Full-Scale Range and LSB Size

RANGE	+FS	MIDSCALE	–FS	LSB
±2.5 V	2.5 V	0 V	–2.5 V	19.07 µV
±3.5 V	3.5 V	0 V	–3.5 V	26.70 µV
±5 V	5 V	0 V	–5 V	38.15 µV
±7 V	7 V	0 V	–7 V	53.41 µV
±10 V	10 V	0 V	–10 V	76.29 µV
±12 V	12 V	0 V	–12 V	91.55 µV

6.3.3 ADC Sampling Clock Input

Use a low-jitter external clock with a high slew rate to maximize SNR performance. The ADS981x can be operated with a differential or a single-ended clock input. Clock amplitude impacts the ADC aperture jitter and consequently the SNR. For maximum SNR performance, provide a clock signal with fast slew rates that maximizes swing between IOVDD and GND levels.

The sampling clock must be a free-running continuous clock. The ADC generates a valid output data, data clock, and frame clock $t_{PU\_SMPL\_CLK}$, as specified in the *Switching Characteristics* after a free-running sampling clock is applied. The ADC output data, data clock, and frame clock are invalid when the sampling clock is stopped.

Figure 6-4 shows a diagram of the differential sampling clock input. For this configuration, connect the differential sampling clock input to the SMPL_CLKP and SMPL_CLKM pins. Figure 6-5 shows a diagram of the single-ended sampling clock input. In this configuration, connect the single-ended sampling clock to SMPL_CLKP and connect SMPL_CLKM to ground.

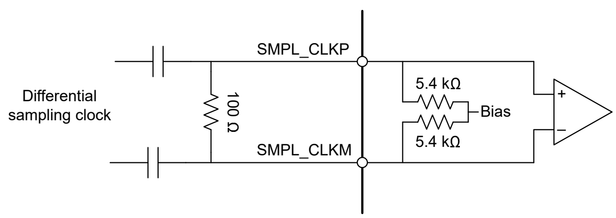


Figure 6-4. AC-Coupled Differential Sampling Clock

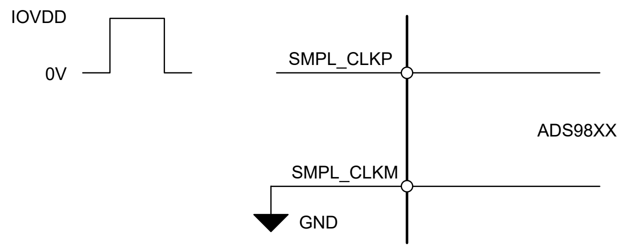


Figure 6-5. Single-Ended Sampling Clock

6.3.4 Reference

The ADS981x has a precision, low-drift voltage reference internal to the device. For best performance, filter the internal reference noise by connecting a 10-µF ceramic bypass capacitor to the REFIO pin. An external reference can also be connected at the REFIO pin and the internal reference voltage can be disabled by writing to PD_REF = 1b in address 0xC1 of register bank 1.

6.3.4.1 Internal Reference Voltage

The ADS981x features an internal reference voltage with a nominal output voltage of 4.096 V. On power-up, the internal reference is enabled by default. As shown in Figure 6-6, place a minimum 10-µF decoupling capacitor between the REFIO and REFM pins.

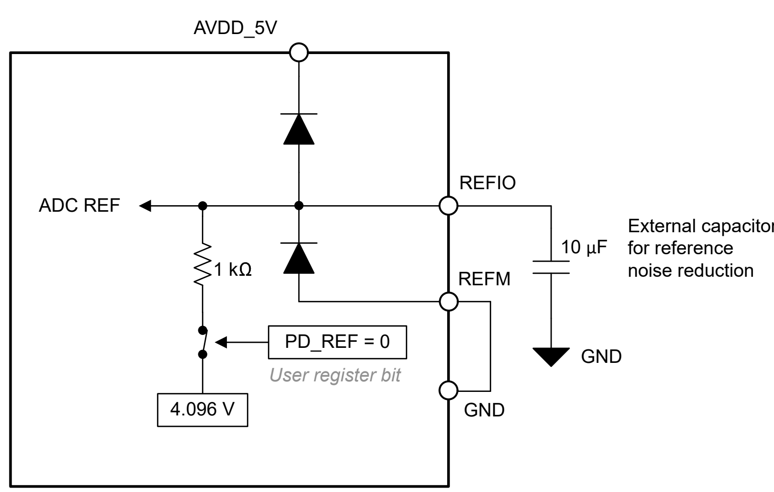


Figure 6-6. Internal Reference Voltage

6.3.4.2 External Reference Voltage

An external 4.096-V reference voltage, as shown in Figure 6-7, can be connected at the REFIO pin with an appropriate decoupling capacitor placed between the REFIO and REFM pins. For improved thermal drift performance, the REF7040 is recommended. To disable the internal reference, set PD_REF = 1b in address 0xC1 in register bank 1. The REFIO pin has ESD protection diodes connected to the AVDD_5V and REFM pins.

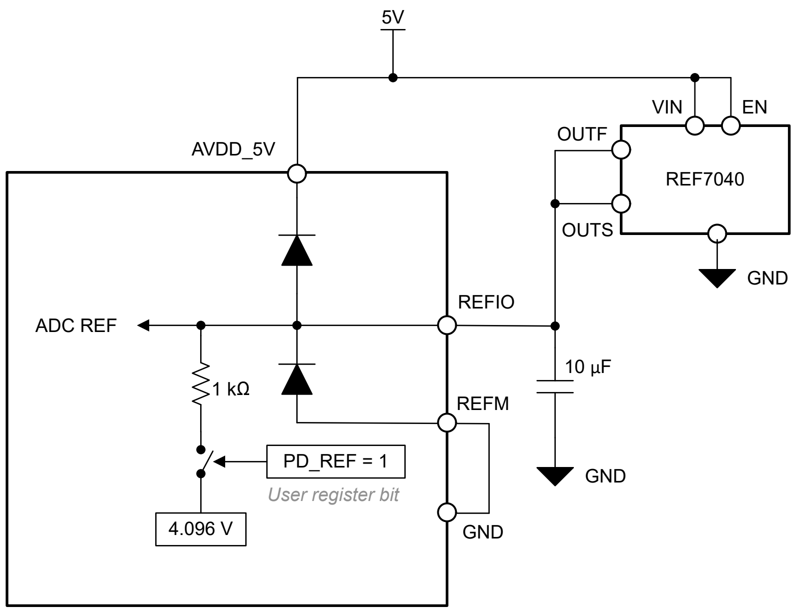


Figure 6-7. External Reference Voltage

6.3.5 Sample Synchronization

As illustrated in Figure 5-2, Figure 5-3, Figure 5-4, and Figure 5-5, the SMPL_SYNC pin can synchronize multiple ADCs using an external SYNC signal. The SMPL_SYNC pin is latched in by the falling edge of the sampling clock.

The synchronization signal is only required one time during power-up. As illustrated in Figure 5-2, Figure 5-3, Figure 5-4, and Figure 5-5, the SYNC signal resets the internal analog channel selection logic and aligns the FCLKOUT signal to the data frame. If no SYNC signal is given, the internal analog channel selection logic and FCLKOUT are not synchronized, which can lead to a different alignment between the sequence of channel output data and FCLKOUT. When using multiple ADCs with the same sampling clock, the SYNC signal makes sure all ADCs sample the same respective analog input channel at the same time.

6.3.6 Data Interface

The ADS981x supports 2-lane and 4-lane mode with single-data-rate (SDR) and double-data-rate (DDR) interface modes. The data interface can be selected using the configuration SPI as described in Table 6-7. The ADC generates the data (D[3:0]), data clock (DCLKOUT), and frame clock (FCLKOUT) in response to the sampling clock signal on the SMPL_CLK input pin. The 18-bit ADC conversion result is output MSB first in a 24-bit data packet and the last six bits are zeroes.

The data interface signals can be described as:

- D[3:0]: Data output from the ADC. In 4-lane mode all four lanes are used, whereas in 2-lane mode D3 and D1 are used to output ADC data.
- DCLKOUT: Data clock output from the ADC.
- FCLKOUT: Frame clock output from the ADC delimiting each set of 8-channel data. A SYNC pulse is required on power-up or after device reset to align the rising edge of FCLKOUT with channel 0 data output, as described in the *Sample Synchronization* section.

Use the registers in Table 6-7 to configure the data interface.

Table 6-7. Register Configurations For Interface Modes

INTERFACE MODE	FIGURE	DATA_RATE (Address = 0xC1)	DATA_LANES (Address = 0xC1)
4-lane, DDR	Figure 5-2	0	0
2-lane, DDR	Figure 5-3	0	1
4-lane, SDR	Figure 5-4	1	0
2-lane, SDR	Figure 5-5	1	1

6.3.6.1 Data Clock Output

The ADS981x features a source-synchronous data interface where the ADC provides the output data and the clock to capture the data. The clock to capture the data is output on the DCLKOUT pin. The clock frequency depends on the sampling clock speed, data rate (SDR or DDR), and number of output lanes (4-lanes or 2-lanes) and is given by Equation 3. The frame clock frequency is given by Equation 4.

$$\text{Data clock frequency} = \frac{24\ \text{bits/channel} \times 8\ \text{channels}}{\text{Number of data lanes} \times \text{Data rate (SDR} = 1,\ \text{DDR} = 2)} \times \text{Sampling clock frequency} \quad (3)$$

$$\text{Frame clock frequency} = \frac{\text{Sampling clock frequency}}{4} \quad (4)$$

Table 6-8 shows the data clock frequency for the maximum sampling rates for the ADS9817 and ADS9815 for various interface modes.

Table 6-8. Data Clock Frequency for Interface Modes

INTERFACE MODE	ADS9815 (f_{SMPL_CLK} = 4 MHz)	ADS9817 (f_{SMPL_CLK} = 8 MHz)
4-lane, DDR	24 MHz	48 MHz
2-lane, DDR	48 MHz	96 MHz
4-lane, SDR	48 MHz	96 MHz
2-lane, SDR	96 MHz	Not supported

6.3.6.2 ADC Output Data Randomizer

As shown in Figure 6-8, the ADS981x features a data output randomizer. When enabled, the ADC conversion result is bit-wise exclusive-ORed (XOR) with the LSB of the conversion result. The LSB of the ADC conversion result has equal probability of being either 1 or 0. As a result of the XOR operation, the data output from the ADS981x is randomized. The ground bounce created by the transmission of this randomized result over the data interface is uncorrelated with the analog input voltage. This uncorrelated transmission helps minimize interference between data transmission and analog performance of the ADC when the PCB layout does not minimize ground bounce.

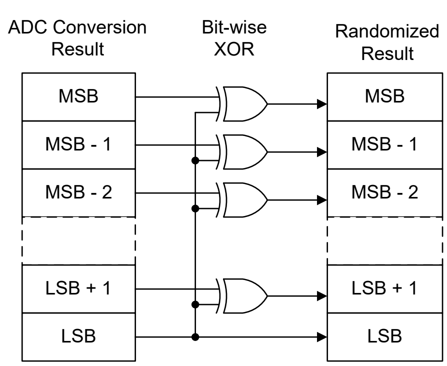


Figure 6-8. Bit-Wise XOR Operation

6.3.6.3 Test Patterns for Data Interface

The ADS981x features test patterns that can be used by the host for debugging and verifying the data interface. The test patterns replace the ADC output data with predefined digital data. The test patterns can be enabled by configuring the corresponding register addresses 0x13 through 0x1B in bank 1.

The ADS981x supports the following test patterns:

- User-defined output: User-defined, 24-bit pattern. Separate patterns for ADC A and ADC B; see the *User-Defined Test Pattern* section.
- Ramp output: Digital ramp output with a user-defined increment between two steps. There are separate ramp outputs for ADC A and ADC B; see the *Ramp Test Pattern* section.
- Alternate output: User-defined, 24-bit outputs that alternate between two user-defined patterns; see the *User-Defined Alternating Test Pattern* section.

To disable the test patterns, set TEST_PAT_EN_CHA and TEST_PAT_EN_CHB to 0b.

6.3.6.3.1 User-Defined Test Pattern

The user-defined test pattern allows the host to specify a fixed 24-bit value that is output by the ADS981x. Configure the registers in bank 1 to enable the user-defined test pattern:

- Configure the test patterns in TEST_PAT0_ADC_A (address = 0x15 MSB, 0x14 LSB) and TEST_PAT0_ADC_B (address = 0x1A MSB, 0x19 LSB)
- Set TEST_PAT_EN_ADC_A = 1, TEST_PAT_MODE_ADC_A = 0 (address = 0x13) and TEST PAT_EN_ADC_B = 1, TEST_PAT_MODE_ADC_B = 0 (address = 0x18)

The ADS981x outputs the TEST_PAT0_ADC_A (address 0x15 [7:0], address 0x14 [15:0]) and TEST_PAT0_ADC_B (address 0x1A [7:0], address 0x19 [15:0]) register values in place of ADC A and ADC B data, respectively.

6.3.6.3.2 User-Defined Alternating Test Pattern

The user-defined alternating test pattern allows the host to specify two fixed 24-bit values that are output by the ADS981x alternately. Configure the registers in bank 1 to enable the user-defined alternating test pattern:

- Configure the test patterns in TEST_PAT0_CHA (address = 0x14, 0x15), TEST_PAT1_CHA (address = 0x15, 0x16) and TEST_PAT0_CHB (address = 0x19, 0x1A), TEST_PAT1_CHB (address = 0x1A, 0x1B)
- Set TEST_PAT_EN_CHA = 1, TEST_PATMODE_CHA = 3 (address = 0x13) and TEST PAT_EN_CHB = 1, TEST_PATMODE_CHB = 3 (address = 0x18)

The ADS981x outputs the TEST_PAT0_CHA and TEST_PAT0_CHB register values in place of the ADC A and ADC B data, respectively, in one output frame and the TEST_PAT1_CHA and TEST_PAT1_CHB register values in the next frame.

6.3.6.3.3 Ramp Test Pattern

The ramp test pattern allows the host to specify a digital ramp that is output by the ADS981x. Configure the registers in bank 1 to enable the ramp test pattern:

- Configure the increment value between two successive steps of the digital ramp in the RAMP_INC_CHA (address = 0x13) and RAMP_INC_CHB (address = 0x18) registers, respectively. The digital ramp increments by N + 1, where N is the value configured in these registers.
- Set TEST_PAT_EN_CHA = 1, TEST_PATMODE_CHA = 2 (address = 0x13) and TEST PAT_EN_CHB = 1, TEST_PATMODE_CHB = 2 (address = 0x18).

The ADS981x outputs digital ramp values in place of the ADC A and ADC B data, respectively.

6.4 Device Functional Modes

6.4.1 Power-Down

The ADS981x can be powered-down by either a logic 0 on the $\overline{PWDN}$ pin or by writing 11b to the PD_CH field in address 0xC0 in register bank 1. The device registers are initialized to the default values after power-up and the device must be initialized with a sequence of register write operations; see the *Initialization Sequence* section.

6.4.2 Reset

The ADS981x can be powered down by either a logic 0 on the $\overline{RESET}$ pin or by writing 1b to the RESET field in address 0x00 in register bank 0. The device registers are initialized to the default values after reset and the device must be initialized with a sequence of register write operations; see the *Initialization Sequence* section.

6.4.3 Initialization Sequence

As shown in Table 6-9, the ADS981x must be initialized by a sequence of register writes after device power-up or reset. A free-running sampling clock must be connected to the ADC before executing the initialization sequence. The ADS981x registers are initialized with the default value after the initialization sequence is complete.

Table 6-9. ADS981x Initialization Sequence

STEP NUMBER	REGISTER			COMMENT
	BANK	ADDRESS	VALUE[15:0]	
1	0	0x03	0x0002	Select register bank 1
2	1	0xF6	0x0002	INIT_2 = 1
3	0	0x04	0x000B	INIT_1 = 1011b
4	0	0x03	0x0010	Select register bank 2
5	2	0x12	0x0040	INIT_3 = 1
6	2	0x13	0x8000	INIT_4 = 1
7	2	0x0A	0x4000	INIT_5 = 1
8	Wait 10 µs (min)			
9	2	0x0A	0x0000	INIT_5 = 0
10	0	0x03	0x0002	Select register bank 1
11	1	0xF6	0x0000	INIT_2 = 0
12	0	0x03	0x0010	Select register bank 2
13	2	0x13	0x0000	INIT_5 = 0
14	2	0x12	0x0000	INIT_4 = 0
15	0	0x04	0x0000	INIT_1 = 0
16	0	0x03	0x0002	Select register bank 1
17	1	0x33	0x0030	Write INIT_KEY
18	1	0xF4	0x0000	INIT = 0
19	1	0xF4	0x0002	INIT = 1
20	Wait 1 ms (min)			
21	1	0xF4	0x0000	INIT = 0
22	Wait 1 ms (min)			
23	1	0x33	0x0000	INIT_KEY = 0
24	1	0x0D	<user-defined>	Enable gain error calibration and select ADC output data format
25	1	0x33	0x2040	Enable gain error calibration
26	1	0x34	0x0010	Enable gain error calibration

As shown in Table 6-10, the default settings of the ADS981x can be changed for user-defined configuration:

- Analog inputs: analog input range, bandwidth, and common-mode voltage range
- Data interface: number of output lanes, single or double data rate

Table 6-10. ADS981x User-Configuration

STEP	REGISTER			COMMENT
	BANK	ADDRESS	VALUE[15:0]	
1	1	0xC1	<user-defined>	Configure data interface (data rate, number of lanes) and select internal or external reference
2	1	0xC2 and 0xC3	<user-defined>	Select analog input ranges. See Table 6-1
3	1	0xC0	<user-defined>	Select analog input bandwidth. See Table 6-2
4	1	0xC4 and 0xC5	<user-defined>	Select common-mode range for analog inputs. See Table 6-3 and Table 6-4

6.4.4 Normal Operation

After the ADS981x is initialized (see Table 6-9), the ADS981x converts analog input voltages to digital output. A free-running sampling clock is required for normal device operation; see the *ADC Sampling Clock Input* section.

6.5 Programming

6.5.1 Register Write

Register write access is enabled by setting SPI_RD_EN = 0b. The 16-bit configuration registers are grouped in three register banks and are addressable with an 8-bit register address. Register bank 1 and register bank 2 can be selected for read or write operation by configuring the PAGE_SEL0 and PAGE_SEL1 bits, respectively. Registers in bank 0 are always accessible, irrespective of the PAGE_SELx bits because the register addresses in bank 0 are unique and are not used in register banks 1 and 2.

As shown in Figure 6-9, steps to write to a register are:

1. Frame 1: Write to register address 0x03 in register bank 0 to select either register bank 1 or bank 2 for a subsequent register write. This frame has no effect when writing to registers in bank 0.
2. Frame 2: Write to a register in the bank selected in frame 1. Repeat this step for writing to multiple registers in the same register bank.

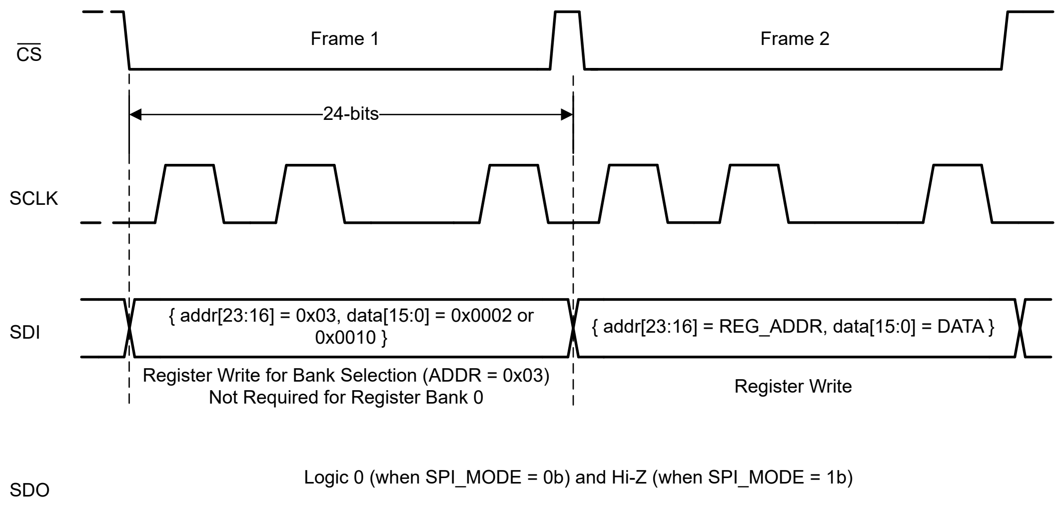


Figure 6-9. Register Write

6.5.2 Register Read

Select the desired register bank by writing to register address 0x03 in register bank 0. Register read access is enabled by setting SPI_RD_EN = 1b and SPI_MODE = 1b in register bank 0. As illustrated in Figure 6-10, registers can be read using two 24-bit SPI frames after SPI_RD_EN and SPI_MODE are set. The first SPI frame selects the register bank. The ADC returns the 16-bit register value in the second SPI frame corresponding to the 8-bit register address.

As illustrated in Figure 6-10, steps to read a register are:

1. Frame 1: With SPI_RD_EN = 0b, write to register address 0x03 in register bank 0 to select the desired register bank 0 for reading.
2. Frame 2: Set SPI_RD_EN = 1b and SPI_MODE = 1b in register address 0x00 in register bank 0.
3. Frame 3: Read any register in the selected bank using a 24-bit SPI frame containing the desired register address. Repeat this step with the address of any register in the selected bank to read the corresponding register.
4. Frame 4: Set SPI_RD_EN = 0 to disable register reads and re-enable register writes.
5. Repeat steps 1 through 4 to read registers in a different bank.

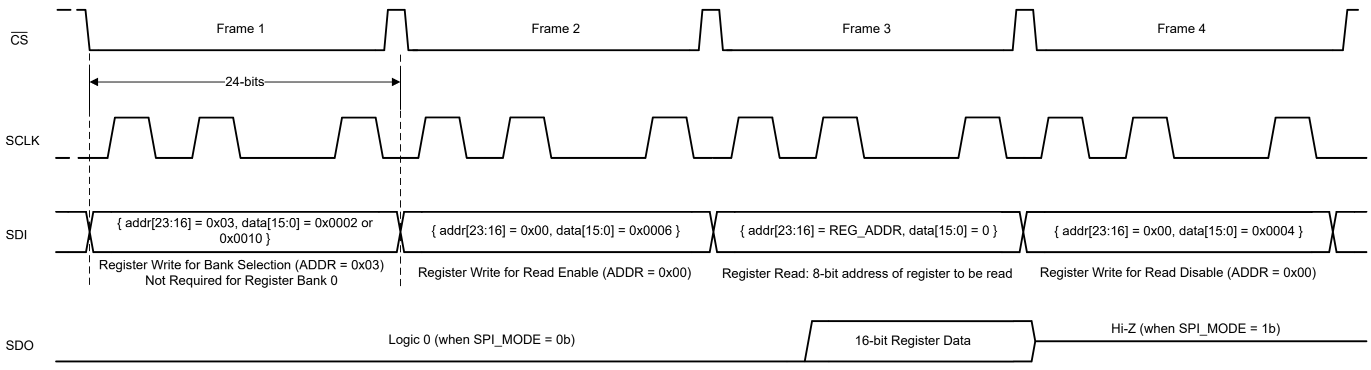


Figure 6-10. Register Read

6.5.3 Multiple Devices: Daisy-Chain Topology for SPI Configuration

Figure 6-11 shows a typical connection diagram showing multiple devices in a daisy-chain topology.

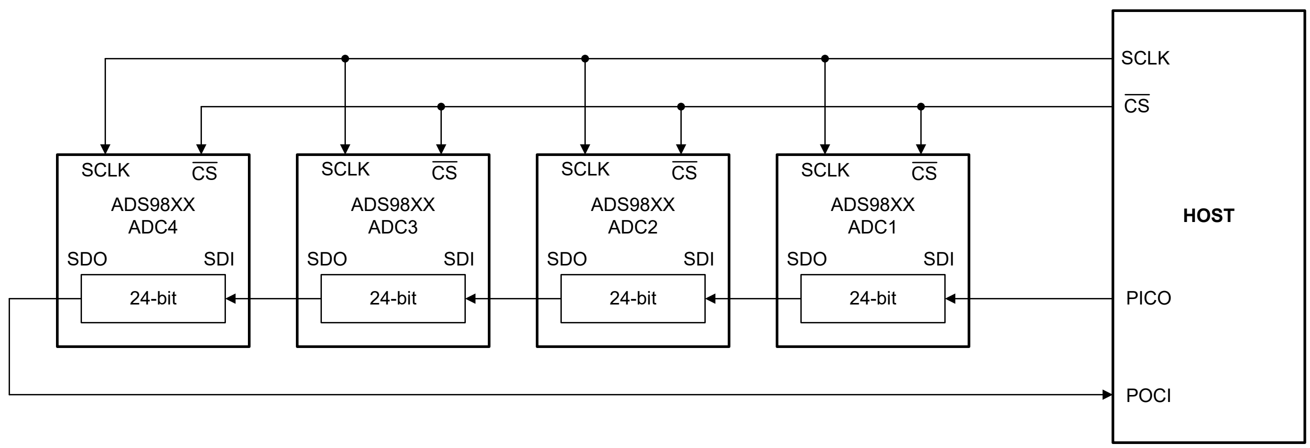


Figure 6-11. Daisy-Chain Connections for SPI Configuration

The $\overline{CS}$ and SCLK inputs of all ADCs are connected together and controlled by a single $\overline{CS}$ and SCLK pin of the controller, respectively. The SDI input pin of the first ADC in the chain (ADC1) is connected to the peripheral IN controller OUT (PICO) pin of the controller, the SDO output pin of ADC1 is connected to the SDI input pin of ADC2, and so on. The SDO output pin of the last ADC in the chain (ADC4) is connected to the peripheral OUT controller IN (POCI) pin of the controller. The data on the PICO pin passes through ADC1 with a 24-SCLK delay, as long as $\overline{CS}$ is active.

The daisy-chain mode must be enabled after power-up or after the device is reset. Set the daisy-chain length in the DAISY_CHAIN_LENGTH register to enable daisy-chain mode. The daisy-chain length is the number of ADCs in the chain excluding ADC1. In Figure 6-11, the DAISY_CHAIN_LENGTH = 3.

6.5.3.1 Register Write With Daisy-Chain

Writing to registers in a daisy-chain configuration requires N × 24-SCLKs in one SPI frame. A register write in a daisy-chain containing four ADCs, as shown in Figure 6-12, requires 96 SCLKs.

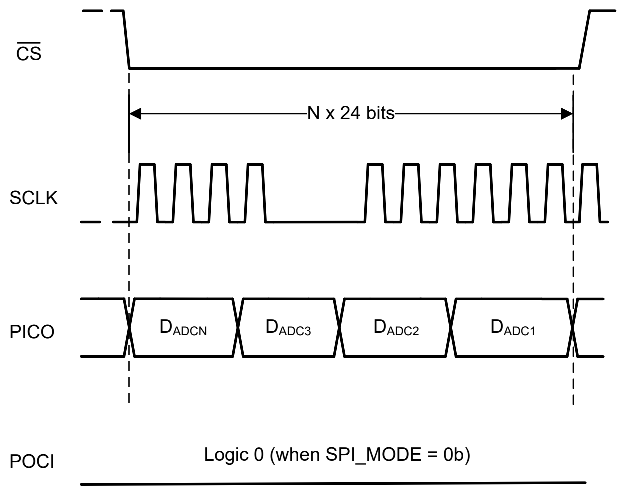


Figure 6-12. Register Write With Daisy-Chain

Daisy-chain mode is enabled on power-up or after device reset. Configure the DAISY_CHAIN_LENGTH field to enable daisy-chain mode. The waveform shown in Figure 6-12 must be repeated N times, where N is the number of ADCs in the daisy-chain. Figure 6-13 provides the SPI waveform, containing N SPI frames, for enabling daisy-chain mode for N ADCs.

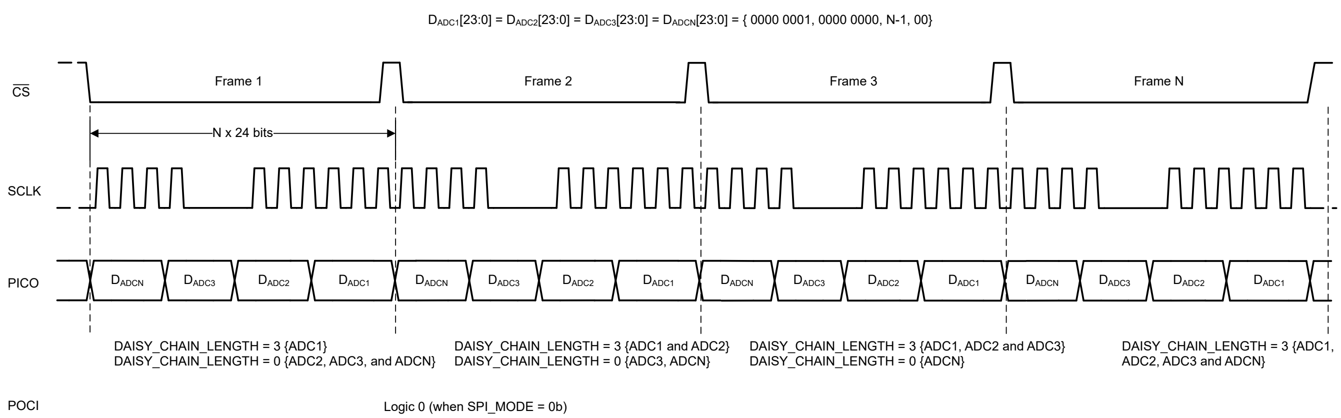


Figure 6-13. Register Write to Configure Daisy-Chain Length

6.5.3.2 Register Read With Daisy-Chain

Figure 6-14 illustrates an SPI waveform for reading registers in a daisy-chain configuration. The steps for reading registers from N ADCs connected in a daisy-chain are as follows:

1. Register read is enabled by writing to the following registers using the *Register Write With Daisy-Chain*:
   a. Write to PAGE_SEL to select the desired register bank
   b. Enable register read by writing SPI_RD_EN = 0b (default on power-up)
2. With the register bank selected and SPI_RD_EN = 0b, the controller can read register data in the following two steps:
   a. N × 24-bit SPI frame containing the 8-bit register address to be read: N-times {0xFE, 0x00, 8-bit register address}
   b. N × 24-bit SPI frame to read out register data: N-times {0xFF, 0xFF, 0xFF}

The 0xFE in step 2a configures the ADC for register read from the specified 8-bit address. At the end of step 2a, the output shift register in the ADC is loaded with register data. The ADC returns the 8-bit register address and corresponding 16-bit register data in step 2b.

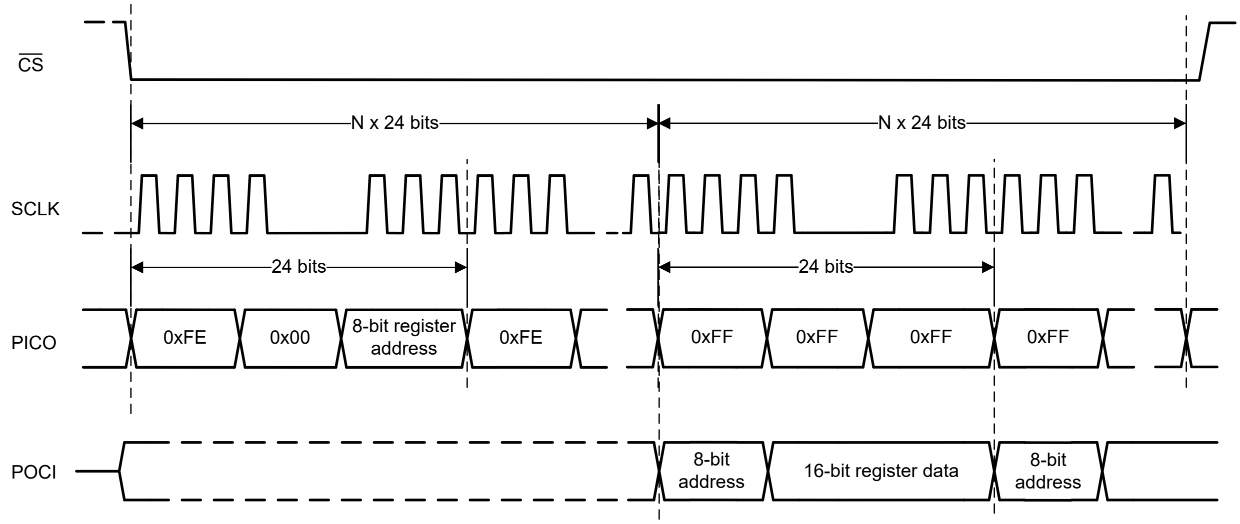


Figure 6-14. Register Read With Daisy-Chain

7 Register Map

7.1 Register Bank 0

Figure 7-1. Register Bank 0 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	RESERVED													SPI_MODE	SPI_RD_EN	RESET
01h	RESERVED									DAISY_CHAIN_LEN					RESERVED	
03h	RESERVED								REG_BANK_SEL							
04h	RESERVED												INIT_1			
06h	REG_00H_READBACK															

Table 7-1. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-*n*		Value after reset or the default value

7.1.1 Register 00h (offset = 0h) [reset = 0h]

Figure 7-2. Register 00h

15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					SPI_MODE	SPI_RD_EN	RESET
W-0h					W-0h	W-0h	W-0h

Figure 7-3. Register 00h Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	W	0h	Reserved. Do not change from the default reset value.
2	SPI_MODE	W	0h	Select between legacy SPI mode and daisy-chain SPI mode for the configuration interface for register access. 0 : Daisy-chain SPI mode 1 : Legacy SPI mode
1	SPI_RD_EN	W	0h	Enable register read access in legacy SPI mode. This bit has no effect in daisy-chain SPI mode. 0 : Register read disabled 1 : Register read enabled
0	RESET	W	0h	ADC reset control. 0 : Normal device operation 1 : Reset ADC and all registers

7.1.2 Register 01h (offset = 1h) [reset = 0h]

Figure 7-4. Register 01h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	DAISY_CHAIN_LEN					RESERVED	
R/W-0h	R/W-0h					R/W-0h	

Figure 7-5. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6-2	DAISY_CHAIN_LEN	R/W	0h	Configure the number of ADCs connected in daisy-chain for the SPI configuration. 0 : 1 ADC 1 : 2 ADCs 31 : 32 ADCs
1-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.1.3 Register 03h (offset = 3h) [reset = 2h]

Figure 7-6. Register 03h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
REG_BANK_SEL							
R/W-2h							

Figure 7-7. Register 03h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-0	REG_BANK_SEL	R/W	2h	Register bank selection for read and write operations. 0 : Select register bank 0 2 : Select register bank 1 16 : Select register bank 2

7.1.4 Register 04h (offset = 4h) [reset = 0h]

Figure 7-8. Register 04h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				INIT_1			
R/W-0h							

Figure 7-9. Register 04h Field Descriptions

Bit	Field	Type	Reset	Description
3-0	INIT_1	R/W	0h	INIT_1 field for device initialization. Write 1011b during the initialization sequence. Write 0000b for normal operation.

7.1.5 Register 06h (offset = 6h) [reset = 2h]

Figure 7-10. Register 06h

15	14	13	12	11	10	9	8
REG_00H_READBACK							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
REG_00H_READBACK							
R-5h							

Figure 7-11. Register 06h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	REG_00H_READ BACK	R	2h	This register is a copy of the register address 0x00 for readback. The register address 0x00 is write-only. The default readback value is 2h because SPI_RD_EN in address 0x00 must be set to 1 for register reads.

7.2 Register Bank 1

Figure 7-12. Register Bank 1 Map

<table>
<tr><th>ADD</th><th>D15</th><th>D14</th><th>D13</th><th>D12</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0Dh</td><td colspan="2">RESERVED</td><td>DATA_FORMAT</td><td colspan="4">RESERVED</td><td colspan="2">GE_CAL_EN1</td><td colspan="7">RESERVED</td></tr>
<tr><td>12h</td><td colspan="12">RESERVED</td><td>XOR_EN</td><td colspan="2">RESERVED</td><td>DATA_LANES</td></tr>
<tr><td>13h</td><td colspan="8">RESERVED</td><td colspan="4">RAMP_INC_ADC_A</td><td colspan="2">TEST_PAT_MODE_ADC_A</td><td>TEST_PAT_EN_ADC_A</td><td>RESERVED</td></tr>
<tr><td>14h</td><td colspan="16">TEST_PAT0_ADC_A</td></tr>
<tr><td>15h</td><td colspan="8">TEST_PAT1_ADC_A</td><td colspan="8">TEST_PAT0_ADC_A</td></tr>
<tr><td>16h</td><td colspan="16">TEST_PAT1_ADC_A</td></tr>
<tr><td>18h</td><td colspan="8">RESERVED</td><td colspan="4">RAMP_INC_ADC_B</td><td colspan="2">TEST_PAT_MODE_ADC_B</td><td>TEST_PAT_EN_ADC_B</td><td>RESERVED</td></tr>
<tr><td>19h</td><td colspan="16">TEST_PAT0_ADC_B</td></tr>
<tr><td>1Ah</td><td colspan="8">TEST_PAT1_ADC_B</td><td colspan="8">TEST_PAT0_ADC_B</td></tr>
<tr><td>1Bh</td><td colspan="16">TEST_PAT1_ADC_B</td></tr>
<tr><td>1Ch</td><td colspan="2">RESERVED</td><td colspan="6">USER_BITS_ADC_B</td><td colspan="2">RESERVED</td><td colspan="6">USER_BITS_ADC_A</td></tr>
<tr><td>33h</td><td colspan="2">RESERVED</td><td>GE_CAL_EN3</td><td colspan="6">RESERVED</td><td>GE_CAL_EN2</td><td colspan="2">INIT_KEY</td><td colspan="4">RESERVED</td></tr>
<tr><td>34h</td><td colspan="11">RESERVED</td><td>GE_CAL_EN4</td><td colspan="4">RESERVED</td></tr>
<tr><td>C0h</td><td colspan="6">RESERVED</td><td colspan="8">ANA_BW</td><td colspan="2">PD_CH</td></tr>
<tr><td>C1h</td><td colspan="4">RESERVED</td><td>PD_REF</td><td>RESERVED</td><td>DATA_LANES</td><td>DATA_RATE</td><td colspan="8">RESERVED</td></tr>
<tr><td>C2h</td><td colspan="4">RANGE_CH4</td><td colspan="4">RANGE_CH3</td><td colspan="4">RANGE_CH2</td><td colspan="4">RANGE_CH1</td></tr>
<tr><td>C3h</td><td colspan="4">RANGE_CH8</td><td colspan="4">RANGE_CH7</td><td colspan="4">RANGE_CH6</td><td colspan="4">RANGE_CH5</td></tr>
<tr><td>C4h</td><td colspan="6">RESERVED</td><td colspan="2">CM_RNG_ADC_B</td><td colspan="2">CM_RNG_ADC_A</td><td colspan="2">RESERVED</td><td>CM_EN_ADC_B</td><td>CM_EN_ADC_A</td><td>RESERVED</td><td>PD_CHIP</td></tr>
<tr><td>C5h</td><td colspan="11">RESERVED</td><td>CM_CTRL_EN</td><td colspan="4">RESERVED</td></tr>
<tr><td>F4h</td><td colspan="14">RESERVED</td><td>INIT</td><td>RESERVED</td></tr>
<tr><td>F6h</td><td colspan="14">RESERVED</td><td>INIT_2</td><td>RESERVED</td></tr>
</table>

Table 7-2. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-n		Value after reset or the default value

7.2.1 Register 0Dh (offset = Dh) [reset = 2002h]

Figure 7-13. Register 0Dh

15	14	13	12	11	10	9	8
RESERVED		DATA_FORMAT	RESERVED				GE_CAL_EN1
R/W-0h		R/W-1h	R/W-0h				R/W-0h

7	6	5	4	3	2	1	0
GE_CAL_EN1	RESERVED						
R/W-0h	R/W-2h						

Figure 7-14. Register 0Dh Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
13	DATA_FORMAT	R/W	1h	Select data format for the ADC conversion result. 0 : Straight binary format 1 : Two's-complement format
12-9	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
8-7	GE_CAL_EN1	R/W	0h	Global control for gain error calibration. 0 : Gain error calibration disabled for all channels 3 : Gain error calibration enabled for all channels
6-0	RESERVED	R/W	2h	Reserved. Do not change from the default reset value.

7.2.2 Register 12h (offset = 12h) [reset = 2h]

Figure 7-15. Register 12h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							

7	6	5	4	3	2	1	0
RESERVED				XOR_EN	RESERVED		
R/W-0h				R/W-0h	R/W-2h		

Figure 7-16. Register 12h Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
3	XOR_EN	R/W	0h	Enables XOR operation on ADC conversion result. 0 : XOR operation is disabled 1 : ADC conversion result is bit-wise XOR with the LSB of the ADC conversion result
2-0	RESERVED	R/W	2h	Reserved. Do not change from the default reset value.

7.2.3 Register 13h (offset = 13h) [reset = 0h]

Figure 7-17. Register 13h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMP_INC_ADC_A				TEST_PAT_MODE_ADC_A		TEST_PAT_EN_ADC_A	RESERVED
R/W-0h				R/W-0h		R/W-0h	R/W-0h

Figure 7-18. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-4	RAMP_INC_ADC_A	R/W	0h	Increment value for the ramp pattern output. The output ramp increments by N+1, where N is the value configured in this register.
3-2	TEST_PAT_MODE_ADC_A	R/W	0h	Select digital test pattern for analog input channels 1, 2, 3, and 4. 0 : Fixed pattern as configured in the TEST_PAT0_ADC_A register 1 : Fixed pattern as configured in the TEST_PAT0_ADC_A register 2 : Digital ramp output 3 : Alternate fixed pattern output as configured in the TEST_PAT0_ADC_A and TEST_PAT1_ADC_A registers
1	TEST_PAT_EN_ADC_A	R/W	0h	Enable digital test pattern for data corresponding to channels 1, 2, 3, and 4. 0 : ADC conversion result is launched on the data interface 1 : Digital test pattern is launched corresponding to channels 1, 2, 3, and 4 on the data interface
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.4 Register 14h (offset = 14h) [reset = 0h]

Figure 7-19. Register 14h

15	14	13	12	11	10	9	8
TEST_PAT0_ADC_A[15:0]							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TEST_PAT0_ADC_A[15:0]							
R/W-0h							

Figure 7-20. Register 14h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TEST_PAT0_ADC_A[15:0]	R/W	0h	Lower 16 bits of test pattern 0 for channels 1, 2, 3, and 4 corresponding to ADC A.

7.2.5 Register 15h (offset = 15h) [reset = 0h]

Figure 7-21. Register 15h

15	14	13	12	11	10	9	8
TEST_PAT1_ADC_A[7:0]							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TEST_PAT0_ADC_A[23:16]							
R/W-0h							

Figure 7-22. Register 15h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TEST_PAT1_ADC_A[7:0]	R/W	0h	Lower eight bits of test pattern 1 for channels 1, 2, 3, and 4 corresponding to ADC A.
7-0	TEST_PAT0_ADC_A[23:16]	R/W	0h	Upper eight bits of test pattern 0 for channels 1, 2, 3, and 4 corresponding to ADC A.

7.2.6 Register 16h (offset = 16h) [reset = 0h]

Figure 7-23. Register 16h

15	14	13	12	11	10	9	8
TEST_PAT1_ADC_A[23:8]							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TEST_PAT1_ADC_A[23:8]							
R/W-0h							

Figure 7-24. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TEST_PAT1_ADC_A[23:8]	R/W	0h	Upper 16 bits of test pattern 1 for channels 1, 2, 3, and 4 corresponding to ADC A.

7.2.7 Register 18h (offset = 18h) [reset = 0h]

Figure 7-25. Register 18h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RAMP_INC_ADC_B				TEST_PAT_MODE_ADC_B		TEST_PAT_EN_ADC_B	RESERVED
R/W-0h				R/W-0h		R/W-0h	R/W-0h

Figure 7-26. Register 18h Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
7-4	RAMP_INC_ADC_B	R/W	0h	Increment value for the ramp pattern output. The output ramp increments by N+1, where N is the value configured in this register.
3-2	TEST_PAT_MODE_ADC_B	R/W	0h	Select digital test pattern for analog input channels 5, 6, 7, and 8. 0 : Fixed pattern as configured in the TEST_PAT0_ADC_B register 1 : Fixed pattern as configured in the TEST_PAT0_ADC_B register 2 : Digital ramp output 3 : Alternate fixed pattern output as configured in the TEST_PAT0_ADC_B and TEST_PAT1_ADC_B registers
1	TEST_PAT_EN_ADC_B	R/W	0h	Enable digital test pattern for data corresponding to channel 5, 6, 7, and 8. 0 : ADC conversion result is launched on the data interface 1 : Digital test pattern is launched corresponding to channels 5, 6, 7, and 8 on the data interface
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.8 Register 19h (offset = 19h) [reset = 0h]

Figure 7-27. Register 19h

15	14	13	12	11	10	9	8
TEST_PAT0_ADC_B[15:0]							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TEST_PAT0_ADC_B[15:0]							
R/W-0h							

Figure 7-28. Register 19h Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TEST_PAT0_ADC_B[15:0]	R/W	0h	Lower 16 bits of test pattern 0 for channels 5, 6, 7, and 8 corresponding to ADC B.

7.2.9 Register 1Ah (offset = 1Ah) [reset = 0h]

Figure 7-29. Register 1Ah

15	14	13	12	11	10	9	8
TEST_PAT1_ADC_B[7:0]							
R/W-0h							
7	6	5	4	3	2	1	0
TEST_PAT0_ADC_B[23:16]							
R/W-0h							

Figure 7-30. Register 1Ah Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TEST_PAT1_ADC_B[7:0]	R/W	0h	Lower eight bits of test pattern 1 for channels 5, 6, 7, and 8 corresponding to ADC B.
7-0	TEST_PAT0_ADC_B[23:16]	R/W	0h	Upper eight bits of test pattern 0 for channels 5, 6, 7, and 8 corresponding to ADC B.

7.2.10 Register 1Bh (offset = 1Bh) [reset = 0h]

Figure 7-31. Register 1Bh

15	14	13	12	11	10	9	8
TEST_PAT1_ADC_B[23:8]							
R/W-0h							
7	6	5	4	3	2	1	0
TEST_PAT1_ADC_B[23:8]							
R/W-0h							

Figure 7-32. Register 1Bh Field Descriptions

Bit	Field	Type	Reset	Description
15-0	TEST_PAT1_ADC_B[23:8]	R/W	0h	Upper 16 bits of test pattern 1 for channels 5, 6, 7, and 8 corresponding to ADC B.

7.2.11 Register 1Ch (offset = 1Ch) [reset = 0h]

Figure 7-33. Register 1Ch

15	14	13	12	11	10	9	8
RESERVED		USER_BITS_ADC_B					
R/W-0h		R/W-0h					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		USER_BITS_ADC_A					
R/W-0h		R/W-0h					

Figure 7-34. Register 1Ch Field Descriptions

Bit	Field	Type	Reset	Description
15-8	USER_BITS_ADC_B	R/W	0h	User-defined bits appended to the ADC conversion result from channels 5, 6, 7, and 8.
7-0	USER_BITS_ADC_A	R/W	0h	User-defined bits appended to the ADC conversion result from channels 1, 2, 3, and 4.

7.2.12 Register 33h (offset = 33h) [reset = 0h]

Figure 7-35. Register 33h

15	14	13	12	11	10	9	8
RESERVED		GE_CAL_EN3	RESERVED				
R/W-0h		R/W-0h	R/W-0h				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	GE_CAL_EN2	INIT_KEY		RESERVED			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			

Figure 7-36. Register 33h Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
13	GE_CAL_EN3	R/W	0h	Global control for gain error calibration. 0 : Gain error calibration disabled for all channels 1 : Gain error calibration enabled for all channels
12-7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6	GE_CAL_EN2	R/W	0h	Global control for gain error calibration. 0 : Gain error calibration disabled for all channels 1 : Gain error calibration enabled for all channels
5-4	INIT_KEY	R/W	0h	Device initialization sequence access key. Write 11b to access the device initialization sequence. Write 00b for normal operation.
3-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.13 Register 34h (offset = 34h) [reset = 0h]

Figure 7-37. Register 34h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							

7	6	5	4	3	2	1	0
RESERVED			GE_CAL_EN4	RESERVED			
R/W-0h			R/W-0h	R/W-0h			

Figure 7-38. Register 34h Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
4	GE_CAL_EN4	R/W	0h	Global control for gain error calibration. 0 : Gain error calibration disabled for all channels 1 : Gain error calibration enabled for all channels
3-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.14 Register C0h (offset = C0h) [reset = 0h]

Figure 7-39. Register C0h

15	14	13	12	11	10	9	8
RESERVED						ANA_BW	
R/W-0h						R/W-0h	

7	6	5	4	3	2	1	0
ANA_BW						PD_CH	
R/W-0h						R/W-0h	

Figure 7-40. Register C0h Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
9-2	ANA_BW	R/W	0h	Select analog input bandwidth for the respective analog input channels. MSB = BW control for channel 8. LSB = BW control for channel 1. 0 : Low-noise mode 1 : Wide-bandwidth mode
1-0	PD_CH	R/W	0h	Power-down control for the analog input channels. 0 : Normal operation 1 : Channels 1, 2, 3, and 4 powered down 2 : Channels 5, 6, 7, and 8 powered down 3 : All channels powered down

7.2.15 Register C1h (offset = C1h) [reset = 0h]

Figure 7-41. Register C1h

15	14	13	12	11	10	9	8
RESERVED				PD_REF	RESERVED	DATA_LANES	DATA_RATE
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R/W-0h							

Figure 7-42. Register C1h Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
11	PD_REF	R/W	0h	ADC reference voltage source selection. 0 : Internal reference enabled. 1 : Internal reference disabled. Connect the external reference voltage to the REFIO pin.
10	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
9	DATA_LANES	R/W	0h	Select number of output data lanes per ADC channel. 0 : 2-lane mode. ADC A data are output on pins D3 and D2. ADC B data are output on pins D1 and D0. 1 : 1-lane mode. ADC A data are output on pin D3. ADC B data are output on pin D1.
8	DATA_RATE	R/W	0h	Select data rate for the data interface. 0 : Double data rate (DDR) 1 : Single data rate (SDR)
7-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.16 Register C2h (offset = C2h) [reset = 0h]

Figure 7-43. Register C2h

15	14	13	12	11	10	9	8
RANGE_CH4				RANGE_CH3			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
RANGE_CH2				RANGE_CH1			
R/W-0h				R/W-0h			

Figure 7-44. Register C2h Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RANGE_CH4	R/W	0h	Select input voltage range for channel 4. 0 : ±5 V 1 : ±3.5 V 2 : ±2.5 V 3 : ±7 V 4 : ±10 V 5 : ±12 V
11-8	RANGE_CH3	R/W	0h	Select input voltage range for channel 3. 0 : ±5 V 1 : ±3.5 V 2 : ±2.5 V 3 : ±7 V 4 : ±10 V 5 : ±12 V
7-4	RANGE_CH2	R/W	0h	Select input voltage range for channel 2. 0 : ±5 V 1 : ±3.5 V 2 : ±2.5 V 3 : ±7 V 4 : ±10 V 5 : ±12 V
3-0	RANGE_CH1	R/W	0h	Select input voltage range for channel 1. 0 : ±5 V 1 : ±3.5 V 2 : ±2.5 V 3 : ±7 V 4 : ±10 V 5 : ±12 V

7.2.17 Register C3h (offset = C3h) [reset = 0h]

Figure 7-45. Register C3h

15	14	13	12	11	10	9	8
RANGE_CH8				RANGE_CH7			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
RANGE_CH6				RANGE_CH5			
R/W-0h				R/W-0h			

Figure 7-46. Register C3h Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RANGE_CH8	R/W	0h	Select input voltage range for channel 8. 0 : ±5 V 1 : ±3.5 V 2 : ±2.5 V 3 : ±7 V 4 : ±10 V 5 : ±12 V
11-8	RANGE_CH7	R/W	0h	Select input voltage range for channel 7. 0 : ±5 V 1 : ±3.5 V 2 : ±2.5 V 3 : ±7 V 4 : ±10 V 5 : ±12 V
7-4	RANGE_CH6	R/W	0h	Select input voltage range for channel 6. 0 : ±5 V 1 : ±3.5 V 2 : ±2.5 V 3 : ±7 V 4 : ±10 V 5 : ±12 V
3-0	RANGE_CH5	R/W	0h	Select input voltage range for channel 5. 0 : ±5 V 1 : ±3.5 V 2 : ±2.5 V 3 : ±7 V 4 : ±10 V 5 : ±12 V

7.2.18 Register C4h (offset = C4h) [reset = 0h]

Figure 7-47. Register C4h

15	14	13	12	11	10	9	8
RESERVED						CM_RNG_ADC_B	
R/W-0h						R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CM_RNG_ADC_A		RESERVED		CM_EN_ADC_B	CM_EN_ADC_A	RESERVED	PD_CHIP
R/W-0h		R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

Figure 7-48. Register C4h Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
9-8	CM_RNG_ADC_B	R/W	0h	Common-mode range for channels 5, 6, 7, and 8. 0 : CM range equal to ±RANGE / 2 for the respective channels 1 : CM range equal to ±6 V for channels 5, 6, 7, and 8 2 : CM range equal to ±12 V for channels 5, 6, 7, and 8
7-6	CM_RNG_ADC_A	R/W	0h	Common-mode range for channels 1, 2, 3, and 4. 0 : CM range equal to ±RANGE / 2 for the respective channels 1 : CM range equal to ±6 V for channels 1, 2, 3, and 4 2 : CM range equal to ±12 V for channels 1, 2, 3, and 4
5-4	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
3	CM_EN_ADC_B	R/W	0h	Enable wide-common-mode range control for analog input channels 1 to 4. 0 : Wide-common-mode range control disabled 1 : Wide-common-mode range control enabled for channels 1, 2, 3, and 4
2	CM_EN_ADC_A	R/W	0h	Enable wide-common-mode range control for analog input channels 5 to 8. 0 : Wide-common-mode range control disabled 1 : Wide-common-mode range control enabled for channels 5, 6, 7, and 8
1	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
0	PD_CHIP	R/W	0h	Full chip power-down control. 0 : Normal device operation 1 : Full device powered-down

7.2.19 Register C5h (offset = C5h) [reset = 0h]

Figure 7-49. Register C5h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							

7	6	5	4	3	2	1	0
RESERVED			CM_CTRL_EN	RESERVED			
R/W-0h			R/W-0h	R/W-0h			

Figure 7-50. Register C5h Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
4	CM_CTRL_EN	R/W	0h	Enable wide-common-mode range control for all analog input channels. 0 : CM range for all analog input channels is ±12 V 1 : CM range is user-defined in the CM_EN_ADC_A, CM_EN_ADC_B, CM_RNG_ADC_A, and CM_RNG_ADC_B registers
3-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.20 Register F4h (offset = F4h) [reset = 0h]

Figure 7-51. Register F4h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							

7	6	5	4	3	2	1	0
RESERVED						CM_CTRL_EN	RESERVED
R/W-0h						R/W-0h	R/W-0h

Figure 7-52. Register F4h Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
1	INIT	R/W	0h	INIT field for device initialization. Write 1b during the initialization sequence. Write 0b for normal operation.
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.2.21 Register F6h (offset = F6h) [reset = 0h]

Figure 7-53. Register F6h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						INIT_2	RESERVED
R/W-0h						R/W-0h	R/W-0h

Figure 7-54. Register F6h Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
1	INIT_2	R/W	0h	INIT_2 field for device initialization. Write 1b during the initialization sequence. Write 0b for normal operation.
0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.3 Register Bank 2

Figure 7-55. Register Bank 2 Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
12h	RESERVED									INIT_3	RESERVED					
13h	INIT_4	RESERVED														
0Ah	RESERVED	INIT_2	RESERVED													

Table 7-3. Register Section/Block Access Type Codes

Access Type	Code	Description
R	R	Read
W	W	Write
R/W	R/W	Read or write
Reset or Default Value		
-*n*		Value after reset or the default value

7.3.1 Register 12h (offset = 12h) [reset = 0h]

Figure 7-56. Register 12h

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	INIT_3	RESERVED					
R/W-0h	R/W-0h	R/W-0h					

Figure 7-57. Register 12 Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
6-6	INIT_3	R/W	0h	INIT_3 field for device initialization. Write 1b during the initialization sequence. Write 0b for normal operation.
5-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.3.2 Register 13h (offset = 13h) [reset = 0h]

Figure 7-58. Register 13h

15	14	13	12	11	10	9	8
INIT_4	RESERVED						
R/W-0h	R/W-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R/W-0h							

Figure 7-59. Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
15-15	INIT_4	R/W	0h	INIT_4 field for device initialization. Write 1b during initialization sequence. Write 0b for normal operation.
14-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

7.3.3 Register 0Ah (offset = 0Ah) [reset = 0h]

Figure 7-60. Register 0Ah

15	14	13	12	11	10	9	8
RESERVED	INIT_5	RESERVED					
R/W-0h	R/W-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R/W-0h							

Figure 7-61. Register 0A Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.
14	INIT_5	R/W	0h	INIT_5 field for device initialization. Write 1b during initialization sequence. Write 0b for normal operation.
13-0	RESERVED	R/W	0h	Reserved. Do not change from the default reset value.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following section gives an example circuit and recommendations for using the ADS9817 in a data acquisition (DAQ) system. The ADS9817 includes an integrated analog front-end for each input channel and an integrated precision reference with a buffer. As such, this device family does not require any additional external circuits for driving the reference or analog input pins of the ADC.

8.2 Typical Application

8.2.1 Data Acquisition (DAQ) System

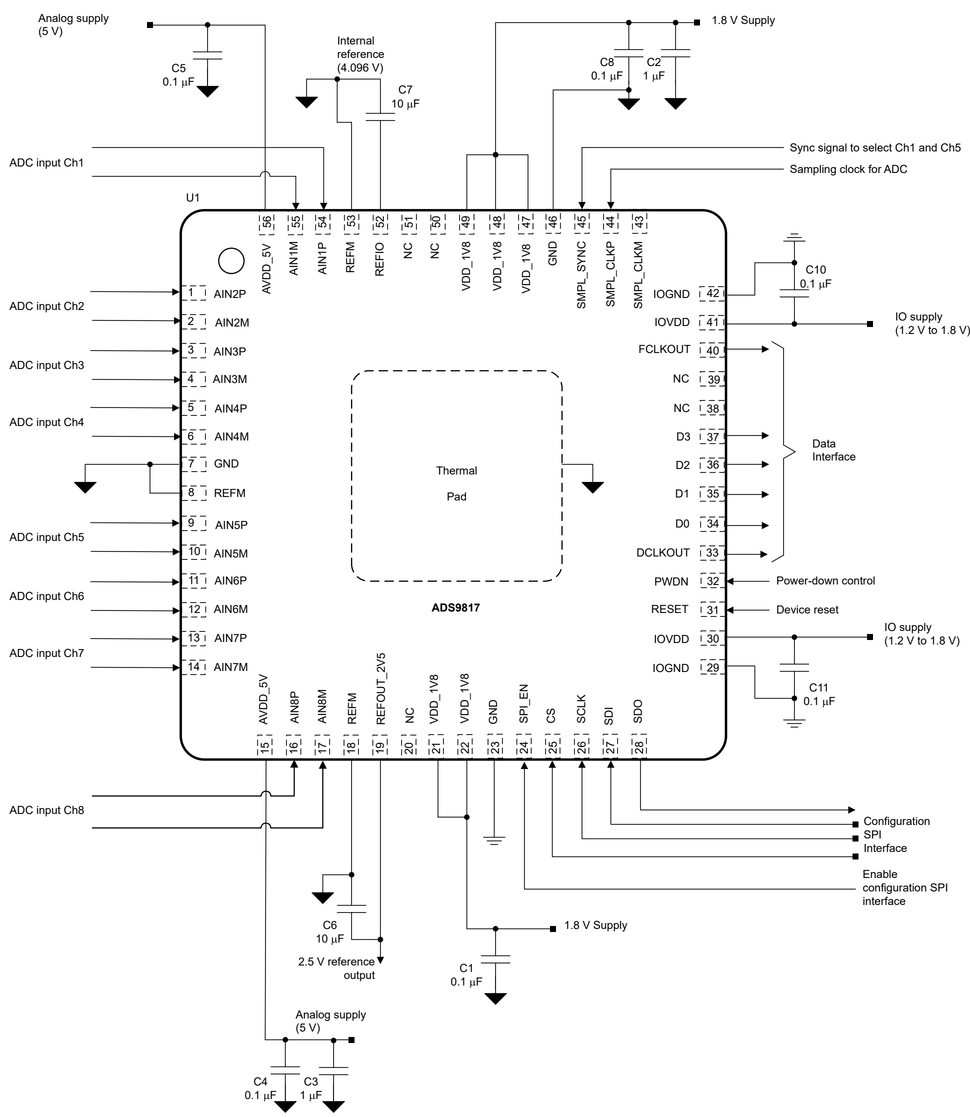


Figure 8-1. Recommended Schematic

8.2.2 Design Requirements

The goal of this application is to design an 8-channel data acquisition system (DAQ) based on the ADS981x with an internal reference. Table 8-1 lists the parameters for this design.

Table 8-1. Design Parameters

PARAMETER	VALUE
Sampling rate	Up to 2 MSPS/channel
ADC reference	Internal, 4.096 V
ADC analog input type	Differential
ADC analog input range	–5 V to +5 V
Output impedance of the source driving the ADC analog inputs	Up to 200 Ω

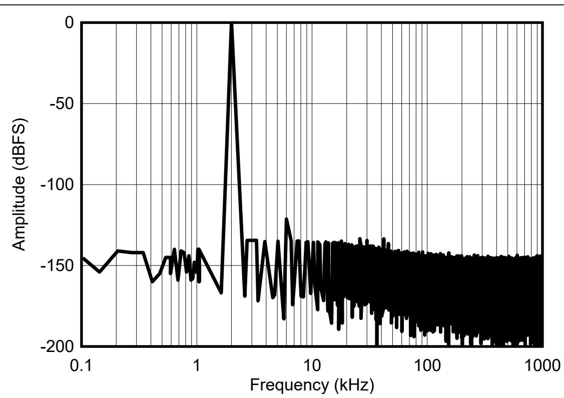
8.2.3 Detailed Design Procedure

8.2.3.1 CMOS Data Interface

The ADS981x features a high-speed CMOS serial interface for ADC data output. ADC data are launched on D[3:0] and the corresponding data clock is launched on DCLKOUT. The DCLKOUT frequency is 192 MHz for 2 MSPS/channel sampling rate (24 SMPL_CLK bits and an 8-MHz SMPL_CLK rate).

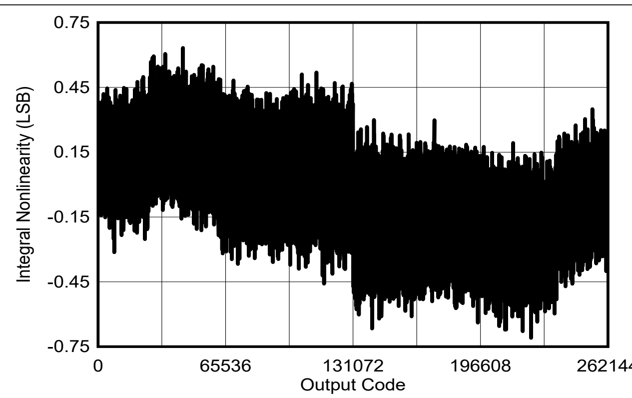
High-speed CMOS switching can create ground bounce that adversely impacts the SNR of the ADC. Ground bounce increments with increases in PCB trace capacitance. Minimize the PCB trace length for D[3:0] and DCLKOUT. Place a CMOS buffer, with low input capacitance, close to the ADS981x to minimize the effect of CMOS switching noise.

8.2.4 Application Curves



SNR = 91.5 dBFS, THD = –113 dB at f_{IN} = 2 kHz

Figure 8-2. Typical FFT With Low-Bandwidth LPF, RANGE = ±5 V



Typical INL = ±0.75 LSB

Figure 8-3. Typical INL With Low-Bandwidth LPF

8.3 Power Supply Recommendations

The ADS981x has three separate power supplies: AVDD_5V, VDD_1V8, and IOVDD. There is no requirement for a specific power-up sequence. The data and configuration digital interfaces are powered by IOVDD. A common 1.8-V supply powers the VDD_1V8 and IOVDD pins. Figure 8-4 illustrates the decoupling capacitor connections for the respective power supplies. Each power-supply pin must have separate decoupling capacitors.

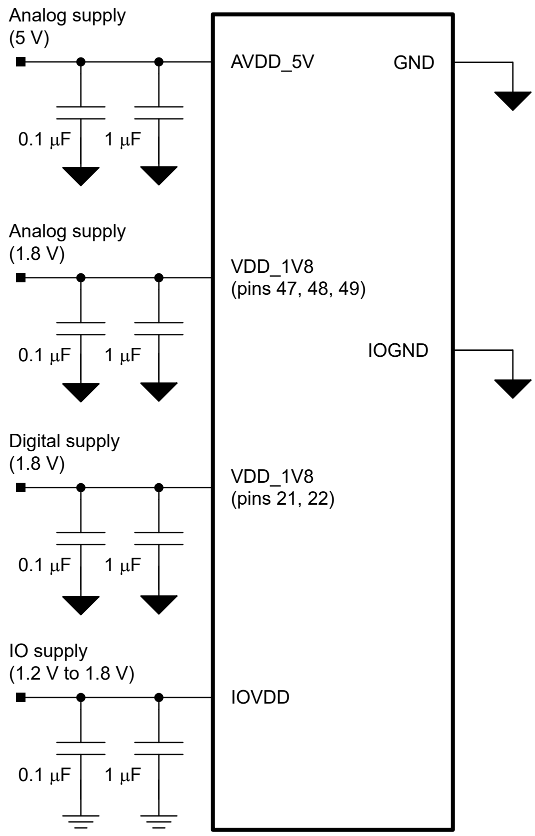


Figure 8-4. Power-Supply Decoupling

8.4 Layout

8.4.1 Layout Guidelines

Figure 8-5 illustrates a board layout example for the ADS981x. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference signals away from noise sources.

Use 0.1-µF ceramic bypass capacitors in close proximity to the AVDD_5V, VDD_1V8, and IOVDD power-supply pins. Avoid placing vias between the power-supply pins and the bypass capacitors.

Place the reference decoupling capacitor close to the device REFIO and REFM pins. Avoid placing vias between the REFIO pin and the bypass capacitors. Connect the GND, REFM, and IOGND pins to a ground plane using short, low-impedance paths.

8.4.2 Layout Example

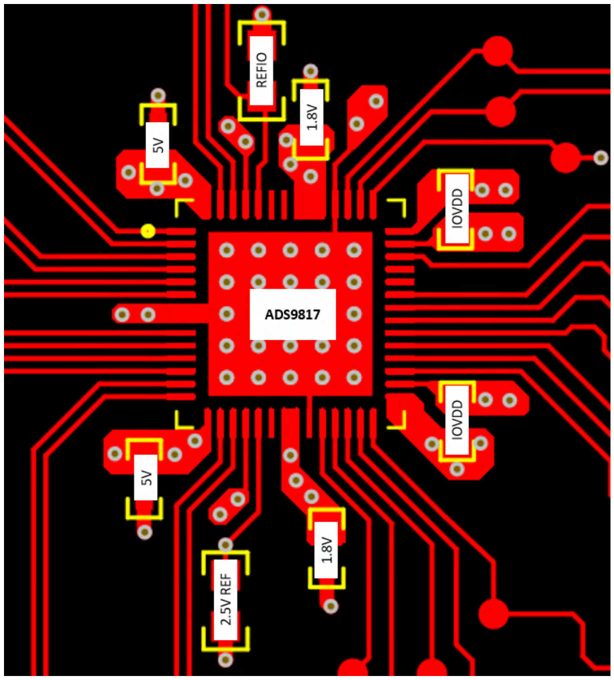


Figure 8-5. Example Layout

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2023) to Revision A (December 2023)	Page
• Changed document status from *Advance Information* to *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS9817RSHR	ACTIVE	VQFN	RSH	56	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS9817	Samples
ADS9817RSHT	ACTIVE	VQFN	RSH	56	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS9817	Samples
PADS9815RSHT	ACTIVE	VQFN	RSH	56	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

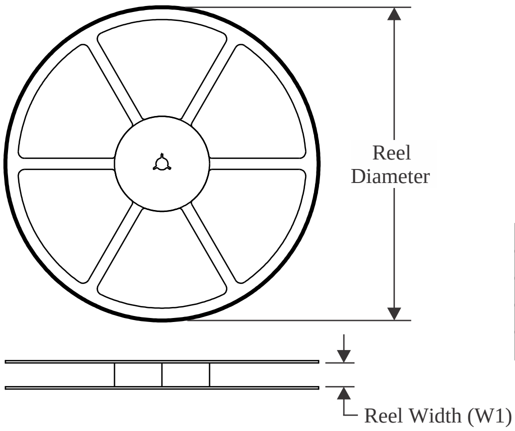
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

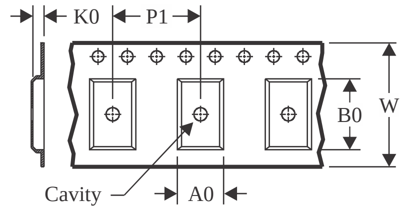
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

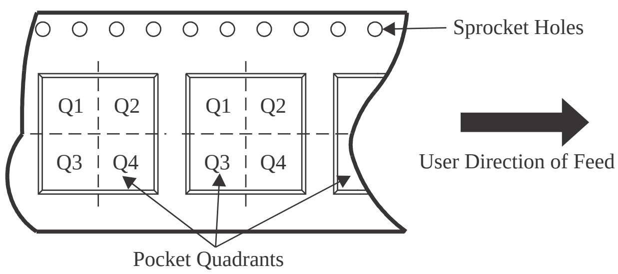


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

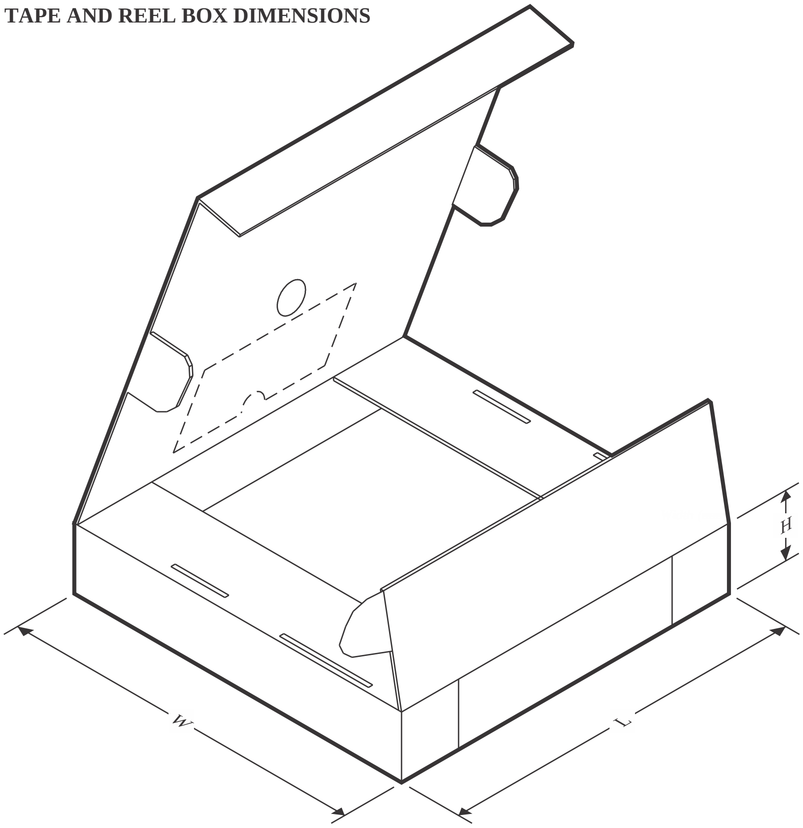
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS9817RSHR	VQFN	RSH	56	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
ADS9817RSHT	VQFN	RSH	56	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

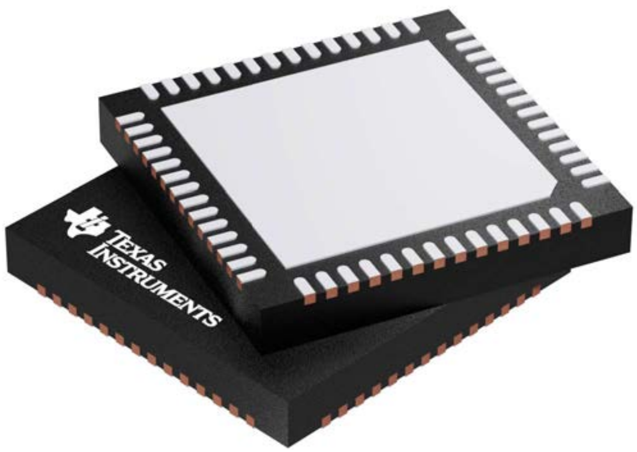


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS9817RSHR	VQFN	RSH	56	2500	367.0	367.0	35.0
ADS9817RSHT	VQFN	RSH	56	250	210.0	185.0	35.0

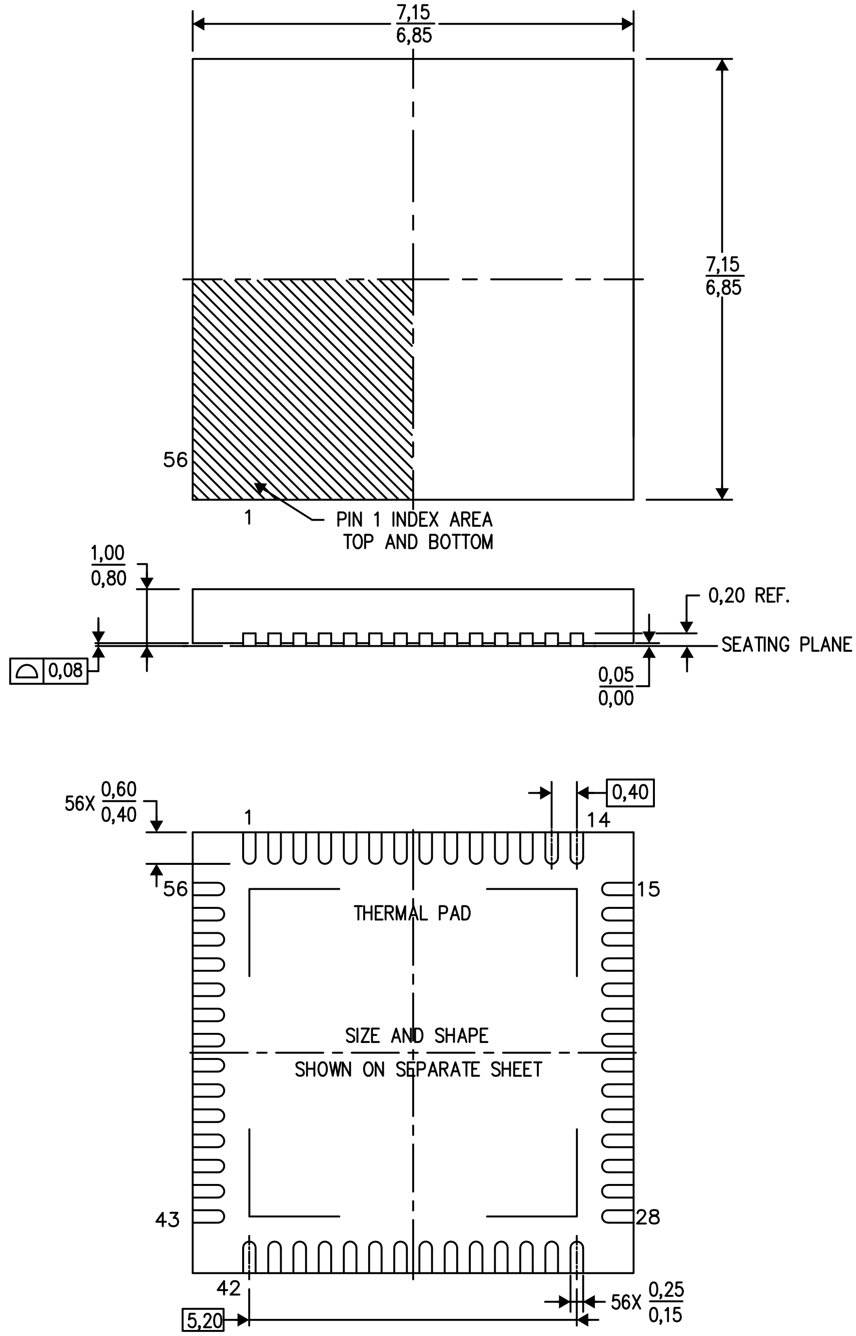
RSH 56 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RSH (S-PVQFN-N56) PLASTIC QUAD FLATPACK NO-LEAD



4207513/C 03/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

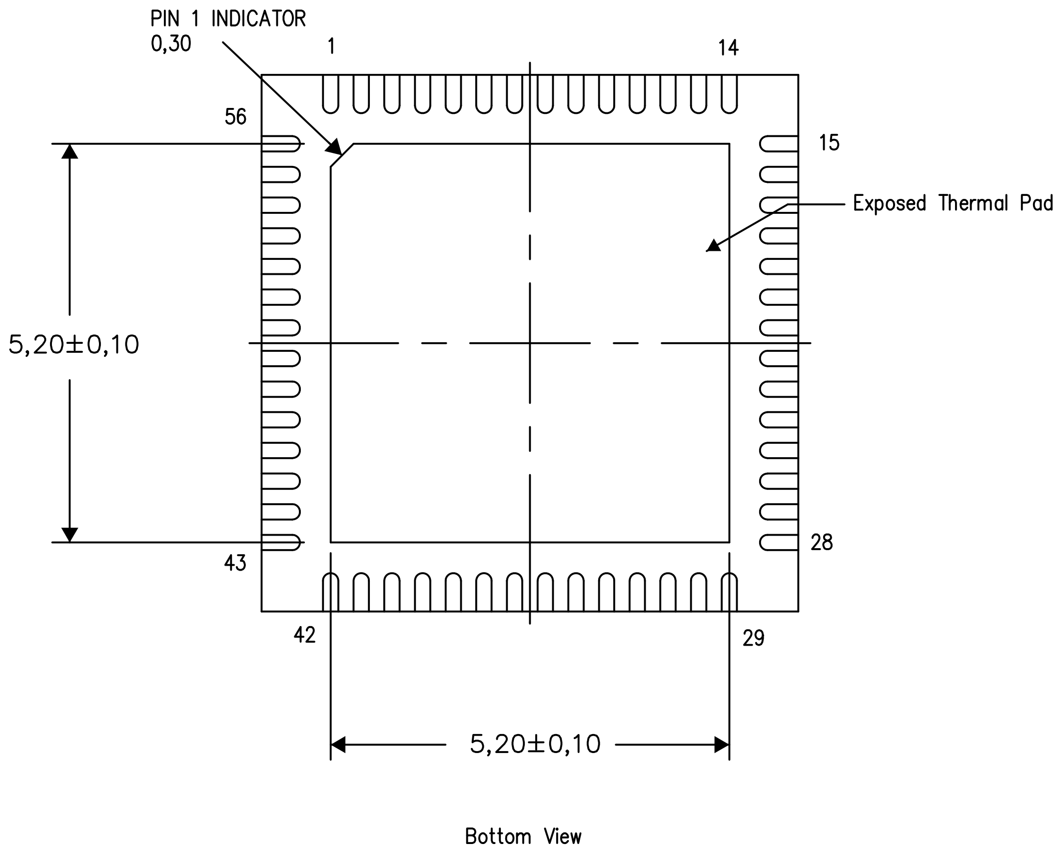
RSH (S-PVQFN-N56) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

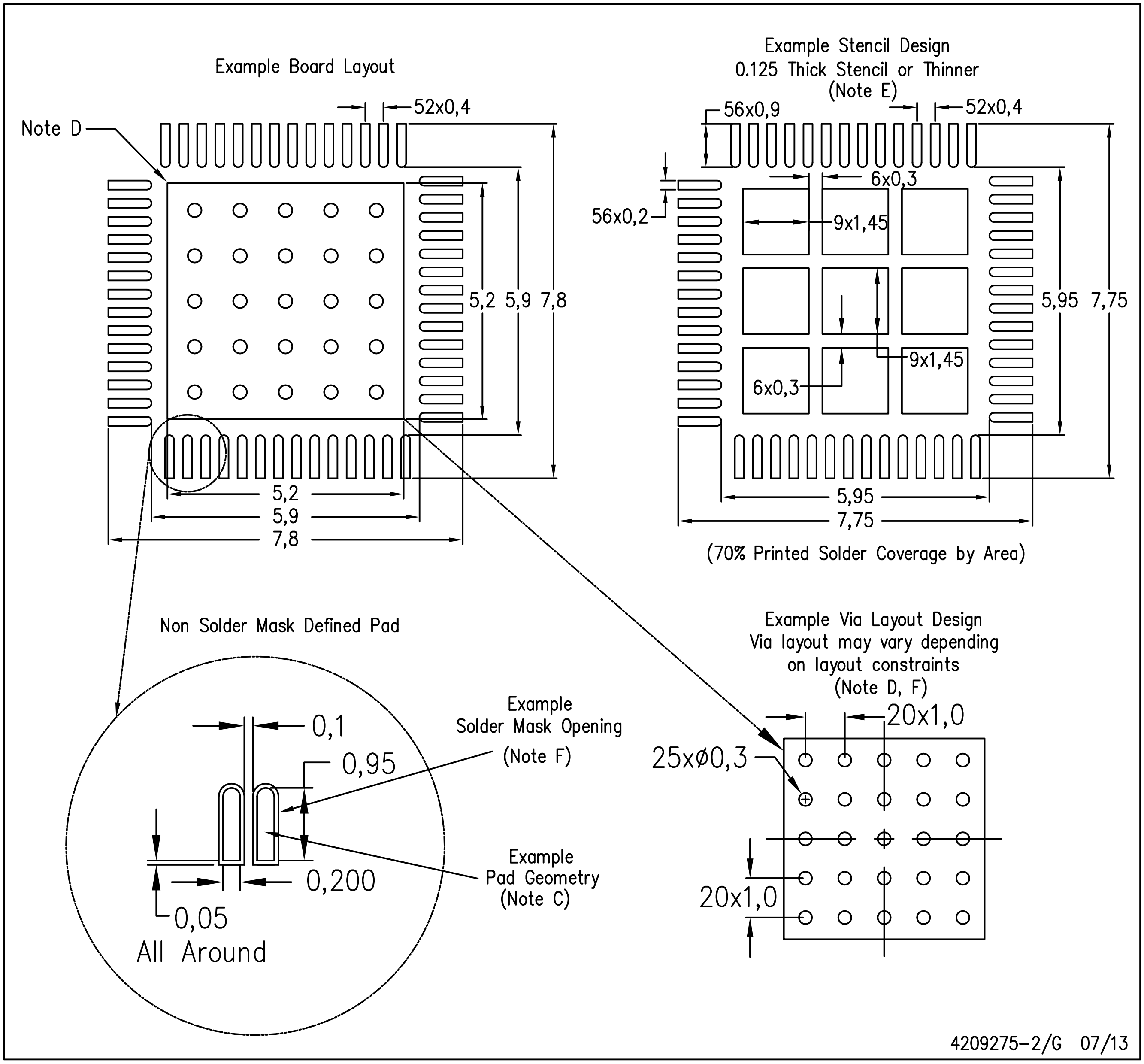


Exposed Thermal Pad Dimensions

4207553-2/I 07/13

NOTE: All linear dimensions are in millimeters

RSH (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.