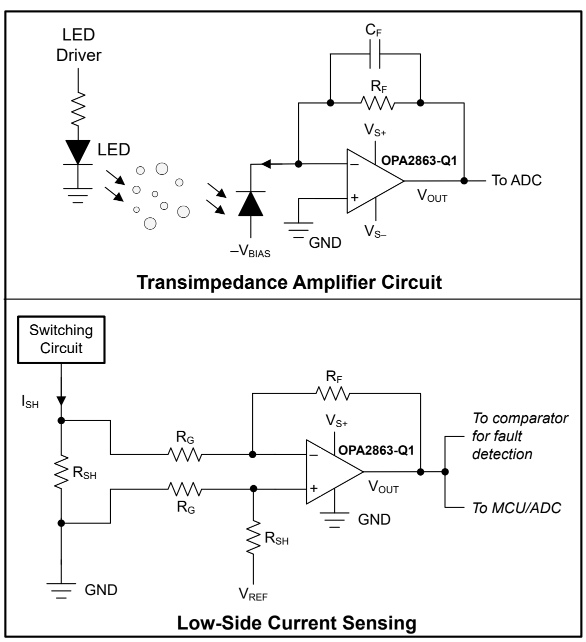
OPA2863-Q1 Automotive, Low-Power, 110-MHz, Rail-to-Rail Input/Output Amplifier

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Wide-bandwidth
  - Unity-gain bandwidth: 110 MHz
  - Gain-bandwidth product: 50 MHz
- Low power
  - Quiescent current: 700 µA/ch (typical)
  - Supply voltage: 2.7 V to 12.6 V
- Input voltage noise: 5.9 nV/√Hz
- Slew rate: 105 V/µs
- Rail-to-rail input and output
- HD_2/HD_3: –129 dBc/–138 dBc at 20 kHz (2 V_{PP})
- Additional features:
  - Overload power limit
  - Output short-circuit protection

2 Applications

- Low-side current sensing
- DC/DC converters
- Inverter and motor control
- Onboard and wireless chargers
- HVAC compressors
- Photodiode TIA interface
- Head-up display (HUD)



Application Circuits Using the OPA2863-Q1

3 Description

The OPA2863-Q1 is a low-power, unity-gain stable, rail-to-rail input and output, voltage-feedback operational amplifier designed to operate over a power-supply range of 2.7 V to 12.6 V. Consuming only 700 µA per channel, the OPA2863-Q1 offers a gain-bandwidth product of 50 MHz, slew rate of 105 V/µs with a voltage noise density of 5.9 nV/√Hz.

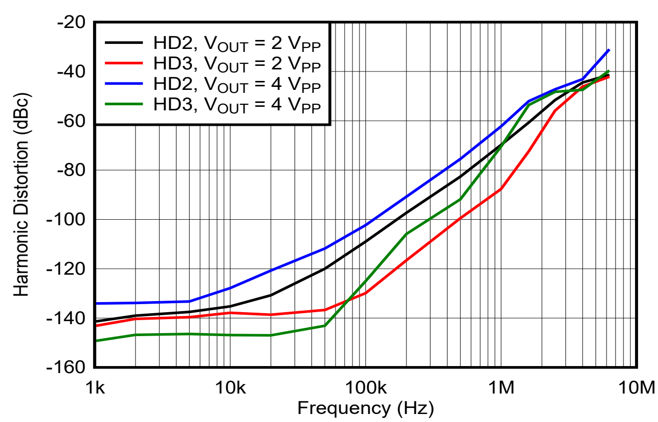
The rail-to-rail input stage makes OPA2863-Q1 an excellent choice for general-purpose applications like current sensing and photodiode interface. The rail-to-rail input stage is well-matched for gain-bandwidth product and noise across the full input common-mode voltage range, enabling excellent performance with wide-input dynamic range.

The OPA2863-Q1 includes overload power limiting to limit the increase in I_Q with saturated outputs, thereby preventing excessive power dissipation in power-conscious, battery-operated systems. The output stage is short-circuit protected, making these devices conducive to ruggedized environments.

Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)
OPA2863-Q1	D (SOIC, 8)	4.9 mm × 6 mm

(1) For related products, see the *Device Comparison Table*.
(2) For all available packages, see the orderable addendum at the end of the data sheet.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Distortion Performance at G = 1 V/V

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2023) to Revision A (July 2023)	Page
• Changed data sheet status from advanced information (preview) to production data (active)........	1

5 Device Comparison Table

DEVICE	±V_S (V)	I_Q/CHANNEL (mA)	GBWP (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPA2863-Q1	±6.3	0.70	50	105	5.9	Unity-gain-stable. RRIO bipolar amplifier
OPA2365-Q1	±2.75	4.6	50	25	4.5	Unity-gain-stable, zero-crossover, RRIO CMOS amplifier
OPA2607-Q1	±2.75	0.9	50	24	3.8	Gain of 6 V/V stable, NRI/RRO CMOS amplifier
OPA2836-Q1	±2.75	1	110	560	4.6	Unity-gain stable, low-power, NRI/RRO bipolar amplifier

6 Pin Configuration and Functions

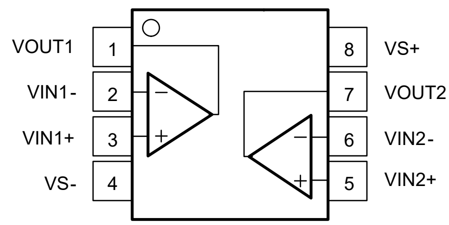


Figure 6-1. D Package, 8-Pin SOIC (Top View)

Table 6-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
VIN1–	2	I	Amplifier 1 inverting input pin
VIN1+	3	I	Amplifier 1 noninverting input pin
VIN2–	6	I	Amplifier 2 inverting input pin
VIN2+	5	I	Amplifier 2 noninverting input pin
VOUT1	1	O	Amplifier 1 output pin
VOUT2	7	O	Amplifier 2 output pin
VS–	4	P	Negative power-supply pin
VS+	8	P	Positive power-supply pin

(1) I = input, O = output, and P = power.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{S-} to V_{S+}	Supply voltage		13	V
	Supply turn-on/off maximum dV/dt		1	V/µs
V_I	Input voltage	V_{S-} – 0.5	V_{S+} + 0.5	V
V_{ID}	Differential input voltage		±1	V
I_I	Continuous input current[2]		±10	mA
I_O	Continuous output current[3]		±30	mA
	Continuous power dissipation	See *Thermal Information*		
T_J	Junction temperature		150	°C
T_A	Operating ambient temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Continuous input current limit for both the ESD diodes to the supply pins and amplifier differential input clamp diode. The differential input clamp diodes limit the voltage between the two inputs to 1 V with this continuous input current flowing through these diodes.
(3) Long-term continuous current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1] HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{S+} – V_{S-}$	Total supply voltage	2.7	10	12.6	V
T_A	Ambient temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		OPA2863-Q1	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	62.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics: V_S = ±5 V

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output common-mode is at mid-supply, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1		110		MHz
GBWP	Gain-bandwidth product			50		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		17		MHz
	Bandwidth for 0.1-dB flatness	V_{OUT} = 20 mV_{PP}		15		MHz
SR	Slew rate	V_{OUT} = 2-V step, G = –1		105		V/µs
	Rise, fall time	V_{OUT} = 200-mV step		9		ns
	Settling time	To 0.1%, V_{OUT} = 2-V step		57		ns
		To 0.01%, V_{OUT} = 2-V step		70		
	Overshoot/undershoot	V_{OUT} = 2-V step		1		%
	Overdrive recovery time	G = –1, 0.5-V overdrive beyond supplies		70		ns
		G = 1, 0.5-V overdrive beyond supplies		100		
HD2	Second-order harmonic distortion	f = 20 kHz, V_{OUT} = 2 V_{PP}		–129		dBc
HD3	Third-order harmonic distortion	f = 20 kHz, V_{OUT} = 2 V_{PP}		–138		dBc
HD2	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP}		–107		dBc
HD3	Third-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP}		–125		dBc
e_N	Input voltage noise	1/f corner at 25 Hz		5.9		nV/√Hz
i_N	Input current noise	1/f corner at 2 kHz		0.4		pA/√Hz
	Closed-loop output impedance	f = 1 MHz		0.2		Ω
	Channel-to-channel crosstalk	f = 1 MHz, V_{OUT} = 2 V_{PP}		–124		dBc
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = ±2.5 V	110	128		dB
V_{OS}	Input-referred offset voltage		–1.5	±0.4	1.5	mV
	Input offset voltage drift	T_A = –40°C to +125°C	–4	±1	4	µV/°C
	Input bias current	T_A ≅ 25°C		0.3	0.73	µA
		T_A = –40°C to +85°C			1.2	
		T_A = –40°C to +125°C			1.6	
	Input bias current drift	T_A = –40°C to +125°C		±3	7.6	nA/°C
	Input offset current		–30	±10	30	nA
INPUT						
	Input common-mode voltage		V_{S-}–0.2		V_{S+}+0.2	V
CMRR	Common-mode rejection ratio	V_{CM} = V_{S-} – 0.2 V to V_{S+} – 1.6 V	100	120		dB
	Input impedance common-mode			650 || 0.8		MΩ || pF
	Input impedance differential mode			200 || 0.5		kΩ || pF
OUTPUT						
V_{OL}	Output voltage, low	T_A ≅ 25°C		V_{S-}+0.14	V_{S-}+0.2	V
		T_A = –40°C to +125°C		V_{S-}+0.15	V_{S-}+0.22	
V_{OH}	Output voltage, high	T_A ≅ 25°C	V_{S+}–0.2	V_{S+}–0.14		V
		T_A = –40°C to +125°C	V_{S+}–0.2	V_{S+}–0.15		
	Linear output drive (sourcing and sinking)	V_{OUT} = ±2.5 V, ΔV_{OS} < 1 mV(1)	25	30		mA
	Short-circuit current			45		mA

7.5 Electrical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output common-mode is at mid-supply, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current per amplifier	T_A ≅ 25°C		700	970	µA
		T_A = –40°C to +125°C			1280	
PSRR	Power-supply rejection ratio	ΔV_S = ±2 V(2)	100	120		dB
AUXILIARY INPUT STAGE						
	Gain-bandwidth product			50		MHz
	Input voltage noise	1/f corner at 25 Hz		6		nV/√Hz
	Input current noise	1/f corner at 100 Hz		0.4		pA/√Hz
	Input-referred offset voltage		–1.5	±0.15	1.5	mV
	Input bias current	T_A ≅ 25°C		0.2	0.6	µA
		T_A = –40°C to +125°C			1.3	
	Common-mode rejection ratio	V_{CM} = 4.1 V to 5.2 V	100	120		dB
	Power supply rejection ratio	ΔV_S = ±0.6 V	100	120		dB

(1) Change in input offset voltage from no-load condition.
(2) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.

7.6 Electrical Characteristics: V_S = 3 V

at G = 1 V/V, R_F = 0 Ω for G =1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1		97		MHz
GBWP	Gain-bandwidth product			50		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}		26		MHz
	Bandwidth for 0.1-dB flatness	V_{OUT} = 20 mV_{PP}		10		MHz
SR	Slew rate	V_{OUT} = 1-V step, G = –1		105		V/µs
	Rise, fall time	V_{OUT} = 200-mV step		10		ns
	Settling time	To 0.1%, V_{OUT} = 1-V step		58		ns
		To 0.01%, V_{OUT} = 1-V step		90		
	Overshoot	V_{OUT} = 1-V step		2		%
	Undershoot	V_{OUT} = 1-V step		16		%
	Overdrive recovery time	G = –1, 0.5-V overdrive beyond supplies		95		ns
		G = 1, 0.5-V overdrive beyond supplies		100		
HD2	Second-order harmonic distortion	f = 20 kHz, V_{OUT} = 1 V_{PP}		–123		dBc
HD3	Third-order harmonic distortion	f = 20 kHz, V_{OUT} = 1 V_{PP}		–132		dBc
HD2	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 1 V_{PP}		–109		dBc
HD3	Third-order harmonic distortion	f = 100 kHz, V_{OUT} = 1 V_{PP}		–129		dBc
e_N	Input voltage noise	1/f corner at 25 Hz		6		nV/√Hz
i_N	Input current noise	1/f corner at 2 kHz		0.4		pA/√Hz
	Closed-loop output impedance	f = 1 MHz		0.2		Ω
	Channel-to-channel crosstalk	f = 1 MHz, V_{OUT} = 1 V_{PP}		–127		dBc

7.6 Electrical Characteristics: V_S = 3 V (continued)

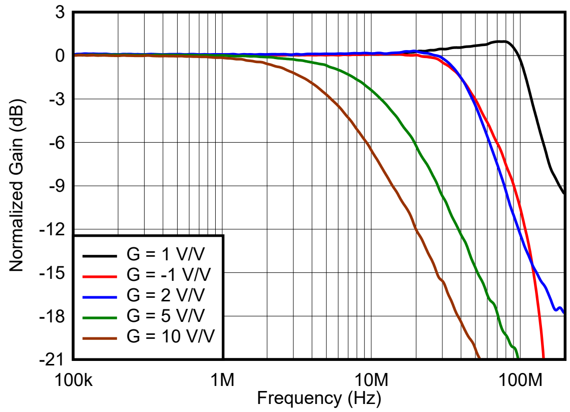
at G = 1 V/V, R_F = 0 Ω for G =1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = 1 V to 2 V	104	123		dB
V_{OS}	Input-referred offset voltage		–1.5	±0.4	1.5	mV
	Input offset voltage drift	T_A = –40°C to +125°C	–4	±1	4	µV/°C
	Input bias current	T_A ≅ 25°C		0.3	0.73	µA
		T_A = –40°C to +85°C			1.2	
		T_A = –40°C to +125°C			1.6	
	Input bias current drift	T_A = –40°C to +125°C		±3	7.4	nA/°C
	Input offset current		–30	±10	30	nA
INPUT						
	Input common-mode voltage		$V_{S–}$–0.2		V_{S+}+0.2	V
CMRR	Common-mode rejection ratio	V_{CM} = $V_{S–}$ – 0.2 V to V_{S+} – 1.6 V	94	115		dB
	Input impedance common-mode			360 || 0.9		MΩ || pF
	Input impedance differential mode			200 || 0.5		kΩ || pF
OUTPUT						
V_{OL}	Output voltage, low	T_A ≅ 25°C		$V_{S–}$+ 0.13	$V_{S–}$+ 0.15	V
		T_A = –40°C to +125°C		$V_{S–}$+ 0.13	$V_{S–}$+ 0.16	
V_{OH}	Output voltage, high	T_A ≅ 25°C	V_{S+}–0.15	V_{S+}–0.13		V
		T_A = –40°C to +125°C	V_{S+}–0.15	V_{S+}–0.13		
	Linear output drive (sourcing and sinking)	V_{OUT} = ±0.7 V, ΔV_{OS} < 1 mV(1)	23	33		mA
	Short-circuit current			45		mA
POWER SUPPLY						
I_Q	Quiescent current per amplifier	T_A ≅ 25°C		690	910	µA
		T_A = –40°C to +125°C			1180	
PSRR	Power-supply rejection ratio	ΔV_S = ±1 V(2)	100	120		dB
AUXILIARY INPUT STAGE						
	Gain-bandwidth product			50		MHz
	Input voltage noise	1/f corner at 25 Hz		6		nV/√Hz
	Input current noise	1/f corner at 100 Hz		0.4		pA/√Hz
	Input-referred offset voltage		–1.5	±0.15	1.5	mV
	Input bias current	T_A ≅ 25°C		0.2	0.6	µA
		T_A = –40°C to +125°C			1.2	
	Common-mode rejection ratio	V_{CM} = 2.1 V to 3.2 V	100	120		dB
	Power supply rejection ratio	ΔV_S = ±0.6 V	100	115		dB

(1) Change in input offset voltage from no-load condition.
(2) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.

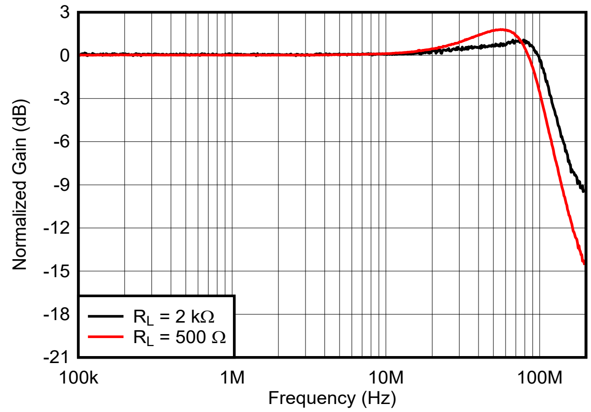
7.7 Typical Characteristics: V_S = ±5 V

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



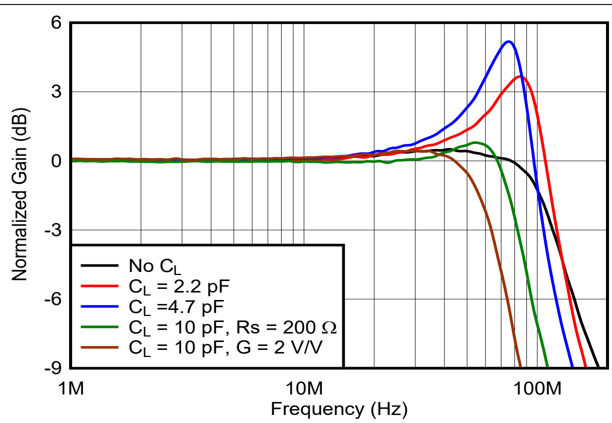
V_{OUT} = 20 mV_{PP}

Figure 7-1. Small-Signal Frequency Response vs Gain



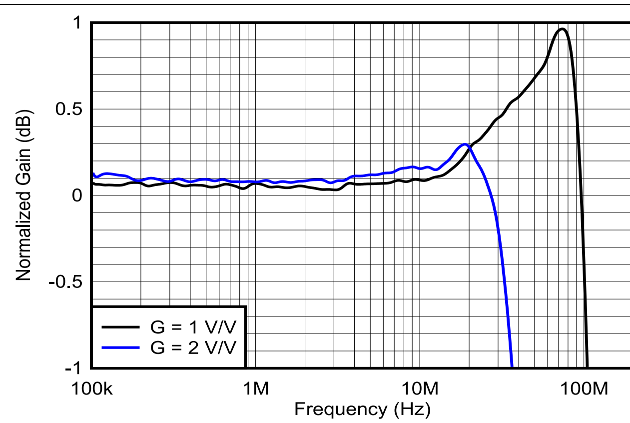
V_{OUT} = 20 mV_{PP}

Figure 7-2. Small-Signal Frequency Response vs Output Load



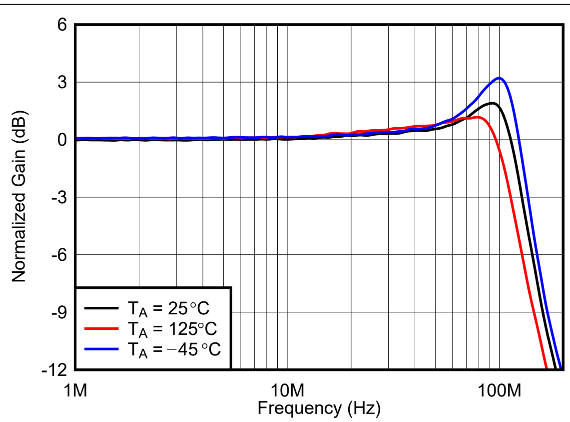
V_{OUT} = 20 mV_{PP}

Figure 7-3. Frequency Response vs Load Capacitance



V_{OUT} = 20 mV_{PP}

Figure 7-4. Small-Signal Response Flatness vs Gain



V_{OUT} = 20 mV_{PP}

Figure 7-5. Frequency Response vs Ambient Temperature

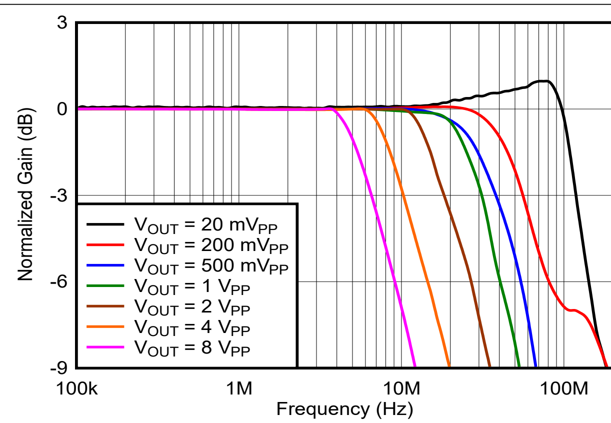
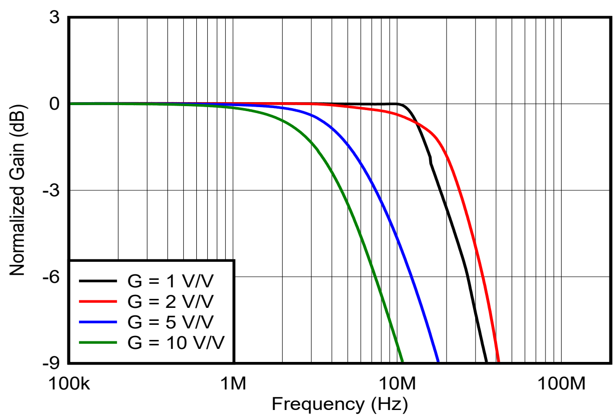


Figure 7-6. Frequency Response vs Output Voltage

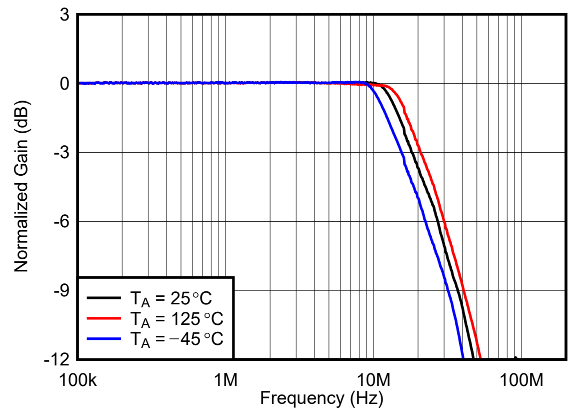
7.7 Typical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



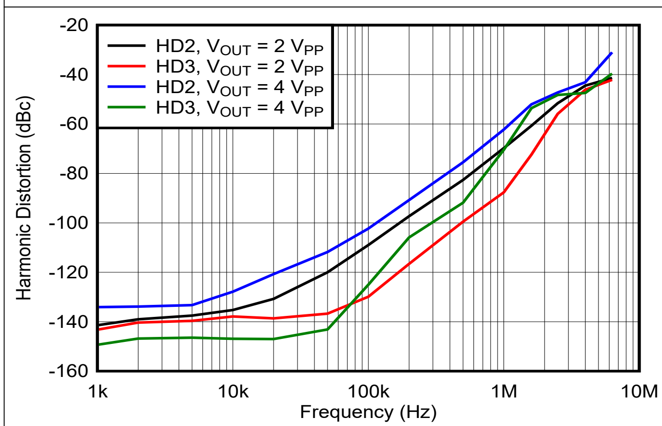
V_{OUT} = 2 V_{PP}

Figure 7-7. Large-Signal Frequency Response vs Gain



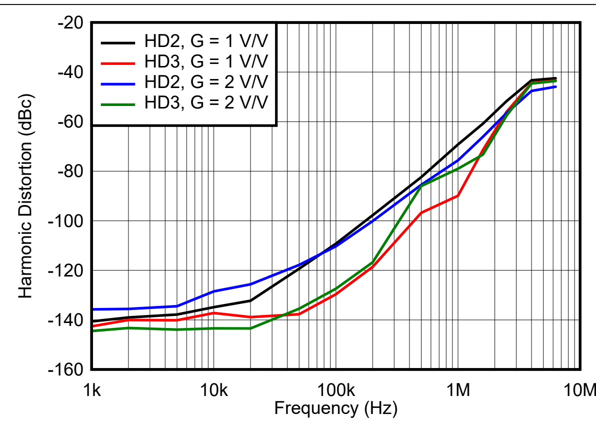
V_{OUT} = 2 V_{PP}

Figure 7-8. Frequency Response vs Ambient Temperature



G = 1 V/V

Figure 7-9. Harmonic Distortion vs Frequency



V_{OUT} = 2 V_{PP}

Figure 7-10. Harmonic Distortion vs Gain

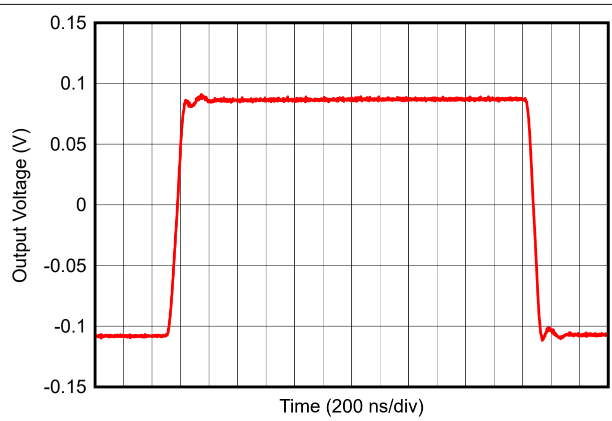


Figure 7-11. Small-Signal Transient Response

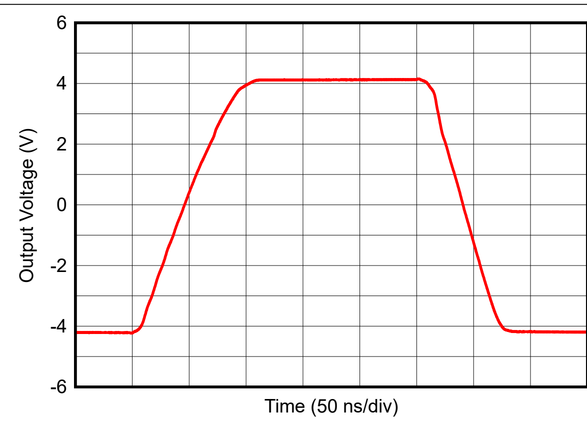
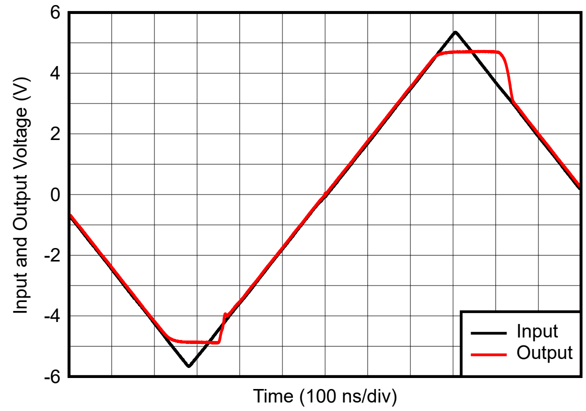


Figure 7-12. Large-Signal Transient Response

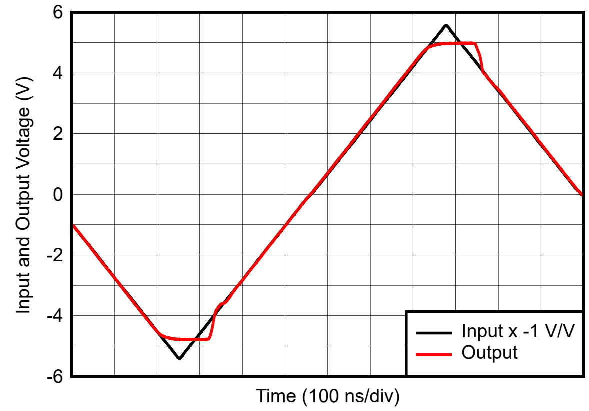
7.7 Typical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



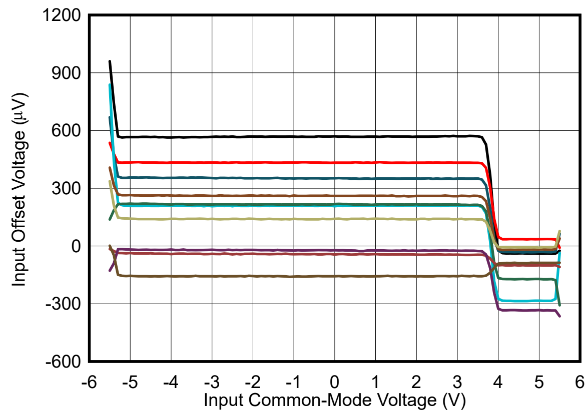
G = 1 V/V

Figure 7-13. Input Overdrive Recovery



G = –1 V/V

Figure 7-14. Output Overdrive Recovery



Measured for 10 units

Figure 7-15. Input Offset Voltage vs Input Common-Mode Voltage

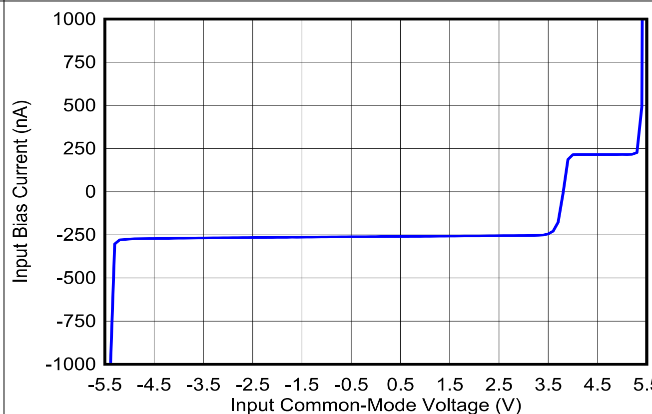


Figure 7-16. Input Bias Current vs Input Common-Mode Voltage

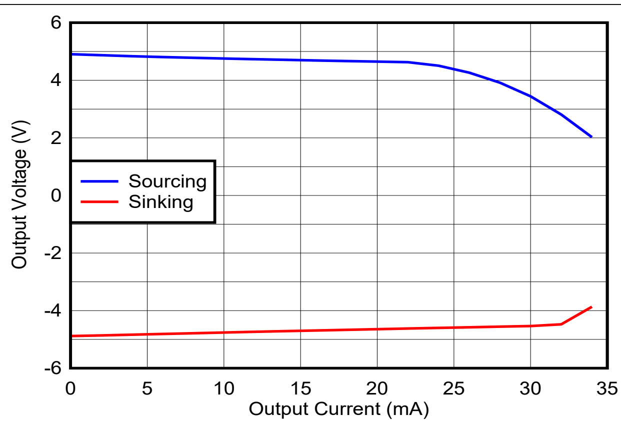
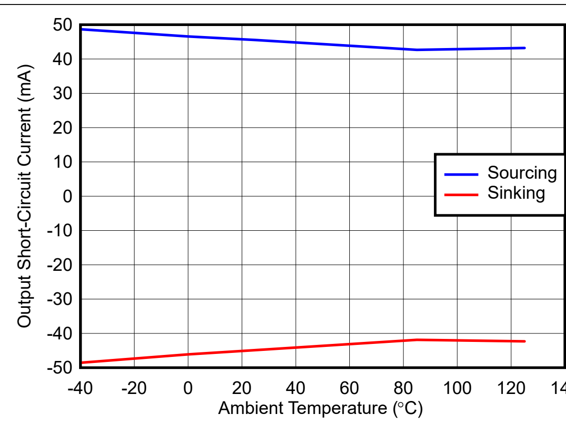


Figure 7-17. Output Voltage vs Load Current

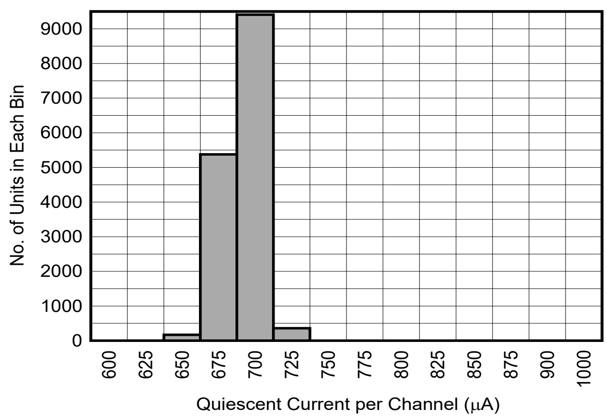


Output saturated and then short-circuited to opposite supply

Figure 7-18. Output Short-Circuit Current vs Ambient Temperature

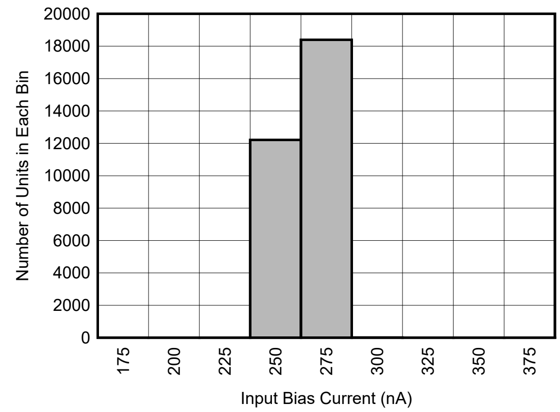
7.7 Typical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



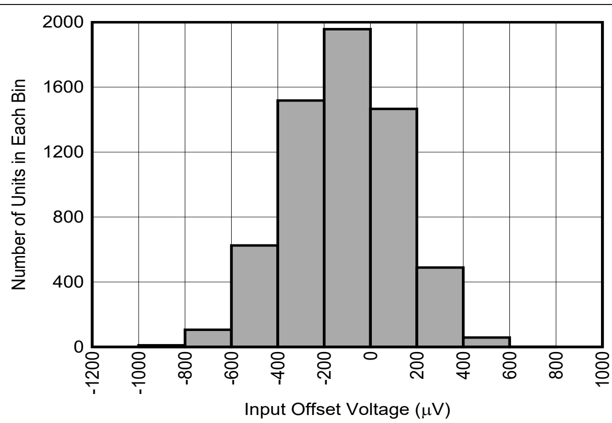
μ = 678 μA, σ = 13 μA

Figure 7-19. Quiescent Current Distribution



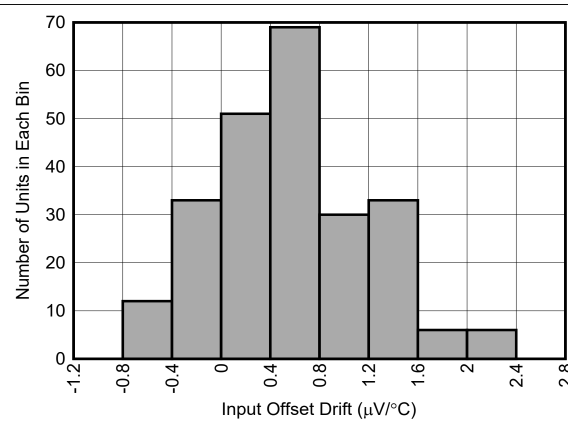
μ = 251 nA, σ = 5.6 nA

Figure 7-20. Input Bias Current Distribution



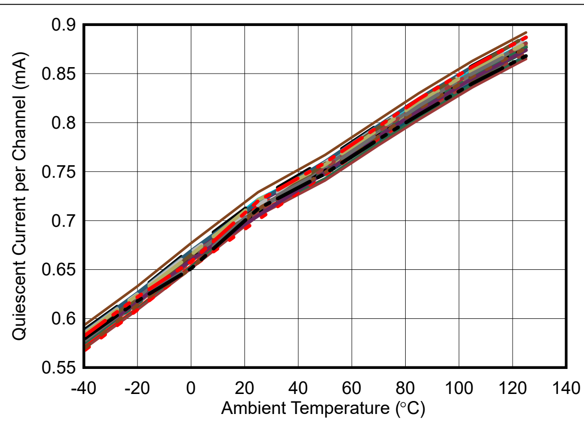
μ = –116 μV, σ = 234 μV

Figure 7-21. Input Offset Voltage Distribution



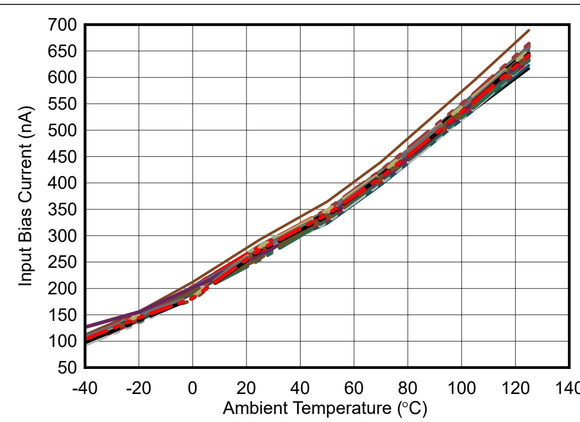
μ = 0.57 μV/°C, σ = 0.64 μV/°C

Figure 7-22. Input Offset Voltage Drift Distribution



35 units

Figure 7-23. Quiescent Current vs Ambient Temperature

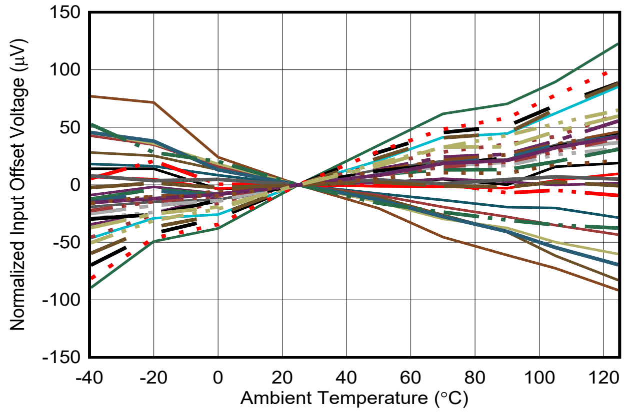


35 units

Figure 7-24. Input Bias Current vs Ambient Temperature

7.7 Typical Characteristics: V_S = ±5 V (continued)

at G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)

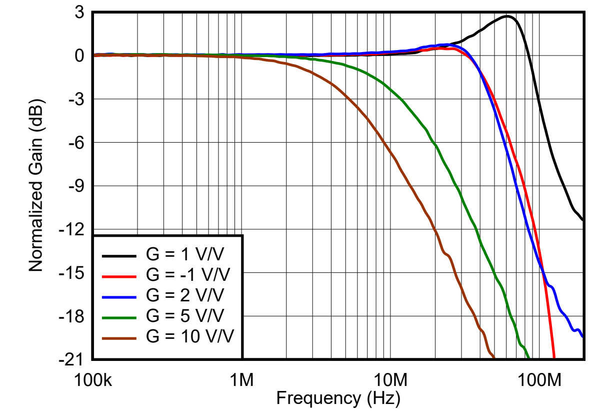


Normalized to 25°C values, 32 units

Figure 7-25. Input Offset Voltage vs Ambient Temperature

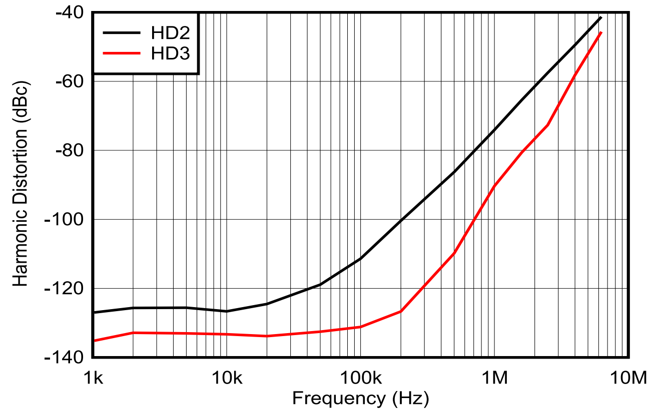
7.8 Typical Characteristics: V_S = 3 V

at V_{S+} = 3 V, $V_{S–}$ = 0 V, G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)



V_{OUT} = 20 mV_{PP}

Figure 7-26. Small-Signal Frequency Response vs Gain



V_{OUT} = 1 V_{PP}

Figure 7-27. Harmonic Distortion vs Frequency

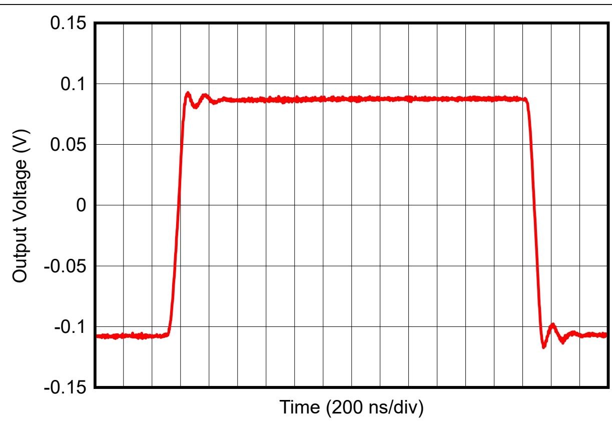


Figure 7-28. Small-Signal Transient Response

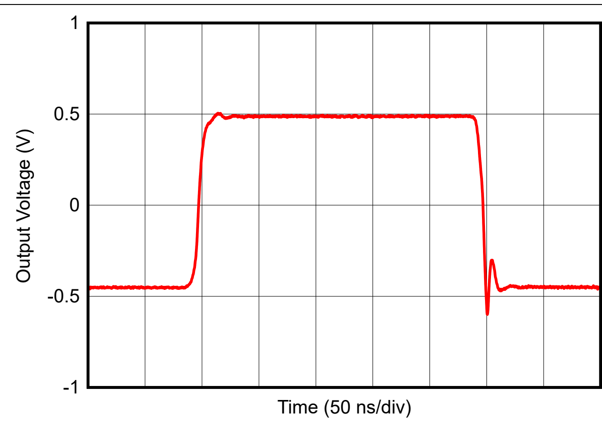
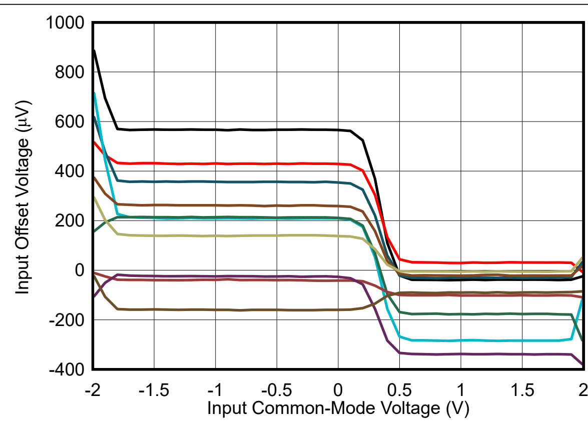


Figure 7-29. Large-Signal Transient Response



Measured for 10 units

Figure 7-30. Input Offset Voltage vs Input Common-Mode Voltage

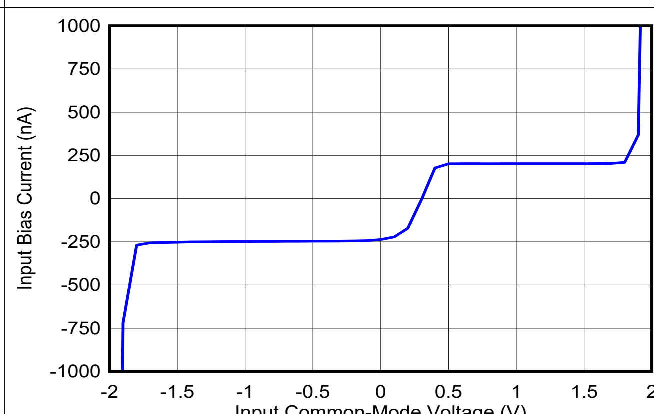


Figure 7-31. Input Bias Current vs Input Common-Mode Voltage

7.8 Typical Characteristics: V_S = 3 V (continued)

at V_{S+} = 3 V, $V_{S–}$ = 0 V, G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

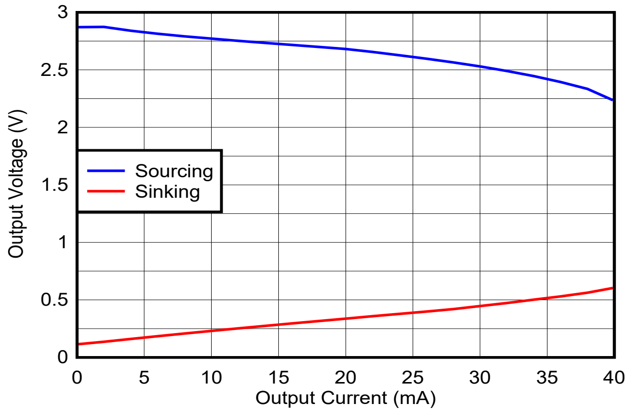
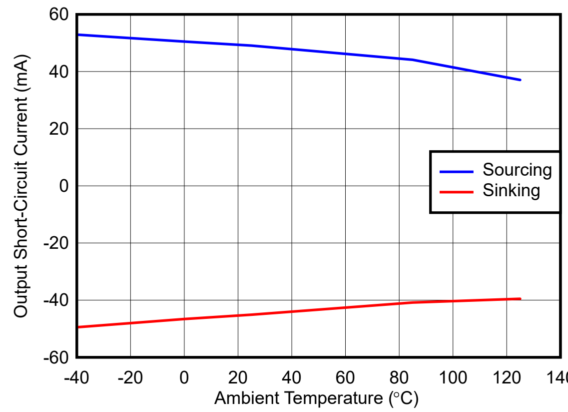


Figure 7-32. Output Voltage vs Load Current

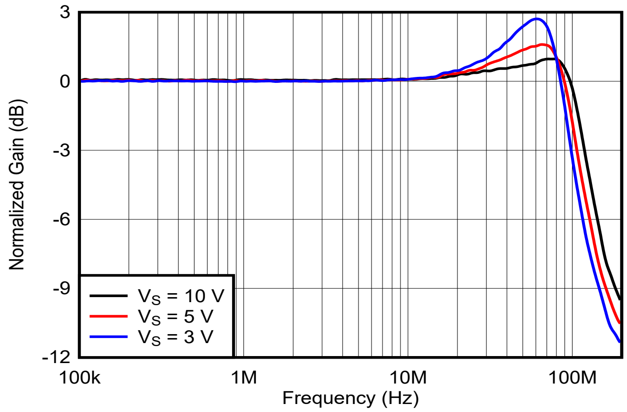


Output saturated and then short-circuited to other supply

Figure 7-33. Output Short-Circuit Current vs Ambient Temperature

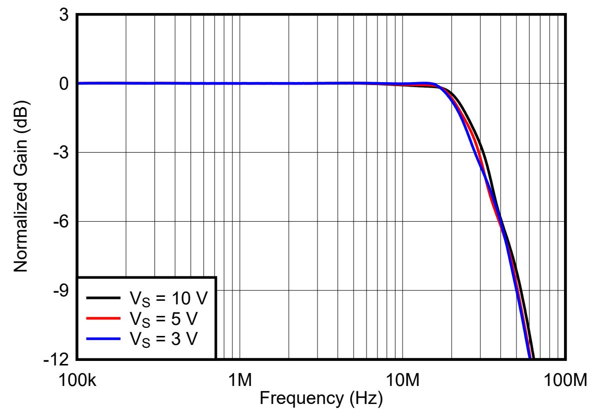
7.9 Typical Characteristics: V_S = 3 V to 10 V

at G = 1 V/V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



V_{OUT} = 20 mV_{PP}

Figure 7-34. Frequency Response vs Supply Voltage



V_{OUT} = 1 V_{PP}

Figure 7-35. Frequency Response vs Supply Voltage

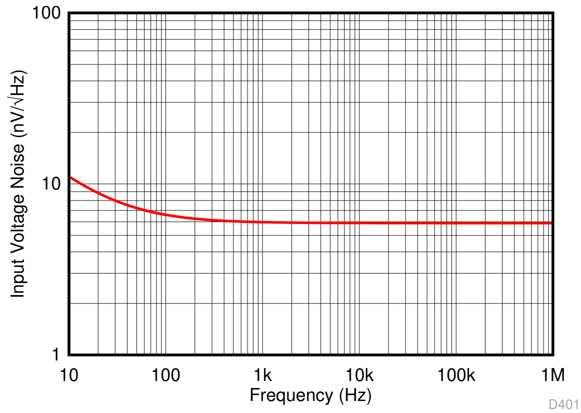


Figure 7-36. Input Voltage Noise Density vs Frequency

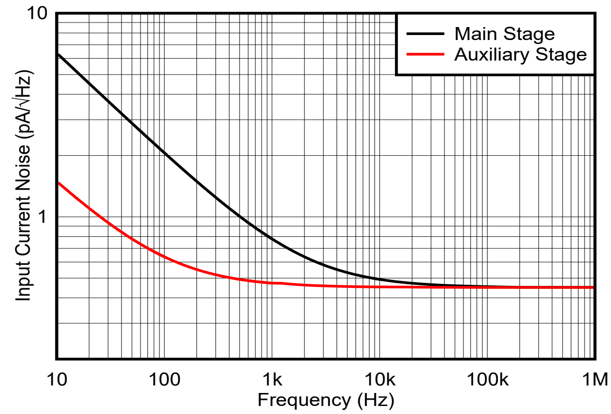


Figure 7-37. Input Current Noise Density vs Frequency

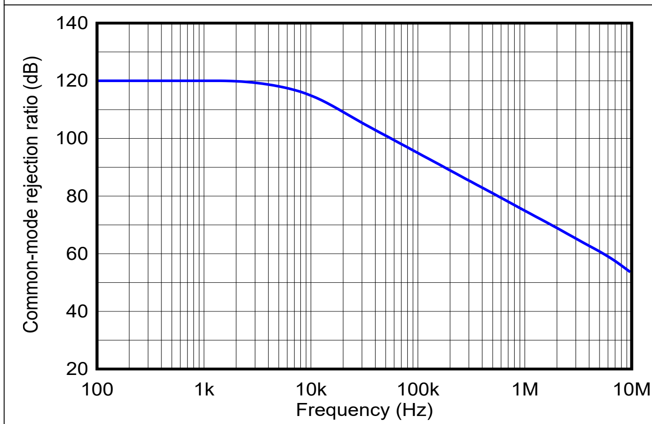


Figure 7-38. Common-Mode Rejection Ratio vs Frequency

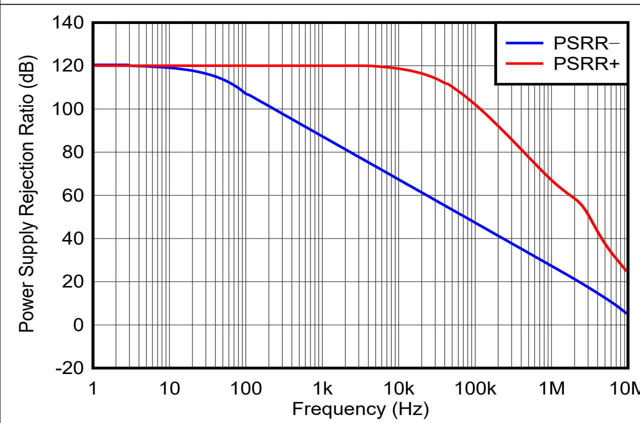


Figure 7-39. Power Supply Rejection Ratio vs Frequency

7.9 Typical Characteristics: V_S = 3 V to 10 V (continued)

at G = 1 V/V, V_{OUT} = 2 V_{PP}, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)

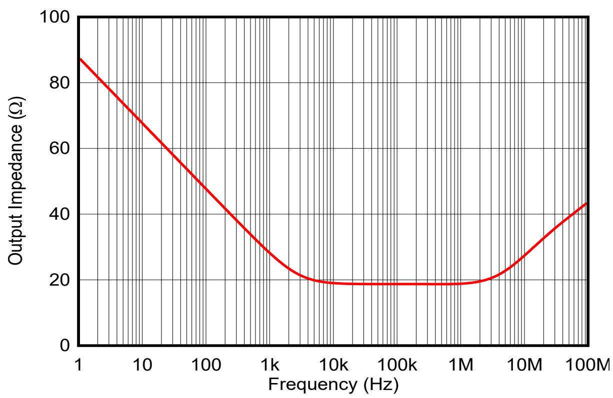
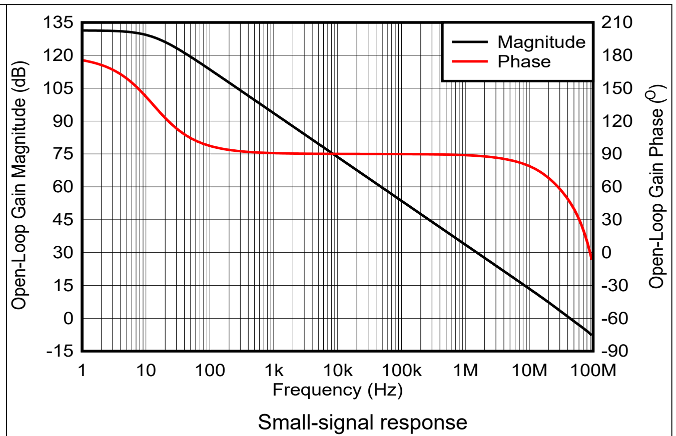
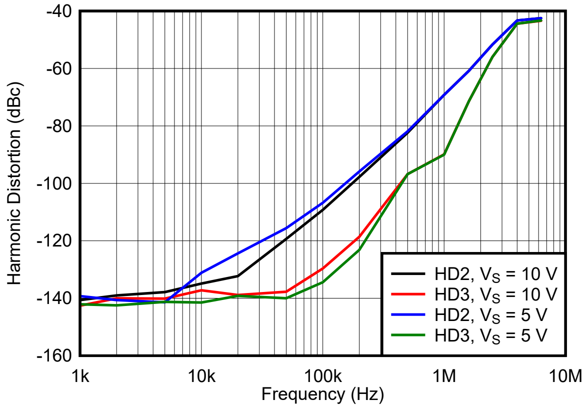


Figure 7-40. Open-Loop Output Impedance vs Frequency



Small-signal response

Figure 7-41. Open-Loop Gain and Phase vs Frequency



V_{OUT} = 2 V_{PP}

Figure 7-42. Harmonic Distortion vs Supply Voltage

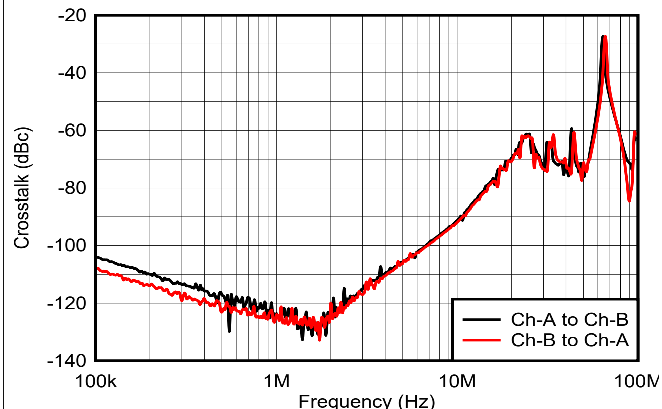


Figure 7-43. Crosstalk vs Frequency

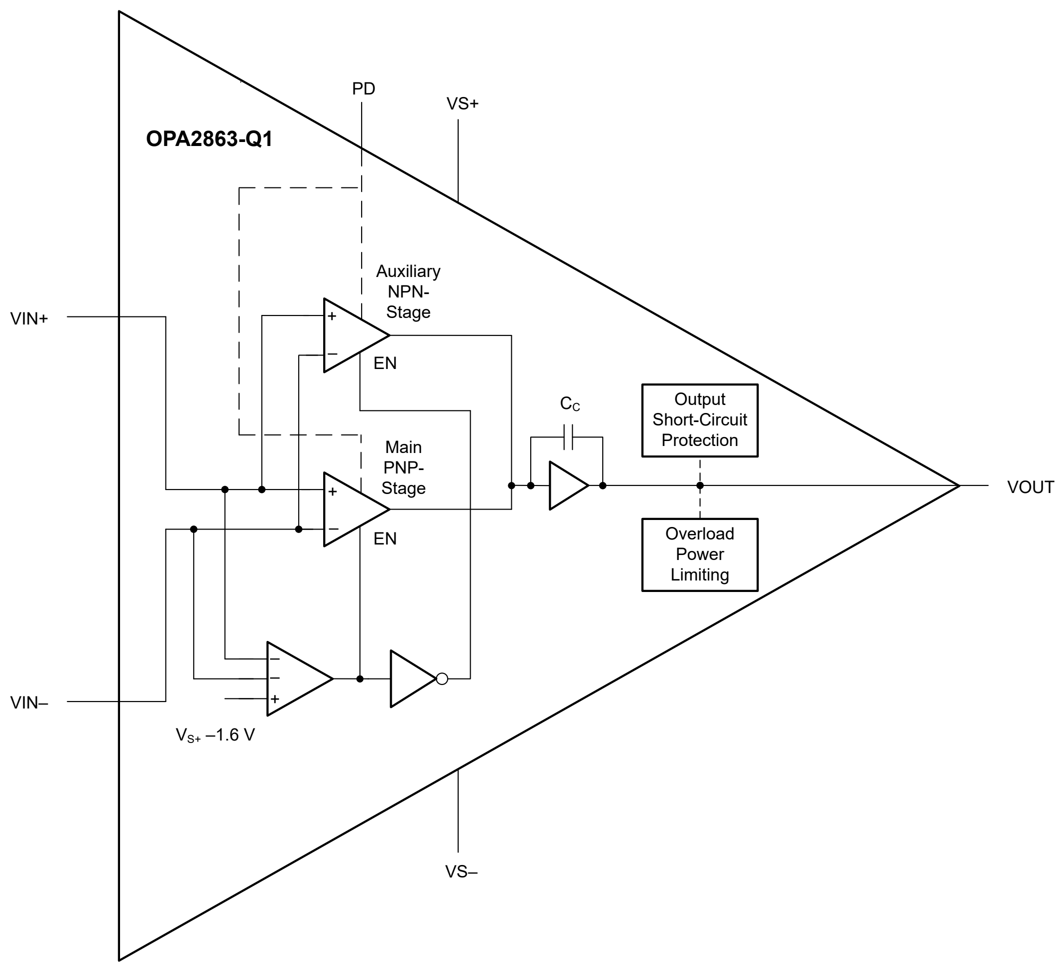
8 Detailed Description

8.1 Overview

The OPA2863-Q1 is a low-power, 50-MHz, rail-to-rail input and output (RRIO), bipolar, voltage-feedback operational amplifier with a voltage noise density of 5.9 nV/√Hz and 1/f noise corner at 25 Hz. The OPA2863-Q1 works with a wide-supply voltage range of 2.7 V to 12.6 V, and consume only 700 µA quiescent current. The OPA2863-Q1 operates with a 2.7 V supply, is RRIO capable, consumes low-power, which makes this a great amplifier for 3.3-V or lower-voltage applications that require excellent ac performance. The main and auxiliary input stages of the amplifier are matched for gain bandwidth product (GBW), noise, and offset voltage and designed for applications that require wide dynamic input range and good SNR.

The device includes an overload power limit feature which limits the increase in quiescent current with over-driven and saturated outputs to either of the supply rails. For more details of this overload power limit feature, see Section 8.3.2.1. The output of the amplifier is protected against short-circuit fault conditions.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Stage

The OPA2863-Q1 includes a rail-to-rail input stage. The main stage differential pair using PNP bipolar transistors operates for common-mode input voltages from V_{S-} – 0.2 V to V_{S+} – 1.6 V. The amplifier inputs transition into the auxiliary stage using NPN transistors for common-mode input voltages from V_{S+} – 1.6 V till V_{S+} + 0.2 V. The PNP and NPN input stages offer a gain-bandwidth product of 50 MHz and a voltage noise density of 5.9 nV/√Hz. The offset voltage for the two input stages is matched to lie within the device specifications. The auxiliary NPN input stage does not use the slew-boost circuit during large-signal transient response. The input bias current for the PNP and NPN input stages is opposite in polarity, which adds an additional offset based on the values of the gain-setting and feedback resistors. A common-mode input voltage transition between these input stages causes a crossover distortion that must be considered in high-frequency applications requiring excellent linearity. Limit the common-mode input voltage to V_{S+} – 1.6 V (maximum) for main-stage operation across process and ambient temperature.

The OPA2863-Q1 is a bipolar amplifier; therefore, the two inputs are protected with antiparallel back-to-back diodes between them, which limits the maximum input differential voltage to 1 V. The amplifier is slew limited, and the two inputs are pulled apart up to 1 V when the antiparallel diodes begin to conduct in very fast input or output transient conditions. Make sure to use gain-setting and feedback resistors large enough to limit the current through these diodes in such conditions.

8.3.2 Output Stage

The OPA2863-Q1 features a rail-to-rail output stage with possible signal swing from V_{S-} + 0.2 V to V_{S+} – 0.2 V. Violating the output headroom to either of the supplies causes output signal clipping and introduces distortion.

The OPA2863-Q1 integrates an output short-circuit protection circuit, which makes the device rugged for use in real-world applications.

8.3.2.1 Overload Power Limit

The OPA2863-Q1 includes overload power limiting that limits the increase in device quiescent current with output saturated to either of the supplies. Typically, when an amplifier output saturates, the two inputs are pulled apart, which can enable the slew-boost circuit. The input differential voltage is an error voltage in negative feedback that the amplifier core nullifies by engaging the slew-boost circuit and driving the output stage deeper into saturation. After the input to an amplifier attains a value large enough to saturate the output, any further increase in this input excitation results in a finite input differential voltage. As the output stage transistor is pushed deeper into saturation, the base-to-collector current gain (h_{FE}) drops with an increase in the base and collector current, and an increase in the device quiescent current. This increase in quiescent current can cause a catastrophic failure in multichannel, high-gain, high-density front-end designs, and reduce operating lifetime in portable, battery-powered systems.

The OPA2863-Q1 overload power limiting includes an intelligent output saturation-detection circuit that limits the device quiescent current to 2.2-mA per channel under dc overload conditions. This increase in quiescent current is smaller with ac input or output and output saturation duration for only a fraction of the overall signal time period. Table 8-1 compares the increase in quiescent current with 50-mV input overdrive for OPA2863-Q1 and other voltage-feedback amplifiers without overload power limit.

Table 8-1. Quiescent Current with Saturated Outputs

DEVICE	INPUT DIFFERENTIAL VOLTAGE	QUIESCENT CURRENT DURING OVERLOAD	INCREASE IN I_Q FROM STEADY-STATE CONDITION
OPA2863-Q1 with overload power limit	50 mV	1.1 mA	1.57 ×
Competitor amplifier without overload power limit	50 mV	1.96 mA	3.43 ×

8.3.3 ESD Protection

Figure 8-1 shows that all device pins are protected with internal ESD protection diodes to the power supplies. These diodes provide moderate protection to input overdrive voltages greater than the supplies. The protection diodes typically support 10-mA continuous input and output currents. Use series current limiting resistors if input voltages exceeding the supply voltages occur at the amplifier inputs, which makes sure that the current through the ESD diodes remains within the rated value. OPA2863-Q1 is a bipolar amplifier; therefore, the two inputs are protected with antiparallel, back-to-back diodes between the inputs that limits the maximum input differential voltage to approximately 1 V. Make sure to use gain-setting and feedback resistors large enough to limit the current through these diodes in fast slewing conditions.

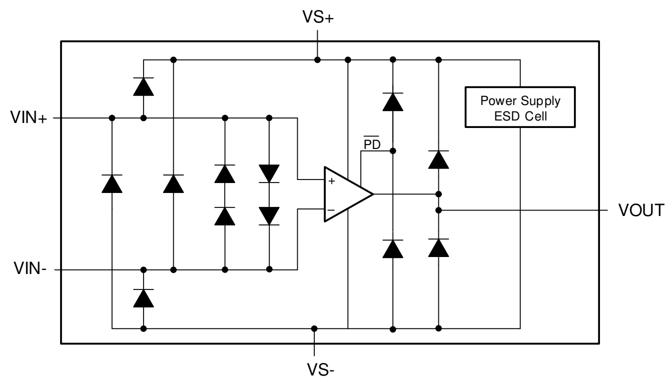


Figure 8-1. Internal ESD Protection

8.4 Device Functional Modes

The OPAx863-Q1 is operational with a supply voltage greater than 2.7 V (±1.35 V). The maximum recommended supply voltage is 12.6 V (±6.3 V). The OPAx863-Q1 can be used with unipolar, bipolar or asymmetric supplies.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The OPA2863-Q1 is a classic voltage-feedback amplifier with two high-impedance inputs and a low-impedance output. This device has a GBW of 50 MHz, 5.9 nV/√Hz of noise, RRIO capability, and precision performance, consuming only 700 µA quiescent current per channel. These features make the OPA2863-Q1 an excellent choice for use in low-side current sensing, ADC input driver, and reference buffering with fast settling, buffers, high gain and filter circuits. The overload power limit makes the OPA2863-Q1 truly low-power in high-gain, multichannel systems, limiting any increase in quiescent current during output overload conditions.

9.2 Typical Applications

9.2.1 Low-Side Current Sensing

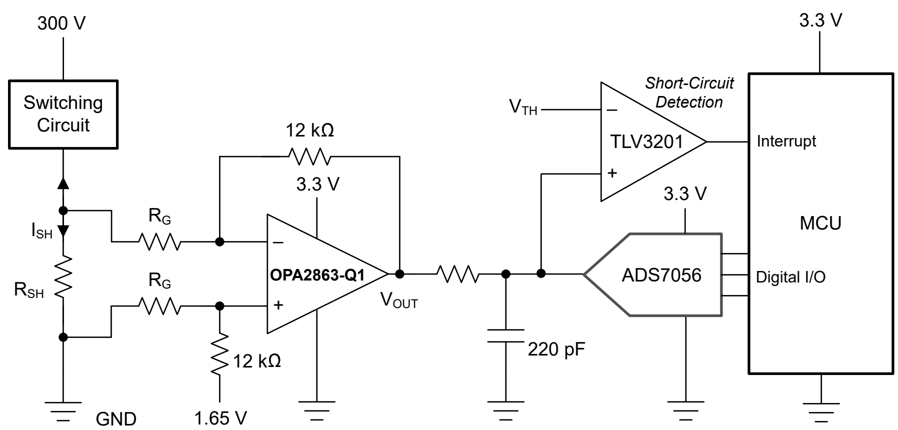


Figure 9-1. Low-Side Current Sensing in Power Converters

Power converters use current-mode feedback control for excellent transient response and multiphase load sharing. Inverter stages control the phase currents for torque control in motor drives. As a result of the simplicity and low-cost, many of these topologies use difference-amplifier-based, low-side current sensing. Figure 9-1 shows the use of the OPA2863-Q1 in a difference amplifier circuit for low-side current sensing.

9.2.1.1 Design Requirements

Table 9-1. Design Requirements

PARAMETER	DESIGN REQUIREMENT
Shunt resistor	10 mΩ
Input current	15 A_{PP}
Output voltage	3 V_{PP}
Switching frequency	50 kHz
Data acquisition	1 MSPS with 0.1% accuracy
Input voltage due to ground bounce	10 Vpk

9.2.1.2 Detailed Design Procedure

In a difference amplifier circuit, the output voltage is given by:

$$V_0 = \frac{R_F}{R_G} I_{SH} R_{SH} + V_{REF} \quad (1)$$

For lowest system noise, small values of R_F and R_G are preferred. The smallest value of R_G is limited by the input transient voltage (10 V here) seen by the circuit, and is given by:

$$R_G = \frac{V_{IN}\,(max) - V_D - V_S}{I_D\,(max)} \quad (2)$$

where

- $V_{IN(maximum)}$ is the maximum input transient voltage seen by the circuit
- V_D is the forward voltage drop of ESD diodes at the amplifier input
- $I_{D(maximum)}$ is the maximum current rating of the ESD diodes at the amplifier input

For a difference amplifier gain of 20 V/V, an R_F of 12 kΩ and R_G of 600 Ω are used. With a clock frequency of 40 MHz and ADS7056 sampling at 1 MSPS, the available acquisition time for amplifier output settling is 550 ns. Table 9-1 shows the simulation results for the circuit in Figure 9-1. The worst-case peak-to-peak input transient condition is simulated. The output of the OPA2863-Q1 settles to within 0.1% accuracy within 543 ns. If using a slower clock frequency with the ADC is desired, then the acquisition time reduces with the same sampling rate, which degrades measurement accuracy. Alternatively, the sampling rate can be reduced to recover the required acquisition time and 0.1% accuracy.

9.2.1.3 Application Curve

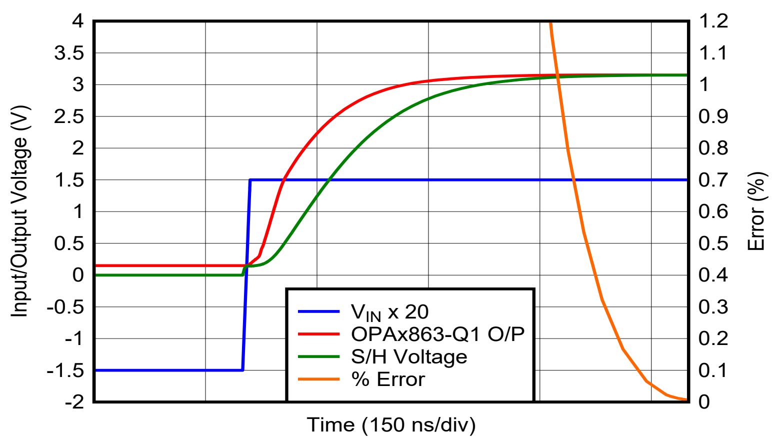


Figure 9-2. 0.1% Settling Performance

9.2.2 Front-End Gain and Filtering

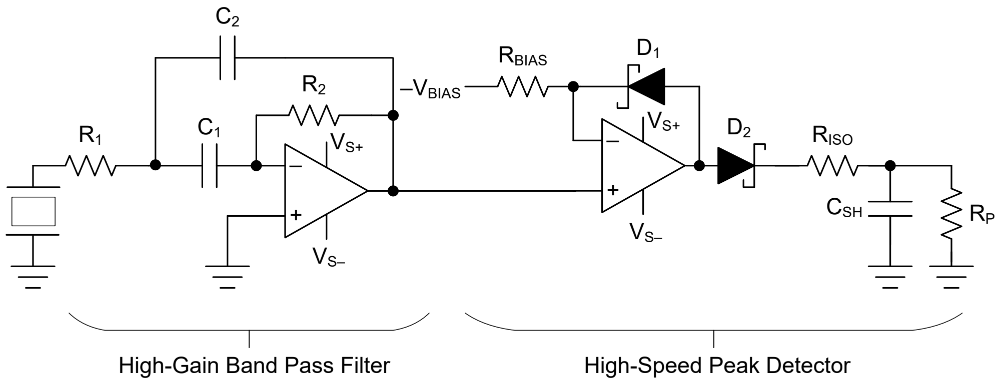


Figure 9-3. High-Gain Narrow Bandpass Filter and Peak Detector Circuit

Ultrasonic signaling is used for proximity and obstacle detection, level sensing, sonars, and so forth. Such signal chains detect the amplitude of received ultrasonic signal at a particular center frequency. Figure 9-3 shows a high-gain narrow bandpass filter and peak detector circuit using the OPA2863-Q1. The signal at the frequency of interest is filtered out, gained, and peak detected to report the amplitude at the output of this circuit. The phase information is lost in this circuit. The OPA2863-Q1 is used with the 50-MHz GBW to add a single-stage gain, and the peak detection capability is easily made with the RRIO capability of these amplifiers.

9.3 Power Supply Recommendations

The OPA2863-Q1 is intended to operate on supplies ranging from 2.7 V to 12.6 V. The OPA2863-Q1 operates on single-sided supplies, split and balanced bipolar supplies, or unbalanced bipolar supplies. Operating from a single supply has numerous advantages. The dc errors, due to the –PSRR term, can be minimized with the negative supply at ground. Typically, ac performance improves slightly at 10-V operation with minimal increase in supply current. Minimize the distance (< 0.1 in) from the power supply pins to high-frequency, 0.01-µF decoupling capacitors. A larger capacitor (2.2 µF typical) is used along with a high-frequency, 0.01-µF supply-decoupling capacitor at the device supply pins. Only the positive supply has these capacitors for single-supply operation. Use these capacitors from each supply to ground when a split-supply is used. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). An optional supply decoupling capacitor across the two power supplies (for split-supply operation) reduces second harmonic distortion.

9.4 Layout

9.4.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier (like the OPA2863-Q1) requires careful attention to board layout parasitics and external component types. The *DEM-OPA-SO-2A Demonstration Fixture user's guide* can be used as a reference when designing the circuit board. Recommendations that optimize performance include the following:

1. **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability—on the noninverting input, parasitic capacitance can react with the source impedance to cause unintentional band-limiting. Open a window around the signal I/O pins in all of the ground and power planes around those pins to reduce unwanted capacitance. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. **Minimize the distance** (< 0.1 in) from the power-supply pins to high-frequency 0.01-μF decoupling capacitors. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-μF to 6.8-μF) decoupling capacitors, effective at lower frequency, must also be used on the supply pins. These capacitors can be placed somewhat farther from the device and shared among several devices in the same area of the PCB.
3. **Careful selection and placement of external components preserves the high-frequency performance of the OPA2863-Q1.** Resistors must be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Keep resistor values as low as possible and consistent with load-driving considerations. Lowering the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. Lower resistor values, however, increase the dynamic power consumption because R_F and R_G become part of the amplifier output load network.

9.4.2 Layout Example

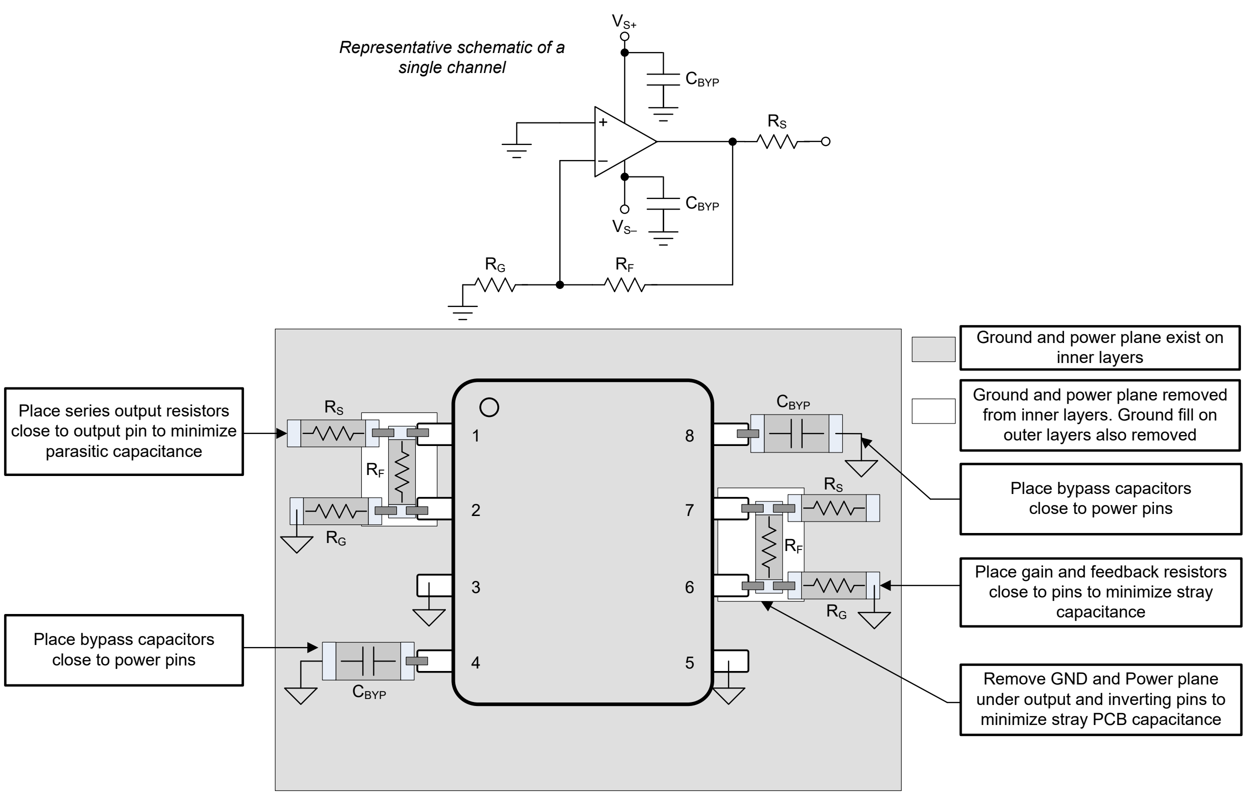


Figure 9-4. Layout Recommendation for Dual-Channel D Package

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *DEM-OPA-SO-2A Demonstration Fixture* user's guide
- Texas Instruments, *Single-Supply Op Amp Design Techniques* application report

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2863QDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2863Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2863-Q1 :

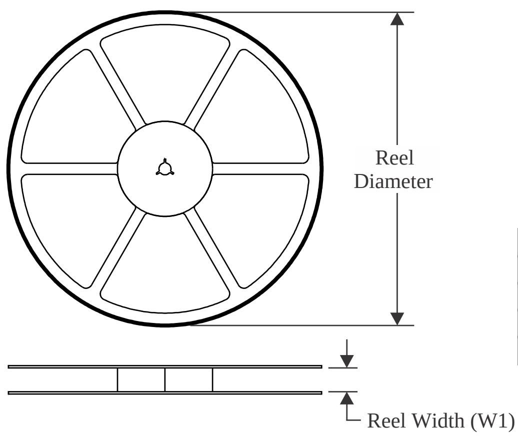
- Catalog : OPA2863

NOTE: Qualified Version Definitions:

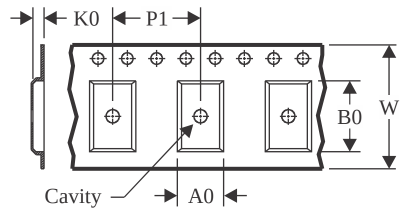
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

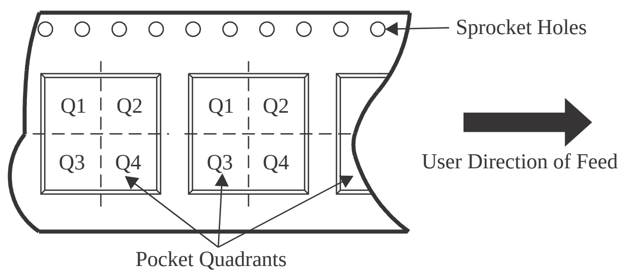


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

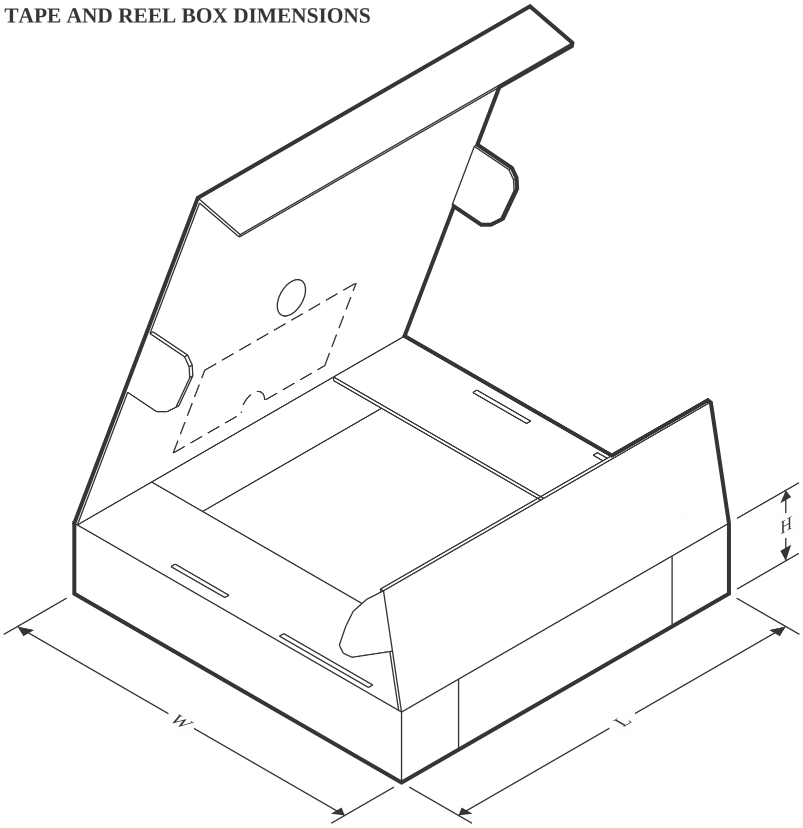
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

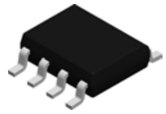
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2863QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2863QDRQ1	SOIC	D	8	3000	367.0	367.0	35.0

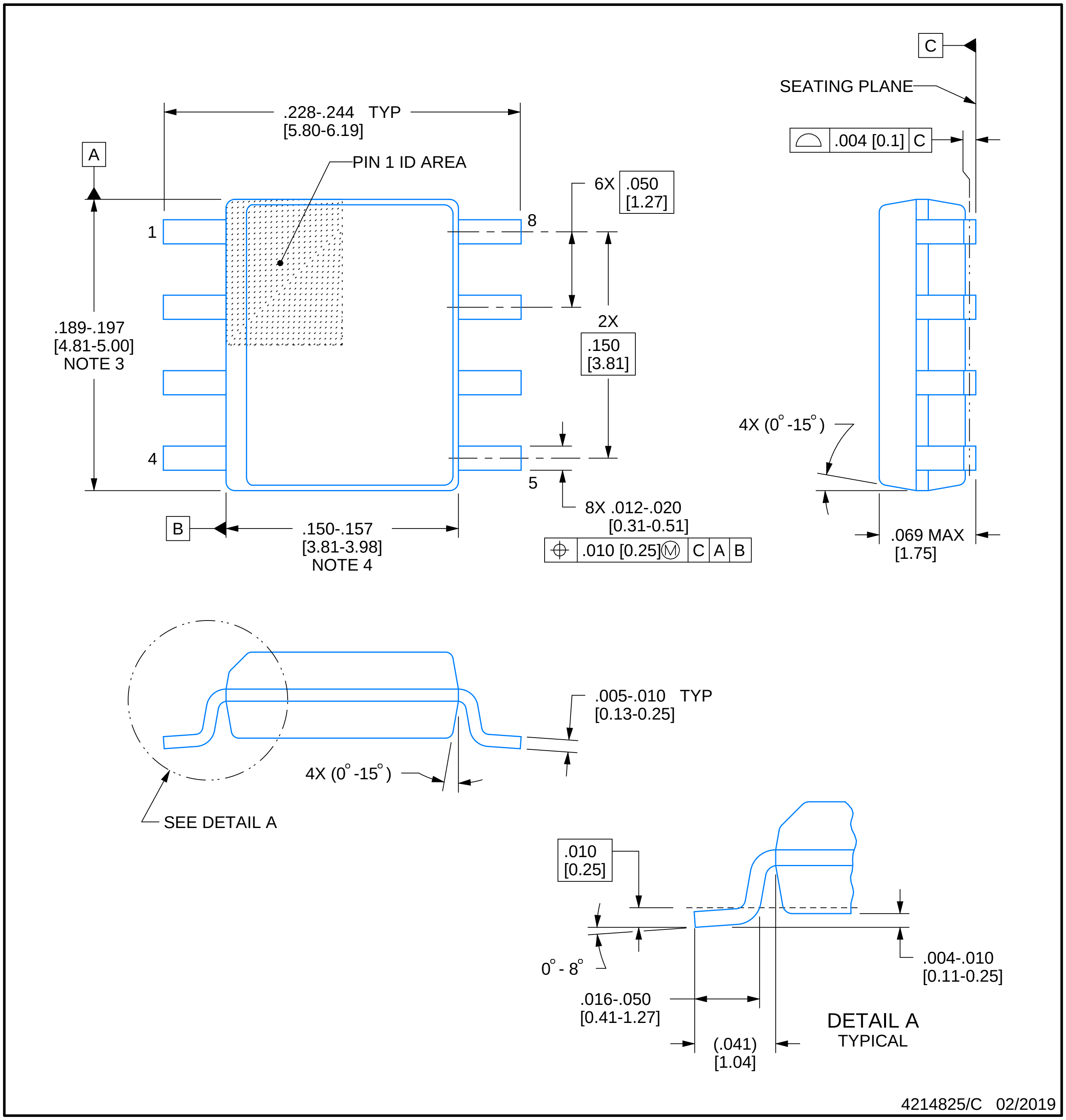


PACKAGE OUTLINE

D0008A

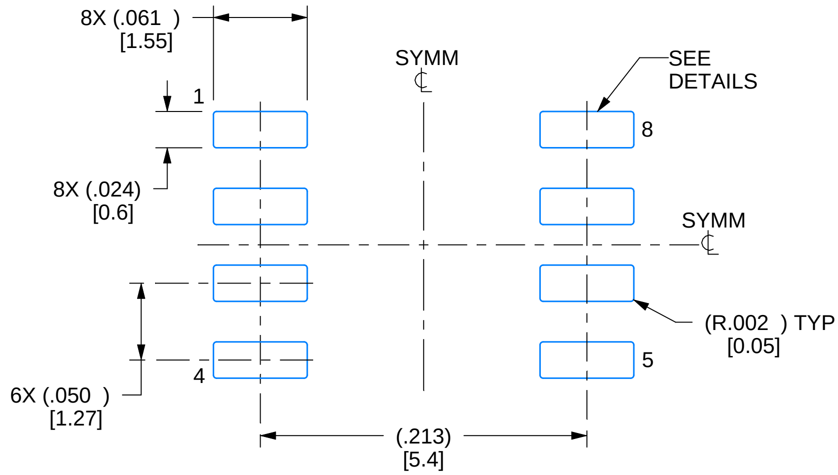
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

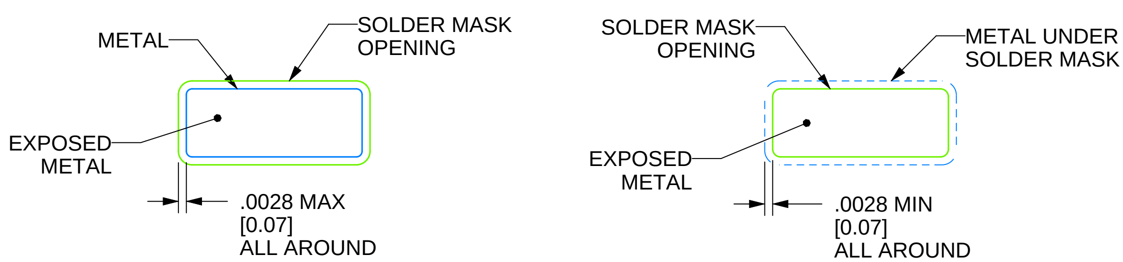


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

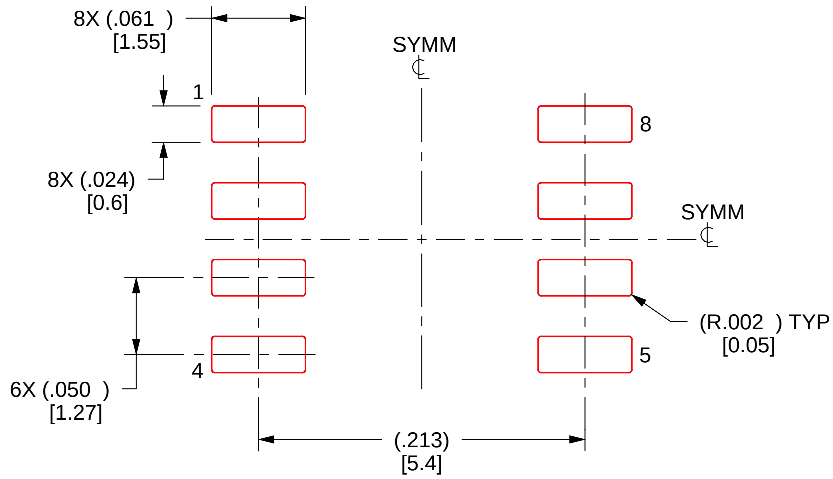
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.