双路，2 每秒百万次采样 (MSPS)，12 位，2 + 2 或 3 + 3 通道同步采样模数转换器

查询样片: ADS7863A

特性

- 四个完全或六个伪差分输入
- 信噪比 (SNR)：71dB
- 总谐波失真 (THD)：-81dB
- 可编程和经缓冲内部 2.5V 基准
- 灵活的节电特性
- 可变电源范围：2.7V 至 5.5V
- 低功耗运行：5V 时为 45mW
- 工作温度范围：
  -40°C 至 +125°C
- 与 ADS7861 和 ADS8361（窄间距小外形尺寸 (SSOP) 封装）引脚兼容

应用范围

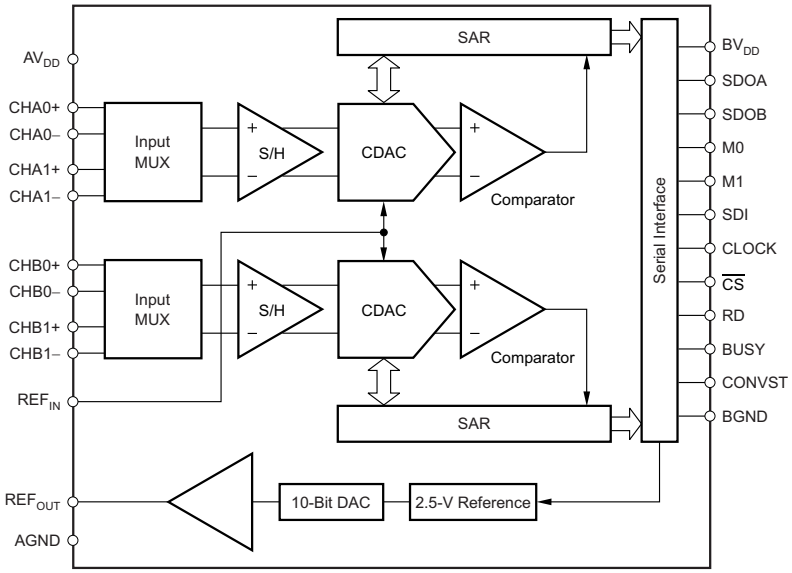
- 电机控制
- 多轴定位系统
- 三相电源控制

描述

ADS7863A 是一款双路，12 位，2MSPS，模数转换器 (ADC)，此模数转换器具有被分成两组的四个全差分或六个伪差分输入通道，以实现高速、同时信号采集。 到采样保持 (S/H) 放大器的输入为全差分，并且对 ADC 输入保持为差分信号。 这个架构在 100kHz 时提供值为 72dB 的出色共模抑制，这在嘈杂环境中是一个关键的性能特性。

此器件与 ADS7861 引脚兼容，但是提供诸如可编程基准输出，灵活电源电压（AV_{DD} 和 BV_{DD} 为 2.7V 至 5.5V），每个 ADC 上具有三通道的伪差分输入复用器和几个节电特性。

此器件采用紧缩小型封装(SSOP)-24 和4mm × 4mm 四方扁平无引线(QFN)-24 封装。 此器件在 -40℃ 至 +125℃ 的扩展工作温度范围内额定运行。



功能方框图

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Supply voltage	AV_{DD} to AGND	–0.3 to +6	V
	BV_{DD} to BGND	–0.3 to +6	V
	BV_{DD} to AV_{DD}	1.5 × AV_{DD}	V
Analog and reference input voltage with respect to AGND		AGND – 0.3 to AV_{DD} + 0.3	V
Digital input voltage with respect to BGND		BGND – 0.3 to BV_{DD} + 0.3	V
Ground voltage difference	|AGND – BGND|	0.3	V
Input current to any pin except supply pins		–10 to +10	mA
Maximum virtual junction temperature, T_J		+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM), JEDEC standard 22, test method A114-C.01, all pins	±4000	V
	Charged device model (CDM), JEDEC standard 22, test method C101, all pins	±1500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage	AV_{DD} to AGND	2.7	5.0	5.5	V
	BV_{DD} to BGND, low voltage levels	2.7		3.6	V
	BV_{DD} to BGND, 5-V logic levels	4.5	5.0	5.5	V
Reference input voltage on REF_{IN}		0.5	2.5	2.525	V
Analog differential input voltage	(CHXX+) – (CHXX–)	$–V_{REF}$		$+V_{REF}$	V
Operating ambient temperature range, T_A		–40		+125	°C

THERMAL INFORMATION

THERMAL METRIC(1)		ADS7863A		UNITS
		DBQ (SSOP)	RGE (QFN)	
		24 PINS	24 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	80.9	35.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.6	36.1	
θ_{JB}	Junction-to-board thermal resistance	34.2	12.8	
ψ_{JT}	Junction-to-top characterization parameter	9.2	0.5	
ψ_{JB}	Junction-to-board characterization parameter	33.8	12.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	4.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +125°C, entire power-supply range, V_{REF} = 2.5 V (internal), f_{CLK} = 32 MHz, and t_{DATA} = 2 MSPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
RESOLUTION						
	Resolution		12			Bits
ANALOG INPUT						
FSR	Full-scale differential input range	(CHxx+) – (CHxx–)	$–V_{REF}$		$+V_{REF}$	V
V_{IN}	Absolute input voltage	CHxx+ or CHxx+ to AGND	–0.1		AV_{DD} + 0.1	V
C_{IN}	Input capacitance	CHxx+ or CHxx– to AGND		2		pF
C_{ID}	Differential input capacitance			4		pF
I_{IL}	Input leakage current		–1		+1	nA
CMRR	Common-mode rejection ratio	Both ADCs, dc to 100 kHz		72		dB
DC ACCURACY						
INL	Integral nonlinearity	–40°C < T_A < +125°C	–1.25	±0.6	+1.25	LSB
		–40°C < T_A < +85°C	–1	±0.5	+1	LSB
DNL	Differential nonlinearity		–1	±0.5	+1	LSB
V_{OS}	Input offset error		–3	±0.5	+3	LSB
	V_{OS} match		–3	±0.5	+3	LSB
dV_{OS}/dT	Input offset thermal drift			±3		µV/°C
G_{ERR}	Gain error	Referred to voltage at REF_{IN}	–0.5%		+0.5%	
	G_{ERR} match		–0.5%	±0.1%	+0.5%	
G_{ERR}/dT	Gain error thermal drift	Referred to voltage at REF_{IN}		±1		ppm/°C
PSRR	Power-supply rejection ratio	AV_{DD} = 5.5 V		70		dB
AC ACCURACY						
SINAD	Signal-to-noise + distortion	V_{IN} = 5 V_{PP} at 100 kHz	69.8	71		dB
SNR	Signal-to-noise ratio	V_{IN} = 5 V_{PP} at 100 kHz	70	71.5		dB
THD	Total harmonic distortion	V_{IN} = 5 V_{PP} at 100 kHz		–81	–76	dB
SFDR	Spurious-free dynamic range	V_{IN} = 5 V_{PP} at 100 kHz	76	84		dB
SAMPLING DYNAMICS						
t_{CONV}	Conversion time per ADC	1 MHz < f_{CLK} ≤ 32 MHz	16			t_{CLK}
t_{ACQ}	Acquisition time		2			t_{CLK}
t_{DATA}	Data rate	1 MHz < f_{CLK} ≤ 32 MHz	62.5		2000	kSPS
t_A	Aperture delay				6	ns
	t_A match			50		ps
t_{AJIT}	Aperture jitter			50		ps
f_{CLK}	Clock frequency on CLOCK		1		32	MHz
T_{CLK}	Clock period		31.25		1000	ns
INTERNAL VOLTAGE REFERENCE						
Resolution	Reference output DAC resolution		10			Bits
V_{REFOUT}	Reference output voltage	Over 20% to 100% DAC range	0.2 V_{REFOUT}		V_{REFOUT}	V
		DAC = 3FFh, –40°C < T_A < +125°C	2.485	2.500	2.515	V
		DAC = 3FFh at +25°C	2.495	2.500	2.505	V
dV_{REFOUT}/dT	Reference voltage drift			±10		ppm/°C
DNL_{DAC}	DAC differential nonlinearity		–9.76	±2.44	9.76	mV
			–4	±1	4	LSB
INL_{DAC}	DAC integral nonlinearity		–9.76	±1.22	9.76	mV
			–4	±0.5	4	LSB
V_{OSDAC}	DAC offset error	V_{REFOUT} = 0.5 V	–9.76	±2.44	9.76	mV
			–4	±1	4	LSB
PSRR	Power-supply rejection ratio			73		dB
I_{REFOUT}	Reference output dc current		–2		+2	mA

(1) All typical values are at T_A = +25°C.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +125°C, entire power-supply range, V_{REF} = 2.5 V (internal), f_{CLK} = 32 MHz, and t_{DATA} = 2 MSPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
INTERNAL VOLTAGE REFERENCE (continued)						
I_{REFSC}	Reference output short-circuit current(2)			50		mA
t_{REFON}	Reference output settling time			0.5		ms
VOLTAGE REFERENCE INPUT						
V_{REF}	Reference input voltage range		0.5		2.525	V
I_{REF}	Reference input current			50		µA
C_{REF}	Reference input capacitance			10		pF
DIGITAL INPUTS (Logic Family: CMOS with Schmitt-Trigger)						
V_{IH}	High-level input voltage		0.7 × BV_{DD}		BV_{DD} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × BV_{DD}	V
I_{IN}	Input current	V_{IN} = BV_{DD} to BGND	–50		+50	nA
C_{IN}	Input capacitance			5		pF
DIGITAL OUTPUTS (Logic Family: CMOS)						
V_{OH}	High-level output voltage	BV_{DD} = 4.5 V, I_{OH} = –100 µA	BV_{DD} – 0.2			V
V_{OL}	Low-level output voltage	BV_{DD} = 4.5 V, I_{OH} = 100 µA			0.2	V
I_{OZ}	High-impedance-state output current		–50		+50	nA
C_{OUT}	Output capacitance			5		pF
C_{LOAD}	Load capacitance				30	pF
POWER SUPPLY						
AV_{DD}	Analog supply voltage	AV_{DD} to AGND	2.7	5.0	5.5	V
BV_{DD}	Buffer I/O supply voltage	BV_{DD} to BGND	2.7	3.0	5.5	V
AI_{DD}	Analog supply current	AV_{DD} = 2.7 V		4.5	6	mA
		AV_{DD} = 5.0 V		6.5	8	mA
		AV_{DD} = 2.7 V, NAP power-down		1.1	1.5	mA
		AV_{DD} = 5.0 V, NAP power-down		1.4	2.0	mA
		AV_{DD} = 2.7 V, deep power-down			0.001	mA
		AV_{DD} = 5.0 V, deep power-down			0.001	mA
BI_{DD}	Buffer I/O supply current	BV_{DD} = 2.7 V, C_{LOAD} = 10 pF		0.5	1.3	mA
		BV_{DD} = 3.3 V, C_{LOAD} = 10 pF		0.9	1.6	mA
P_{DISS}	Power dissipation	AV_{DD} = 2.7 V, BV_{DD} = 2.7 V		13.5	19.7	mW
		AV_{DD} = 5.0 V, BV_{DD} = 3.3 V		35.5	45.3	mW

(2) Reference output current is not limited internally.

PARAMETRIC MEASUREMENT INFORMATION

EQUIVALENT INPUT CIRCUIT

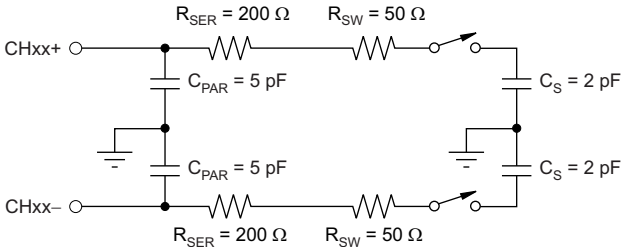


Figure 1. Equivalent Input Circuit

TIMING CHARACTERISTICS

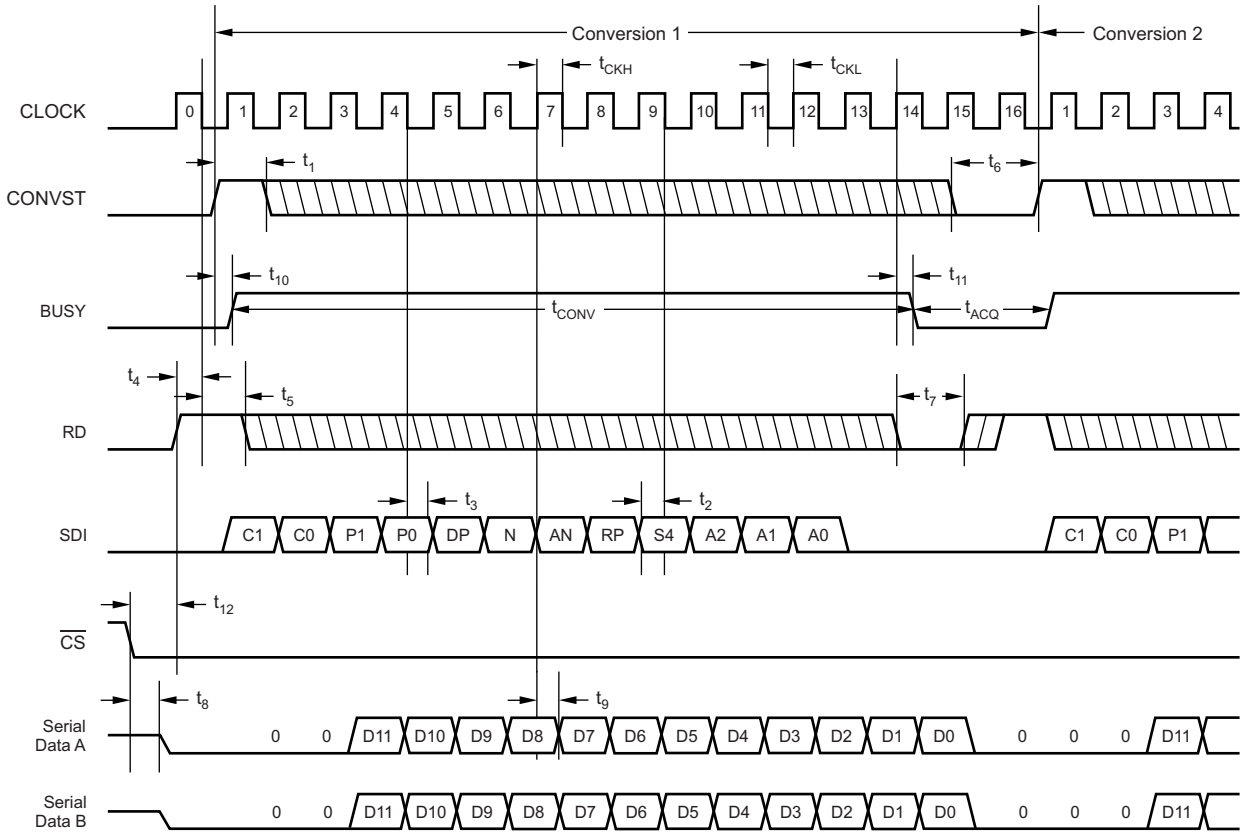
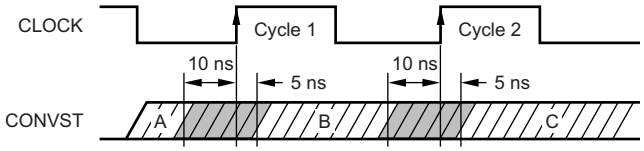


Figure 2. Detailed Timing Diagram (Mode I)



NOTE: All CONVST commands that occur more than 10 ns before the cycle 1 rising edge of the external clock (region *A*) initiate a conversion on the cycle 1 rising edge. All CONVST commands that occur 5 ns after the cycle 1 rising edge or 10 ns before the cycle 2 rising edge (region *B*) initiate a conversion on the cycle 2 rising edge. All CONVST commands that occur 5 ns after the cycle 2 rising edge (region *C*) initiate a conversion on the rising edge of the next clock period.
The CONVST pin should never be switched from low to high in the region 10 ns prior to the CLOCK rising edge and 5 ns after the rising edge (gray areas). If CONVST is toggled in this gray area, the conversion could begin on either the same CLOCK rising edge or the following edge.

Figure 3. CONVST Timing

TIMING REQUIREMENTS(1)

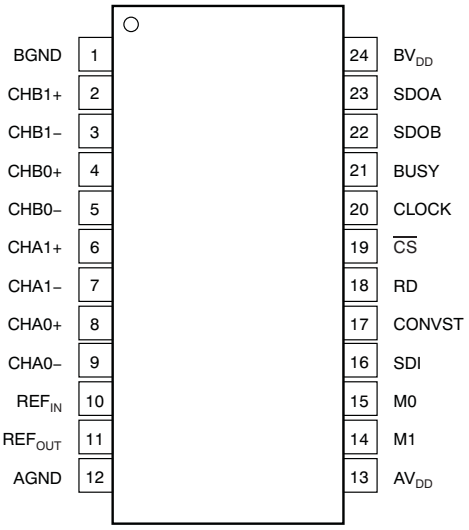
Over recommended operating free-air temperature range at –40°C to +125°C, AV_{DD} = 5 V, and BV_{DD} = 2.7 V to 5 V, unless otherwise noted.

PARAMETER		COMMENTS	MIN	MAX	UNIT
t_{CONV}	Conversion time	f_{CLOCK} = 32 MHz	406.25		ns
t_{ACQ}	Acquisition time	f_{CLOCK} = 32 MHz	62.5		ns
f_{CLOCK}	CLOCK frequency	See Figure 2	1	32	MHz
t_{CLOCK}	CLOCK period	See Figure 2	31.25	1000	ns
t_{CKL}	CLOCK low time	See Figure 2	9.4		ns
t_{CKH}	CLOCK high time	See Figure 2	9.4		ns
t_1	CONVST high time	See Figure 2	20		ns
t_2	SDI setup time to CLOCK falling edge	See Figure 2	10		ns
t_3	SDI hold time to CLOCK falling edge	See Figure 2	5		ns
t_4	RD high setup time to CLOCK falling edge	See Figure 2	10		ns
t_5	RD high hold time to CLOCK falling edge	See Figure 2	5		ns
t_6	CONVST low time	See Figure 2	1		t_{CLOCK}
t_7	RD low time relative to CLOCK falling edge	See Figure 2	1		t_{CLOCK}
t_8	$\overline{CS}$ low to SDOx valid	See Figure 2	13		ns
t_9	CLOCK rising edge to DATA valid delay (MIN = minimum hold time of current data; MAX = maximum delay to new data valid)	See Figure 2, 2.7 V ≤ BV_{DD} ≤ 3.6 V	4	11	ns
		See Figure 2, 4.5 V ≤ BV_{DD} ≤ 5.5 V	3	9	ns
t_{10}	CONVST rising edge to BUSY high delay(2)	See Figure 2	3		ns
t_{11}	CLOCK rising edge to BUSY low delay	See Figure 2	3		ns
t_{12}	$\overline{CS}$ low to RD high delay	See Figure 2	10		ns

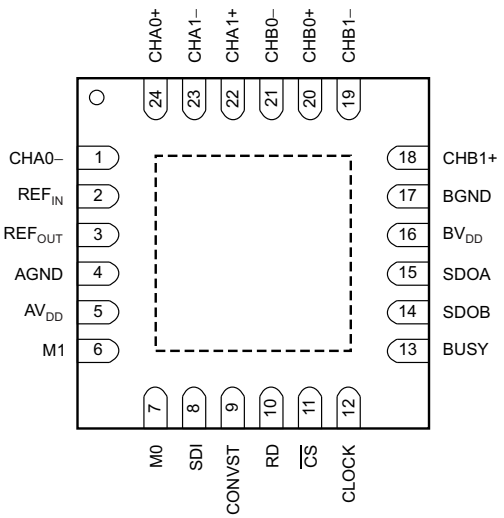
(1) All input signals are specified with $t_R = t_F$ = 1.5 ns (10% to 90% of BV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH}) / 2.
(2) Not applicable in auto-NAP power-down mode.

PIN CONFIGURATIONS

DBQ PACKAGE
SSOP-24
(Top View)



RGE PACKAGE
4-mm × 4-mm QFN-24
(TOP VIEW)



PIN DESCRIPTIONS

	PIN NUMBER		
NAME	**SSOP**	**QFN**	**DESCRIPTION**
AGND	12	4	Analog ground. Connect to analog ground plane.
AV_{DD}	13	5	Analog power supply, 2.7 V to 5.5 V. Decouple to AGND with a 1-µF ceramic capacitor.
BGND	1	17	Buffer I/O ground. Connect to digital ground plane.
BUSY	21	13	ADC busy indicator. BUSY goes high when the inputs are in hold mode and returns to low after the conversion finishes.
BV_{DD}	24	16	Buffer I/O supply, 2.7 V to 5.5 V. Decouple to BGND with a 1-µF ceramic capacitor.
CHA0–	9	1	Inverting analog input channel A0
CHA0+	8	24	Noninverting analog input channel A0
CHA1–	7	23	Inverting analog input channel A1
CHA1+	6	22	Noninverting analog input channel A1
CHB0–	5	21	Inverting analog input channel B0
CHB0+	4	20	Noninverting analog input channel B0
CHB1–	3	19	Inverting analog input channel B1
CHB1+	2	18	Noninverting analog input channel B1
CLOCK	20	12	External clock input
CONVST	17	9	Conversion start. The ADC switches from sample mode into hold mode on the CONVST rising edge, independent of the CLOCK status. The conversion starts with the next CLOCK rising edge.
$\overline{CS}$	19	11	Chip select. When low, the SDOx outputs are active; when high, the SDOx outputs 3-state.
M0	15	7	Mode pin 0. Selects between analog input channels (see Table 8).
M1	14	6	Mode pin 1. Selects between the SDOx digital outputs (see Table 8).
RD	18	10	Read data. Synchronization pulse for the SDOx outputs and SDI input. RD only triggers when $\overline{CS}$ is low.
REF_{IN}	10	2	Reference voltage input. A 470-nF ceramic capacitor (min) is required at this terminal.
REF_{OUT}	11	3	Reference voltage output. The programmable internal voltage reference output is available on this pin.
SDI	16	8	Serial data input. This pin allows the additional device features to be used but SDI can also be used in an ADS7861-compatible manner.
SDOA	23	15	Serial data output for converter A. When M1 is high, both SDOA and SDOB are active. Data are valid on the falling CLOCK edge.
SDOB	22	14	Serial data output for converter B. Data are valid on the falling CLOCK edge.

TYPICAL CHARACTERISTICS

Over the entire supply voltage range, V_{REF} = 2.5 V (internal), f_{CLK} = 32 MHz, and t_{DATA} = 2 MSPS, unless otherwise noted.

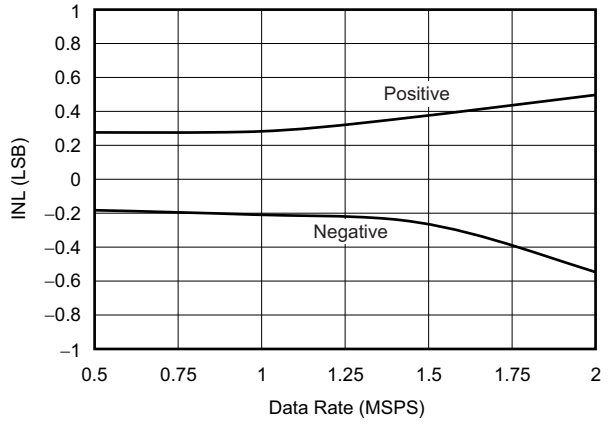


Figure 4. INTEGRAL NONLINEARITY vs DATA RATE

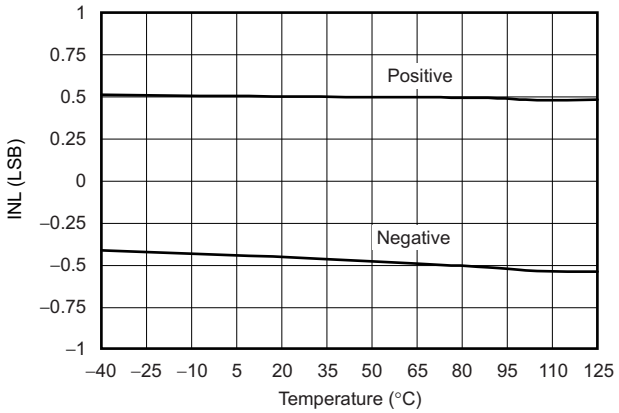


Figure 5. INTEGRAL NONLINEARITY vs TEMPERATURE

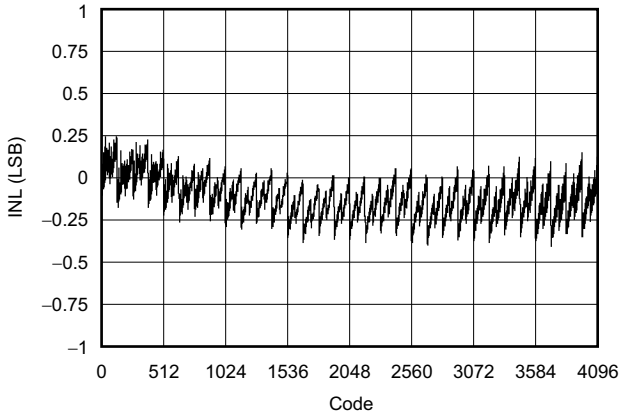


Figure 6. INTEGRAL NONLINEARITY vs CODE

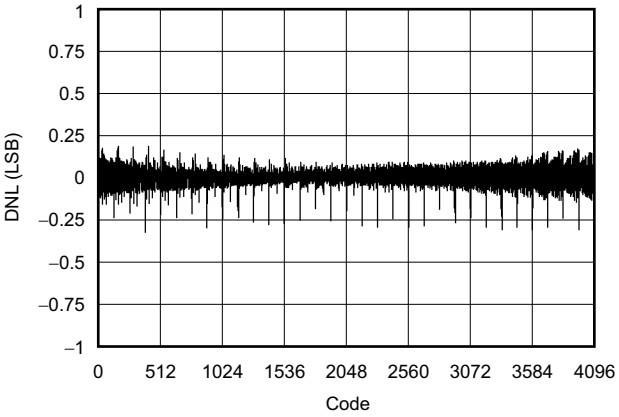


Figure 7. DIFFERENTIAL NONLINEARITY vs CODE

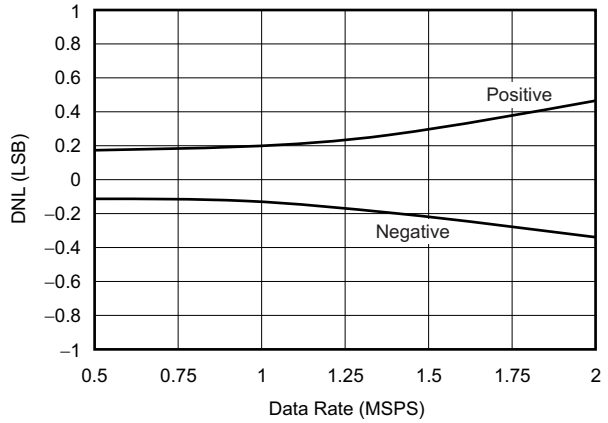


Figure 8. DIFFERENTIAL NONLINEARITY vs DATA RATE

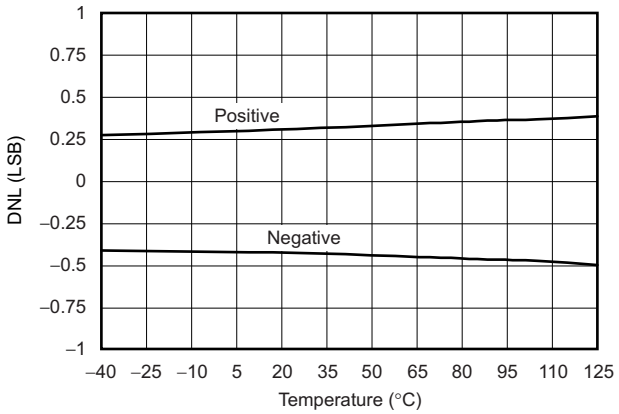


Figure 9. DIFFERENTIAL NONLINEARITY vs TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

Over the entire supply voltage range, V_{REF} = 2.5 V (internal), f_{CLK} = 32 MHz, and t_{DATA} = 2 MSPS, unless otherwise noted.

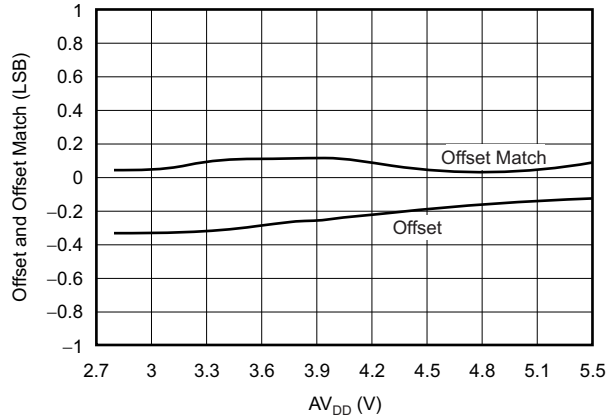


Figure 10. OFFSET ERROR AND OFFSET MATCH vs ANALOG SUPPLY VOLTAGE

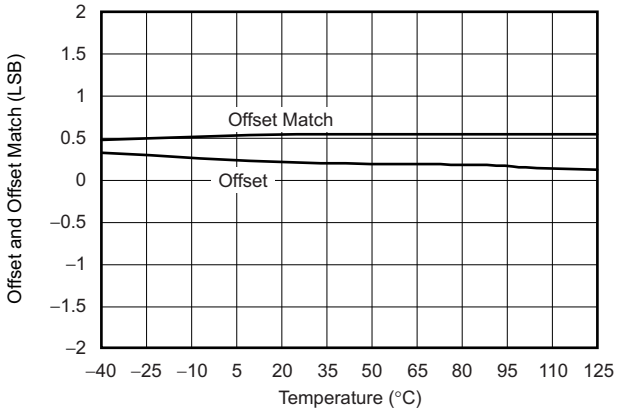


Figure 11. OFFSET ERROR AND OFFSET MATCH vs TEMPERATURE

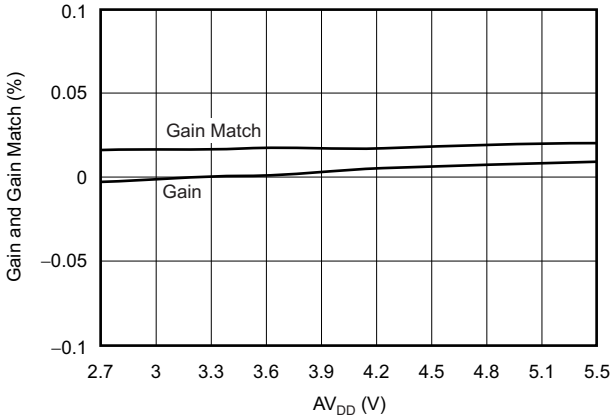


Figure 12. GAIN ERROR AND GAIN MATCH vs ANALOG SUPPLY VOLTAGE

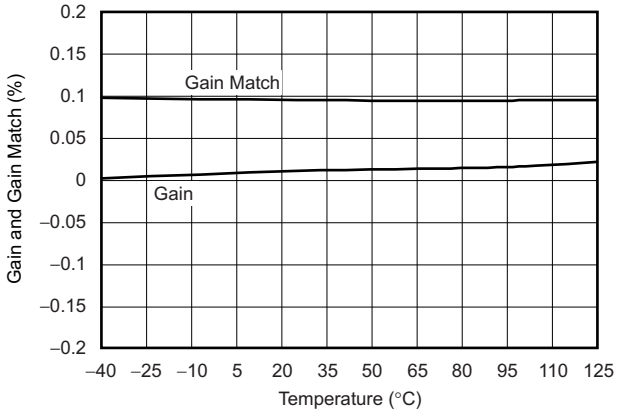


Figure 13. GAIN ERROR AND GAIN MATCH vs TEMPERATURE

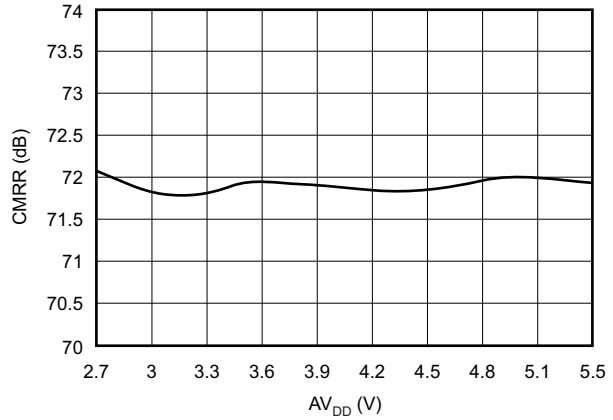


Figure 14. COMMON-MODE REJECTION RATIO vs ANALOG SUPPLY VOLTAGE

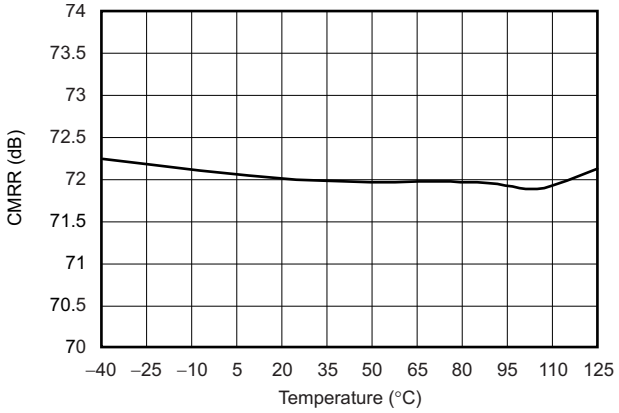


Figure 15. COMMON-MODE REJECTION RATIO vs TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

Over the entire supply voltage range, V_{REF} = 2.5 V (internal), f_{CLK} = 32 MHz, and t_{DATA} = 2 MSPS, unless otherwise noted.

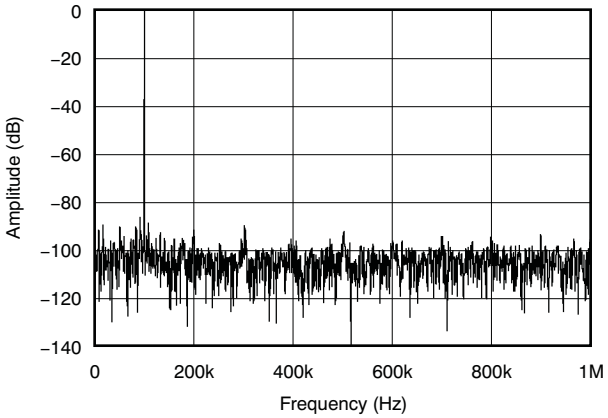


Figure 16. FREQUENCY SPECTRUM (4096-Point FFT; f_{IN} = 100 kHz)

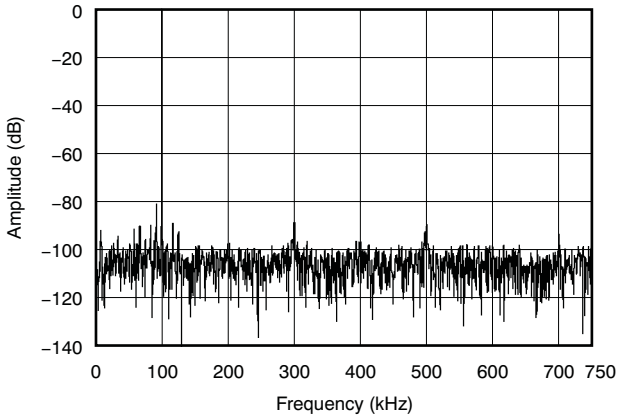


Figure 17. FREQUENCY SPECTRUM (4096-Point FFT; f_{IN} = 100 kHz, f_{SAMPLE} = 1.5 MSPS)

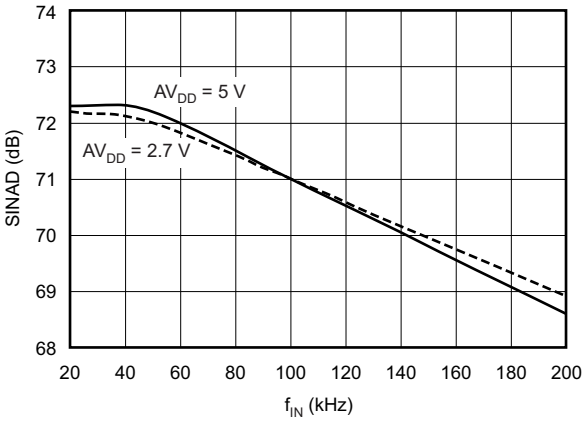


Figure 18. SIGNAL-TO-NOISE RATIO AND DISTORTION vs INPUT SIGNAL FREQUENCY

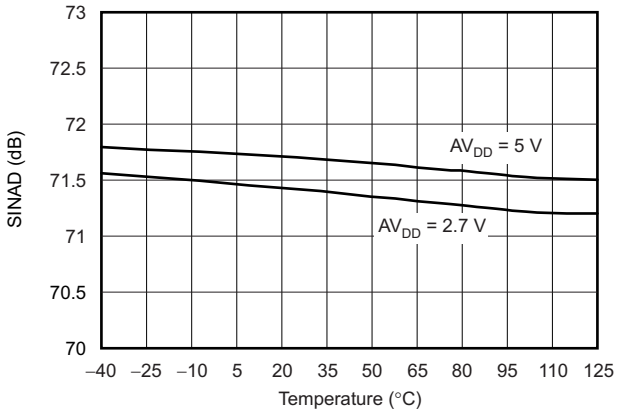


Figure 19. SIGNAL-TO-NOISE RATIO AND DISTORTION vs TEMPERATURE

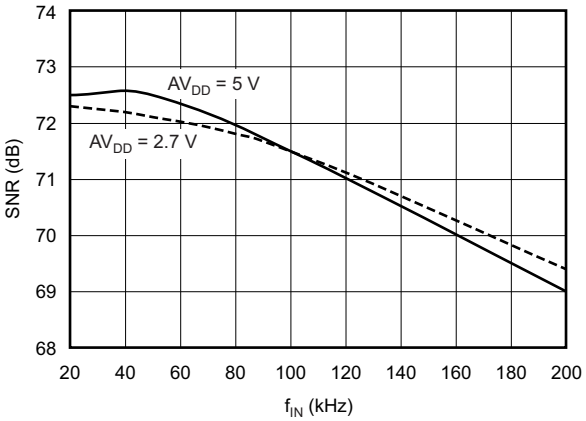


Figure 20. SIGNAL-TO-NOISE RATIO vs INPUT SIGNAL FREQUENCY

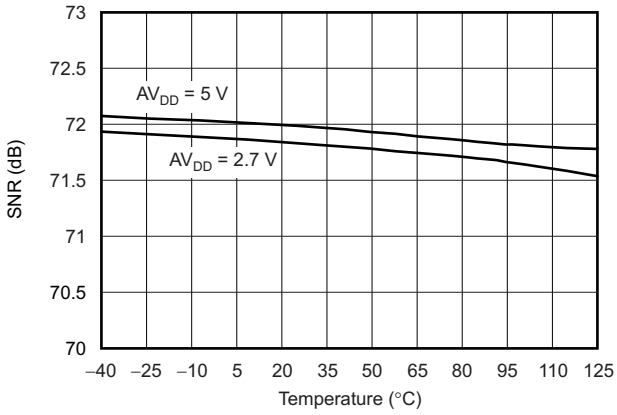


Figure 21. SIGNAL-TO-NOISE RATIO vs TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

Over the entire supply voltage range, V_{REF} = 2.5 V (internal), f_{CLK} = 32 MHz, and t_{DATA} = 2 MSPS, unless otherwise noted.

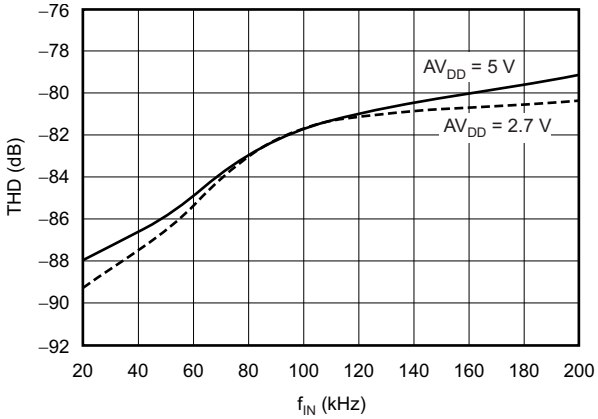


Figure 22. TOTAL HARMONIC DISTORTION vs INPUT SIGNAL FREQUENCY

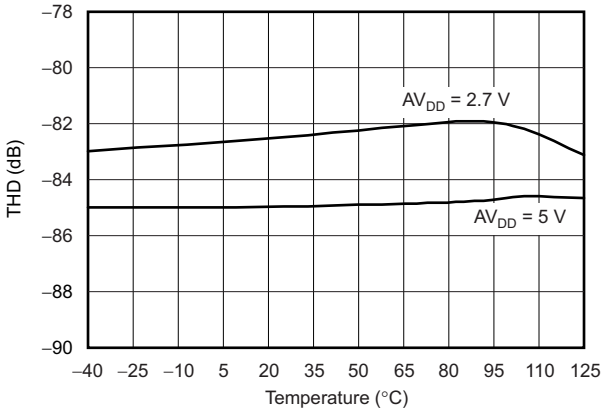


Figure 23. TOTAL HARMONIC DISTORTION vs TEMPERATURE

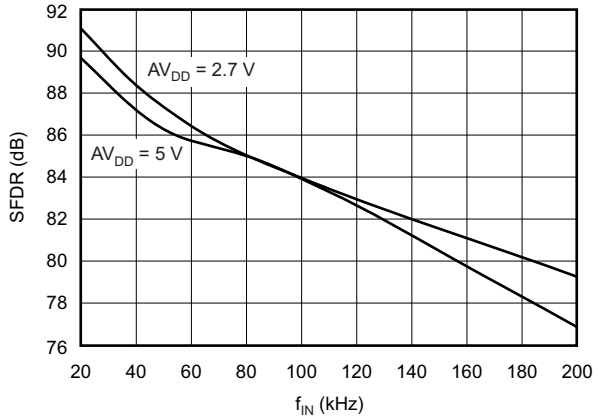


Figure 24. SPURIOUS-FREE DYNAMIC RANGE vs INPUT SIGNAL FREQUENCY

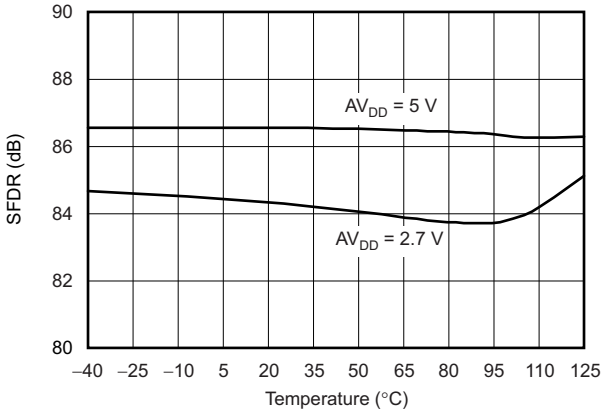


Figure 25. SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE

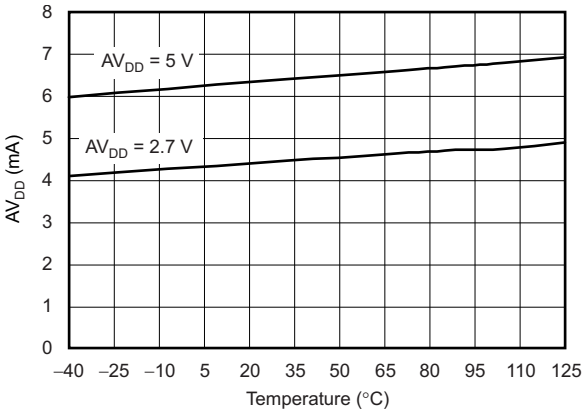


Figure 26. ANALOG SUPPLY CURRENT vs TEMPERATURE

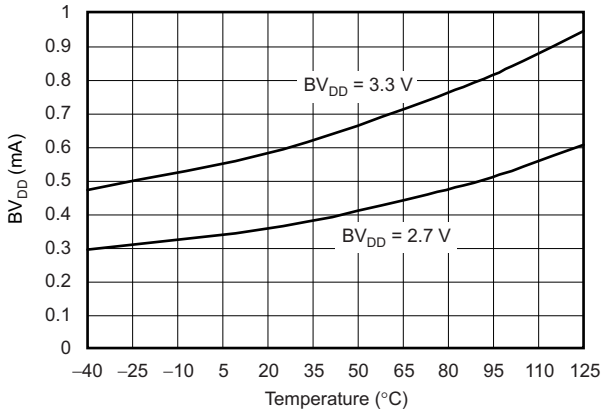


Figure 27. DIGITAL SUPPLY CURRENT vs TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

Over the entire supply voltage range, V_{REF} = 2.5 V (internal), f_{CLK} = 32 MHz, and t_{DATA} = 2 MSPS, unless otherwise noted.

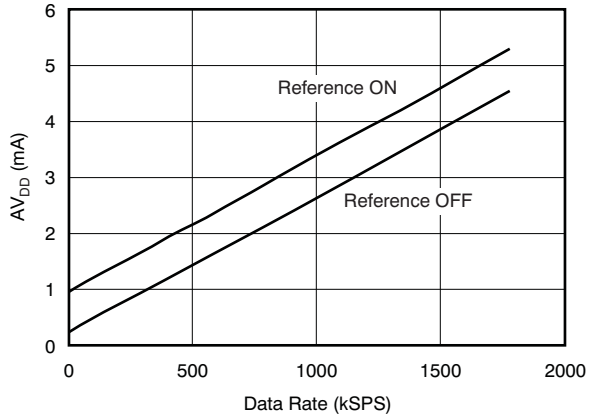


Figure 28. ANALOG SUPPLY CURRENT vs DATA RATE (Auto-NAP Mode)

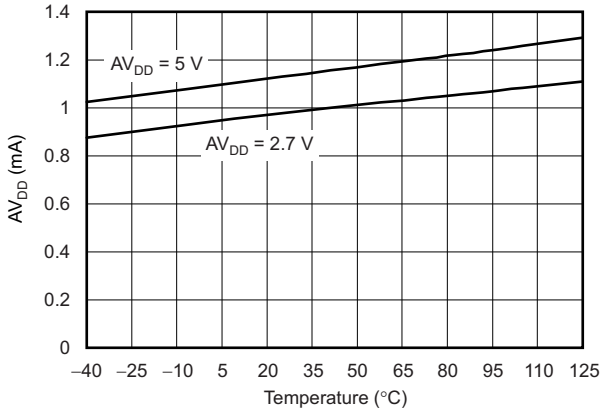


Figure 29. ANALOG SUPPLY CURRENT vs TEMPERATURE (Auto-NAP Mode)

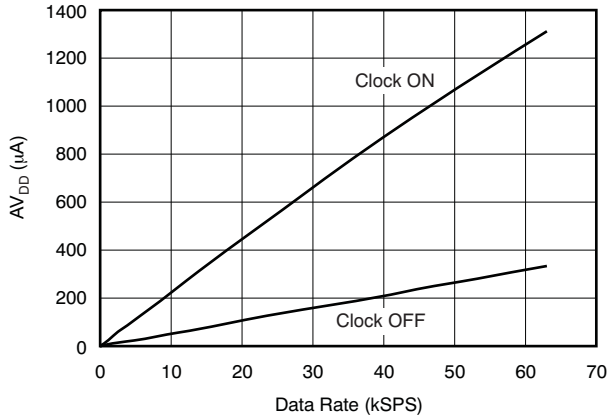


Figure 30. ANALOG SUPPLY CURRENT vs DATA RATE (Deep Power-Down Mode)

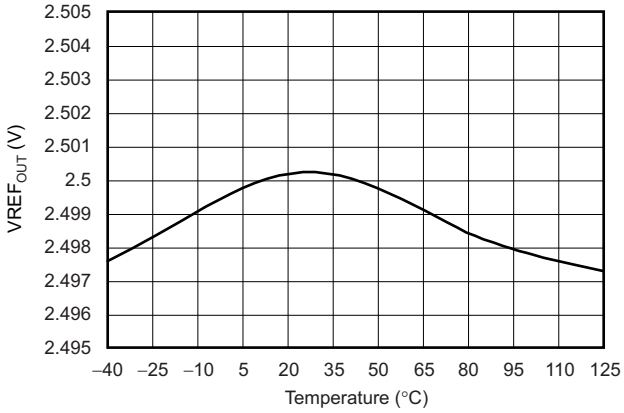


Figure 31. REFERENCE OUTPUT VOLTAGE vs TEMPERATURE

APPLICATIONS INFORMATION

GENERAL DESCRIPTION

The ADS7863A includes two 12-bit, analog-to-digital converters (ADCs) that operate based on the successive-approximation register (SAR) principle. The ADCs sample and convert simultaneously. Conversion time can be as low as 406.25 ns. Adding the 62.5-ns acquisition time and an additional clock cycle for setup and hold time requirements and skew results in a maximum conversion rate of 2 MSPS.

Each ADC has a fully-differential, 2:1 multiplexer front-end. In many common applications, all negative input signals remain at the same constant voltage (for example, 2.5 V). In this type of application, the multiplexer can be used in a pseudo-differential 3:1 mode, where CHx0– functions as a common-mode input and the remaining three inputs (CHx0+, CHx1–, and CHx1+) operate as separate inputs referred to the common-mode input.

The ADS7863A also includes a 2.5-V internal reference. The reference drives a 10-bit digital-to-analog converter (DAC), allowing the voltage at the REF_{OUT} pin to be adjusted via the serial interface in 2.44-mV steps. A low-noise operational amplifier with unity gain buffers the DAC output voltage and drives the REF_{OUT} pin.

The ADS7863A offers a serial interface that is compatible with the ADS7861. However, instead of the A0 pin of the ADS7861 controlling channel selection, the ADS7863A offers a serial data input (SDI) pin that supports additional functions described in the *Digital* section (see also the *ADS7861 Compatibility* section).

ANALOG

This section addresses the analog input circuit, the ADCs, and the reference design of the device.

Analog Inputs

Each ADC is fed by an input multiplexer, as shown in Figure 32. Each multiplexer is either used in a fully-differential 2:1 configuration (as described in Table 1) or a pseudo-differential 3:1 configuration (as shown in Table 2). The channel selection is performed using bits C1 and C0 in the SDI register (see also the *Serial Data Input* section).

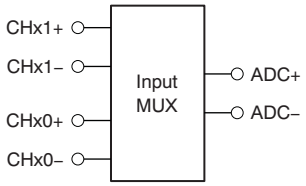


Figure 32. Input Multiplexer Configuration

The input path for the converter is fully differential and provides a common-mode rejection of 72 dB at 100 kHz. The high CMRR also helps suppress noise in harsh industrial environments.

Table 1. Fully Differential 2:1 Multiplexer Configuration

C1	C0	ADC+	ADC–
0	0	CHx0+	CHx0–
1	1	CHx1+	CHx1–

Table 2. Pseudo-Differential 3:1 Multiplexer Configuration

C1	C0	ADC+	ADC–
0	0	CHx0+	CHx0–
0	1	CHx1–	CHx0–
1	0	CHx1+	CHx0–

Each 2-pF sample-and-hold capacitor (defined as C_S in Figure 1) is connected via switches to the multiplexer output. Opening the switches holds the sampled data during the conversion process. After finishing the conversion, both capacitors are pre-charged for the duration of one clock cycle to the voltage present at the REF_{IN} pin. After the pre-charging, the multiplexer outputs are connected to the sampling capacitors again. The voltage at the analog input pin is usually different from the reference voltage; therefore, the sample capacitors must be charged to within one-half LSB for 12-bit accuracy during the acquisition time t_{ACQ} (see the Timing Characteristics).

Acquisition time is indicated with the BUSY signal being held low. t_{ACQ} starts by closing the input switches (after finishing the previous conversion and pre-charging) and finishes with the rising edge of the CONVST signal. If the ADS7863A operates at full speed, the acquisition time is typically 62.5 ns.

The minimum –3-dB bandwidth of the driving operational amplifier can be calculated as shown in Equation 1:

$$f_{-3dB} = \frac{\ln(2) \times (n + 1)}{2\pi \times t_{ACQ}} \quad (1)$$

where:

- n = 12 is the device resolution

With t_{ACQ} = 62.5 ns, the minimum bandwidth of the driving amplifier is 23 MHz. The required bandwidth can be lower if the application allows a longer acquisition time.

A gain error occurs if a given application does not fulfill the settling requirement shown in Equation 1. As a result of pre-charging the capacitors, linearity and THD are not directly affected, however.

The OPA365 from Texas Instruments is recommended as a driver; in addition to offering the required bandwidth, the OPA365 provides a low offset and also offers excellent THD performance.

The phase margin of the driving operational amplifier is usually reduced by the ADC sampling capacitor. A resistor placed between the capacitor and amplifier limits this effect; therefore, an internal 200-Ω resistor (R_{SER}) is placed in series with the switch. The switch resistance (R_{SW}) is typically 50 Ω (see Figure 1).

The differential input voltage range of the ADC is $\pm V_{REF}$, the voltage at the REF_{IN} pin.

The voltage to all inputs must be kept within the 0.3-V limit below AGND and above AV_{DD} while not allowing dc current to flow through the inputs. Current is only necessary to recharge the sample-and-hold capacitors.

Analog-to-Digital Converter (ADC)

The ADS7863A includes two SAR-type, 2-MSPS, 12-bit ADCs (see the functional block diagram on the front page of this data sheet).

CONVST

The analog inputs are held with the rising edge of the CONVST (conversion start) signal. The CONVST setup time referred to the next rising edge of CLOCK (system clock) is 10 ns (minimum). The conversion automatically starts with the rising CLOCK edge. CONVST should not be issued during a conversion, that is, when BUSY is high.

RD (read data) and CONVST can be shorted to minimize necessary software and wiring. The RD signal is triggered by the ADS7863A on the falling CLOCK edge. Therefore, the combined signals must be activated with the rising CLOCK edge. The conversion then starts with the subsequent rising CLOCK edge.

CLOCK

The ADC uses an external clock in the range of 1 MHz to 32 MHz. 12 clock cycles are needed for a complete conversion; the following clock cycle is used for pre-charging the sample capacitors and a minimum of two clock cycles are required for the sampling. With a minimum of 16 clocks used for the entire process, one clock cycle is left for the required setup and hold times along with some margin for delay caused by layout. The clock input can remain low between conversions (after applying the 16th falling edge to complete a running conversion). The input can also remain low after applying the 14th falling edge during a DAC register write access if the device is not required to perform a conversion on CHBx (for example, during an initiation phase after power-up).

The CLOCK duty cycle should be 50%. However, the ADS7863A functions properly with a duty cycle between 30% and 70%.

RESET

The ADS7863A features an internal power-on-reset (POR) function. When the device is powered up, the POR sets the device in default mode when AV_{DD} reaches 1.8 V. An external software reset can be issued using the SDI register bits A[2:0] (see the *Digital* section).

REF_{IN}

The reference input is not buffered and is directly connected to the ADC. The converter generates spikes on the reference input voltage because of internal switching. Therefore, an external capacitor to the analog ground (AGND) should be used to stabilize the reference input voltage. This capacitor should be at least 470 nF. Ceramic capacitors (X5R type) with values up to 1 µF are commonly available as SMD in 0402 size.

REF_{OUT}

The ADS7863A includes a low-drift, 2.5-V internal reference source. This source feeds a 10-bit string DAC that is controlled via the serial interface. As a result of this architecture, the voltage at the REF_{OUT} pin is programmable in 2.44-mV steps and can be adjusted to specific application requirements without the use of additional external components.

However, the DAC output voltage should not be programmed below 0.5 V to ensure the correct functionality of the reference output buffer. This buffer is connected between the DAC and the REF_{OUT} pin, and is capable of driving the capacitor at the REF_{IN} pin. A minimum of 470 nF is required to keep the reference stable (see the *REFIN* section). For applications that use an external reference source, the internal reference can be disabled using bit RP in the SDI register (see the *Digital* section). The settling time of the REF_{OUT} pin is 500 µs (maximum) with the reference capacitor connected. The default value of the REF_{OUT} pin after power-up is 2.5 V.

For operation with a 2.7-V analog supply and a 2.5-V reference, the internal reference buffer requires a rail-to-rail input and output. Such buffers typically contain two input stages; when the input voltage passes the mid-range area, a transition occurs at the output because of switching between the two input stages. In this voltage range, rail-to-rail amplifiers generally show a very poor power-supply rejection.

As a result of this poor performance, the ADS7863A buffer has a fixed transition at DAC code 509 (1FDh). At this code, the DAC may show a jump of up to 10 mV in the transfer function.

DIGITAL

This section addresses the timing and control of the ADS7863A serial interface.

Serial Data Input (SDI)

The serial data input or SDI pin is coupled to RD and clocked into the ADS7863A on each falling CLOCK edge. The data word length of the SDI register is 12 bits. Table 3 shows the register structure. Data must be transferred MSB-first. Table 4 through Table 6 describe specific bits of this register. The default value of this register after power-up is 000h.

Table 3. SDI Register Contents

SDI REGISTER BIT											
11	10	9	8	7	6	5	4	3	2	1	0
C1	C0	P1	P0	DP	N	AN	RP	S4	A2	A1	A0

Table 4. C1 and C0: Channel Selection

C1	C0	ADC A, B	
		POSITIVE INPUT	NEGATIVE INPUT
0	0	CHA0+, CHB0+	CHA0–, CHB0–
0	1	CHA1–, CHB1–	CHA0–, CHB0–
1	0	CHA1+, CHB1+	CHA0–, CHB0–
1	1	CHA1+, CHB1+	CHA1–, CHB1–

Table 5. P1 and P0: Additional Features Enable

P1	P0	FUNCTION
0	0	Additional features are not changed
0	1	Update additional features
1	0	Reserved for factory test (do not use)
1	1	Additional features are not changed

DP: Deep power-down enable (1 = device in deep power-down mode)

N: NAP power-down enable (1 = device in NAP power-down mode)

AN: AutoNAP power-down enable (1 = device in AutoNAP power-down mode)

RP: Reference power-down(1 = reference turned off)

S4: Special read mode for Modes II and IV (1 = special mode enabled)

Table 6. A2, A1, and A0: DAC Control and Device Reset

A2	A1	A0	FUNCTION
0	0	0	No action
0	0	1	DAC write with next access
0	1	0	No action
0	1	1	DAC read with next access
1	0	0	No action
1	0	1	Device reset
1	1	0	No action
1	1	1	No action

All additional features become active with the rising edge of the 12th CLOCK signal after issuing the RD pulse.

The reference DAC is controlled by the 12-bit DAC register that can also be accessed using the SDI pin (refer to Figure 41 for details). Table 7 shows the content of this register; the default value after power-up is 3FFh.

Table 7. DAC Register Contents

DAC REGISTER CONTENT											
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
X(1)	X	MSB	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

(1) X = don't care.

Serial Data Output (SDOx)

Converted data on the SDOx pins become valid with the third falling CLOCK edge after generating an RD pulse. The following sections explain the different modes of operation in detail.

The digital output code format of the ADS7863A is binary twos complement, as shown in Table 9. Conversion results can be read out multiple times until a new conversion is issued from the CONVST input.

Timing and Control

IMPORTANT:
Consider the detailed timing diagram (Figure 2) and CONVST timing diagram (Figure 3) within the Timing Characteristics section. For maximum data throughput, the descriptions and diagrams given in this data sheet assume that the CONVST and RD pins are tied together. Note that these pins can also be controlled independently.

Device operation can be configured in four different modes by using the M0 and M1 mode pins, as shown in Table 8.

Pin M0 sets either manual or automatic channel selection. In manual mode, the SDI register bits C[1:0] are used to select between channels CHx0 and CHx1; in automatic operation, the SDI register bits C[1:0] are ignored and channel selection is controlled by the device after each conversion. Pin M1 selects between serial data being transmitted simultaneously on both outputs SDOA and SDOB for each channel respectively, or using only the SDOA output for transmitting data from both channels (see Figure 33 through Figure 40 and the associated text for more information).

Table 8. M0, M1 Truth Table

M0	M1	CHANNEL SELECTION	SDOx USED
0	0	Manual (via SDI)	SDOA and SDOB
0	1	Manual (via SDI)	SDOA only
1	0	Automatic	SDOA and SDOB
1	1	Automatic	SDOA only

Additionally, the SDI pin is used for controlling device functionality; see the *Serial Data Input* section for details.

Table 9. ADS7863A Output Data Format

DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE (CHxx+) – (CHxx–)	INPUT VOLTAGE AT CHxx+ (CHxx– = V_{REF} = 2.5 V)	BINARY CODE	HEXADECIMAL CODE
Positive full-scale	V_{REF}	5 V	0111 1111 1111	7FF
Mid-scale	0V	2.5 V	0000 0000 0000	000
Mid-scale – 1LSB	$–V_{REF}$ / 4096	2.49878 V	1111 1111 1111	FFF
Negative full-scale	$–V_{REF}$	0 V	1000 0000 0000	800

Mode I

With the M0 and M1 pins are both set to '0', the device enters manual channel control operation and outputs data on both SDOA and SDOB, respectively. The SDI pin switches between the channels. A conversion is initiated by bringing CONVST high.

16 clock cycles are required to perform a single conversion. With the CONVST rising edge, the ADS7863A switches asynchronously to the external CLOCK from sample to hold mode.

After a delay (t_{12}), the BUSY output pin goes high and remains high for the duration of the conversion cycle. On the falling edge of the second CLOCK cycle, the ADS7863A latches in the channel for the next conversion cycle, depending on the status of the SDI register bits C[1:0]. $\overline{CS}$ must be brought low to enable both serial outputs. Data are valid on the falling edge of every 16 clock cycles per conversion. The first two bits are set to '0'. The subsequent data contain the 12-bit conversion result (the most significant bit is transferred first), followed by two '0's (see Figure 2 and Figure 33).

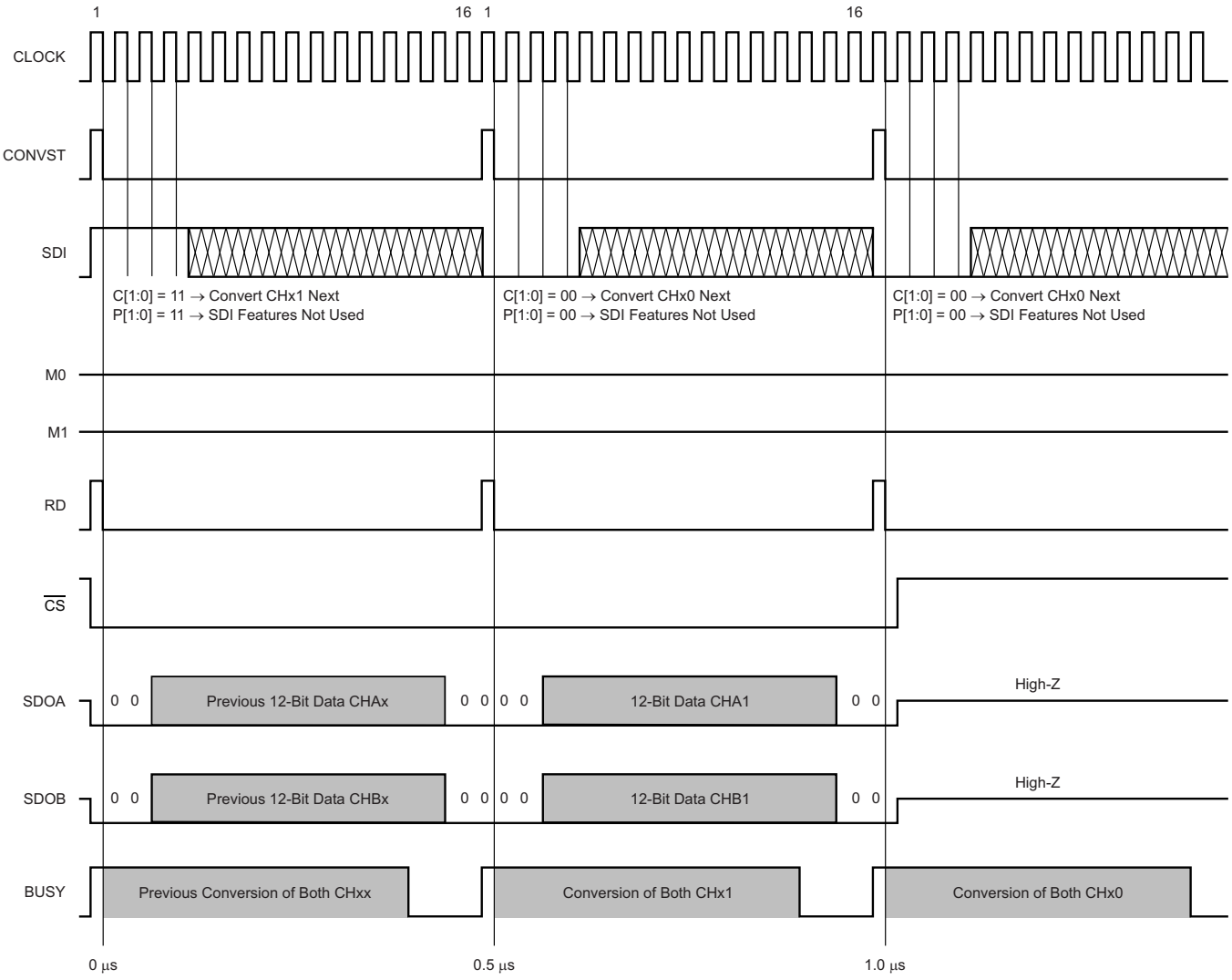


Figure 33. Mode I Timing Diagram (M0 = 0, M1 = 0)

Mode II

With M0 = 0 and M1 = 1, the device also operates in manual channel control mode and outputs data on the SDOA pin only when SDOB is set to 3-state. All other pins function in the same manner as they do in Mode I.

Because 32 clock cycles are required to output the results from both ADCs (instead of 16 cycles, if M1 = 0), the device requires 1.0 µs to perform a complete conversion or read cycle. If the CONVST signal is issued every 0.5 µs (required for the RD signal) as in Mode I, every second pulse is ignored, as shown in Figure 34.

Output data consist of a '0' followed by an ADC indicator ('0' for CHAx or '1' for CHBx), 12 bits of conversion results, and another '00'.

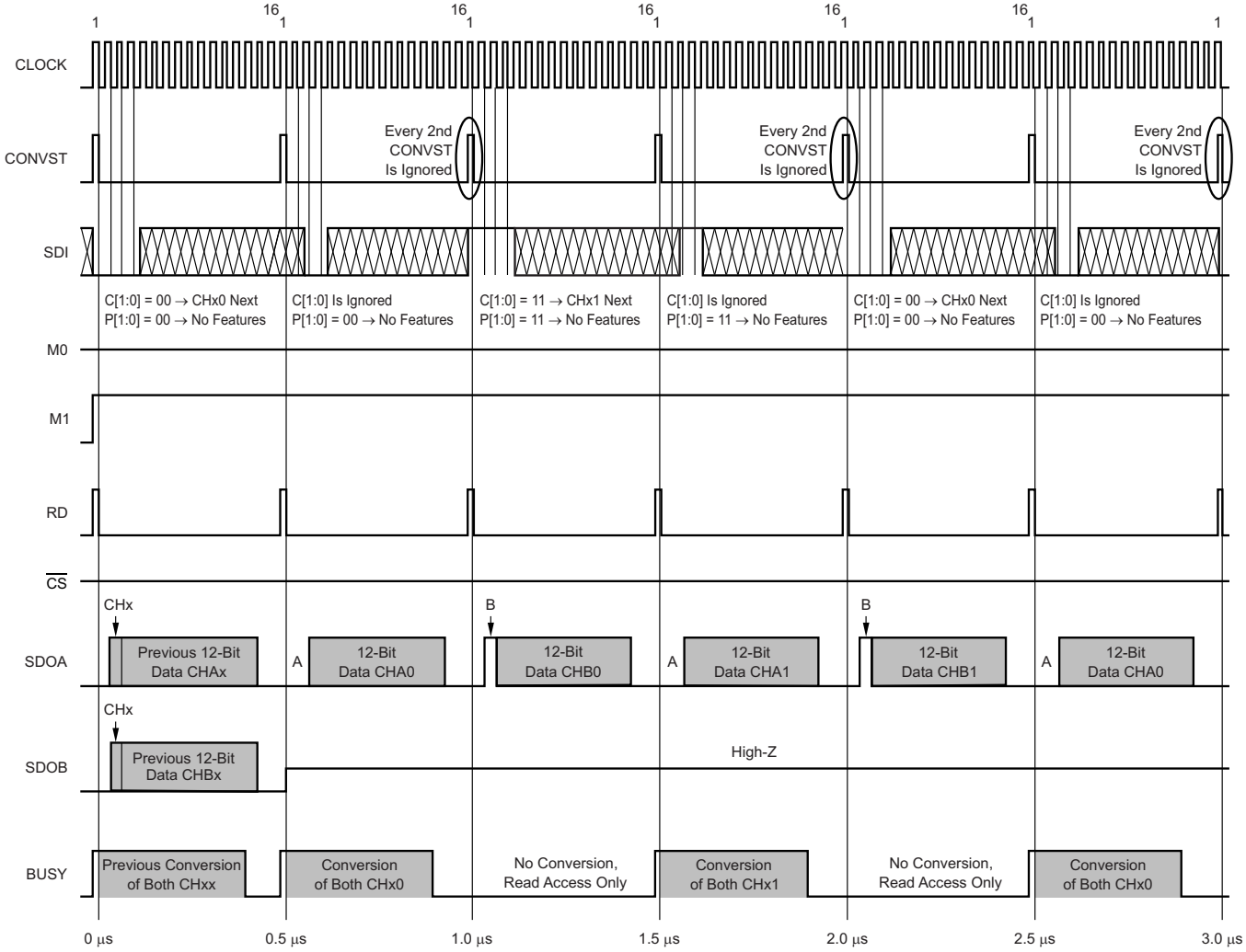


Figure 34. Mode II Timing Diagram (M0 = 0, M1 = 1)

Mode III

With M0 = 1 and M1 = 0, the device automatically cycles between the differential inputs (ignoring the SDI register bits C[1:0]) while offering the conversion result of CHAx on SDOA and the conversion result of CHBx on SDOB (as shown in Figure 35).

Output data consist of a channel indicator ('0' for CHx0 or '1' for CHx1), followed by a '0', 12 bits of conversion results, and another '00'.

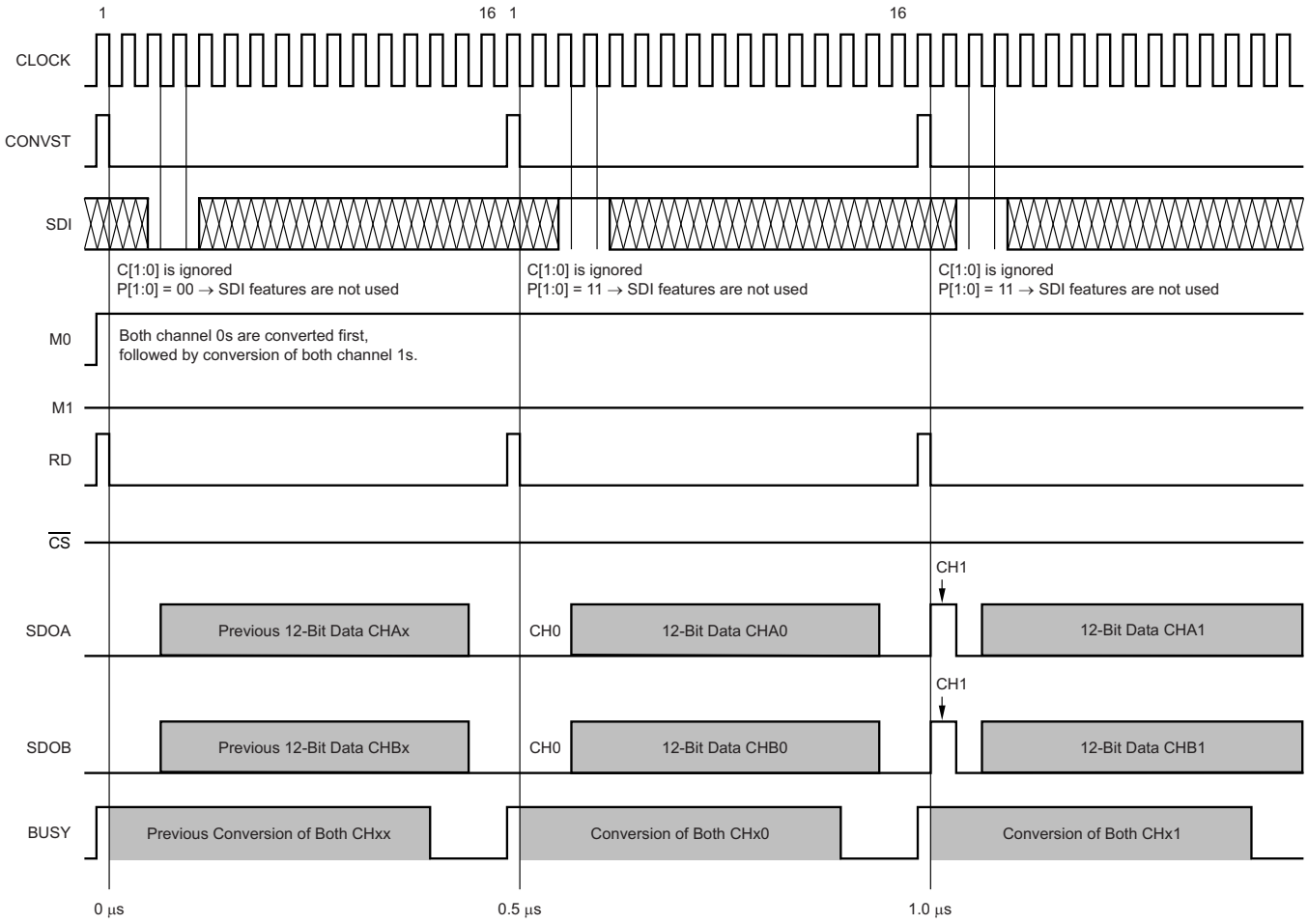


Figure 35. Mode III Timing Diagram (M0 = 1, M1 = 0)

Mode IV

In the same way as Mode II, Mode IV uses the SDOA output line exclusively to transmit data while the differential channels are switched automatically. Following the first conversion after M1 goes high, the SDOB output 3-states (as shown in Figure 36).

Output data consist of a channel indicator ('0' for CHx0 or '1' for CHx1), followed by the ADC indicator ('0' for CHAx or '1' for CHBx), 12 bits of conversion results, and end with '00'.

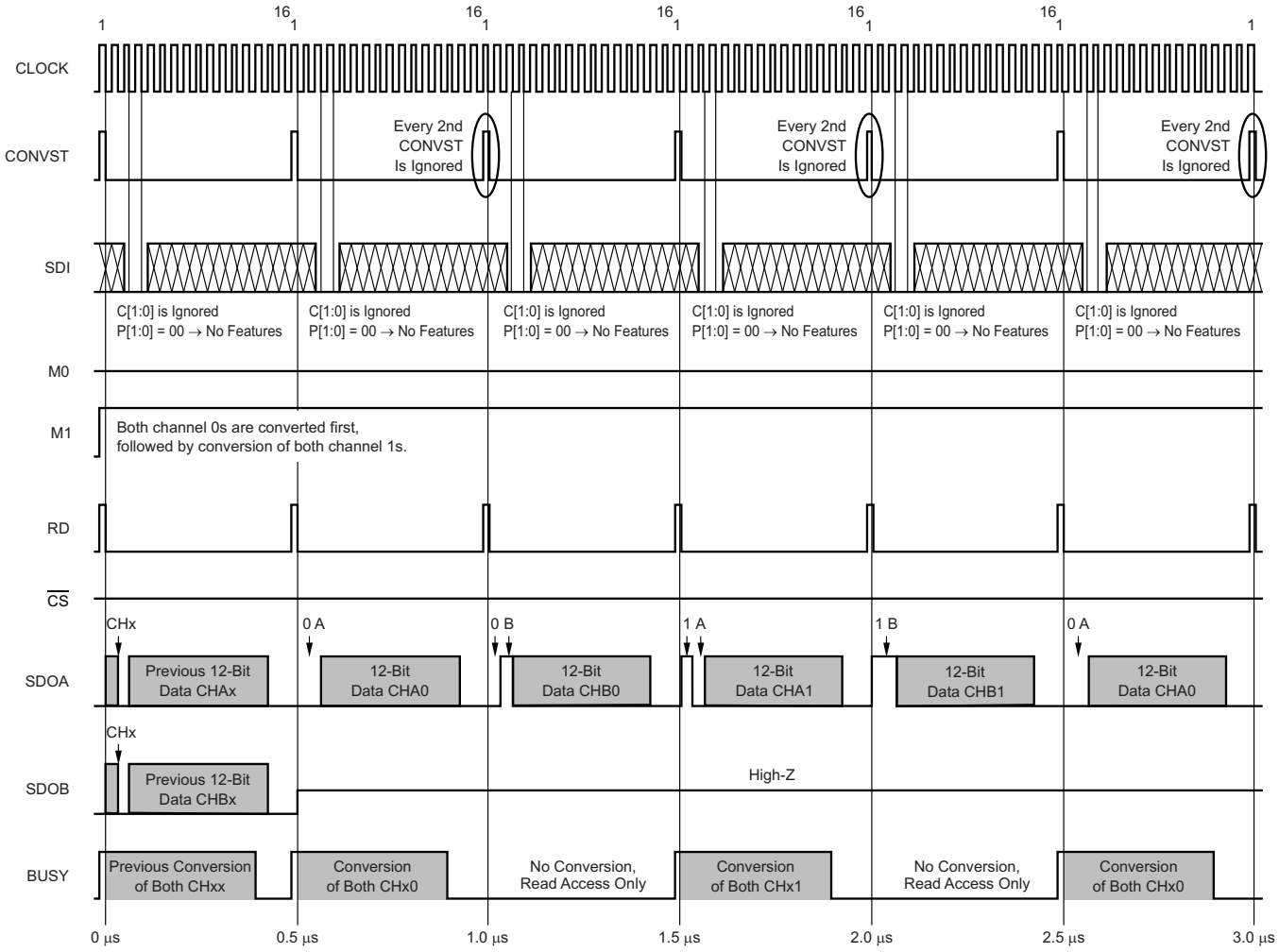


Figure 36. Mode IV Timing Diagram (M0 = 1, M1 = 1)

Special Mode II (Not ADS7861-Compatible)

For Mode II, a special read mode is available in the ADS7863A where both data results can be read out, triggered by a single RD pulse. To activate this mode, bit S4 in the SDI register must be set to '1' (see also the *Serial Data Input* section).

The CONVST and RD pins can remain tied together, but do not need to be issued every 16 CLOCK cycles. Output data are presented on both terminals, SDOA and SDOB. Figure 37 illustrates the special read mode.

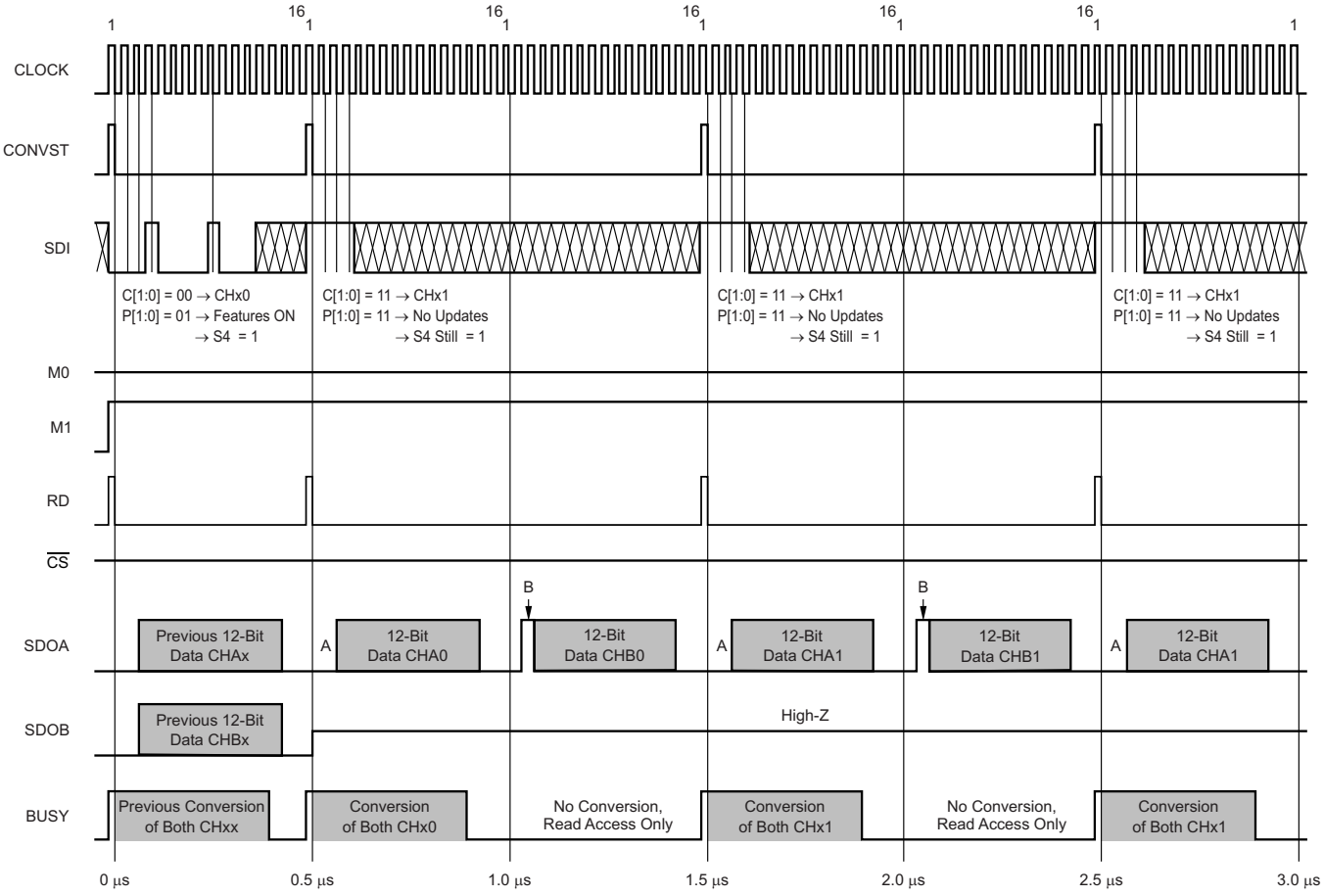


Figure 37. Special Mode II Timing Diagram (M0 = 0, M1 = 1, S4 = 1)

Special Mode IV (Not ADS7861-Compatible)

Analogous to Special Mode II, the device also offers a special read mode for Mode IV in which both data results of a conversion can be read, triggered by a single RD pulse. In this case as well, bit S4 in the SDI register must be set to '1' while the CONVST and RD pins can still be tied together .

As with Special Mode II, these two pins do not need to be issued every 16 CLOCK cycles. Data are available on the SDOA pin.

This special read mode (shown in Figure 38) is not available in Mode I or Mode III.

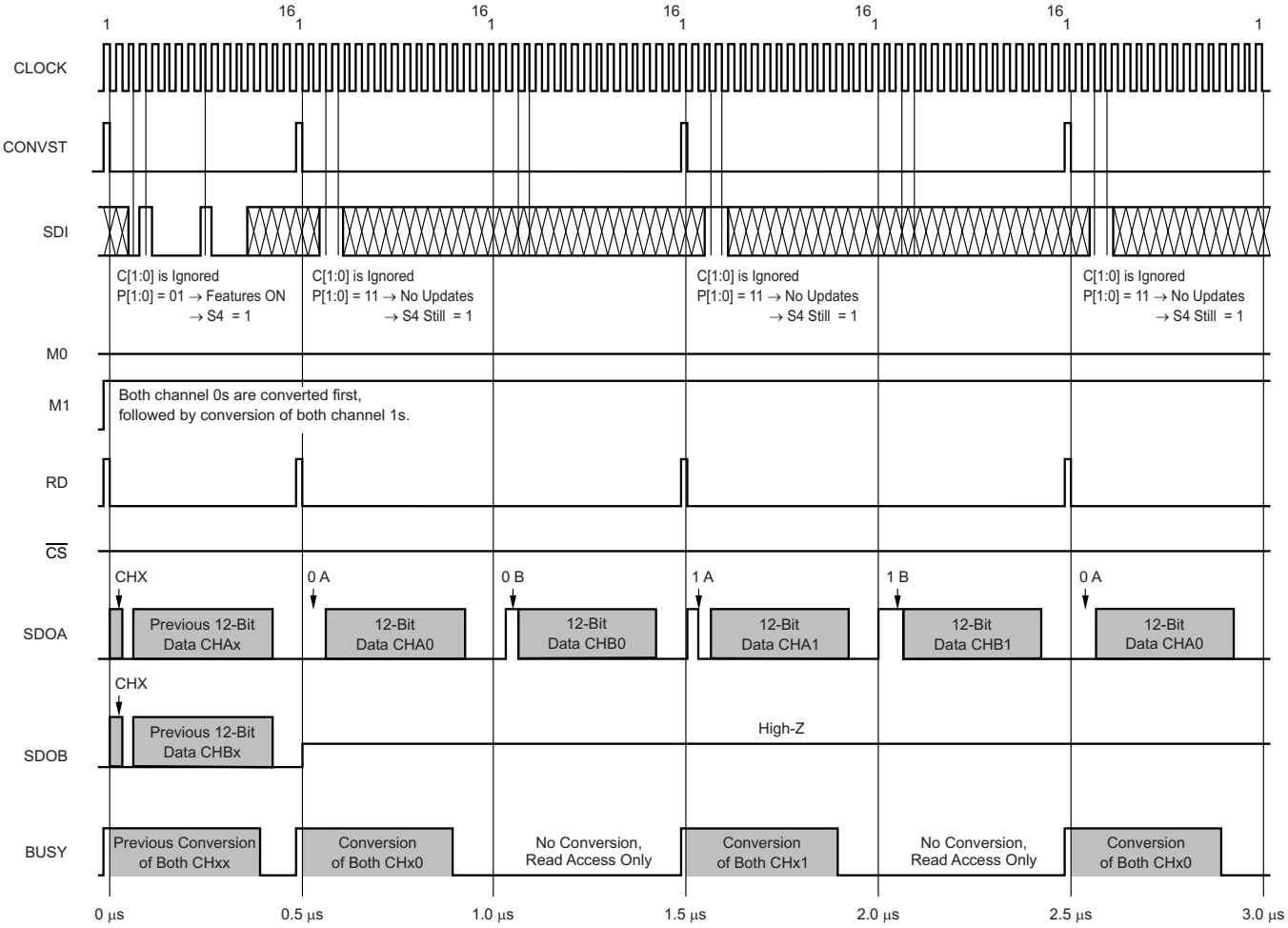


Figure 38. Special Mode IV Timing Diagram (M0 = 1, M1 = 1, S4 = 1)

Pseudo-Differential Mode I (Not ADS7861-Compatible)

In Mode I, the device input multiplexers can also operate in a pseudo-differential manner. In this case, the SDI bits (C[1:0]) are used to choose the channels accordingly.

For more details, see the *Serial Data Input* section. Data are available on both output terminals, SDOA and SDOB.

The input multiplexer cannot be used for pseudo-differential signals in Mode III or Mode IV.

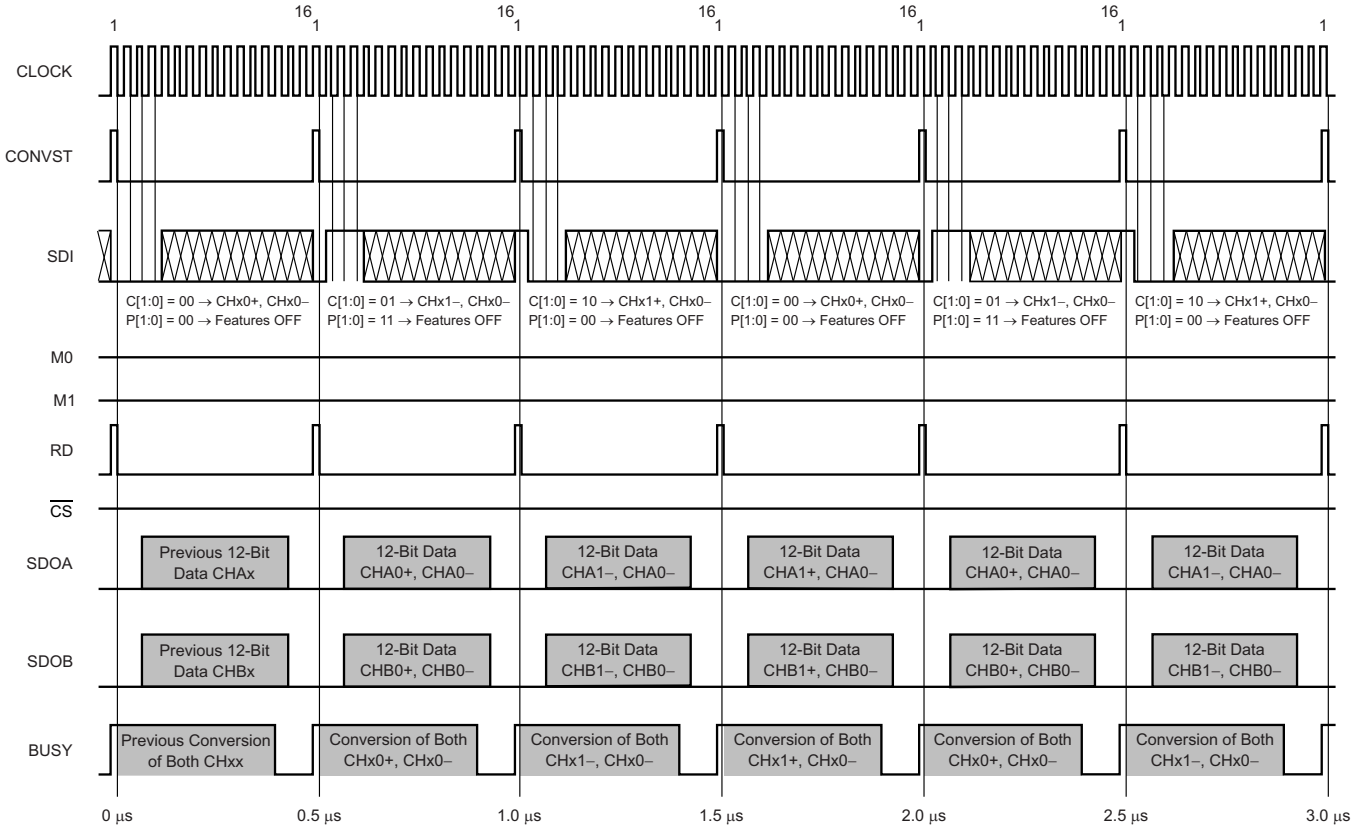


Figure 39. Pseudo-Differential Mode I (M0 = 0, M1 = 0)

Pseudo-Differential Mode II (Not ADS7861-Compatible)

In Mode II, the device input multiplexers can also operate in a pseudo-differential configuration. In this case, output data are available on terminal SDOA only, while SDOB is held in 3-state.

Channel switching is performed by setting the C[1:0] bits in the SDI register accordingly (see also the *Serial Data Input* section).

The input multiplexer cannot be used for pseudo-differential signals in Mode III or Mode IV.

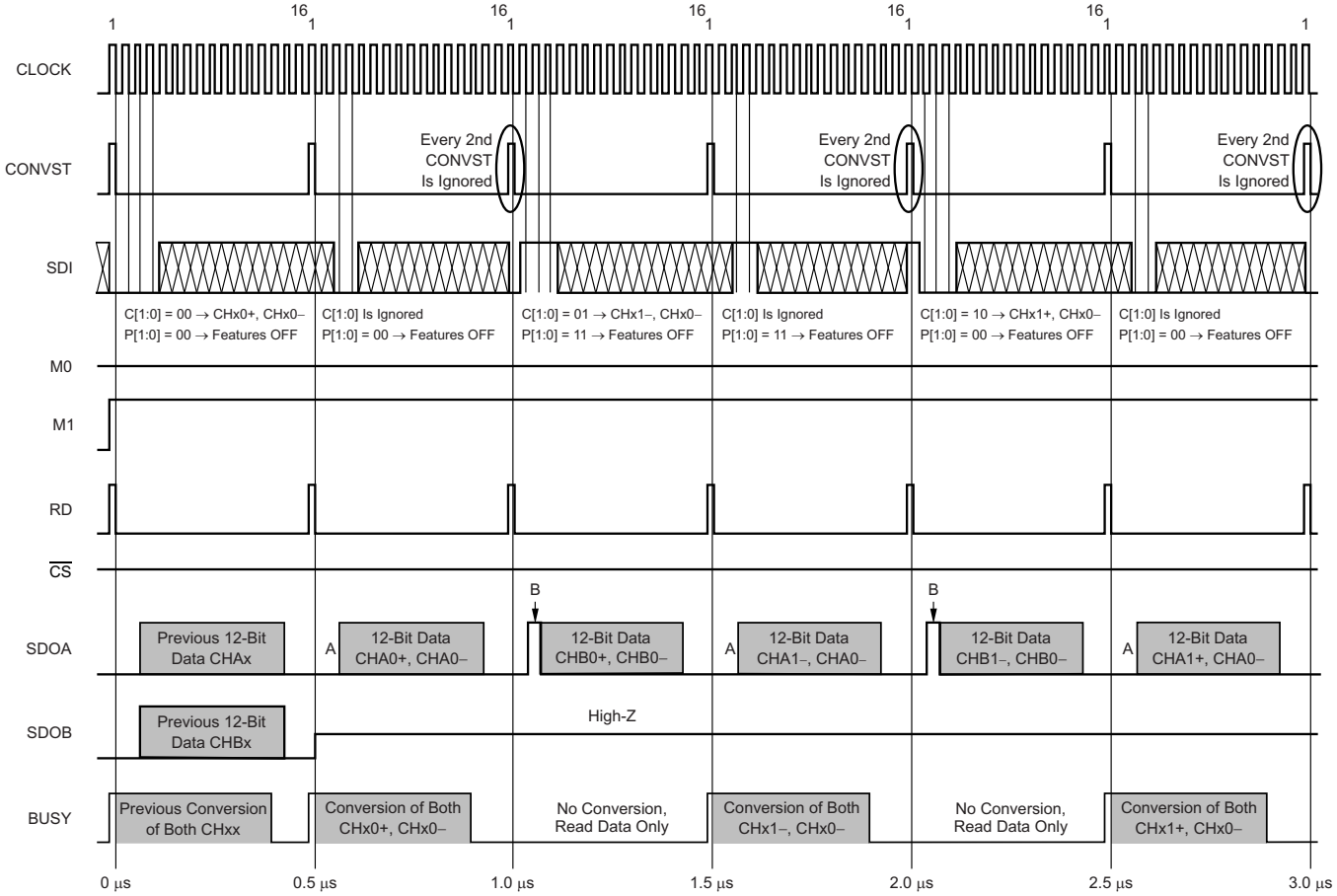


Figure 40. Pseudo-Differential Mode II (M0 = 0, M1 = 1)

Programming the Reference DAC (Not ADS7861-Compatible)

The internal reference DAC can be set by issuing an RD pulse while providing an SDI word with P[1:0] = 01 and A[2:0] = 001. Thereafter, a second RD pulse must be generated with an SDI word starting with the first two bits ignored, followed by the actual 10-bit DAC value (as shown in Figure 41).

To verify the DAC setting, an RD pulse must be generated while providing an SDI word containing P[1:0] = 01 and A[2:0] = 011 to initialize the DAC read access. Triggering the RD line again causes the SDOA output to send '0000' followed by the 10-bit DAC value and another '00'. During the second RD access, data present on SDI are ignored, while in Mode I and Mode III valid conversion data for channel B are present on SDOB; the conversion results of channel A are lost. The default value of the DAC register after power-up is 3FFh, corresponding to a 2.5-V reference voltage on the REF_{OUT} pin.

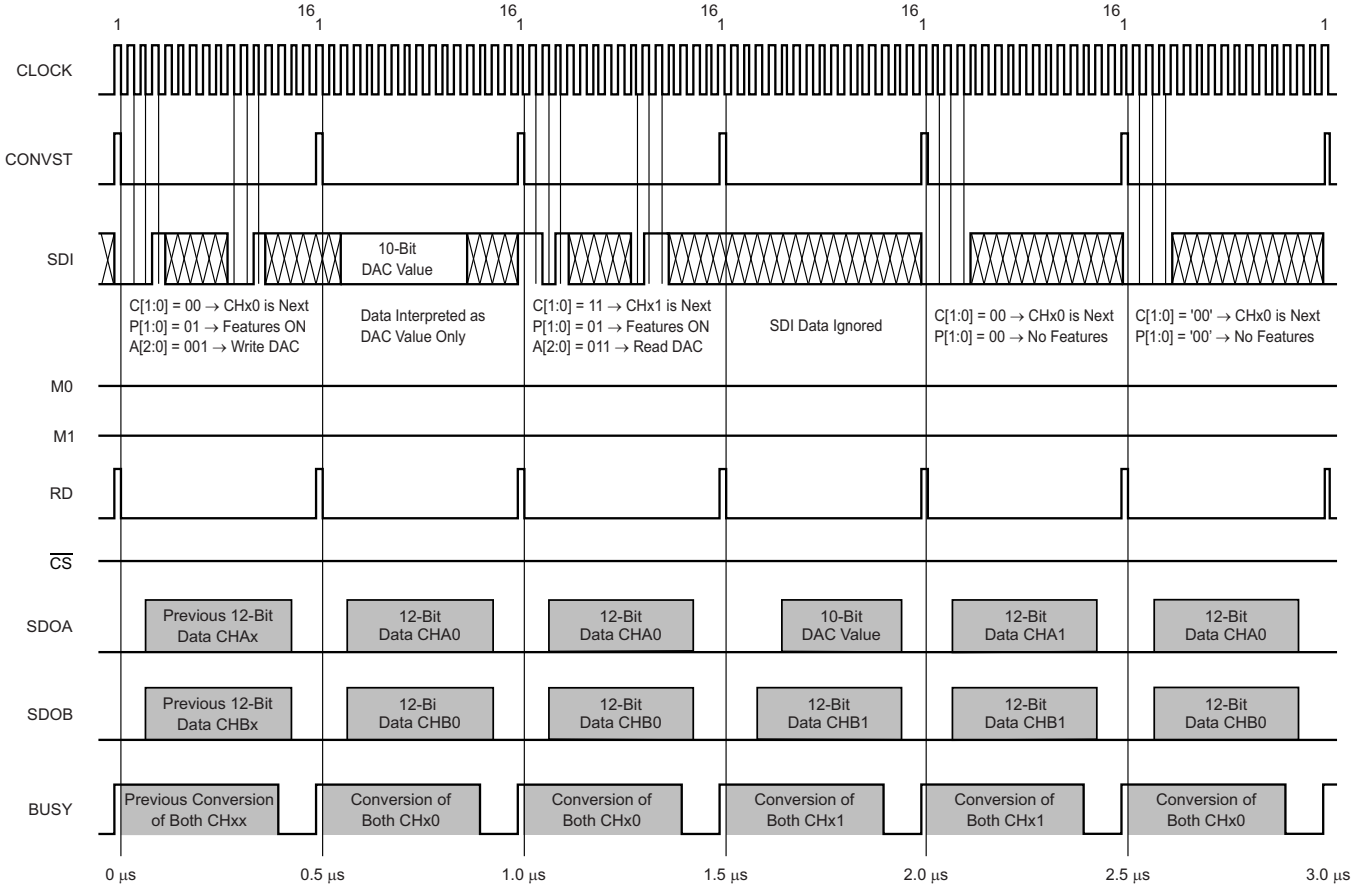


Figure 41. DAC Write and Read Access Timing Diagram

Power-Down Modes and Reset (Not ADS7861-Compatible)

The device has a comprehensive built-in power-down feature. There are three power-down modes: deep power-down, NAP power-down, and auto-NAP power-down. All three power-down modes are activated with the 12th falling CLOCK edge of the SDI access, during which the related bit asserts (DP = 1, N = 1, or AN = 1). All modes are deactivated by de-asserting the respective bit in the SDI register. The SDI register contents are not affected by the power-down modes. Any ongoing conversion aborts when deep or NAP power-down is initiated. Table 10 lists the differences among the three power-down modes.

In *deep power-down mode*, all functional blocks except the digital interface are disabled. The bias currents of the analog block are turned off. In this mode, power dissipation reduces to 1 µA within 2 µs. The wake-up time from deep power-down mode is 1 µs.

In *NAP power-down mode*, the device turns off the biasing of the comparator and the mid-voltage buffer within 200 ns. The device goes into NAP power-down mode regardless of the conversion state.

The *auto-NAP power-down mode* is very similar to NAP mode. The only differences are the methods of powering down and waking up the device. The SDI register bit AN is only used to enable or disable this feature. If the auto-NAP mode is enabled, the device turns off the biasing automatically after finishing a conversion; thus, the end of conversion actually activates the auto-NAP power-down. The device powers down within 200 ns in this mode, as well. Triggering a new conversion by applying a CONVST pulse puts the device back into normal operation and automatically starts a new conversion six CLOCK cycles later. Therefore, a complete conversion cycle takes 19 CLOCK cycles; thus, the maximum throughput rate in auto-NAP power-down mode is reduced to 1.68 MSPS.

To issue a *device reset*, an RD pulse must be generated along with an SDI word containing A[2:0] = 101. With the 12th falling edge after generating the RD pulse, the entire device (including the serial interface) is forced into reset. After approximately 500 ns, the serial interface becomes active again.

Table 10. Power-Down Modes

POWER-DOWN TYPE	ENABLED BY	ACTIVATED BY	ACTIVATION TIME	RESUMED BY	REACTIVATION TIME	DISABLED BY
Deep	DP = 1	13th clock	2µs	DP = 0	1 µs	DP = 0
NAP	N = 1	13th clock	200ns	N = 0	3 clocks	N = 0
Auto-NAP	AN = 1	Each end of conversion	200ns	CONVST pulse	3 clocks	AN = 0

ADS7861 COMPATIBILITY

The ADS7863AIDBQ is pin-compatible with the ADS7861E, ADS7861EB, and ADS7861EG4. However, there are some differences between the two devices that must be considered when migrating from the ADS7861 to the ADS7863A in an existing design.

SDI versus A0

One of the differences is that pin 16 (A0), which updates the internal SDI register of the ADS7863A, is used in conjunction with M0 to select the input channel on the ADS7861.

In an existing design, if the ADS7861 is used in two-channel mode (M0 = 0) and the status of the A0 pin is unchanged within the first four clock cycles after issuing a conversion start (CONVST rising edge), the ADS7863A acts similarly to the ADS7861 and converts either channels CHx0 (if SDI is held low during the entire period) or channels CHx1 (if SDI is held high during the entire period). Figure 34 describes the behavior of the ADS7863A in such a situation.

The ADS7863A can also be used to replace the ADS7861 when run in four-channel mode (M0 = 1). In this case, the A0 pin is held static (high or low) which is also required in the case of SDI to prevent accidentally updating the SDI register.

In both cases, the additional features of the ADS7863A (pseudo-differential input mode, programmable reference voltage output, and the different power-down modes) cannot be accessed but the hardware and software remain backward-compatible to the ADS7861.

REF_{IN}

The ADS7863A offers an unbuffered REF_{IN} input with a code-dependent input impedance while featuring a programmable and buffered reference output (REF_{OUT}). The ADS7861 offers a high-impedance (buffered) reference input. If an existing ADS7861-based design uses the internal reference of the device and relies on an external resistor divider to adjust the input voltage range of the ADC, migration to ADS7863A requires one of the following conditions:

- a software change to setup the internal reference DAC properly via SDI while removing the external resistors, or
- an additional external buffer between the resistor divider and the required 470-nF (minimum) capacitor on the REF_{IN} input.

In the latter case, while the capacitor stabilizes the reference voltage during the entire conversion, the buffer must recharge the capacitor by providing an average current only. The required minimum bandwidth of the buffer can be calculated using Equation 2:

$$f_{-3dB} = \frac{\ln(2) \times 2}{2\pi \times 16 \times T_{CLK}} \quad (2)$$

The buffer must also be capable of driving the 470-nF load while maintaining stability.

Timing

The only timing requirement that may cause the ADS7863A to malfunction in an existing ADS7861-based design is the CONVST high time (t_1) which is specified to be 20 ns minimum while the ADS7861 works properly with a pulse as short as 15 ns. All other required minimum setup and hold times are specified to be either the same as or lower than the ADS7863A; therefore, there are no conflicts with the ADS7861 requirements.

APPLICATION INFORMATION

The absolute minimum configuration of the ADS7863A is shown in Figure 42. In this case, the ADS7863A is used in dual-channel mode only, with the default settings of the device after power up.

The input signal for the amplifiers must fulfill the common-mode voltage requirements of the ADS7863A in this configuration. The actual values of the resistors and capacitors depend on the bandwidth and performance requirements of the application.

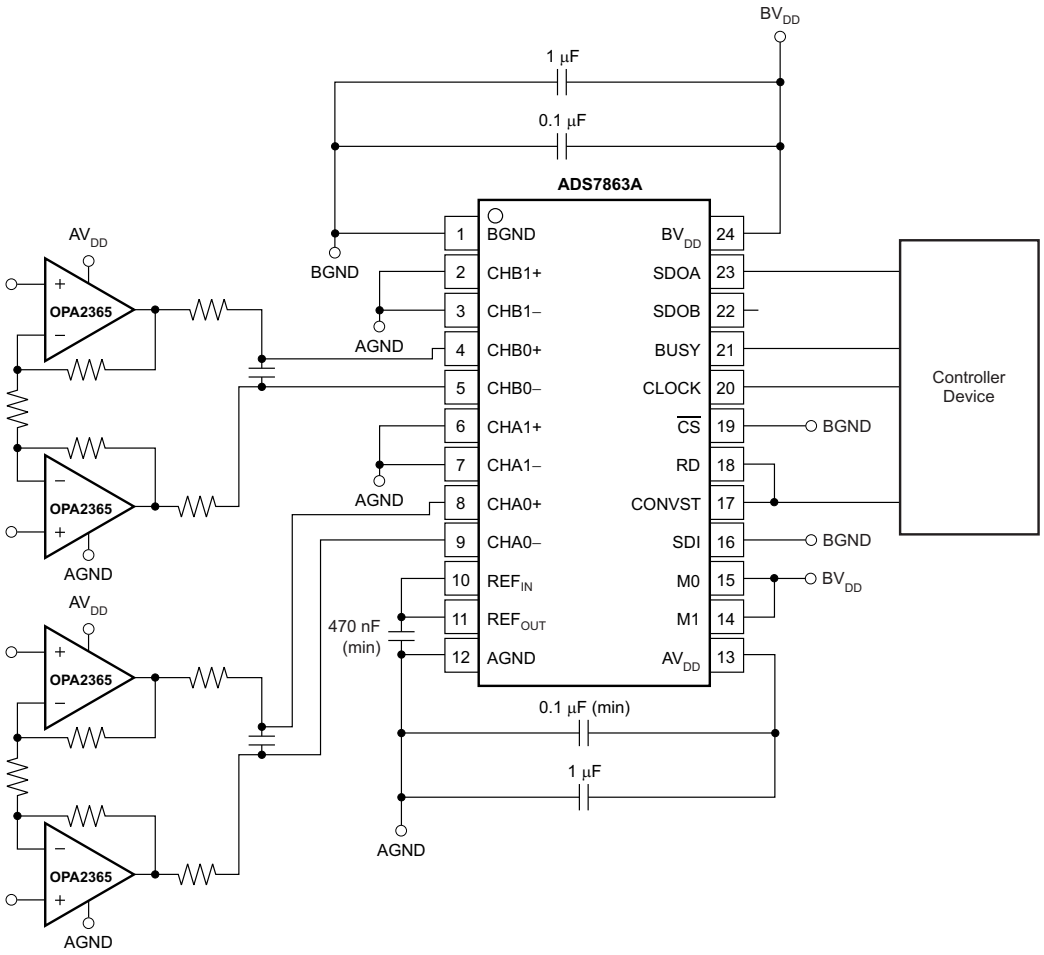


Figure 42. Minimum ADS7863A Configuration

These values can be calculated using Equation 3, with n = 12 is the device resolution of the ADS7863A.

$$f_{FILTER} = \frac{\ln(2) \times (n + 1)}{2 \times \pi \times 2 \times R \times C} \quad (3)$$

where:

- n = 12 is the resolution of the ADS7863A

TI recommends using a capacitor value of at least 20 pF.

Keep the acquisition time in mind; the resistor value can be calculated as shown in Equation 4 for each of the series resistors.

$$R = \frac{t_{ACQ}}{\ln(2) \times (n + 1) \times 2 \times C} \quad (4)$$

where:

- n = 12 is the resolution of the ADS7863A

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7863A circuitry. This condition is particularly true if the CLOCK input is approaching the maximum throughput rate. In this case, TI recommends having a fixed phase relationship between CLOCK and CONVST. Best performance can be achieved when the digital interface is run in SPI mode; thus, the CLOCK signal is switched off after the 16th cycle and remains low when CONVST is issued.

Additionally, the basic SAR architecture is quite sensitive to glitches or sudden changes on the power-supply, reference, ground connections, and digital inputs that occur just before latching the output of the analog comparator. Therefore, when driving any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. These errors can change if the external event also changes in time with respect to the CLOCK input.

With this possibility in mind, power to the device should be clean and well-bypassed. A 0.1-µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1-µF to 10-µF capacitor is recommended. If needed, an even larger capacitor and a 5-Ω or 10-Ω series resistor may be used to low-pass filter a noisy supply.

If the reference voltage is external and originates from an operational amplifier, be sure that the reference voltage can drive the reference capacitor without oscillation. The connection between the output of the external reference driver and REF_{IN} should be of low resistance (10 Ω max) to minimize any code-dependent voltage drop on this path.

Grounding

The xGND pins should be connected to a clean ground reference. These connections should be kept as short as possible to minimize the inductance of these paths. TI recommends using vias connecting the pads directly to the ground plane. In designs without ground planes, the ground trace should be kept as wide as possible. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor (DSP).

Depending on the circuit density of the board, placement of the analog and digital components, and the related current loops, a single solid ground plane for the entire printed circuit board (PCB) or a dedicated analog ground area may be used. In an instance of a separated analog ground area, ensure a low-impedance connection between the analog and digital ground of the ADC by placing a bridge underneath (or next to) the ADC. Otherwise, even short undershoots on the digital interface with a value lower than –300 mV lead to conduction of ESD diodes, causing current flow through the substrate and degrading the analog performance.

During PCB layout, care should also be taken to avoid any return currents crossing any sensitive analog areas or signals. No signal must exceed the limit of –300 mV with respect to the according ground plane. Figure 43 illustrates the recommended layout of the ground and power-supply connections for both package options.

Supply

The ADS7863A has two separate supplies: the BV_{DD} pin for the digital interface and the AV_{DD} pin for all remaining circuits.

BV_{DD} can range from 2.7 V to 5.5 V, allowing the device to easily interface with processors and controllers. To limit the injection of noise energy from external digital circuitry, BV_{DD} should be filtered properly. Bypass capacitors of 0.1 µF and 10 µF should be placed between the BV_{DD} pin and ground plane.

AV_{DD} supplies the internal analog circuitry. For optimum performance, a linear regulator (for example, the UA7805 family) is recommended to generate the analog supply voltage in the range of 2.7 V to 5.5 V for the ADS7863A and the necessary analog front-end circuitry.

Bypass capacitors should be connected to the ground plane such that the current is allowed to flow through the pad of the capacitor (that is, the vias should be placed on the opposite side of the connection between the capacitor and the power-supply pin of the ADC).

Digital Interface

To further optimize device performance, a resistor of 10 Ω to 100 Ω can be used on each digital pin of the ADS7863A. In this way, the slew rate of the input and output signals is reduced, limiting the noise injection from the digital interface.

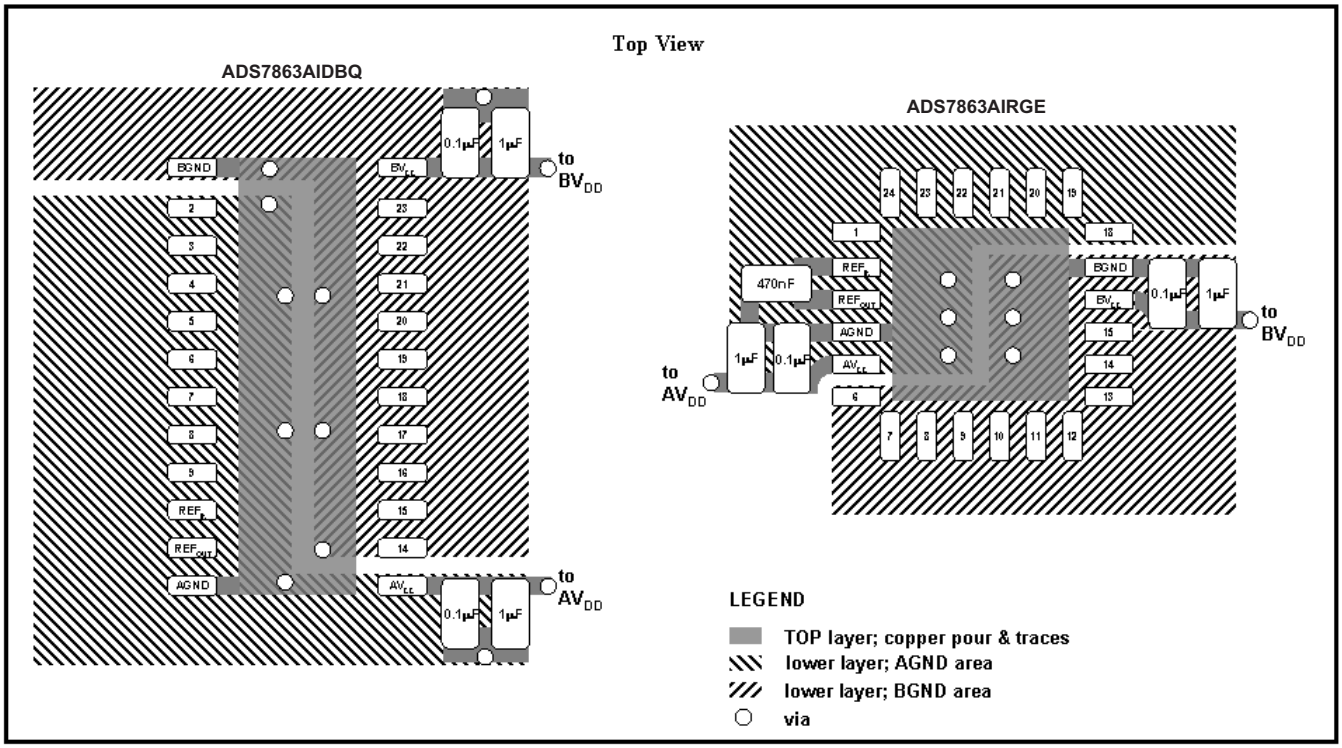


Figure 43. Optimized Layout Recommendation

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7863ADBQ	ACTIVE	SSOP	DBQ	24	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS7863A	Samples
ADS7863ADBQR	ACTIVE	SSOP	DBQ	24	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS7863A	Samples
ADS7863ARGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7863A	Samples
ADS7863ARGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS 7863A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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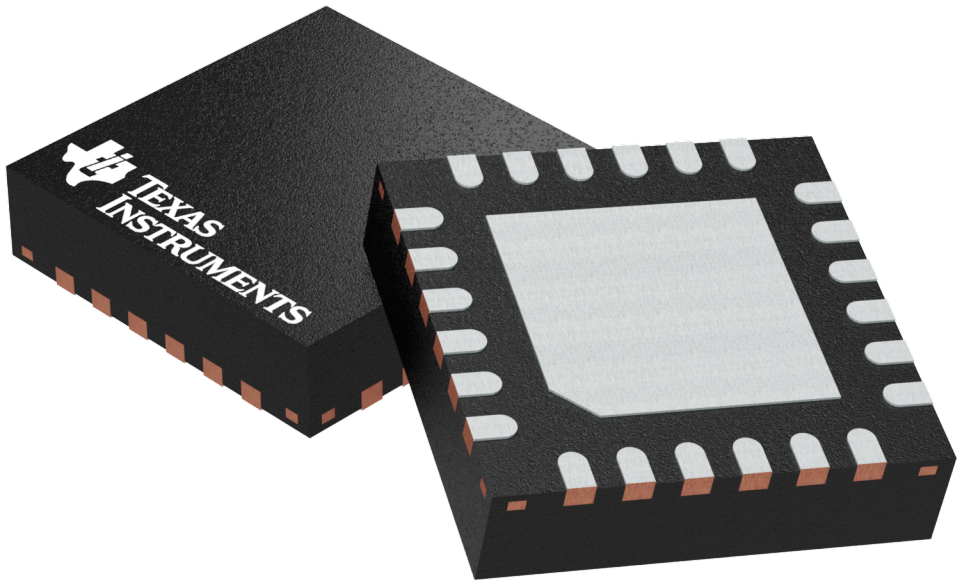
GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

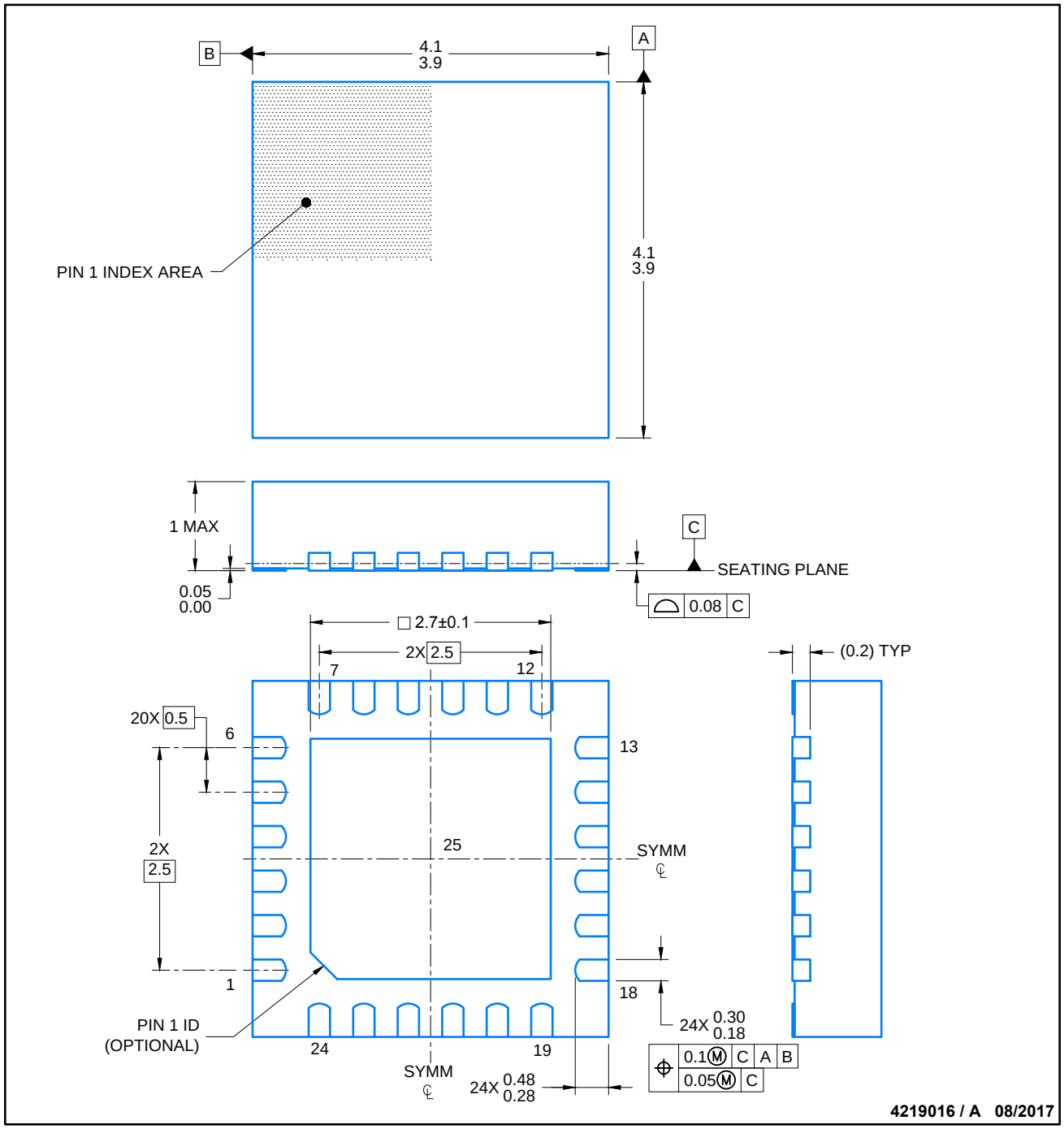
4204104/H

PACKAGE OUTLINE

RGE0024H

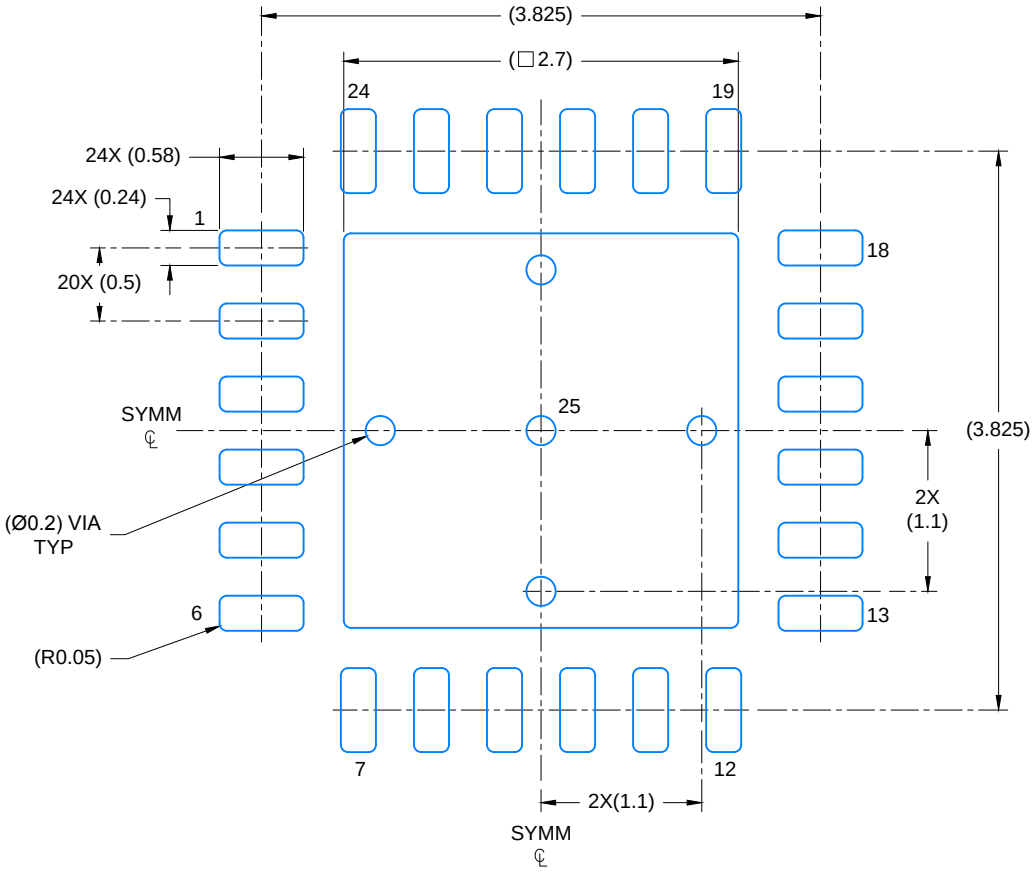
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



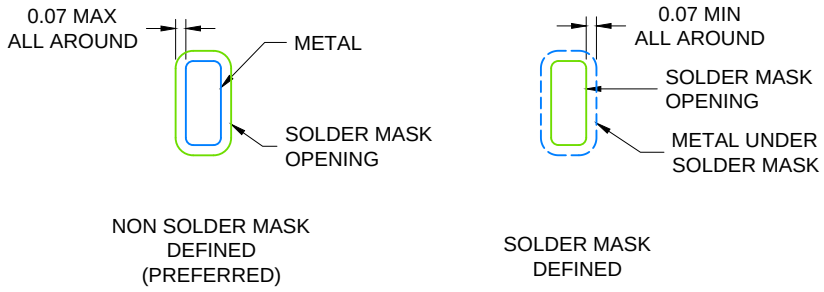
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

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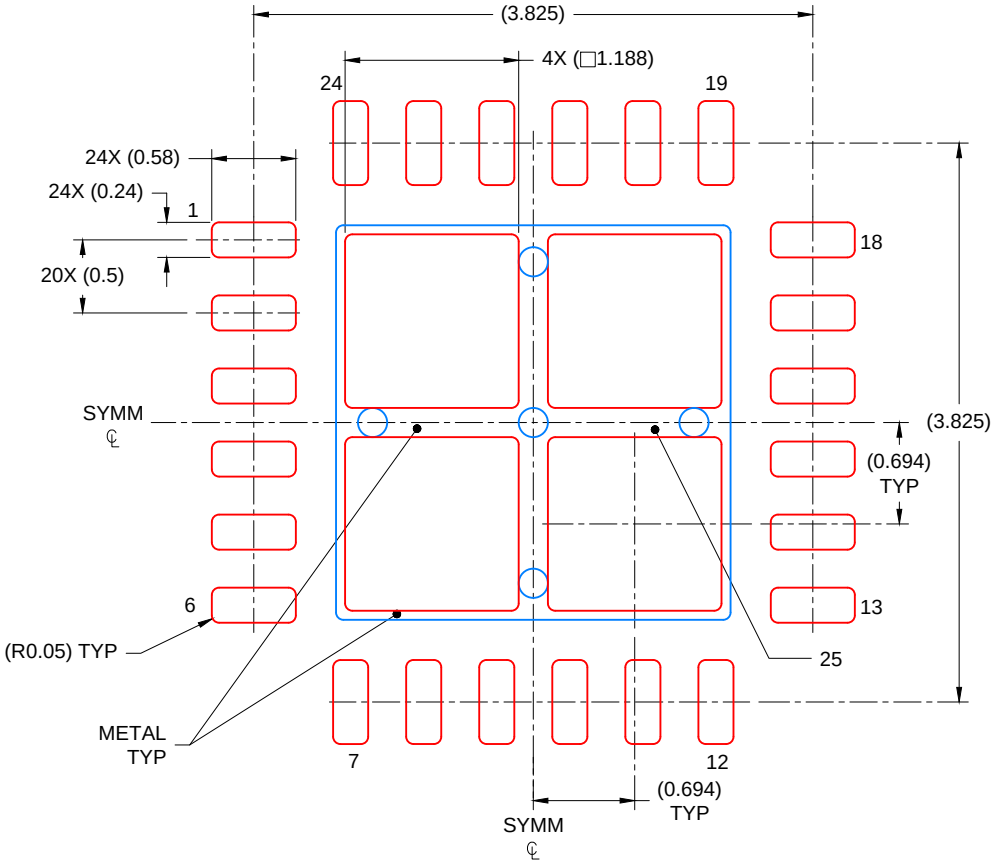
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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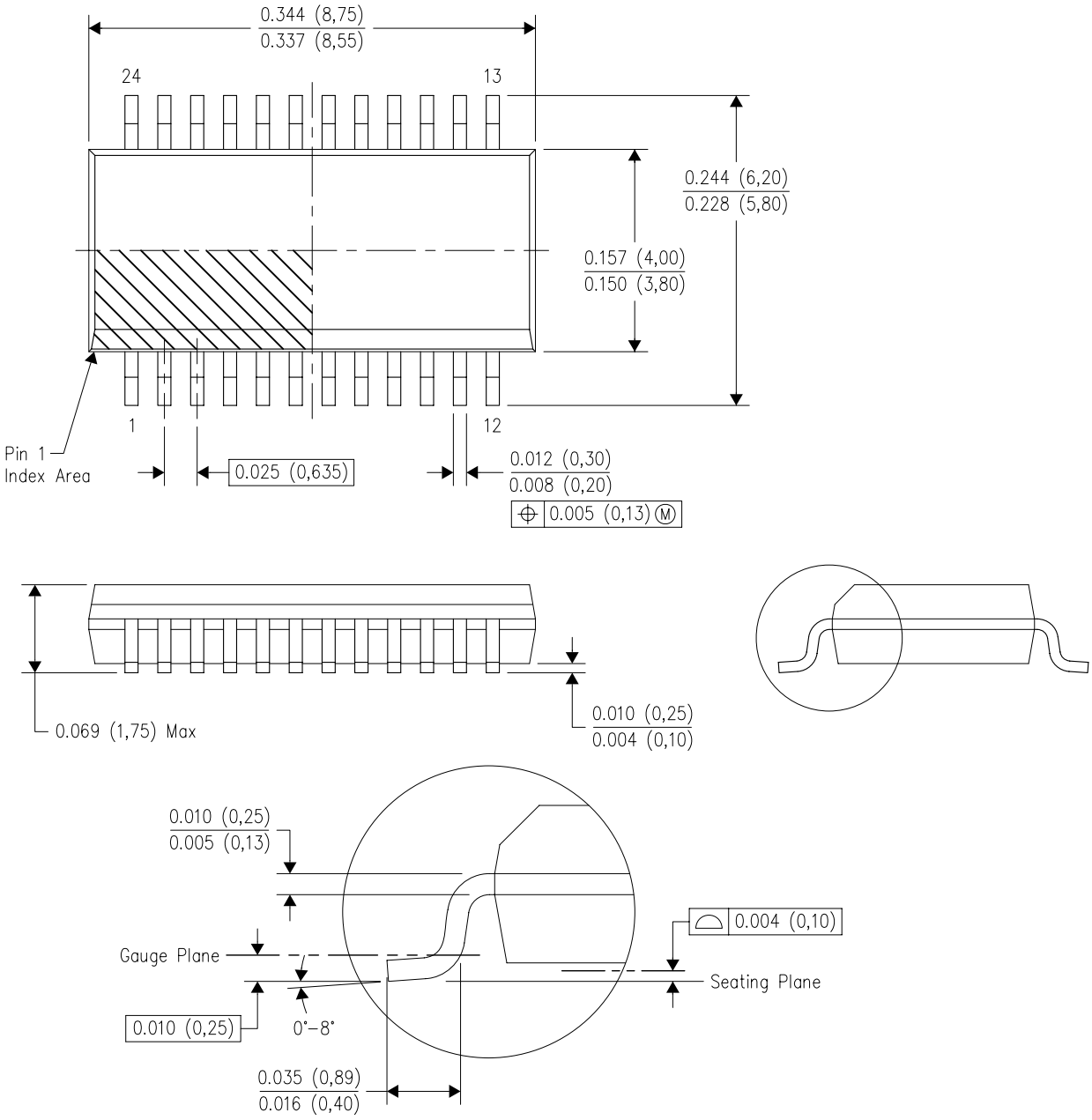
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

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