AMC80 具有双线制和 SMBus 串行接口的系统硬件监控器

1 特性

- 具有七个模拟输入的 10 位模数转换器 (ADC)
- 风扇转速监控输入
- 输入范围/分辨率：
  - 默认值：2.56V/2.5mV
  - 可编程：V_{DD}/6mV
- 机箱入侵检测输入
- 中断报警：
  - 上限
  - 下限值
- 外部温度传感器的中断状态寄存器输入
- 关断模式
- 可编程 $\overline{\text{RST\_OUT}}/\overline{\text{OS}}$
- 与 LM96080 和 LM80 引脚兼容
- 封装：24 引脚薄型小外形尺寸 (TSSOP)

2 应用

- 通信设备
- 服务器
- 工业用和医疗用设备
- 存储区域网络
- 机顶盒
- 测试和测量仪器

3 说明

AMC80 是一款系统硬件监控和控制电路，其中包括一个七通道 10 位模数转换器 (ADC)、两个可编程风扇转速监控器和一个双线制接口。AMC80 还具有可编程上限值及下限值报警功能。当超出编程设定的限值后，该报警即启动。

AMC80 可与线性温度传感器和数字温度传感器相连。凭借 2.5mV 最低有效位 (LSB) 和 2.56V 输入范围，该器件可接收线性传感器（例如 TMP20）的输入。$\overline{\text{BTI}}$ 引脚用作数字传感器（例如 TMP75）的输入。AMC80 可由电压介于 3V 至 5.5V 范围内的电源供电运行，其电源电流较低并可通过双线制接口配置，因此适用于各类 集成电机驱动器解决方案。。

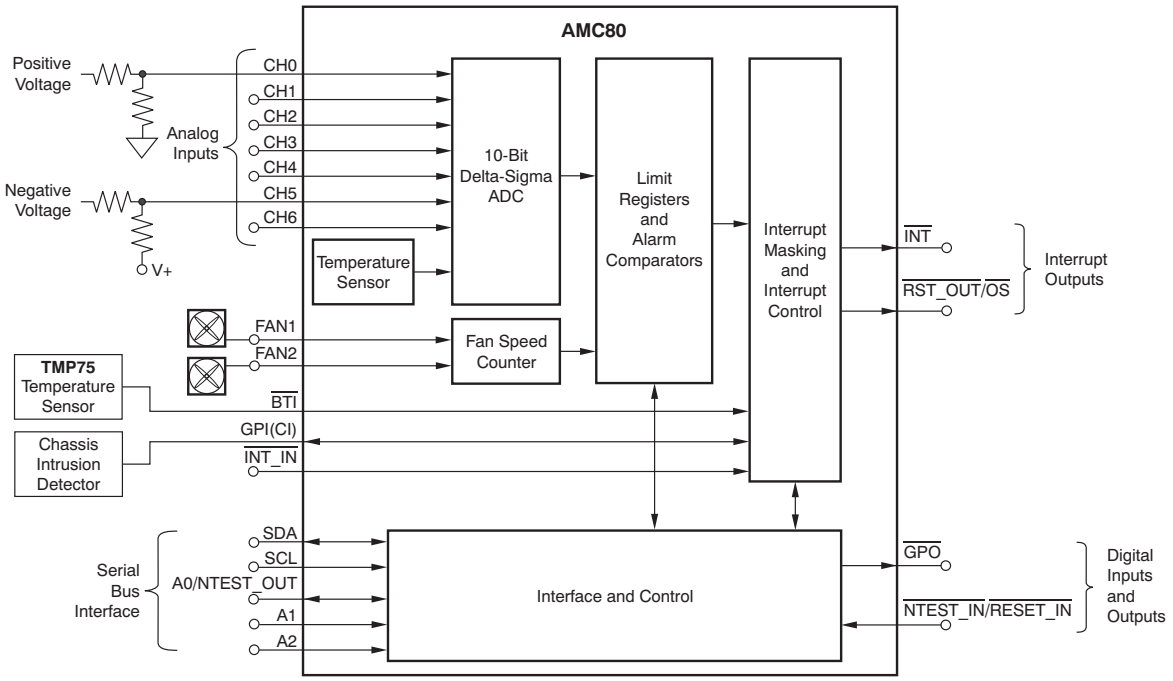
AMC80 采用 24 引脚 TSSOP 封装，可在 –40°C 至 +125°C 的温度范围内完全额定运行。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
AMC80	TSSOP (24)	7.80mm × 4.40mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。

简化电路原理图



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4 修订历史记录

Changes from Revision A (January 2012) to Revision B **Page**

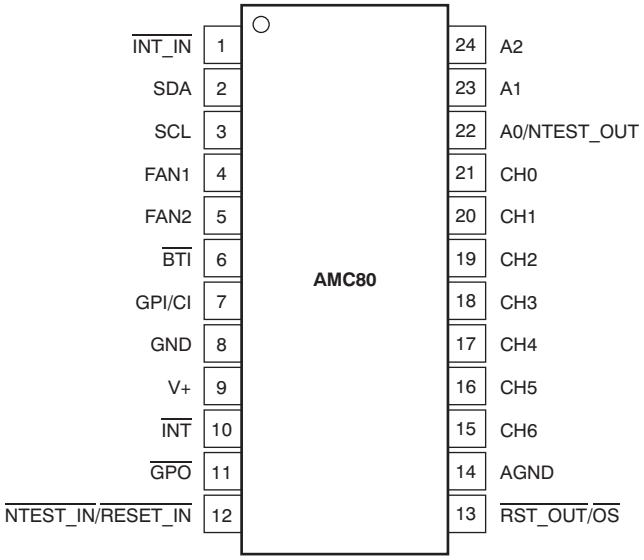
- Changed INT pin description 4
- Added pins to input voltage range in *Absolute Maximum Ratings* table 5
- Added *ESD Ratings* table 5
- Added new note 1 to *Timing Requirements* table 8
- Added *Detailed Description* section 10
- Added *Application and Implementation* section 21
- 已添加*器件和文档支持*章节 23

Changes from Original (May 2011) to Revision A **Page**

- Added SMBus timeout parameter to Electrical Characteristics 6
- Changed Bit 0 = '1' in Table 10 18

5 Pin Configuration and Functions

PW Package
24-Pin TSSOP
Top View



Pin Functions

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	$\overline{\text{INT\_IN}}$	Input	Digital	Interrupt input pin. An active low input that extends the $\overline{\text{INT\_IN}}$ signal to the $\overline{\text{INT}}$ output of the AMC80.
2	SDA	I/O	Digital	Serial bus data line for SMBus, open-drain; requires pull-up resistor.
3	SCL	I/O	Digital	Serial bus clock line for SMBus, open-drain; requires pull-up resistor.
4	FAN1	Input	Digital	Fan tachometer input pin
5	FAN2	Input	Digital	Fan tachometer input pin
6	$\overline{\text{BTI}}$	Input	Digital	Board temperature interrupt pin. $\overline{\text{BTI}}$ is driven by the over-temperature shutdown (OS) outputs of the additional temperature sensors. This pin has an internal 10-kΩ pull-up resistor.
7	GPI(CI)	Input	Digital	General-purpose input pin (chassis interrupt). An active high interrupt input pin to latch a chassis interrupt event.
8	DGND	Power	Analog	Digital ground.
9	V+	Power	Analog	Positive supply voltage (3V to 5.5V).
10	$\overline{\text{INT}}$	Output	Digital	Non-maskable interrupt (active high, PMOS, push-pull) or interrupt request (active low, NMOS, push-pull) pin. The $\overline{\text{INT}}$ pin becomes active when $\overline{\text{INT\_IN}}$, $\overline{\text{BTI}}$, or GPI interrupts. This pin does not require a pullup resistor to V+.
11	$\overline{\text{GPO}}$	Output	Digital	General-purpose output pin. $\overline{\text{GPO}}$ is an active low, NMOS, open-drain output. This pin is intended to drive an external power PMOS for software power control or to control power to a cooling fan.
12	$\overline{\text{NTEST\_IN}}$/$\overline{\text{RESET\_IN}}$	Input	Digital	This pin is an active-low input that enables NAND tree board-level connectivity testing. The AMC80 resets to its power-on state when NAND tree connectivity is enabled.
13	$\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$	Output	Digital	This pin is an NMOS open-drain output. $\overline{\text{RST\_OUT}}$ provides a master reset to devices connected to this line. $\overline{\text{OS}}$ is dedicated to the temperature reading alarm.
14	AGND	Power	Analog	Analog ground. This pin must be tied to a low-noise analog ground plane for optimum performance.
15	CH6	Input	Analog	Analog input channel 6
16	CH5	Input	Analog	Analog input channel 5
17	CH4	Input	Analog	Analog input channel 4
18	CH3	Input	Analog	Analog input channel 3
19	CH2	Input	Analog	Analog input channel 2
20	CH1	Input	Analog	Analog input channel 1
21	CH0	Input	Analog	Analog input channel 0
22	A0/NTEST_OUT	I/O	Digital	The lowest order bit of the serial bus address. During a NAND tree test for ATE board-level connectivity, this pin functions as an output.
23	A1	Input	Digital	Address pin 1
24	A2	Input	Digital	Address pin 2

6 Specifications

6.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
Power-supply voltage range, V+		–0.3	7	V
Input voltage range, V_{IN}	Pins 6, 10, 15, 16, 17, 18, 19, 20, 21, 22, 24	–0.3	(V+) + 0.3	V
	Pins 1, 2, 3, 4, 5, 7, 9, 11, 12, 13, 23	–0.3	7	
Input current, I_{IN}			10	mA
Operating temperature range, T_A		–55	127	°C
Junction temperature range, T_J max			150	°C
Storage temperature range, T_{STG}		–65	150	°C

(1) Stresses above these ratings my cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. ance.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage range, V+	3		5.5	V
Input voltage range, V_{IN}	–0.05		(V+) + 0.05	V
Operating temperature range, T_A	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		AMC80 PW (TSSOP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.72	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A –40°C to +125°C and V+ = 3 V to 5.5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS						
V_{IH}	Input high voltage		2			V
V_{IL}	Input low voltage				0.8	V
V_{HYS}	Hysteresis voltage	V+ = 3.3 V		0.23		V
		V+ = 5 V		0.33		V
I_{IH}	Input high current	V_{IH} = V+, all pins except $\overline{BTI}$	–1	–0.005		µA
		V_{IH} = V+, $\overline{BTI}$ pin	–10	–1		µA
I_{IL}	Input low current	V_{IL} = 0 V, all pins except $\overline{BTI}$		0.005	1	µA
		V_{IL} = 0 V, V+ = 5.5 V, $\overline{BTI}$ pin			2	mA
C_{IN}	Input capacitance			20		pF
ANALOG INPUTS						
V_{IN}	Input voltage range	Default	0		2.56	V
		Programmable	0		V+	V
I_{L-ON}	Input leakage current (on)			±0.005		µA
I_{L-OFF}	Input leakage current (off)			±0.005		µA
R_{IN}	Input resistance			2	10	kΩ
DIGITAL OUTPUTS (A0/NTEST_OUT, INT)						
V_{OH}	Output high voltage	I_{OUT} = 3 mA/5 mA, V+ = 3 V/4.5 V	2.4			V
V_{OL}	Output low voltage	I_{OUT} = 3 mA/5 mA, V+ = 3 V/4.5 V			0.4	V
DIGITAL OPEN-DRAIN OUTPUTS ($\overline{GPO}$, $\overline{RST\_OUT}$/$\overline{OS}$, GPI/CI, SDA)						
V_{OL}	Output low voltage	I_{OUT} = 3 mA/5 mA, V+ = 3 V/4.5 V, all pins except SDA			0.4	V
		I_{OUT} = 4 mA, V+ = 3 V, SDA pin			0.4	
I_{OH}	Output high current	V_{OUT} = V+		0.005	1	µA
t_w	Pulse duration	$\overline{RST\_OUT}$/$\overline{OS}$, GPI/CI	10	22.5		ms
SMBus						
	SMBus timeout(1)			28	35	ms
TEMPERATURE ERROR						
T_E	Temperature error	T_A = –40°C to +125°C			±3	°C
		T_A = –25°C to +100°C			±2	°C
T_R	Temperature resolution		0.0625			°C
ANALOG-TO-DIGITAL CONVERTER						
V_R	Resolution	V_{IN} = 2.56 V		2.5		mV
		V_{IN} = V+		6		
DNL	Differential linearity		–1		1	LSB(2)
ADC_{ERR}	Total unadjusted error(3)		–1%		1%	
PSRR	Power supply rejection ratio			±0.0008 %		
t_C(4)	Total conversion time		662	728	810	ms

(1) The SMBus timeout in the AMC80 resets the interface anytime SCL or SDA is low for over 28 ms.
(2) LSB means least significant bit.
(3) Total unadjusted error contains offset, gain, and linearity errors of the ADC.
(4) Total conversion time contains the temperature conversion, the seven analog input voltage conversions, and the two tachometer readings.

Electrical Characteristics (continued)

At T_A –40°C to +125°C and V+ = 3 V to 5.5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FAN RPM-TO-DIGITAL CONVERTER						
FAN_{ERR}	Fan RPM error		–10%		10%	
f_{CLK}	Internal clock frequency		20.2	22.5	24.8	kHz
FAN_{RPM}	FAN1 and FAN2 nominal input RPM	Divisor = 1, fan count = 153		8800		RPM
		Divisor = 2, fan count = 153		4400		
		Divisor = 3, fan count = 153		2200		
		Divisor = 4, fan count = 153		1100		
FSC	Full-scale count				255	Counts
POWER SUPPLY						
V+	Specified voltage range		3		5.5	V
I_{QA}	Quiescent current, average	V+ = 5.5 V			100	µA
		V+ = 3.8 V			25	
I_{QSD}	Quiescent current, shutdown mode	V+ = 5.5 V			100	µA
		V+ = 3.8 V			25	
TEMPERATURE						
T_A	Specified range		-40		125	°C

6.6 Timing Requirements

At T_A –40°C to +125°C and V_S = 3V to 5.5V, unless otherwise noted.

		FAST MODE(1)		HIGH-SPEED MODE(1)		
		MIN	MAX	MIN	MAX	UNIT
$f_{(SCL)}$	SCL operating frequency	10	400	10	3400	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	600		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	600		160		ns
$t_{(SUSTA)}$	Repeated START condition setup time	600		160		ns
$t_{(SUSTO)}$	STOP condition setup time	600		160		ns
$t_{(HDDAT)}$	Data hold time	0(2)		0(3)		ns
$t_{(SUDAT)}$	Data setup time	100		10		ns
$t_{(LOW)}$	Clock low period	1300		160		ns
$t_{(HIGH)}$	Clock high period	600		60		ns
t_R	Clock/Data input rise time		300		160	ns
t_F	Clock/Data input fall time		300		160	ns

(1) Values based on a statistical analysis of a one-time sample of devices. Minimum and maximum values are not specified and not production tested.
(2) For cases when the fall time of SCL is less than 20 ns and/or the rise time or fall time of SDA is less than 20 ns, the hold time should be greater than 20 ns.
(3) For cases when the fall time of SCL is less than 10 ns and/or the rise or fall time of SDA is less than 10 ns, the hold time should be greater than 10 ns.

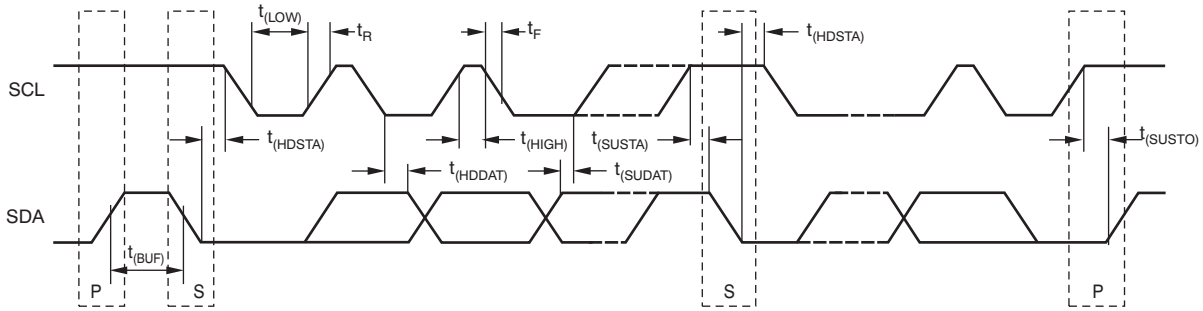


Figure 1. Serial Bus Interface Timing

6.7 Typical Characteristics

At T_A = +25°C and V+ = 3 V to 5.5 V, unless otherwise noted.

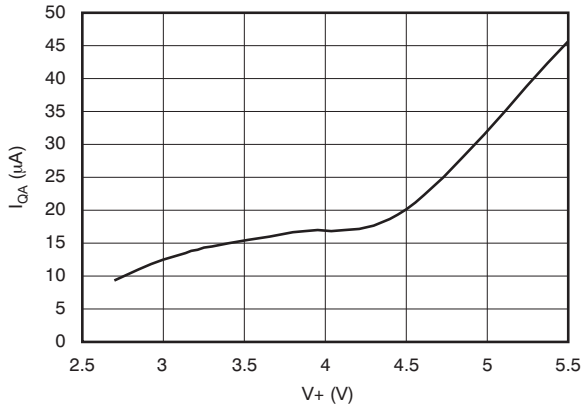


Figure 2. Average Quiescent Current vs Supply Voltage

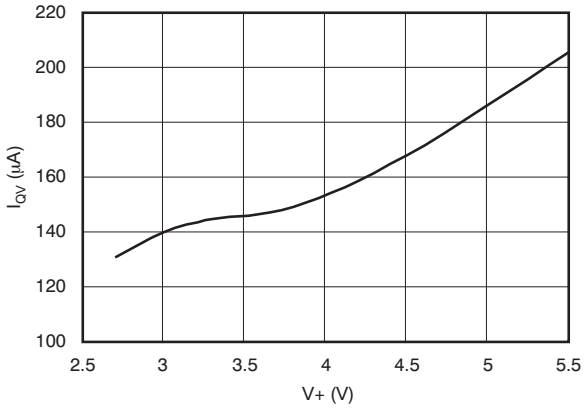


Figure 3. Quiescent Current During Voltage Conversion vs Supply Voltage

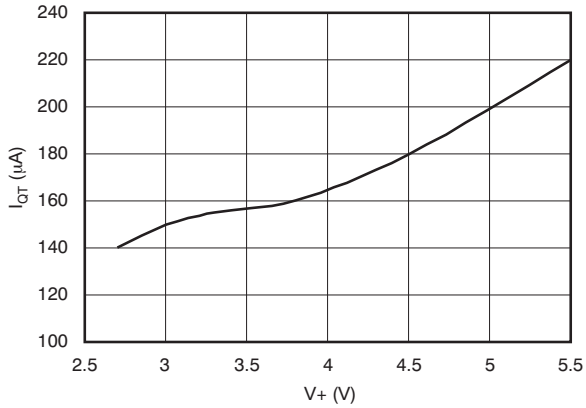


Figure 4. Quiescent Current During Temperature Conversion vs Supply Voltage

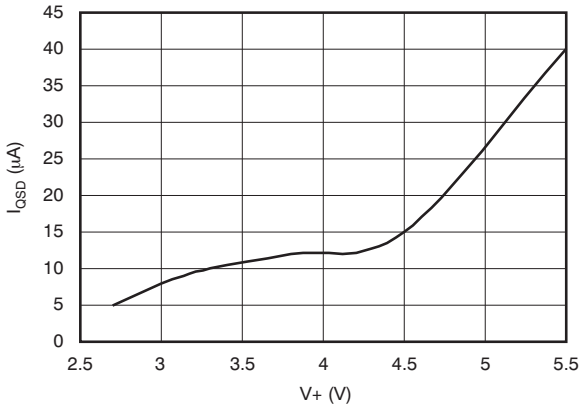


Figure 5. Quiescent Current During Shutdown vs Supply Voltage

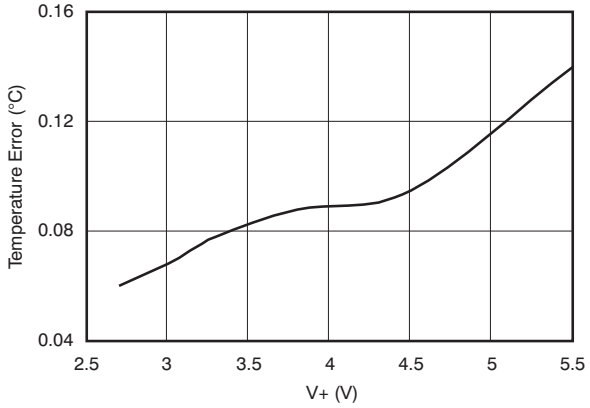


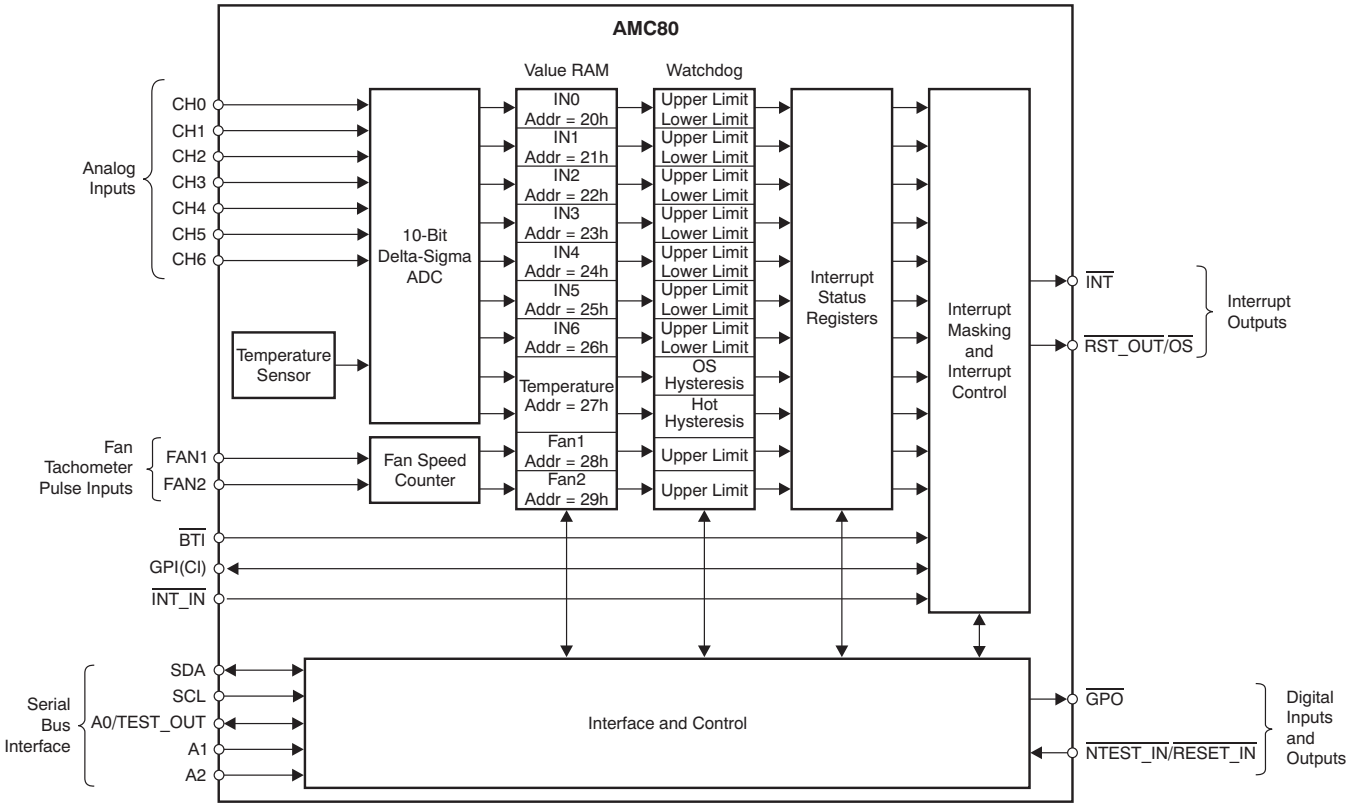
Figure 6. Temperature Error vs Supply Voltage

7 Detailed Description

7.1 Overview

The AMC80 provides seven analog inputs, a temperature sensor, a delta-sigma analog-to-digital converter (ADC), and a variety of inputs and outputs on a single chip. A two-wire SMBus interface is also provided. The AMC80 can continuously perform power-supply, temperature, and fan monitoring for a variety of applications. The AMC80 is fully pin- and software-compatible with the LM96080 and LM80.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Block Level Description

The AMC80 continuously converts analog inputs to 10-bit resolution using a 2.5-mV least significant bit (LSB) with a default input range of 0 V to 2.56 V, or a 6-mV LSB with a programmable input range of 0 V to V+. The analog inputs (CH0 to CH6) are intended for connection to the several power supplies present in any typical system. Temperature can be converted to a 9-bit or 12-bit resolution with either 0.5°C or 0.0625°C LSB, respectively. The FAN1 and FAN2 inputs can be programmed to accept either a fan failure indicator or tachometer signals. Fan failure signals can be programmed to be either active high or active low. Fan inputs measure the period of tachometer pulses from the the fans, providing a higher count for lower fan speeds. The fan inputs are digital inputs with transition levels according to the Digital Inputs section of the *Electrical Characteristics* table. Full-scale fan counts are 255 (8-bit counter), which represent a stopped or very slow fan. Nominal speeds, based on a count of 153, are programmable from 1100 RPM to 8800 RPM. Signal conditioning circuitry is included to accommodate slow rise and fall times.

The AMC80 provides a number of internal registers:

- **Configuration Register:** Provides control and configuration.
- **Interrupt Status Registers:** Two registers that provide the status of each interrupt alarm.
- **Interrupt Mask Registers:** Allows masking of individual interrupt sources, as well as separate masking for

Feature Description (continued)

both hardware interrupt outputs.

- **Fan Divisor/RST_OUT/OS Register:** Bits 0 to 5 of this register contain the divisor bits for the FAN1 and FAN2 inputs. Bits 6 and 7 control the function of the RST_OUT/OS output.
- **OS Configuration/Temperature Resolution Register:** The configuration of the overtemperature shutdown (OS) is controlled by the lower three bits of this register. Bit 3 enables 12-bit temperature conversions. In 12-bit mode, bits 4 to 7 represent the four LSBs of the temperature measurement. In 9-bit mode, bit 4 represents the LSB of the temperature measurement.
- **Conversion Rate Register:** Sets the time interval of the continuous monitoring cycle to either fixed or programmable (see the Conversion Rate Count Register for setting the programmable time interval).
- **Voltage/Temperature Channel Disable Register:** Allows voltage inputs and the local temperature conversion to be disabled.
- **Input Mode Register:** Allows voltage inputs to be configured as single-ended or as a differential pair with normal or reverse polarity.
- **ADC Control Register:** Bits 0 to 2 set the programmable conversion rate for the 10-bit ADC. Bits 3 to 5 allow for programmable input full-scale voltage.
- **Conversion Rate Count Register:** Selects the adjustable time interval when the conversion rate of the continuous monitoring cycle is set to programmable.
- **Value RAM:** The monitoring results (for temperature, voltages, fan counts, and Fan Divisor/RST_OUT/OS Register limits) are all contained in the Value RAM. The Value RAM consists of 32 bytes. The first 10 bytes are all of the results, the next 20 bytes are the interrupt alarm limits, and the last two bytes are at the upper locations for manufacturer ID and die revision ID.

The AMC80 SMBus is compatible with both fast mode (400 kHz) and high-speed mode (3.4 MHz) two-wire interface modes of operation. The AMC80 supports a timeout reset function on SDA and SCL that prevents two-wire bus lockup, and includes an analog filter on the two-wire digital control lines that improves noise immunity. Three address pins (A0 to A2), allow up to eight devices on a single bus. When enabled, the AMC80 starts by cycling through each measurement in sequence, and continuously loops through the sequence based on the Conversion Rate Register (address 07h) setting. Each measured value is compared to values stored in the Value RAM Registers (addresses 2Ah to 3Dh). When the measured value exceeds the programmed limit, the AMC80 sets a corresponding interrupt in the Interrupt Status Registers (addresses 01h and 02h). Two output interrupt lines (INT and RST_OUT/OS) are available. INT is fully programmable with the ability to mask each interrupt source and each output. The Fan Divisor/RST_OUT/OS Register (address 05h) has control bits that enable or disable the hardware interrupts. Additional digital inputs are provided for daisy-chaining the interrupt output pin, INT. This configuration is achieved by connecting multiple external temperature sensors (for example, the TMP75) to the board temperature interrupt (BTI) input and/or the GPI/CI input. The chassis intrusion (CI) input is designed to accept an active high signal from an external circuit that latches (for example, when the chassis from a server rack is removed).

Feature Description (continued)

7.3.2 Temperature Measurement

The AMC80 ΔV_{BE}-type temperature sensor, is a $\Delta\Sigma$ ADC that performs 9-bit or 12-bit twos complement temperature conversions. An 8-bit comparator that compares the readings to the user-programmable hot and overtemperature setpoints, and hysteresis values is also incorporated into the AMC80.

Temperature data can be read from the Temperature Reading Register (address 27h). Temperature limits can be read from and written to the Hot Temperature (T_{HOT}), Hot Temperature Hysteresis (T_{HOT_HYST}), $\overline{OS}$ Temperature (T_{OS}), and $\overline{OS}$ Temperature Hysteresis (T_{OS_HYST}) Limit Registers (addresses 38h to 3Bh). Each limit is represented in 12-bit, 9-bit, or 8-bit resolution, as shown in Table 1.

Table 1. Temperature Lookup

TEMPERATURE	12-BIT DIGITAL OUTPUT (HEX) LSB = 0.0625°C	9-BIT DIGITAL OUTPUT (HEX) LSB = 0.5°C	8-BIT DIGITAL OUTPUT (HEX) LSB = 1°C
+125°C	07D	0FA	7D
+25°C	019	032	19
+1°C	010	003	01
0.0625°C	001	—	—
0°C	000	000	00
–0.0625°C	FFF	—	—
–1°C	FF0	1FF	FF
–25°C	E70	1CE	E7
–55°C	C90	192	C9

When using a single-byte read, the eight MSBs of the temperature reading can be found in the Value RAM Register (address 27h). The remainder of the temperature reading can be found in the $\overline{OS}$ Configuration/Temperature Resolution Register (address 06h), bits 4 to 7. In 9-bit format, bit 7 is the only valid bit. In addition, all nine or 12 bits can be read using a double-byte read at register address 27h.

There are four Value RAM Register limits for the temperature reading that affect the $\overline{INT}$ and $\overline{OS}$ outputs of the AMC80. These are the T_{HOT}, T_{HOT_HYST}, T_{OS}, T_{OS_HYST} Limit Registers (addresses 38h to 3Bh); see Table 15. There are three interrupt modes of operation: Default Interrupt, One-Time Interrupt, and Comparator. The $\overline{OS}$ output of the AMC80 can be programmed for One-Time Interrupt mode and Comparator mode. $\overline{INT}$ can be programmed for Default Interrupt mode and One-Time Interrupt mode. These modes are explained in the following subsections.

7.3.2.1 Default Interrupt Mode

In Default Interrupt mode, exceeding T_{HOT} causes an interrupt that remains active indefinitely until reset by reading Interrupt Status Register 1 (address 01h) or cleared by the INT_Clear bit in the Configuration Register (address 00h, bit 3). When an interrupt event has occurred by exceeding T_{HOT}, and is then reset, another interrupt occurs again when the next temperature conversion has completed. The interrupts continue to occur in this manner until the temperature falls below T_{HOT_HYST}, at which time the interrupt output automatically clears.

7.3.2.2 One-Time Interrupt Mode

In One-Time Interrupt mode, exceeding T_{HOT} causes an interrupt that remains active indefinitely until reset by reading Interrupt Status Register 1 or cleared by the INT_Clear bit in the Configuration Register. When an interrupt event has occurred by exceeding T_{HOT}, and is then reset, an interrupt does not occur again until the temperature falls below T_{HOT_HYST}.

7.3.2.3 Comparator Mode

In Comparator mode, exceeding T_{OS} causes the $\overline{OS}$ output to go low (default) and remain low until the temperature falls below T_{OS_HYST}. When the temperature falls below T_{OS_HYST}, $\overline{OS}$ goes high.

7.3.3 Interrupt Structure

Figure 7 depicts the interrupt structure of the AMC80.

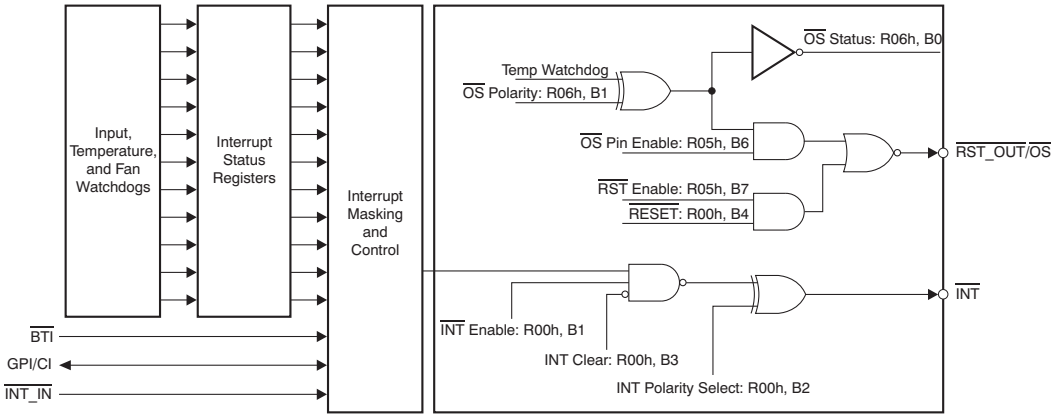


Figure 7. Interrupt Structure

External interrupt inputs can come from the following sources:

- Board Temperature Interrupt (BTI) - This pin is an active low interrupt recommended to come from the overtemperature shutdown (OS) output of TMP75 temperature sensors. The TMP75 OS output activates when its temperature exceeds a programmed threshold. If the temperature of any TMP75 exceeds its programmed limit, BTI is driven low. This action generates an interrupt through bit 1 of Interrupt Status Register 2 (address 02h) that notifies the host of a possible overtemperature condition. To disable this feature, set bit 1 of Interrupt Mask Register 2 (address 04h) to high. This pin also provides an internal, 10-kΩ pull-up resistor.
- GPI/CI - This pin is an active high interrupt from any type of device that detects and captures chassis intrusion violations. This action could be accomplished mechanically, optically, or electrically; circuitry external to the AMC80 is expected to latch the event. Read this interrupt using bit 4 of Interrupt Status Register 2 (address 02h), and disable it using bit 4 of Interrupt Mask Register 2 (address 04h). The design of the AMC80 allows this input to go high even with no power applied, and no clamping or other interference with the line occurs. This line can also be pulled low by the AMC80 for at least 10ms to reset a typical chassis-intrusion circuit. Accomplish this reset by setting bit 5 of the Configuration Register (address 00h) to high; this bit is self-clearing.
- INT_IN - This pin is an active low interrupt that provides a way to connect an INT from other devices through the AMC80 to the processor. If this pin is pulled low, then bit 7 of Interrupt Status Register 1 (address 01h) goes high, indicating this interrupt detection. Setting bit 1 of the Configuration Register (address 00h) also allows the INT pin to go low when INT_IN goes low. To disable this feature, set bit 7 of Interrupt Mask Register 1 (address 03h) to high.

Device interrupt outputs can come from the following sources:

- INT - This pin becomes active whenever INT_IN, BTI, or GPI/CI interrupts. INT is enabled when bit 1 of the Configuration Register (address 00h) is set high. Bits 2 and 3 of the Configuration Register are also used to set the polarity and state of the INT interrupt line.
- OS - In the Fan Divisor/RST_OUT/OS Register (address 05h), bit 6 (OS Pin Enable), must be set high and bit 7 (RST Enable) must be set to low in order to enable the OS function on the RST_OUT/OS pin. The OS pin has two modes of operation: One-Time Interrupt and Comparator. One-Time Interrupt mode is selected by taking bit 2 of the OS Configuration/Temperature Resolution Register (address 06h) high. If bit 2 is taken low, then Comparator mode is selected. Unlike the OS pin, the OS bit in Interrupt Status Register 2 (address 02h, bit 5) functions in Default Interrupt and One-Time Interrupt modes. The OS bit can be masked to the INT pin by taking bit 5 in Interrupt Mask Register 2 (address 04h) low.

Reading the Interrupt Status Registers (addresses 01h to 02h) outputs the contents and then resets the registers and the INT pin. The INT pin is also cleared by the INT_Clear bit (address 00h, bit 3) without affecting the contents of the Interrupt Status Registers. When this bit is high, the AMC80 monitoring loop is inactive; monitoring resumes when this bit is low.

7.4 Programming

7.4.1 Interface and Control

The SMBus control lines in the AMC80 include SDA, SCL, and the A0 to A2 address pins, which allow up to eight AMC80 devices to be on the same bus. The AMC80 can only operate as a slave device. The SCL line controls only the serial interface; all other clock-related functions within the AMC80 (such as the ADC and fan counters) operate with a separate asynchronous internal clock. The default power-on SMBus address for the AMC80 is '0101'(A2)(A1)(A0) binary, where *(A2)(A1)(A0)* is the SMBus address.

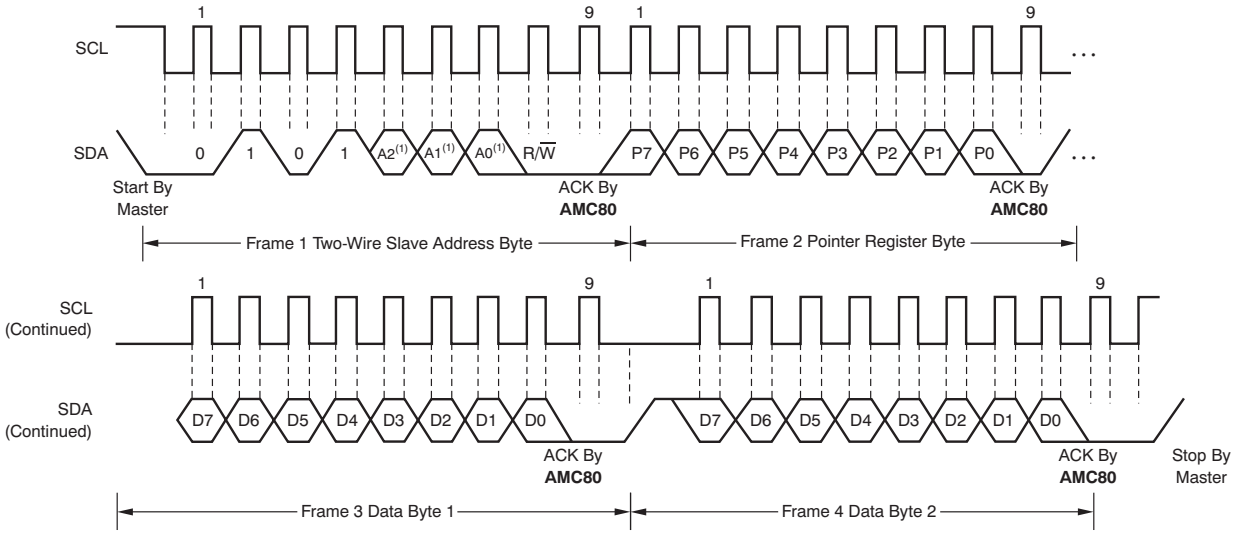
When using the SMBus interface, a write command always consists of the AMC80 SMBus interface address byte, followed by the internal address register byte, and then the data byte (see Figure 8).

See Figure 9 for the read operation timing. There are two cases for a read operation:

1. If the contents of the Internal Address Register are known, simply read the AMC80 with the SMBus interface address byte, followed by the data byte read from the ADC80.
2. If the internal Address Register contents are unknown, write to the AMC80 with the SMBus interface address byte, followed by the internal address register bye. Then restart the serial communication with a read that consist of the SMBus interface address byte, followed by the data byte read from the AMC80.

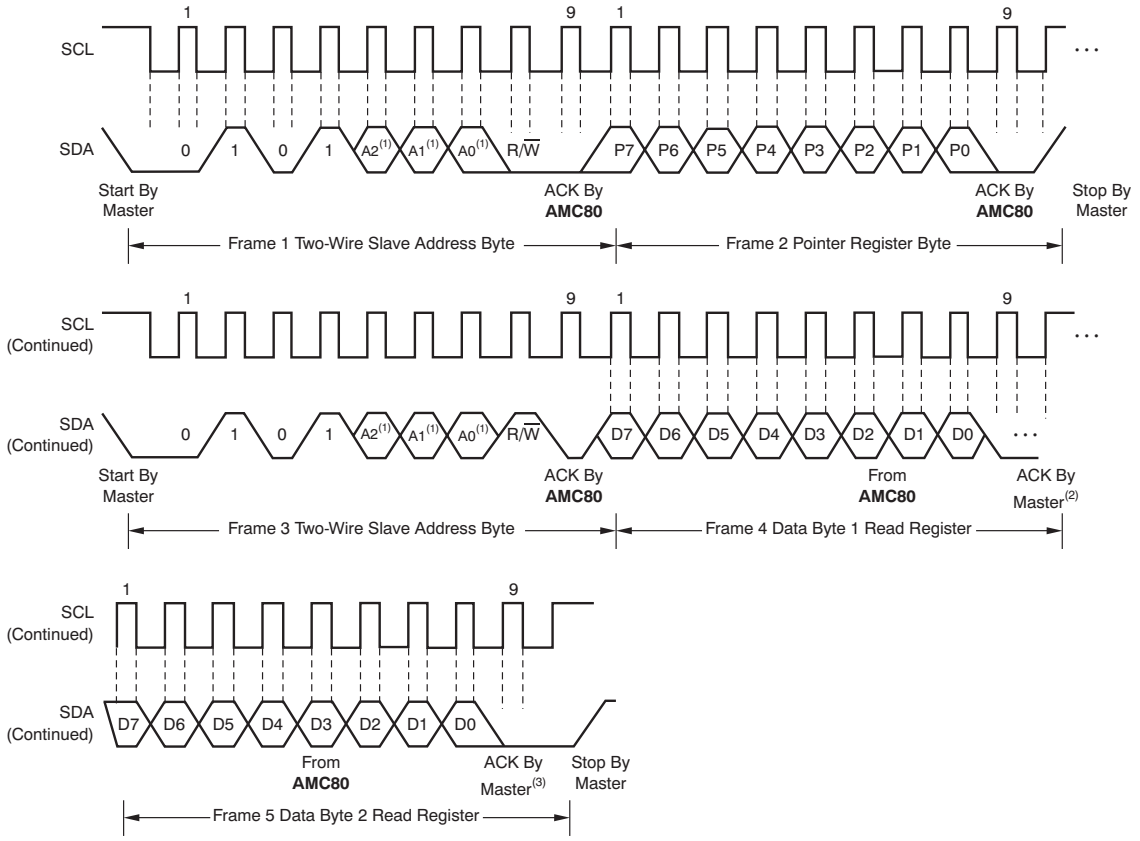
Table 2. Register Overview

REGISTER	INTERNAL ADDRESS (HEX)	POWER-ON VALUE (HEX)	NOTES
Configuration Register	00	08	
Interrupt Status Register 1	01	xx	Indeterminate
Interrupt Status Register 2	02	xx	Indeterminate
Interrupt Mask Register 1	03	00	
Interrupt Mask Register 2	04	00	
Fan Divisor/$\overline{\text{RST}}$_OUT/$\overline{\text{OS}}$ Register	05	14	FAN1 and FAN2 divisor = 2 (count of 153 = 4400 RPM)
$\overline{\text{OS}}$ Configuration/Temperature Resolution Register	06	x1	Four MSBs are indeterminate
Conversion Rate Register	07	40	
Voltage/Temperature Channel Disable Register	08	00	Allows voltage monitoring inputs to be disabled
Input Mode Register	09	00	
ADC Control Register	0A	02	
Conversion Rate Count Register	0B	40	
Value RAM Register	20 to 29	xx	Indeterminate
Value RAM Register	2A to 3D	xx	Indeterminate
Value RAM Register	3E	80	
Value RAM Register	3F	09	



(1) The values of A0, A1, and A2 are determined by the A0, A1, and A2 pins, respectively.

Figure 8. Two-Wire Timing for Write Word Format



(1) The values of A0, A1, and A2 are determined by the A0, A1, and A2 pins, respectively.

(2) Master should leave SDA high to terminate a single-byte read operation.

(3) Master should leave SDA high to terminate a two-byte read operation.

Figure 9. Two-Wire Timing for Read Word Format

7.5 Register Map

7.5.1 Configuration Register

Table 3. Configuration Register (Address = 00h, Default = 08h)

BIT	NAME	TYPE	DESCRIPTION
0	Start	R/W	'1' enables startup of monitoring activity; '0' puts device in shutdown mode.
1	$\overline{\text{INT}}$ Enable	R/W	'1' enables the $\overline{\text{INT}}$ output.
2	$\overline{\text{INT}}$ Polarity Select	R/W	'1' selects active-high, open-source output; '0' selects active-low, open-drain output.
3	INT_Clear	R/W	'1' disables the $\overline{\text{INT}}$ output without affecting the contents of the Interrupt Status Registers. The device stops monitoring and resumes on a '0'.
4	$\overline{\text{RESET}}$	R/W	'1' outputs an active-low reset signal at $\overline{\text{RST\_OUT}}$, if bit 7 and bit 6 in the Fan Divisor/ Register (address 05h) are set to '1' and '0', respectively. This bit is cleared when the pulse becomes inactive.
5	Chassis Clear	R/W	'1' clears the GPI/CI pin. This bit clears itself after 10ms.
6	$\overline{\text{GPO}}$	R/W	'1' drives the $\overline{\text{GPO}}$ pin low.
7	INITIALIZATION	R/W	'1' restores power-on-default values to the registers. This bit is self-clearing

7.5.2 Interrupt Status Registers

Table 4. Interrupt Status Register 1 (Address = 01h, Default = xxh; see Table 2)

BIT	NAME	TYPE	DESCRIPTION
0	CH0	Read	'1' indicates a high or low limit has been exceeded.
1	CH1	Read	'1' indicates a high or low limit has been exceeded.
2	CH2	Read	'1' indicates a high or low limit has been exceeded.
3	CH3	Read	'1' indicates a high or low limit has been exceeded.
4	CH4	Read	'1' indicates a high or low limit has been exceeded.
5	CH5	Read	'1' indicates a high or low limit has been exceeded.
6	CH6	Read	'1' indicates a high or low limit has been exceeded.
7	$\overline{\text{INT\_IN}}$	Read	'1' indicates that a low signal has been detected on the $\overline{\text{INT\_IN}}$ pin.

Table 5. Interrupt Status Register 2 (Address = 02h, Default = xxh; see Table 2)

BIT	NAME	TYPE	DESCRIPTION
0	Hot Temperature	Read	'1' indicates a high or low limit has been exceeded. One-Time Interrupt and Default Interrupt modes are supported and can be set by bit 6 of Interrupt Mask Register 2 (address 04h).
1	$\overline{\text{BTI}}$	Read	'1' indicates that an interrupt has occurred from the $\overline{\text{BTI}}$ input pin.
2	FAN 1	Read	'1' indicates that a fan count limit has been exceeded.
3	FAN 2	Read	'1' indicates that a fan count limit has been exceeded.
4	GPI/CI	Read	'1' indidates that GPI/CI has gone high.
5	$\overline{\text{OS}}$	Read	'1' indicates a high or low temperature limit has been exceeded. One-Time Interrupt and Default Interrupt modes are supported and can be set by bit 7 of Interrupt Mask Register 2 (address 04h).
6	Reserved	Read	This bit is reserved.
7	Reserved	Read	This bit is reserved.

7.5.3 Interrupt Mask Registers

Table 6. Interrupt Mask Register 1 (Address = 03h, Default = 00h)

BIT	NAME	TYPE	DESCRIPTION
0	CH0	R/W	'1' disables the corresponding interrupt status bit in Table 4 to trigger the $\overline{\text{INT}}$ interrupt.
1	CH1	R/W	
2	CH2	R/W	
3	CH3	R/W	
4	CH4	R/W	
5	CH5	R/W	
6	CH6	R/W	
7	$\overline{\text{INT\_IN}}$	R/W	

Table 7. Interrupt Mask Register 2 (Address = 04h, Default = 00h)

BIT	NAME	TYPE	DESCRIPTION
0	Hot Temperature	R/W	'1' disables the corresponding interrupt status bit in Table 5 to trigger the $\overline{\text{INT}}$ interrupt.
1	$\overline{\text{BTI}}$	R/W	
2	FAN 1	R/W	
3	FAN 2	R/W	
4	GPI/CI	R/W	
5	$\overline{\text{OS}}$	R/W	
6	$\overline{\text{INT}}$ Interrupt Mode Select	R/W	'0' selects Default Interrupt mode. '1' selects One-Time Interrupt mode.
7	$\overline{\text{OS}}$ Interrupt Mode Select	R/W	'0' selects Comparator mode. '1' selects One-Time Interrupt mode.

7.5.4 Fan Divisor/$\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ Register

Table 8. Fan Divisor/$\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ Register (Address = 05h, Default = 14h)

BIT	NAME	TYPE	DESCRIPTION
0	FAN1 Mode Select	R/W	'1' selects the level-sensitive input mode. '0' selects the fan count mode for the FAN1 input.
1	FAN2 Mode Select	R/W	'1' selects the level-sensitive input mode. '0' selects the fan count mode for the FAN2 input.
2	FAN1 RPM Control 1	R/W	FAN1 speed control: '00' = divide by 1. '01' = divide by 2. '10' = divide by 4. '11' = divide by 8. If level-sensitive input is selected, '01' selects an active-low input and '00' selects an active-high input.
3	FAN1 RPM Control 0	R/W	
4	FAN2 RPM Control 1	R/W	FAN2 speed control: '00' = divide by 1. '01' = divide by 2. '10' = divide by 4. '11' = divide by 8. If level select input is selected, '01' selects an active-low input and '00' selects an active-high input.
5	FAN2 RPM Control 0	R/W	
6	$\overline{\text{OS}}$ Pin Enable	R/W	'1' enables $\overline{\text{OS}}$ mode on the $\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ pin when bit 7 is set to '0'. NOTE: When bits 6 and 7 are both set to '1', the $\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ pin is disabled.
7	$\overline{\text{RST\_OUT}}$ Pin Enable	R/W	'1' enables $\overline{\text{RST\_OUT}}$ mode on the $\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ pin when bit 6 is set to '0'. NOTE: When bits 6 and 7 are both set to '1', the $\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ pin is disabled.

7.5.5 $\overline{OS}$ Configuration/Temperature Resolution Register

Table 9. $\overline{OS}$ Configuration/Temperature Resolution Register (Address = 06h, Default = x1h; see Table 2)

BIT	NAME	TYPE	DESCRIPTION
0	OS Status	Read	This bit mirrors the state of the $\overline{RST\_OUT}/\overline{OS}$ pin when in $\overline{OS}$ mode.
1	OS Polarity	R/W	'1' selects $\overline{OS}$ to be active-high '0' selects $\overline{OS}$ to be active-low.
2	OS Mode Select	R/W	'1' selects One-Time-Interrupt mode; '0' selects Comparator mode.
3	Temperature Resolution Control	R/W	'1' selects 11-bit plus sign resolution temperature conversion; '0' selects the default 8-bit plus sign resolution temperature conversion.
4	Temp3	R/W	The lower four LSBs of the 11-bit plus sign temperature data. For 8-bit plus sign temperature data, bit 7 is the LSB and bits 4 to 6 are undefined.
5	Temp2	R/W	
6	Temp1	R/W	
7	Temp0	R/W	

7.5.6 Conversion Rate Register

Table 10. Conversion Rate Register (Address = 07h, Default = 40h)

BIT	NAME	TYPE	DESCRIPTION
0	CR1	R/W	Controls conversion rate: '0' = Programmable conversion rate by the following formula: Monitoring delay = (ms) = 1.42 × (8 × *N* + 6) where *N* can be set by bits 7:0 in the Conversion Rate Count Register (address 0Bh). '1' = Continuous conversion.
1	Reserved	R/W	'0' must be written to this bit.
2	Reserved	R/W	'0' must be written to this bit.
3	Reserved	R/W	'0' must be written to this bit.
4	Reserved	R/W	'0' must be written to this bit.
5	Reserved	R/W	'0' must be written to this bit.
6	Reserved	R/W	'0' must be written to this bit.
7	Reserved	R/W	'0' must be written to this bit.

7.5.7 Voltage/Temperature Channel Disable Register

Table 11. Voltage/Temperature Channel Disable Register (Address = 08h, Default = 00h)

BIT	NAME	TYPE	DESCRIPTION
0	CH0	R/W	'1' disables conversions and suppresses error events; Value RAM Register reads '0' for CH0.
1	CH1	R/W	'1' disables conversions and suppresses error events; Value RAM Register reads '0' for CH1.
2	CH2	R/W	'1' disables conversions and suppresses error events; Value RAM Register reads '0' for CH2.
3	CH3	R/W	'1' disables conversions and suppresses error events; Value RAM Register reads '0' for CH3.
4	CH4	R/W	'1' disables conversions and suppresses error events; Value RAM Register reads '0' for CH4.
5	CH5	R/W	'1' disables conversions and suppresses error events; Value RAM Register reads '0' for CH5.
6	CH6	R/W	'1' disables conversions and suppresses error events; Value RAM Register reads '0' for CH6.
7	Temp	R/W	'1' disables conversions and suppresses error events; Value RAM Register reads '0' for temperature.

7.5.8 Input Mode Register

Table 12. Input Mode Register (Address = 09h, Default = 00h)

BIT	NAME	TYPE	DESCRIPTION
0	Diff01	R/W	When set to '1', CH0 and CH1 operate as a differential input. When set to '0', CH0 and CH1 operate as 2 single-ended inputs.
1	Pol01	R/W	When bit 0 = '1', CH0 and CH1 differential inputs are setup in normal polarity mode when this bit is set to '1', and in reverse polarity mode when this bit is set to '0'. When bit 0 is set to “0”, this bit is ignored.
2	Diff23	R/W	When set to '1', CH2 and CH3 operate as a differential input. When set to '0', CH2 and CH3 operate as 2 single-ended inputs.
3	Pol23	R/W	When bit 0 = '1', CH2 and CH3 differential inputs are setup in normal polarity mode when this bit is set to '1', and in reverse polarity mode when this bit is set to '0'. When bit 0 is set to “0”, this bit is ignored.
4	Diff45	R/W	When set to '1', CH4 and CH5 operate as a differential input. When set to '0', CH4 and CH5 operate as 2 single-ended inputs.
5	Pol45	R/W	When bit 0 = '1', CH4 and CH5 differential inputs are setup in normal polarity mode when this bit is set to '1', and in reverse polarity mode when this bit is set to '0'. When bit 0 is set to “0”, this bit is ignored.
6	Reserved	R/W	'0' must be written to this bit.
7	Reserved	R/W	'0' must be written to this bit.

7.5.9 ADC Control Register

Table 13. ADC Control Register (Address = 0Ah, Default = 02h)

BIT	NAME	TYPE	DESCRIPTION
0	DR2	R/W	The 10-bit ADC conversion rate for the analog inputs is set as follows: 000 = 0.512 kHz 001 = 1 kHz 010 = 1.98 kHz 011 = 3.6 kHz 100 = 6.3 kHz 101 = 9.8 kHz 110 = 13.15 kHz 111 = 13.15 kHz
1	DR1	R/W	
2	DR0	R/W	
3	PGA2	R/W	The full-scale analog input range is set as follows: 000 = 2.56 V 001 = V_{DD} 010 = 4.096 V or V_{DD} (whichever is less) 011 = 2.048 V 100 = 1.024 V 101 = 0.512 V 110 = 0.256 V 111 = 0.256 V
4	PGA1	R/W	
5	PGA0	R/W	
6	Reserved	R/W	'0' must be written to this bit.
7	Reserved	R/W	'0' must be written to this bit.

7.5.10 Conversion Rate Count Register

Table 14. Conversion Rate Count Register (Address = 0Bh, Default = 40h)

BIT	NAME	TYPE	DESCRIPTION
0	CRC7	R/W	When bit 0 of the Conversion Rate Register (address 07h) is set to '0', the monitoring conversion delay can be programmed as follows: 0000000 = 0 0000001 = 1 0000010 = 2 … … … 1111111 = 255 When bit 0 of the Conversion Rate Register is set to '1', these bits are ignored.
1	CRC6	R/W	
2	CRC5	R/W	
3	CRC4	R/W	
4	CRC3	R/W	
5	CRC2	R/W	
6	CRC1	R/W	
7	CRC0	R/W	

7.5.11 Value Ram Register

Table 15. Value RAM Register (Addresses = 20h to 3Fh)

ADDRESS (HEX)	DESCRIPTION
20	CH0 reading (10-bit)
21	CH1 reading (10-bit)
22	CH2 reading (10-bit)
23	CH3 reading (10-bit)
24	CH4 reading (10-bit)
25	CH5 reading (10-bit)
26	CH6 reading (10-bit)
27	Temperature reading (9-bit or 12-bit for easy readback)
28	FAN1 reading
29	FAN2 reading
2A	CH0 high limit
2B	CH0 low limit
2C	CH1 high limit
2D	CH1 low limit
2E	CH2 high limit
2F	CH2 low limit
30	CH3 high limit
31	CH3 low limit
32	CH4 high limit
33	CH4 low limit
34	CH5 high limit
35	CH5 low limit
36	CH6 high limit
37	CH6 low limit
38	Hot temperature high limit (T_{HOT})
39	Hot temperature hysteresis low limit (T_{HOT_HYST})
3A	$\overline{OS}$ temperature high limit (T_{OS})
3B	$\overline{OS}$ temperature hysteresis low limit (T_{OS_HYST})
3C	FAN1 fan count limit
3D	FAN2 fan count limit
3E	Manufacturer ID (always defaults to 80h)
3F	Die revision ID (always defaults to 08h)

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Device Power-On

The AMC80 undergoes a power-on-reset condition when power is first applied to the device, or when the Configuration Register INITIALIZATION bit (address 00h, bit 7) is set high; this bit automatically clears after being set. The AMC80 can also be forced to a reset condition by taking the NTEST_IN/RESET_IN pin low for at least 50 ns.

To start the AMC80 monitoring functions (temperature, analog inputs, and fan speeds), write to the Configuration Register with a '0' to INT_Clear (bit 3) and a '1' to Start (bit 0). The AMC80 then performs continuous monitoring of all temperature, analog inputs, and fan speeds. The sequence of items that are monitored (except for the temperature reading) corresponds to locations in the Value RAM, respectively:

1. Temperature
2. CH0
3. CH1
4. CH2
5. CH3
6. CH4
7. CH5
8. CH6
9. Fan 1
10. Fan 2

The conversion results are available in the Value RAM (addresses 20h to 29h). Conversions can be read at any time and provide the result of the last conversion. A typical sequence of events after AMC80 power-on consists of these actions:

1. Set alarm limits
2. Set interrupt masks
3. Start the AMC80 monitoring process

Application Information (continued)

8.1.2 Analog Inputs

In the default state, the 10-bit ADC has a 2.5-mV LSB, yielding a 2.56-V full-scale input range. The input range can also be programmed with several values up to the V+ full-scale input range with a 6-mV LSB. These settings are programmed by bits 3 to 5 in the ADC Control Register.

In most applications, the analog inputs are often connected to power supplies. The voltage inputs should be attenuated with external resistors to any desired value within the input range.

CAUTION

Care should be taken not to exceed V+ on the device input pins at any time.

In select applications where inputs to be monitored are differential in nature, analog inputs (CH0 to CH5) can be configured as up to three differential pairs (inputs 0-1, 2-3, and 4-5) by setting bits 0, 2, and 4 in the Input Mode Register. If needed, the input pair polarity can be changed by setting bits 1, 3, and 5 in the Input Mode Register.

8.1.3 Fan Inputs

Inputs are provided on the AMC80 for signals from fans equipped with tachometer outputs. Signal conditioning in the AMC80 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 V to 5.5 V. In the event that these inputs are supplied from fan outputs that exceed 0 V to 5.5 V, either resistive division or diode clamping must be included to keep inputs within an acceptable range.

The Fan Inputs gate an internal 22.5-kHz oscillator for one period of the Fan signal into an 8-bit counter (maximum count = 255). The default divisor is set to 2 (choices are 1, 2, 4, and 8) providing a nominal count of 153 for a 4400 RPM fan with two pulses per revolution. Typical practice is to consider 70% of normal RPM a fan failure, at which point the count will be 219. The fan count can be determined as shown in Equation 1:

$$\text{Count} = \frac{1.35 \times 10^6}{\text{RPM} \times \text{Divisor}} \quad (1)$$

Where:

RPM = fan speed

Divisor = fan 1 or fan 2 divisor set through the Fan_Divisor/$\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ Register (address 05h)

FAN1 and FAN2 inputs can also be programmed to be level-sensitive interrupt inputs. Fans that provide only one pulse per revolution require a divisor that is set twice as high as fans that provide two pulses, thus maintaining a nominal fan count of 153. Therefore, using Equation 1, the divisor should be set to 4 for a fan that provides one pulse per revolution with a nominal RPM of 4400.

9 器件和文档支持

9.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

9.2 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

9.3 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC80AIPW	Obsolete	Production	TSSOP (PW) | 24	-	-	Call TI	Call TI	-40 to 125	AMC80A
AMC80AIPWR	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	AMC80A
AMC80AIPWR.A	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	AMC80A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

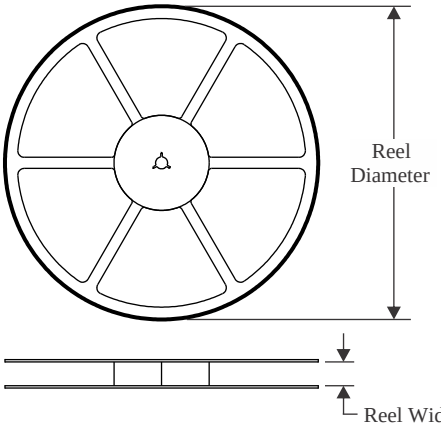
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

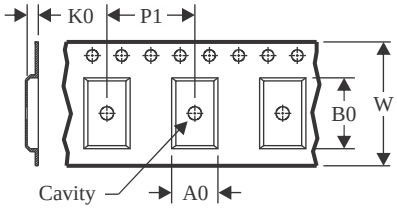
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

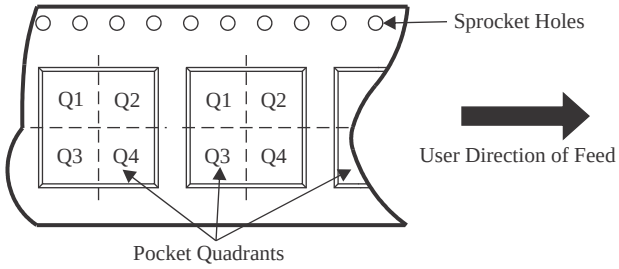


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

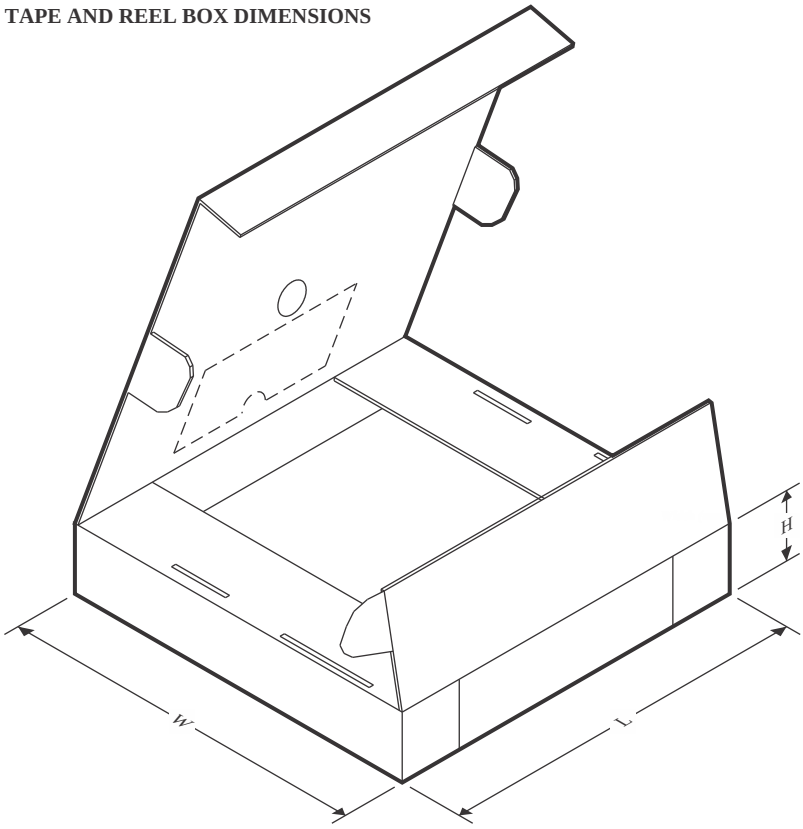
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC80AIPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

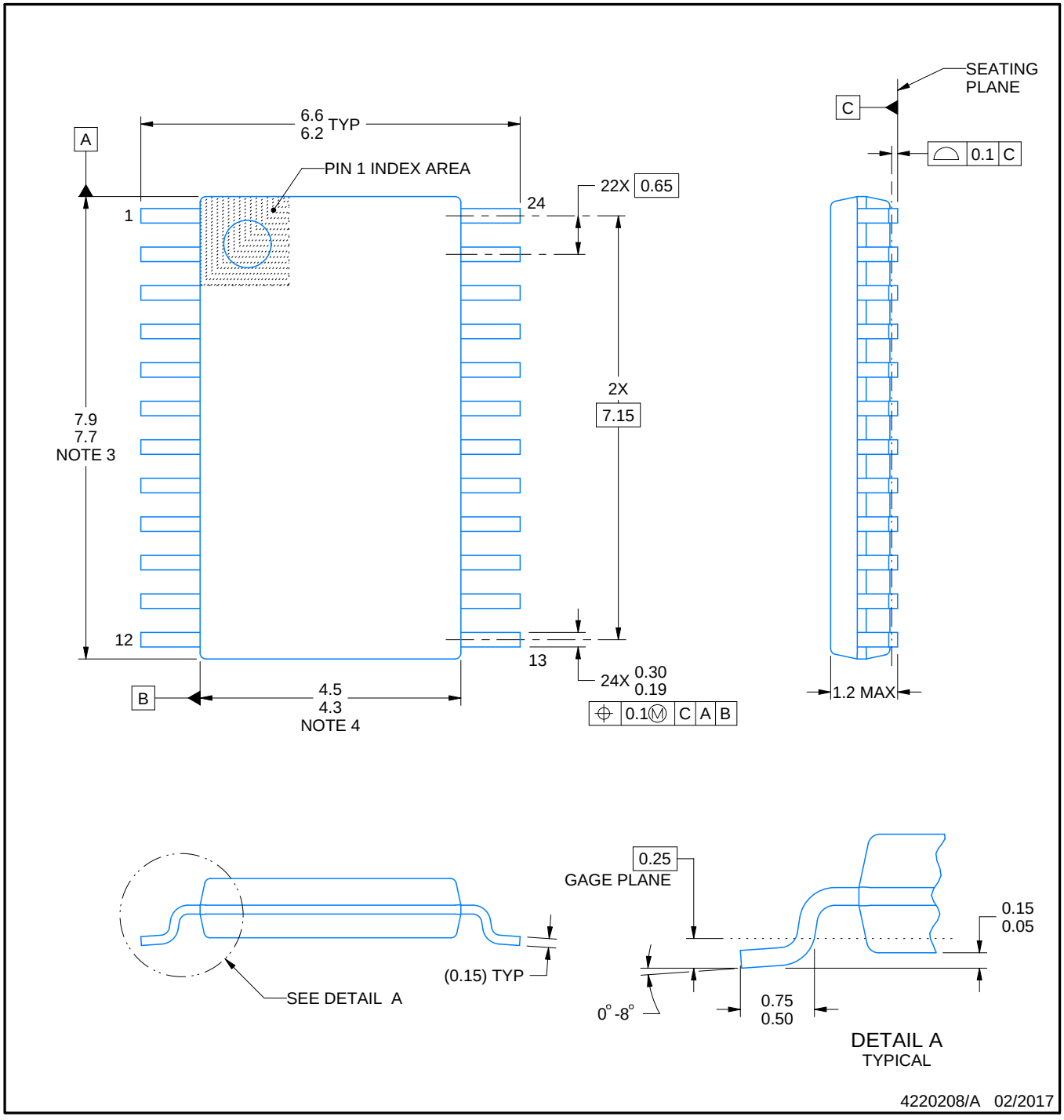
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC80AIPWR	TSSOP	PW	24	2000	350.0	350.0	43.0

PACKAGE OUTLINE

PW0024A

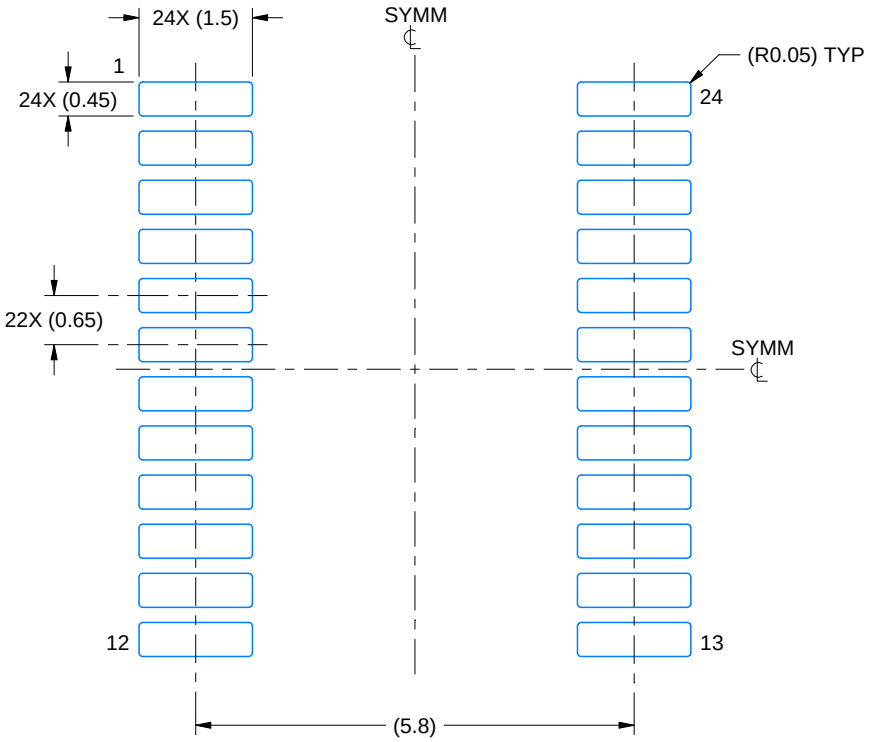
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

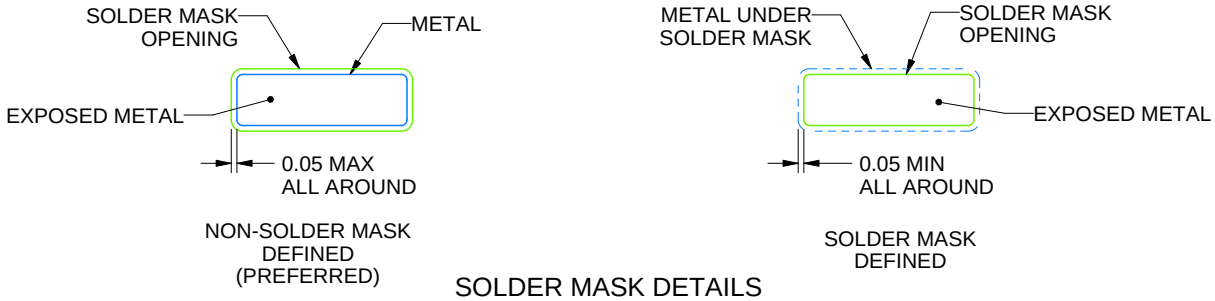


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

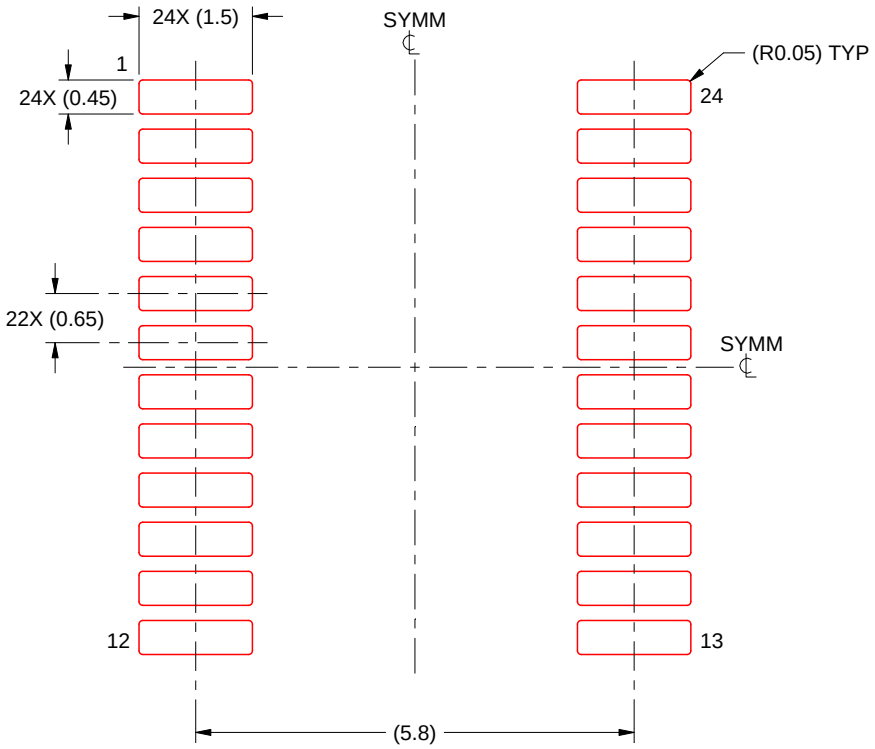


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月