

CD4016B 类 CMOS 四路双向开关

1 特性

- 20V 数字或 $\pm 10V$ 峰峰值开关
- 工作电压为 15V 时典型导通电阻为 280 Ω
- 在 15V 信号输入范围内匹配的开关导通电阻不超过 10 Ω
- 高开关输出电压比：
 $f_{is} = 10\text{kHz}$ 、 $R_L = 10\text{k}\Omega$ 时典型值为 65dB
- 高度线性：
 $f_{is} = 1\text{kHz}$ 、 $V_{is} = 5V_{p-p}$ 、 $V_{DD} - V_{SS} = 10V$ 、 $R_L = 10\text{k}\Omega$ 时失真典型值小于 0.5%
- 超低关断状态开关泄漏，从而产生较低的失调电流和有效关断状态电阻： $V_{DD} - V_{SS} = 18V$ 、 $T_A = 25^\circ\text{C}$ 时典型值为 100pA
- 较高控制输入阻抗（控制电路与信号电路相隔）：典型值为 $10^{12}\Omega$
- 低开关间串扰： $f_{is} = 0.9\text{MHz}$ 、 $R_L = 1\text{k}\Omega$ 时典型值为 -50dB
- 匹配的控制输入到信号输出电容：可减少输出信号瞬态
- 频率响应，开启 = 40MHz（典型值）
- 针对 20V 下的静态电流进行了 100% 测试
- 在全封装温度范围内，18V 时的最大控制输入电流为 1 μA ，18V 和 25 $^\circ\text{C}$ 时为 100nA
- 5V、10V 和 15V 参数额定值

2 应用

- 模拟信号开关/多路复用信号门控
- 调制器静噪控制
- 解调器斩波器
- 换向开关
- 数字信号开关/多路复用
- CMOS 逻辑实现
- 模数和数模转换
- 频率、阻抗、相位和模拟信号增益的数字控制

3 说明

用于模拟或数字信号高压类型（20V 额定值）的传输或多路复用。

CD4016B B 系列类型是用于模拟或数字信号传输或多路复用的四路双向开关。四个独立双向开关中的每一个都有单个控制信号输入，可在给定开关的导通或关断状态下同时偏置 p 和 n 器件。

CD4016B B 系列类型采用 14 引线气密性双列直插式陶瓷封装（后缀为 F3A）、14 引线双列直插式塑料封装（后缀为 E）、14 引线小外形封装（后缀为 M、MT、M96 和 NSR）和 14 引线薄型紧缩小外形封装（后缀为 PW 和 PWR）。

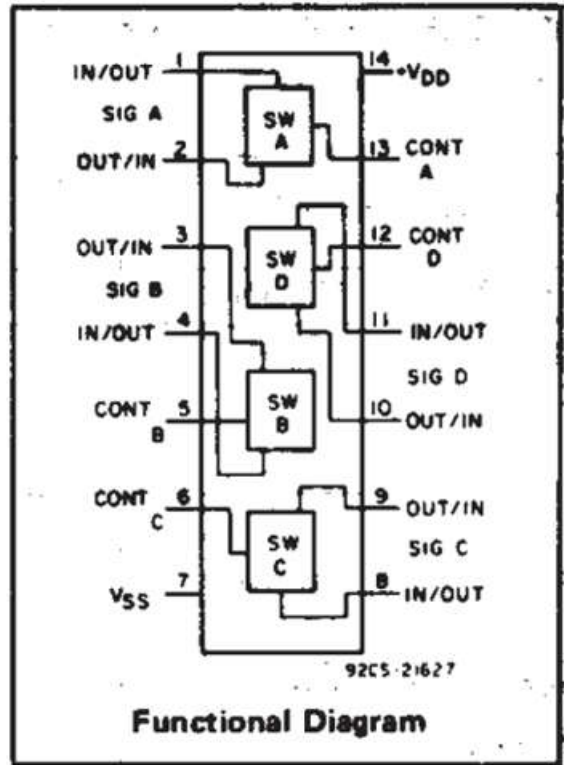
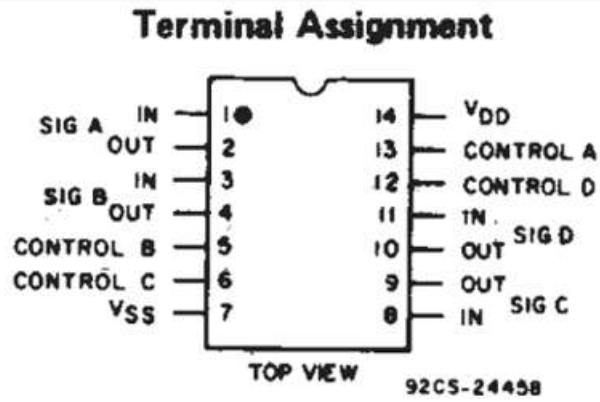
封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
CD4016B	N (PDIP, 14)	19.3mm × 9.4mm
	D (SOIC, 14)	8.65mm × 6mm

(1) 有关更多信息，请参阅节 8。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。





原理图 - (1/4) 转换部分

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4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
$V_{DD} - V_{SS}$	Supply voltage		20	V
V_{DD}		- 0.5	20	V
V_{SS}		- 20	0.5	V
I_{SEL} or I_{EN}	Logic control input pin current (\overline{EN} , Ax, SELx)	- 30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
I_S or I_D (CONT)	Source or drain continuous current (Sx, D)	- 20	20	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} - V_{SS}$ ⁽¹⁾	Power supply voltage differential	3		18	V
V_{DD}	Positive power supply voltage	3		18	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
V_{SEL} or V_{EN}	Address or enable pin voltage	0		V_{DD}	V
I_S or I_D (CONT)	Source or drain continuous current (Sx, D)	- 10		10	mA
T_A	Ambient temperature	- 55		125	°C

- (1) V_{DD} and V_{SS} can be any value as long as $3V \leq (V_{DD} - V_{SS}) \leq 24V$, and the minimum V_{DD} is met.

4.4 Thermal Information

THERMAL METRIC ⁽¹⁾		CD4016		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.7	109.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.5	69.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.0	67.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	50.3	25.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	67.3	67.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

4.5 Electrical Characteristics

Over operating free-air temperature range, $V_{SUPPLY} = \pm 5V$, and $R_L = 100\ \Omega$, (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT	
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})									
I_{DD}	Quiescent Device Current	$V_{IS} = 0$ to 5V $V_{DD} = 5V$	$T_A = -55^\circ C$					5	μA
			$T_A = -40^\circ C$					5	
			$T_A = 25^\circ C$			4.5	6		
			$T_A = 85^\circ C$				7.5		
			$T_A = 125^\circ C$				7.5		
		$V_{IS} = 0$ to 10V $V_{DD} = 10V$	$T_A = -55^\circ C$					6	
			$T_A = -40^\circ C$					6	
			$T_A = 25^\circ C$			5	7		
			$T_A = 85^\circ C$				15		
			$T_A = 125^\circ C$				15		
		$V_{IS} = 0$ to 15V $V_{DD} = 15V$	$T_A = -55^\circ C$					7	
			$T_A = -40^\circ C$					7.2	
			$T_A = 25^\circ C$			6	8		
			$T_A = 85^\circ C$				30		
			$T_A = 125^\circ C$				30		
		$V_{IS} = 0$ to 20V $V_{DD} = 20V$	$T_A = -55^\circ C$					8.5	
			$T_A = -40^\circ C$					8.5	
			$T_A = 25^\circ C$			6.5	9		
			$T_A = 85^\circ C$				150		
			$T_A = 125^\circ C$				150		

4.5 Electrical Characteristics (续)

Over operating free-air temperature range, $V_{SUPPLY} = \pm 5V$, and $R_L = 100 \Omega$, (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
r_{ON}	ON Resistance r_{ON} Max	to ($V_{DD}+V_{SS}$)/2 , $V_C = V_{DD}$, $R_L = 10k \Omega$	$V_{DD} = 10V$ $V_{is} = V_{SS}$ or V_{DD}	$T_A = -55^\circ C$			600	Ω
				$T_A = -40^\circ C$			610	
				$T_A = 25^\circ C$		250	660	
				$T_A = 85^\circ C$			840	
				$T_A = 125^\circ C$			960	
			$V_{DD} = 10V$ $V_{is} = 4.75$ to $5.75V$	$T_A = -55^\circ C$			1870	
				$T_A = -40^\circ C$			1900	
				$T_A = 25^\circ C$			2000	
				$T_A = 85^\circ C$			2380	
				$T_A = 125^\circ C$			2600	
			$V_{DD} = 15V$ $V_{is} = V_{SS}$ or V_{DD}	$T_A = -55^\circ C$			360	
				$T_A = -40^\circ C$			370	
				$T_A = 25^\circ C$		200	400	
				$T_A = 85^\circ C$			520	
				$T_A = 125^\circ C$			600	
			$V_{DD} = 15V$ $V_{is} = 7.25$ to $7.75V$	$T_A = -55^\circ C$			775	
				$T_A = -40^\circ C$			790	
				$T_A = 25^\circ C$			850	
				$T_A = 85^\circ C$			1080	
				$T_A = 125^\circ C$			1230	
r_{ON}	ON Resistance r_{ON} Max	to ($V_{DD}+V_{SS}$)/2 , $V_C = V_{DD}$, $R_L = 10k \Omega$	$V_{DD} = 5V$ $V_{SS} = 0V$	$T_A = 25^\circ C$		580	7000	Ω
			$V_{DD} = 7.5V$ $V_{SS} = -7.5V$	$T_A = 25^\circ C$		200	280	
			$V_{DD} = 5V$ $V_{SS} = -5V$	$T_A = 25^\circ C$		250	580	
			$V_{DD} = 2.5V$ $V_{SS} = -2.5V$	$T_A = 25^\circ C$		520	30000	
ΔR_{ON}	On-state resistance difference between any two switches	$R_L = 10k \Omega$, $V_C = V_{DD}$	$V_{DD} = 5V$			15	Ω	
			$V_{DD} = 10V$			10		
			$V_{DD} = 15V$			5		
THD	Total Harmonic Distortion	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $V_{is(p-p)} = 5V$ (sine wave centered on 0V), $R_L = 10k \Omega$, $f_{is} = 1kHz$ sine wave				0.4	%	
BW	- 3-dB cutoff frequency (switch on)	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $V_{is(p-p)} = 5V$ (sine wave centered on 0V), $R_L = 1k \Omega$				40	MHz	
OISO	- 50-dB feedthrough frequency (switch off)	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $V_{is(p-p)} = 5V$ (sine wave centered on 0V), $R_L = 1k \Omega$				1.25	MHz	
I_{is}	Input/Output Leakage Current (switch off)	$V_{DD} = 18V$ $V_C = 0V$ $V_{is} = 18V$, $V_{os} = 0V$ $V_{is} = 0V$, $V_{os} = 18V$	$T_A = -55^\circ C$		-0.1	0.1	μA	
			$T_A = -40^\circ C$		-0.1	0.1		
			$T_A = 25^\circ C$		0.000 1	0.1		
			$T_A = 85^\circ C$		-1	1		
			$T_A = 125^\circ C$		-1	1		
XTALK	- 50-dB crosstalk frequency	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $V_{is(p-p)} = 5V$ (sine wave centered on 0V), $R_L = 1k \Omega$				0.9	MHz	

4.5 Electrical Characteristics (续)

Over operating free-air temperature range, $V_{SUPPLY} = \pm 5V$, and $R_L = 100\ \Omega$, (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay	$V_C = V_{DD}, V_{SS} = GND$ $V_{IS} = \text{Square Wave 0 to } V_{DD}, C_L = 50\text{pF}, R_L = 200\text{k}\ \Omega$	$V_{DD} = 5V$		40	100	ns	
			$V_{DD} = 10V$		20	40		
			$V_{DD} = 15V$		15	30		
C_{IS}	Input capacitance		$V_{DD} = 5V, V_C = V_{SS} = -5V$		4		pF	
C_{OS}	Output capacitance		$V_{DD} = 5V, V_C = V_{SS} = -5V$		4		pF	
C_{IOS}	Feed through		$V_{DD} = 5V, V_C = V_{SS} = -5V$		0.2		pF	
V_{ILC}	Control input, low voltage (max)	$ I_{is} < 10\ \mu A,$ $V_{is} = V_{SS}, V_{OS} = V_{DD},$ and $V_{is} = V_{DD}, V_{OS} = V_{SS}$	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$	$T_A = -55^\circ C$		0.9	V	
				$T_A = -40^\circ C$		0.9		
				$T_A = 25^\circ C$		0.7		
				$T_A = 85^\circ C$		0.4		
				$T_A = 125^\circ C$		0.4		
V_{IHC}	Control input, high voltage	See Figure 10	$V_{DD} = 5V$		3.5		V	
			$V_{DD} = 10V$		7		V	
			$V_{DD} = 15V$		11		V	
I_{IH}	Input High Leakage		$V_{DD} = 18V$		0.5	1	μA	
I_{IL}	Input Low Leakage		$V_{DD} = 18V$		-1	-0.1	μA	
	Crosstalk (control input to signal output)	$V_C = 10V$ (square wave), $t_r, t_f = 20\text{ns}, R_L = 10\text{k}\ \Omega, V_{DD} = 10V$	$V_{DD} = 10V$		50		mV	
	Turn-on propagation delay	$t_r, t_f = 20\text{ns}$ $C_L = 50\text{pF}, R_L = 1\text{k}\ \Omega$	$V_{DD} = 5V$		35	70	ns	
			$V_{DD} = 10V$		20	40	ns	
			$V_{DD} = 15V$		15	30	ns	
	Maximum control input repetition rate	$V_{IN} = V_{DD}, C_L = 50\text{pF}, R_L = 1\text{k}\ \Omega$ $V_C = 10V$ (square wave centered on 5V), $t_r, t_f = 20\text{ns}, V_{OS} = 1/2V_{OS}$ at 1kHz	$V_{DD} = 10V$		10		MHz	
C_{IN}	Input Capacitance				5	7.5	pF	

4.5 Electrical Characteristics (续)

Over operating free-air temperature range, $V_{\text{SUPPLY}} = \pm 5\text{V}$, and $R_L = 100\ \Omega$, (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT	
I_{IS}	Switch input current	$V_{\text{DD}} = 5\text{V}$ $V_{\text{IS}} = 0\text{V}$	$T_A = -55^\circ\text{C}$					0.25	mA	
			$T_A = -40^\circ\text{C}$					0.2		
			$T_A = 25^\circ\text{C}$					0.2		
			$T_A = 85^\circ\text{C}$					0.12		
			$T_A = 125^\circ\text{C}$					0.14		
		$V_{\text{DD}} = 5\text{V}$ $V_{\text{IS}} = 5\text{V}$	$T_A = -55^\circ\text{C}$						-0.25	mA
			$T_A = -40^\circ\text{C}$						-0.2	
			$T_A = 25^\circ\text{C}$						-0.2	
			$T_A = 85^\circ\text{C}$						-0.12	
			$T_A = 125^\circ\text{C}$						-0.14	
		$V_{\text{DD}} = 10\text{V}$ $V_{\text{IS}} = 0\text{V}$	$T_A = -55^\circ\text{C}$						0.62	mA
			$T_A = -40^\circ\text{C}$						0.5	
			$T_A = 25^\circ\text{C}$						0.5	
			$T_A = 85^\circ\text{C}$						0.3	
			$T_A = 125^\circ\text{C}$						0.35	
		$V_{\text{DD}} = 10\text{V}$ $V_{\text{IS}} = 10\text{V}$	$T_A = -55^\circ\text{C}$						-0.62	mA
			$T_A = -40^\circ\text{C}$						-0.5	
			$T_A = 25^\circ\text{C}$						-0.5	
			$T_A = 85^\circ\text{C}$						-0.3	
			$T_A = 125^\circ\text{C}$						-0.35	
$V_{\text{DD}} = 15\text{V}$ $V_{\text{IS}} = 0\text{V}$	$T_A = -55^\circ\text{C}$						1.8	mA		
	$T_A = -40^\circ\text{C}$						1.4			
	$T_A = 25^\circ\text{C}$						1.5			
	$T_A = 85^\circ\text{C}$						1			
	$T_A = 125^\circ\text{C}$						1.1			
$V_{\text{DD}} = 15\text{V}$ $V_{\text{IS}} = 15\text{V}$	$T_A = -55^\circ\text{C}$						-1.8	mA		
	$T_A = -40^\circ\text{C}$						-1.4			
	$T_A = 25^\circ\text{C}$						-1.5			
	$T_A = 85^\circ\text{C}$						-1			
	$T_A = 125^\circ\text{C}$						-1.1			
V_{OS}	Switch output voltage	$V_{\text{DD}} = 5\text{V}$ $V_{\text{IS}} = 0\text{V}$					0.4	V		
		$V_{\text{DD}} = 5\text{V}$ $V_{\text{IS}} = 5\text{V}$				4.6		V		
		$V_{\text{DD}} = 10\text{V}$ $V_{\text{IS}} = 0\text{V}$					0.5	V		
		$V_{\text{DD}} = 10\text{V}$ $V_{\text{IS}} = 10\text{V}$				9.5		V		
		$V_{\text{DD}} = 15\text{V}$ $V_{\text{IS}} = 0\text{V}$					1.5	V		
		$V_{\text{DD}} = 15\text{V}$ $V_{\text{IS}} = 15\text{V}$				13.5		V		

(1) Peak-to-Peak voltage symmetrical about $(V_{\text{DD}} - V_{\text{EE}}) / 2$.

4.6 Electrical Characteristics

CHARACTERISTIC	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS
		V _{IN} (V)	V _{DD} (V)					+25		
				-55	-40	+85	+125	TYP	MAX	
Quiescent Device Current, I _{DD}		0,5	5	025	0,25	7,5	7,5	0,01	0,25	μA
		0,10	10	0,5	0,5	15	15	0,01	0,5	
		0,15	15	1	1	30	30	0,01	1	
		0,20	20	5	5	150	150	0,02	5	
Signal Inputs (V _{is}) and Output (V _{os})										
On-State Resistance, r _{on} MAX	V _C =V _{DD}	V _{is} =V _{DD} or V _{SS}	10	600	610	840	960	-	660	Ω
	R _L =10k Ω Returned to	V _{is} =4.75 to 5.75V	10	1870	1900	2380	2600	-	2000	
	$\frac{V_{DD}-V_{SS}}{2}$	V _{is} =V _{DD} or V _{SS}	15	360	370	520	600	-	400	
		V _{is} =7.25 to 7.75V	15	775	790	1080	1230	-	850	
Δ On-State Resistance Between Any 2 Switches, Δ r _{on}	R _L =10k Ω, V _C = V _{DD}		5	-	-	-	-	15	-	Ω
			10	-	-	-	-	10	-	
			15	-	-	-	-	5	-	
Total Harmonic Distortion, THD	V _C =V _{DD} =5V, V _{SS} = -5V, V _{is(p-p)} = 5V (Sine wave centered on 0V) R _L = 10k Ω, f _{is} = 1kHz sine wave			-	-	-	-	0,4	-	%
-3dB Cutoff Frequency (Switch on)	V _C =V _{DD} =5V, V _{SS} =-5V, V _{is(p-p)} (Sine wave centered on 0V) R _L =1k Ω,			-	-	-	-	40	-	MHz
-50dB Feed-through Frequency (Switch off)	V _C =V _{SS} = -5V, V _{is(p-p)} =5V (Sine wave centered on 0V) R _L = 1 k Ω			-	-	-	-	1,25	-	MHz
Input/Output Leakage Current (Switch off) I _{is} MAX	V _C = 0V V _{is} = 18V, V _{OS} = 0V; V _{is} = 0V, V _{OS} = 18V	18		±0.1	±0.1	±1	±1	10 ⁻⁴	±0.1	μA
-50dB Crosstalk Frequency	V _C (A) = V _{DD} = +5V, V _C (B) = V _{SS} =-5V, V _{is} (A)= 5V _{p-p} , 50 Ω source R _L = 1k Ω			-	-	-	-	0,9	-	MHz
Propagation Delay (Signal Input to Signal Output) t _{pd}	R _L = 200k Ω V _C = V _{DD} , V _{SS} = GND, C _L = 50pF V _{is} = Square Wave 0 to V _{DD} t _r , t _f = 20ns	5		-	-	-	-	40	100	ns
		10		-	-	-	-	20	40	
		15		-	-	-	-	15	30	
Capacitance: Input, C _{is} Output, C _{OS} Feed-through, C _{ios}	V _{DD} = +5V V _C =V _{SS} =-5V			-	-	-	-	4	-	pF
				-	-	-	-	4	-	
				-	-	-	-	0,2	-	
Control (V _C)										
Control Input Low Voltage, V _{ILC} (MAX)	I _{is} < 10 μA V _{is} = V _{SS} , V _{OS} = V _{DD} and V _{is} = V _{DD} , V _{OS} = V _{SS}	5,10, 15		0,9	0,9	0,4	0,4	-	0,7	V
Control Input High Voltage, V _{IHC}	See 图 4-5	5		3,5 (Min.)						V
		10		7 (Min.)						
		15		11 (Min.)						
Input Current, I _{IN} (MAX)	Input Current, I _{IN} (MAX) V _{is} V _{DD}	18		±0.1	±0.1	±1	±1	±10 ⁻⁵	±0.1	μA
	V _{DD} - V _{SS} = 18V									
	V _{CC} V _{DD} - V _{SS}									
Crosstalk (Control Input to Signal Output)	V _C = 10V (Sq. Wave)	10		-	-	-	-	50	-	mV
	t _r , t _f = 20ns									
	R _L = 10k Ω									

4.6 Electrical Characteristics (续)

CHARACTERISTIC	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS
		V _{IN} (V)	V _{DD} (V)					+25		
				-55	-40	+85	+125	TYP	MAX	
Turn-On Propagation Delay	Turn-On Propagation Delay t _r , t _f = 20ns		5	-	-	-	-	35	70	ns
	C _L = 50pF		10	-	-	-	-	20	40	
	R _L = 1kΩ		15	-	-	-	-	15	30	
Maximum Control Input Repetition Rate	Maximum Control Input Repetition Rate V _{is} = V _{DD} < V _{SS} = GND, R _L = 1kΩ to GND, C _L = 50pF, V _C = 10V (Square wave centered on 5V) t _r , t _f = 20ns, V _{OS} = ½ V _{OS} at 1kHz		10	-	-	-	-	10	-	MHz
Input Capacitance, C _{IN}				-	-	-	-	5	7.5	μF

4.7 Typical Characteristics

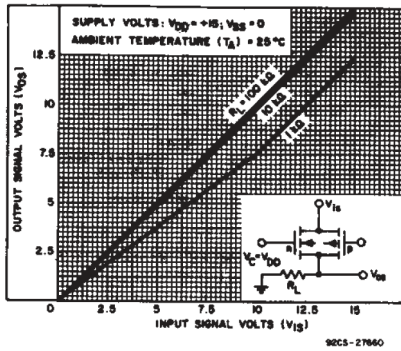


图 4-1. On-state Characteristics for 1 of 4 Switches with v_{DD} = +15V, v_{SS} = 0V.

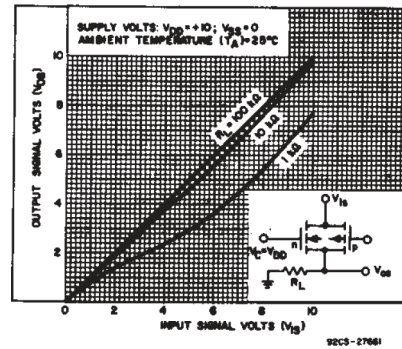


图 4-2. On-state Characteristics for 1 of 4 Switches with v_{DD} = +10V, v_{SS} = 0V.

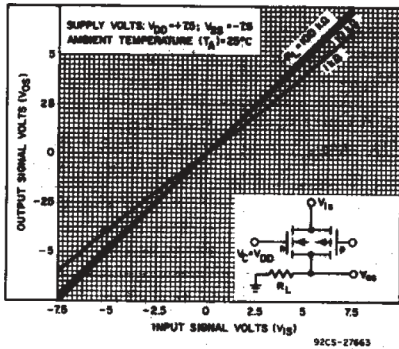


图 4-3. On-state Characteristics for 1 of 4 Switches with v_{DD} = +7.5V, v_{SS} = -7.5V.

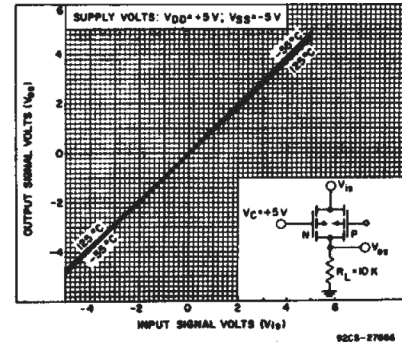


图 4-4. On-state Characteristics as a Function of Temp. for 1 of 4 Switches with v_{DD} = +5V, v_{SS} = -5V.

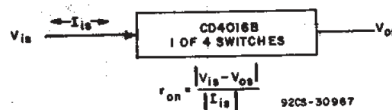


图 4-5. Determination of R_{on} As a Test Condition for Control Input High Voltage Specification.

5 Parameter Measurement Information

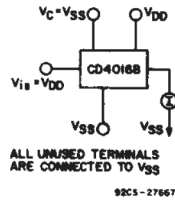


图 5-1. Off-state Switch Input or Output Leakage Current Test Circuit.

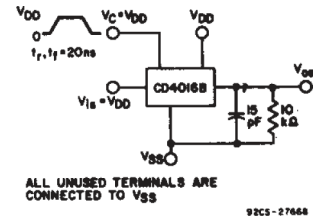


图 5-2. Test Circuit for Square-wave Response.

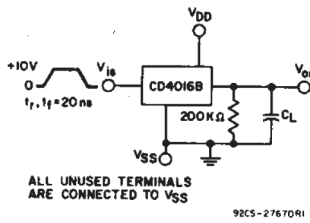


图 5-3. Propagation Delay Time Signal Input (V_{IS}) To Signal Output (V_{OS})

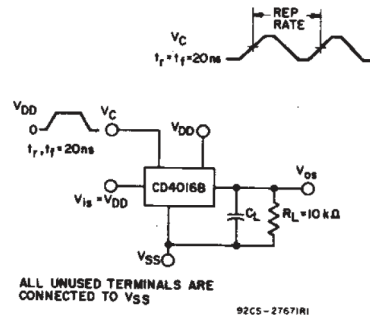


图 5-4. MAX Control-input Repetition Rate.

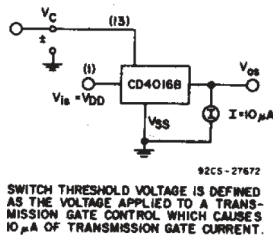


图 5-5. Switch Threshold Voltage.

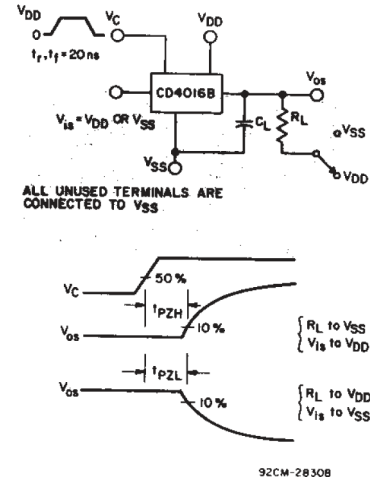


图 5-6. Turn-On Propagation Delay-control Input.

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Documentation Support

6.1.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.1.2 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

6.1.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

6.1.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

6.1.5 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

7 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (September 2003) to Revision D (May 2024)	Page
• Increased IDD max/typ for the lower Temperature cases.....	5
• Changed typical I _{IH} to 0.5μA.....	5
• Changed typical I _{IL} to -0.1μA.....	5

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9064001CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9064001CA CD4016BF3A	Samples
CD4016BE	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4016BE	Samples
CD4016BEE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4016BE	Samples
CD4016BF	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4016BF	Samples
CD4016BF3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9064001CA CD4016BF3A	Samples
CD4016BM96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016BM	Samples
CD4016BNSR	NRND	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4016B	
CD4016BPW	NRND	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B	
CD4016BPWR	NRND	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM016B	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4016B, CD4016B-MIL :

- Catalog : [CD4016B](#)
- Military : [CD4016B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4016BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4016BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4016BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4016BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4016BM96	SOIC	D	14	2500	356.0	356.0	35.0
CD4016BMT	SOIC	D	14	250	210.0	185.0	35.0
CD4016BNSR	SO	NS	14	2000	356.0	356.0	35.0
CD4016BPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4016BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4016BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4016BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4016BEE4	N	PDIP	14	25	506	13.97	11230	4.32
CD4016BM	D	SOIC	14	50	506.6	8	3940	4.32
CD4016BMG4	D	SOIC	14	50	506.6	8	3940	4.32
CD4016BPW	PW	TSSOP	14	90	530	10.2	3600	3.5

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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