# CD74AC253, CD54/74ACT253

Data sheet acquired from Harris Semiconductor
SCHS247A

August 1998 - Revised May 2000

## Dual 4-Input Multiplexer, Three-State

### Features

- **Buffered Inputs**
- **Typical Propagation Delay**
  - **6.3ns at $V_{CC}$ = 5V, $T_A$ = 25°C, $C_L$ = 50pF**
- **Exceeds 2kV ESD Protection MIL-STD-883, Method 3015**
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply**
- **±24mA Output Drive Current**
  - **Fanout to 15 FAST™ ICs**
  - **Drives 50Ω Transmission Lines**

### Description

The CD74AC253 and 'ACT253 dual 4-input multiplexers that utilize Advanced CMOS Logic technology. One of the four sources for each section is selected by the common Select inputs, S0 and S1. When the Output Enable ($\overline{1OE}$ or $\overline{2OE}$) is HIGH, the output is in the high-impedance state.

### Ordering Information

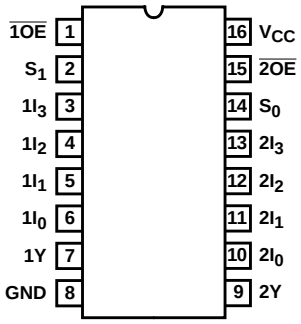
| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|---|---|---|
| CD74AC253E | 0 to 70°C, -40 to 85, -55 to 125 | 16 Ld PDIP |
| CD74AC253M | 0 to 70°C, -40 to 85, -55 to 125 | 16 Ld SOIC |
| CD54ACT253F3A | -55 to 125 | 16 Ld CERDIP |
| CD74ACT253E | 0 to 70°C, -40 to 85, -55 to 125 | 16 Ld PDIP |
| CD74ACT253M | 0 to 70°C, -40 to 85, -55 to 125 | 16 Ld SOIC |

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

### Pinout

**CD54ACT253**
**(CERDIP)**
**CD74AC253, CD74ACT253**
**(PDIP, SOIC)**
**TOP VIEW**




CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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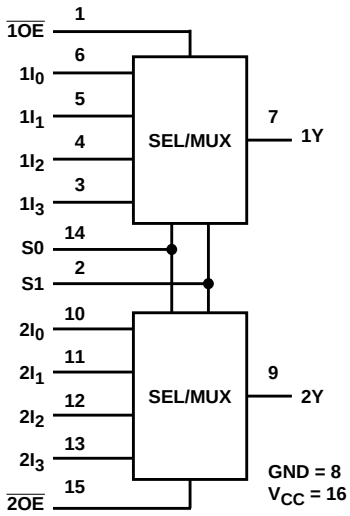
## Functional Diagram




**TRUTH TABLE**

| SELECT INPUTS | | DATA INPUTS | | | | ENABLE INPUTS | OUTPUT |
|---|---|---|---|---|---|---|---|
| S1 | S0 | $nI_0$ | $nI_1$ | $nI_2$ | $nI_3$ | $\overline{nOE}$ | nY |
| X | X | X | X | X | X | H | Z |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| L | H | X | L | X | X | L | L |
| L | H | X | H | X | X | L | H |
| H | L | X | X | L | X | L | L |
| H | L | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

Select inputs S1 and S0 are common to both sections. H = High level, L = Low inputs, X = Don't care, Z = High impedance.

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . -0.5V to 6V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±50mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±50mA
DC $V_{CC}$ or Ground Current, $I_{CC\ or}$ $I_{GND}$ (Note 3) . . . . . ±100mA

## Operating Conditions

Temperature Range, $T_A$ . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$ (Note 4)
AC Types. . . . . 1.5V to 5.5V
ACT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Slew Rate, dt/dv
AC Types, 1.5V to 3V . . . . . 50ns (Max)
AC Types, 3.6V to 5.5V. . . . . 20ns (Max)
ACT Types, 4.5V to 5.5V. . . . . 10ns (Max)

## Thermal Information

Thermal Resistance (Typical, Note 5) $\theta_{JA}$ (°C/W)
PDIP Package . . . . . ___
SOIC Package . . . . . ___
Maximum Junction Temperature (Plastic Package) . . . . . 150C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

3. For up to 4 outputs per device, add ±25mA for each additional output.
4. Unless otherwise specified, all voltages are referenced to ground.
5. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | MAX | MIN | MAX | MIN | MAX | |
| **AC TYPES** | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 1.5 | 1.2 | - | 1.2 | - | 1.2 | - | V |
| | | | | 3 | 2.1 | - | 2.1 | - | 2.1 | - | V |
| | | | | 5.5 | 3.85 | - | 3.85 | - | 3.85 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 1.5 | - | 0.3 | - | 0.3 | - | 0.3 | V |
| | | | | 3 | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | | | 5.5 | - | 1.65 | - | 1.65 | - | 1.65 | V |
| High Level Output Voltage | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.05 | 1.5 | 1.4 | - | 1.4 | - | 1.4 | - | V |
| | | | -0.05 | 3 | 2.9 | - | 2.9 | - | 2.9 | - | V |
| | | | -0.05 | 4.5 | 4.4 | - | 4.4 | - | 4.4 | - | V |
| | | | -4 | 3 | 2.58 | - | 2.48 | - | 2.4 | - | V |
| | | | -24 | 4.5 | 3.94 | - | 3.8 | - | 3.7 | - | V |
| | | | -75 (Note 6, 7) | 5.5 | - | - | 3.85 | - | - | - | V |
| | | | -50 (Note 6, 7) | 5.5 | - | - | - | - | 3.85 | - | V |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Low Level Output Voltage | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.05 | 1.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.05 | 3 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.05 | 4.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 12 | 3 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 24 | 4.5 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 75 (Note 6, 7) | 5.5 | - | - | - | 1.65 | - | - | V |
| | | | 50 (Note 6, 7) | 5.5 | - | - | - | - | - | 1.65 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 5.5 | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Three-State Leakage Current | $I_{OZ}$ | $V_{IH}$ or $V_{IL}$ $V_O = V_{CC}$ or GND | - | 5.5 | - | ±0.5 | - | ±5 | - | ±10 | µA |
| Quiescent Supply Current MSI | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | 8 | - | 80 | - | 160 | µA |
| **ACT TYPES** | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.05 | 4.5 | 4.4 | - | 4.4 | - | 4.4 | - | V |
| | | | -24 | 4.5 | 3.94 | - | 3.8 | - | 3.7 | - | V |
| | | | -75 (Note 6, 7) | 5.5 | - | - | 3.85 | - | - | - | V |
| | | | -50 (Note 6, 7) | 5.5 | - | - | - | - | 3.85 | - | V |
| Low Level Output Voltage | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.05 | 4.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 24 | 4.5 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 75 (Note 6, 7) | 5.5 | - | - | - | 1.65 | - | - | V |
| | | | 50 (Note 6, 7) | 5.5 | - | - | - | - | - | 1.65 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 5.5 | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Three-State or Leakage Current | $I_{OZ}$ | $V_{IH}$ or $V_{IL}$ $V_O = V_{CC}$ or GND | - | 5.5 | - | ±0.5 | - | ±5 | - | ±10 | µA |
| Quiescent Supply Current MSI | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | 8 | - | 80 | - | 160 | µA |
| Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load | $\Delta I_{CC}$ | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 2.4 | - | 2.8 | - | 3 | mA |

NOTES:

6. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
7. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

## ACT Input Load Table

| INPUT | UNIT LOAD |
|---|---|
| S0, S1, $nI_0$, $nI_1$ | 1 |
| $\overline{nOE}$ | 0.83 |

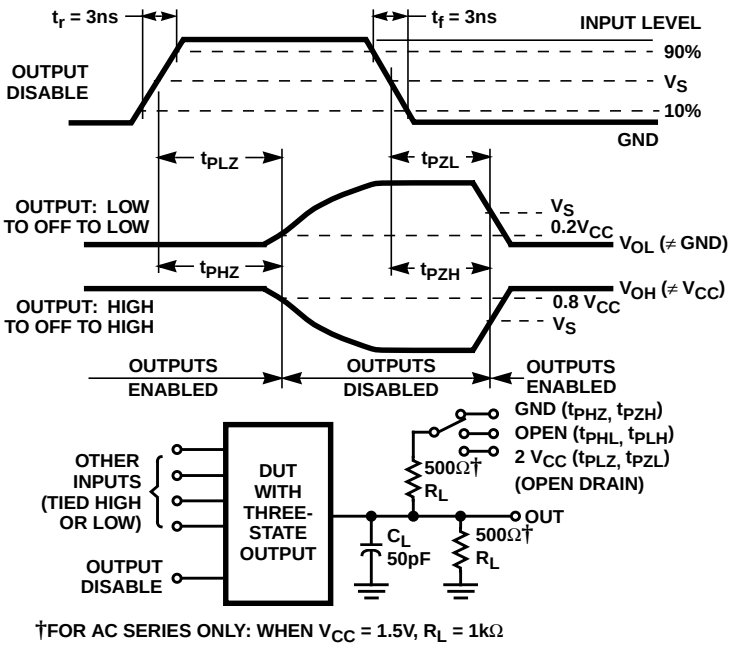
NOTE: Unit load is $\Delta I_{CC}$ limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at $25^oC$.

## Switching Specifications Input $t_r$, $t_f$ = 3ns, $C_L$ = 50pF (Worst Case)

| PARAMETER | SYMBOL | $V_{CC}$ (V) | $-40^oC$ TO $85^oC$ | | | $-55^oC$ TO $125^oC$ | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **AC TYPES** | | | | | | | | | |
| Propagation Delay, S0, S1, to Y | $t_{PLH}$, $t_{PHL}$ | 1.5 | - | - | 227 | - | - | 250 | ns |
| | | 3.3 (Note 9) | 7.2 | - | 25 | 7 | - | 28 | ns |
| | | 5 (Note 10) | 5.2 | - | 18.2 | 5 | - | 20 | ns |
| Propagation Delay, nI to Y | $t_{PLH}$, $t_{PHL}$ | 1.5 | - | - | 151 | - | - | 166 | ns |
| | | 3.3 | 4.8 | - | 16.9 | 4.7 | - | 18.6 | ns |
| | | 5 | 3.4 | - | 12.1 | 3.3 | - | 13.3 | ns |
| Propagation Delay, Output Enable, Output Disable to Y | $t_{PLZ}$, $t_{PHZ}$, $t_{PZL}$, $t_{PZH}$ | 1.5 | - | - | 131 | - | - | 144 | ns |
| | | 3.3 | 4.5 | - | 15.7 | 4.3 | - | 17.3 | ns |
| | | 5 | 3 | - | 10.5 | 2.9 | - | 11.5 | ns |
| Three-State Output Capacitance | $C_O$ | - | - | - | 15 | - | - | 15 | pF |
| Input Capacitance | $C_I$ | - | - | - | 10 | - | - | 10 | pF |
| Power Dissipation Capacitance | $C_{PD}$ (Note 11) | - | - | 107 | - | - | 107 | - | pF |
| **ACT TYPES** | | | | | | | | | |
| Propagation Delay, S0, S1, to Y | $t_{PLH}$, $t_{PHL}$ | 5 (Note 10) | 5.7 | - | 20 | 5.5 | - | 22 | ns |
| Propagation Delay, nI to Y | $t_{PLH}$, $t_{PHL}$ | 5 | 4.6 | - | 16.4 | 4.5 | - | 18 | ns |
| Propagation Delay, Output Enable, Output Disable to Y | $t_{PLZ}$, $t_{PHZ}$, $t_{PZL}$, $t_{PZH}$ | 5 | 3.2 | - | 11.5 | 3.2 | - | 12.6 | ns |
| Three-State Output Capacitance | $C_O$ | - | - | - | 15 | - | - | 15 | pF |
| Input Capacitance | $C_I$ | - | - | - | 10 | - | - | 10 | pF |
| Power Dissipation Capacitance | $C_{PD}$ (Note 11) | - | - | 107 | - | - | 107 | - | pF |

NOTES:

8. Limits tested 100%.
9. 3.3V Min is at 3.6V, Max is at 3V.
10. 5V Min is at 5.5V, Max is at 4.5V.
11. $C_{PD}$ is used to determine the dynamic power consumption per multiplexer.
    AC: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
    ACT: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where $f_i$ = input frequency, $C_L$ = output load capacitance, $V_{CC}$ = supply voltage.




†FOR AC SERIES ONLY: WHEN $V_{CC}$ = 1.5V, $R_L$ = 1kΩ

**FIGURE 1. THREE-STATE PROPAGATION DELAY WAVEFORMS AND TEST CIRCUIT**

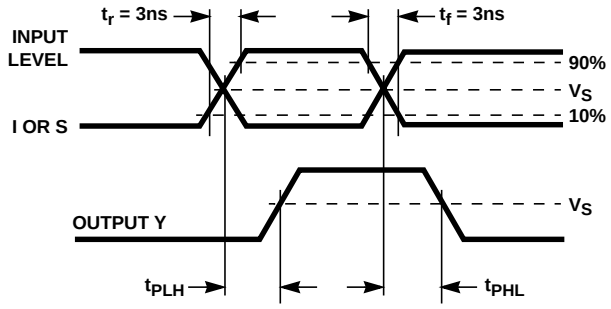
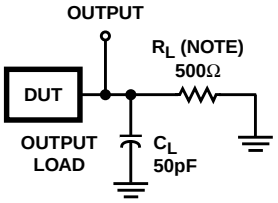



**FIGURE 2. PROPAGATION DELAY TIMES**




NOTE: For AC Series Only: When $V_{CC}$ = 1.5V, $R_L$ = 1kΩ.

| | AC | ACT |
|---|---|---|
| Input Level | $V_{CC}$ | 3V |
| Input Switching Voltage, $V_S$ | 0.5 $V_{CC}$ | 1.5V |
| Output Switching Voltage, $V_S$ | 0.5 $V_{CC}$ | 0.5 $V_{CC}$ |

**FIGURE 3. PROPAGATION DELAY TIMES**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74AC253M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC253M | Samples |
| CD74ACT253E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74ACT253E | Samples |
| CD74ACT253M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT253M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

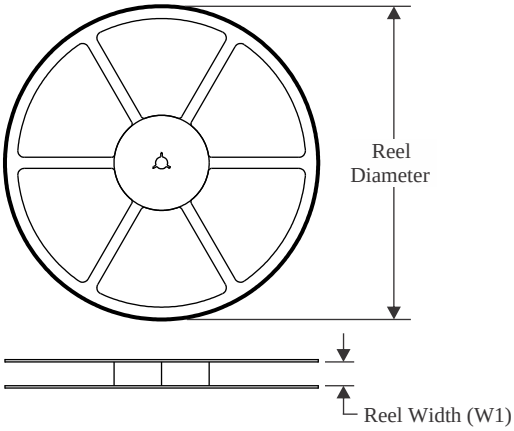
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

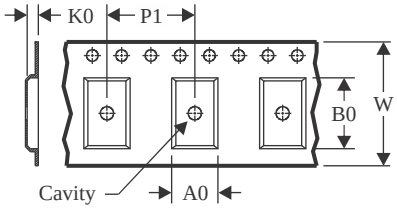
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

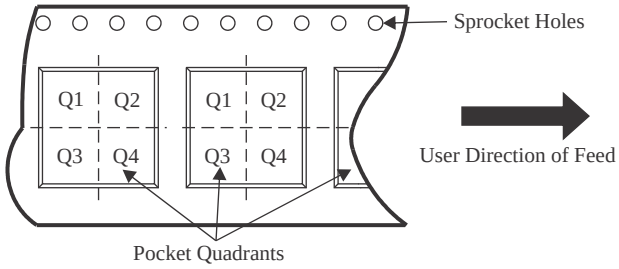



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

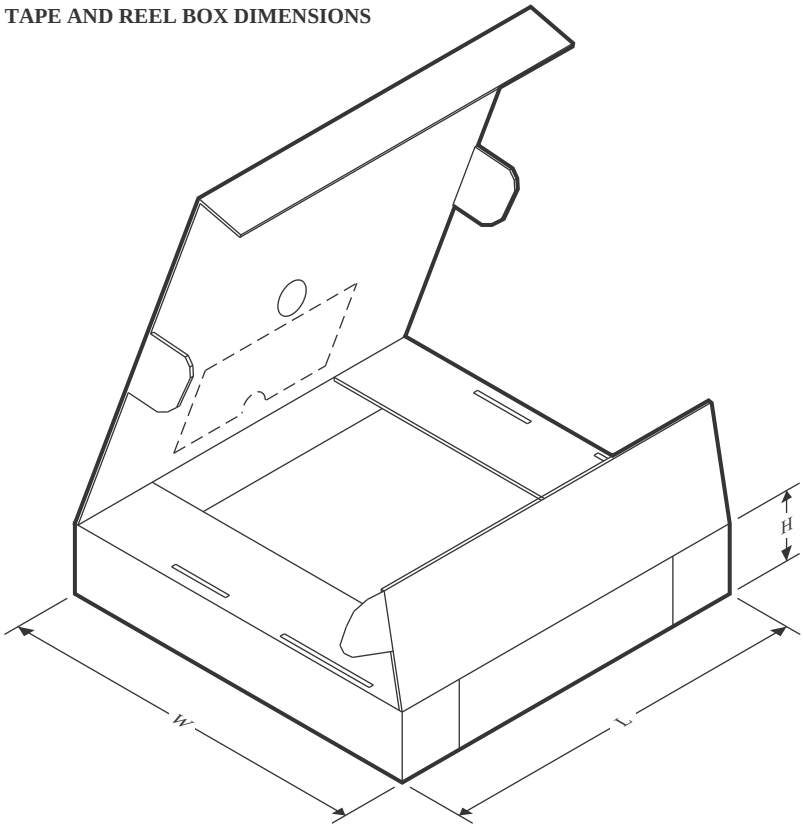
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74AC253M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74ACT253M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

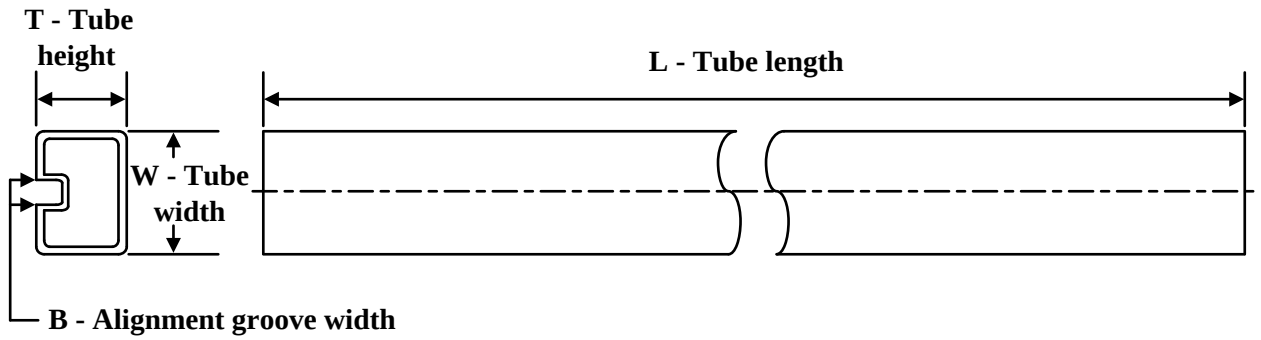
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74AC253M96 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| CD74ACT253M96 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |

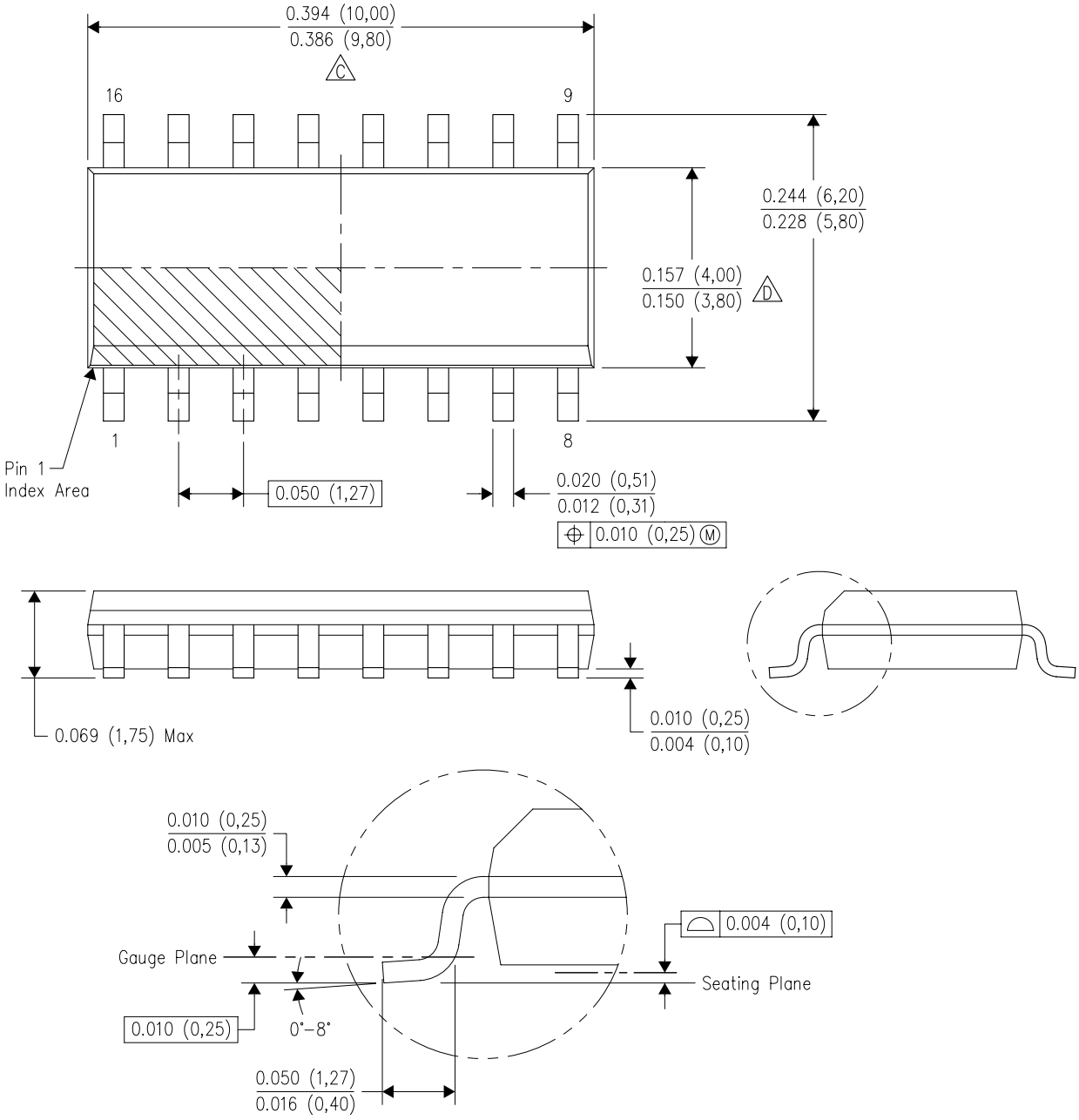
## TUBE




*All dimensions are nominal

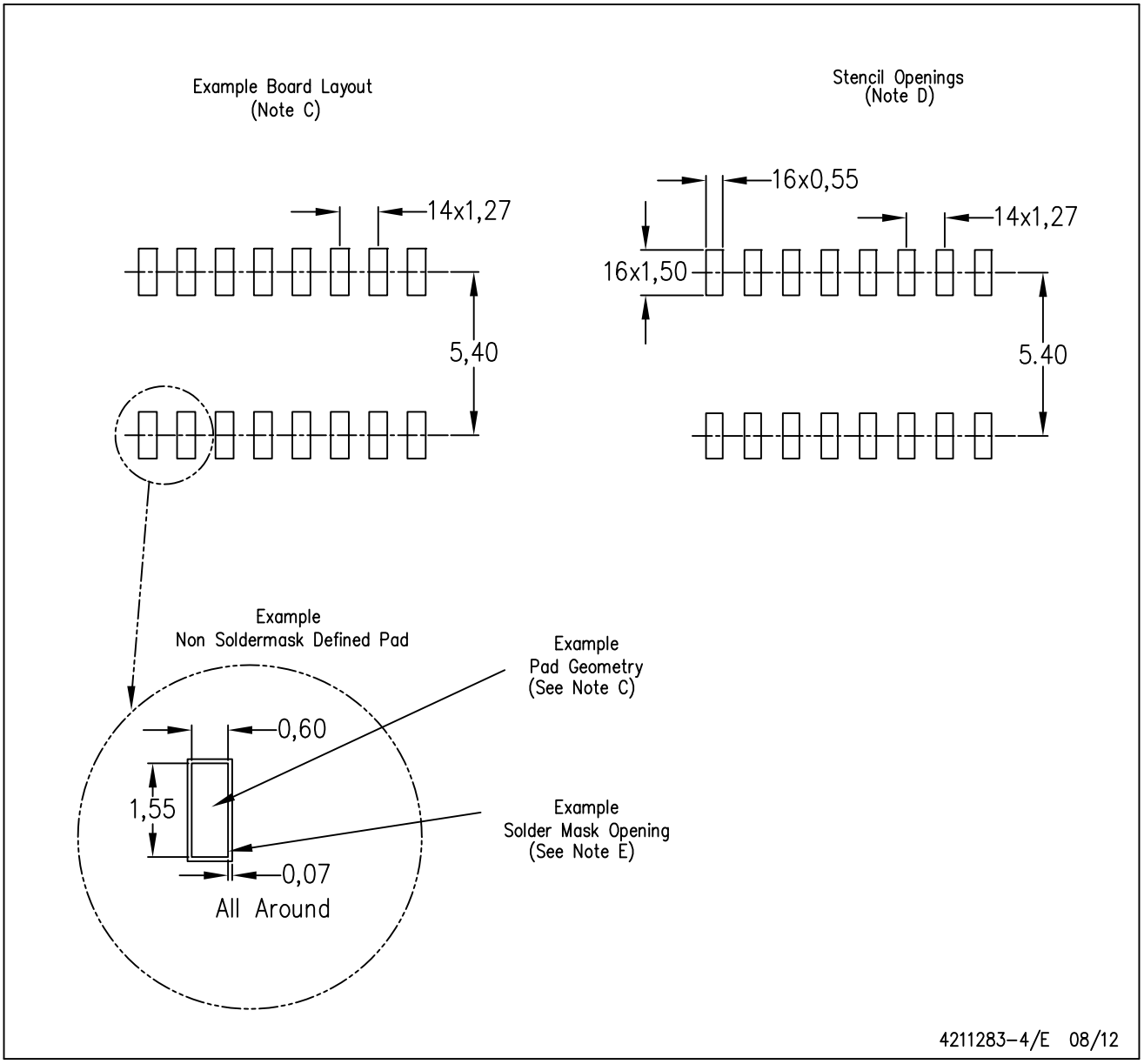
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74ACT253E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT253E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

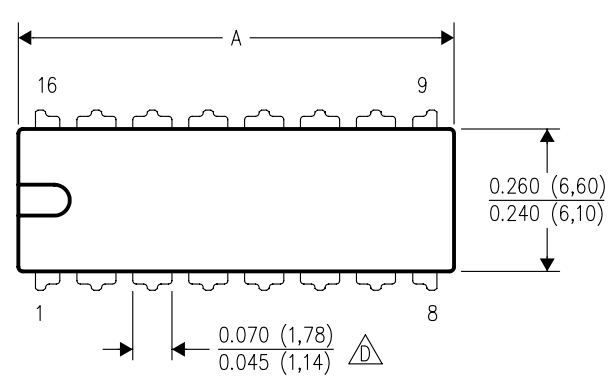



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

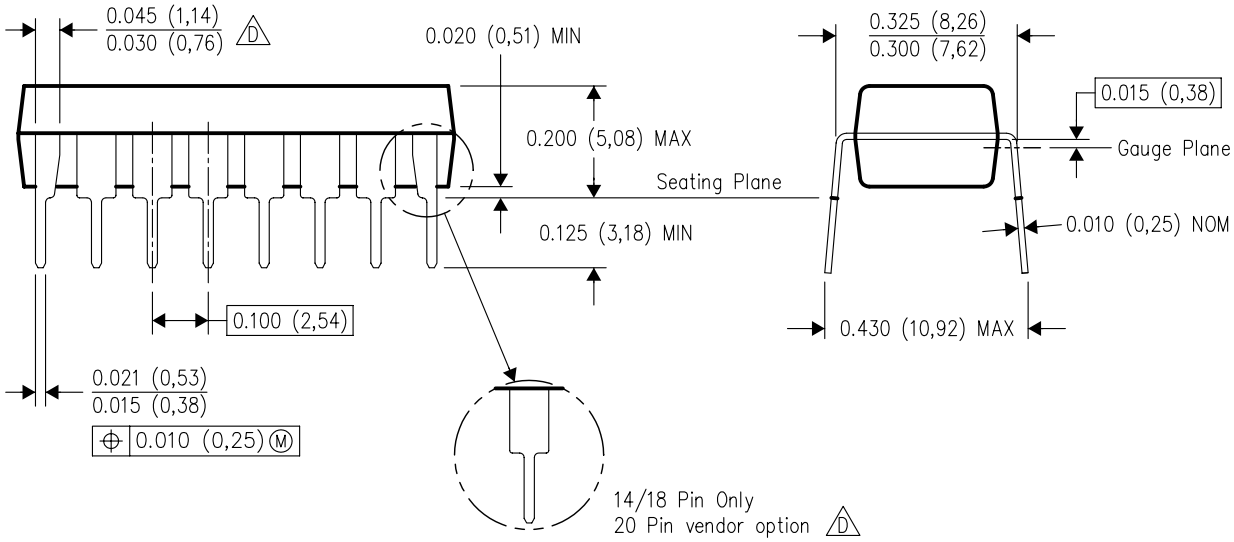
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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