

# CDx4ACT74 具有清零和预设功能的双通道正边沿触发式 D 型触发器

## 1 特性

- 输入兼容 TTL 电压
- 双极 F、AS 和 S 的速度，同时功耗显著降低
- 平衡传播延迟
- $\pm 24\text{mA}$  输出驱动电流
  - 扇出至 15 个 F 器件
- 防 SCR 闩锁 CMOS 工艺和电路设计
- ESD 保护超过 2kV (根据 MIL-STD-883 方法 3015)

## 2 说明

ACT74 双路正边沿触发器是 D 型触发器。

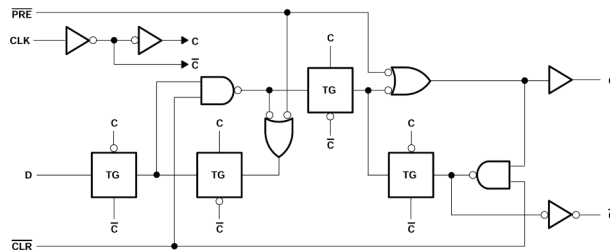
### 器件信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>	本体尺寸 <sup>(3)</sup>
CDx4ACT74	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	N (PDIP, 14)	19.3mm × 9.4mm	19.3mm × 6.35mm
	J (CDIP, 14)	19.56mm × 7.9mm	19.56mm × 6.67mm

(1) 有关更多信息，请参阅节 10。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。

(3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



展示各触发器的逻辑图 (正逻辑)



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### 3 Pin Configuration and Functions

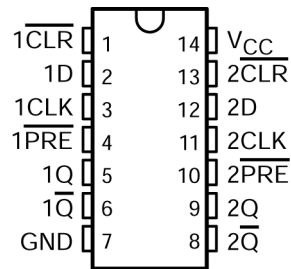


图 3-1. D, N, or J Package  
14-Pin SOIC, PDIP, or CDIP  
(Top View)

表 3-1. Pin Functions

PIN		TYPE <sup>1</sup>	DESCRIPTION
NAME	NO.		
1CLR	1	I	Asynchronous clear for channel 1, active low
1D	2	I	Data for channel 1
1CLK	3	I	Clock for channel 1, rising edge triggered
1PRE	4	I	Asynchronous preset for channel 1, active low
1Q	5	O	Output for channel 1
1Q̄	6	O	Inverted output for channel 1
GND	7	G	Ground
2Q̄	8	O	Inverted output for channel 2
2Q	9	O	Output for channel 2
2PRE	10	I	Asynchronous preset for channel 2, active low
2CLK	11	I	Clock for channel 2, rising edge triggered
2D	12	I	Data for channel 2
2CLR	13	I	Asynchronous clear for channel 2, active low
V <sub>CC</sub>	14	P	Positive supply

1. Signal Types: I = Input, O = Output, I/O = Input or Output.

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range,	- 0.5	6	V
$I_{IK}^{(2)}$	Input clamp current	$(V_I < 0 \text{ or } V_I > V_{CC})$		±20 mA
$I_{OK}^{(2)}$	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		±50 mA
$I_O$	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		±50 mA
	Continuous current through $V_{CC}$ or GND		±100	mA
$T_{stg}$	Storage temperature range	- 65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/ JEDEC JS-001 <sup>(1)</sup>	±2000 V

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		$T_A = 25^\circ\text{C}$		$-55^\circ\text{C to } 125^\circ\text{C}$		$-40^\circ\text{C to } 85^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24		-24		-24	mA
$I_{OL}$	Low-level output current		24		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10		10	ns/V

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### 4.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		CD74ACT74		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80	119.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C		-55°C to 125°C		-40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4		4.4		4.4	V	
		I <sub>OH</sub> = -24 mA	4.5 V	3.94		3.7		3.8		
		I <sub>OH</sub> = -50 mA <sup>(1)</sup>	5.5 V			3.85				
		I <sub>OH</sub> = -75 mA <sup>(1)</sup>	5.5 V					3.85		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	4.5 V		0.1		0.1		V	
		I <sub>OL</sub> = 24 mA	4.5 V		0.36		0.5			0.44
		I <sub>OL</sub> = 50 mA <sup>(1)</sup>	5.5 V				1.65			
		I <sub>OL</sub> = 75 mA <sup>(1)</sup>	5.5 V							1.65
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		5.5 V		±0.1		±1		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		5.5 V		4		80		40	μA
ΔI <sub>CC</sub> <sup>(2)</sup>	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V		4.5 V to 5.5 V		2.4		3		2.8	mA
C <sub>i</sub>					10		10		10	pF

- (1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.
- (2) Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

表 4-1. Act Input Load Table

INPUT	UNIT LOAD
Data	0.53
PRE or CLR	0.58
CLK	1

## 4.6 Timing Requirements

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

			-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency			85		97	MHz
t <sub>w</sub>	Pulse duration	PRE or CLR low		5		4.4	ns
		CLK		5.7		5	
t <sub>su</sub>	Setup time	Data		4		3.5	ns
		PRE or CLR inactive					
t <sub>h</sub>	Hold time	Data after CLK ↑		0		0	ns
t <sub>rec</sub>	Recovery time, before CLK	CLR ↑ or PRE ↑		2.7		2.4	ns

## 4.7 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f <sub>max</sub>				85		97	MHz

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 over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

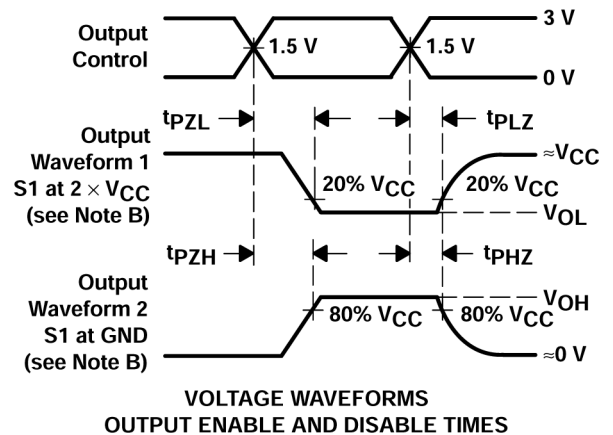
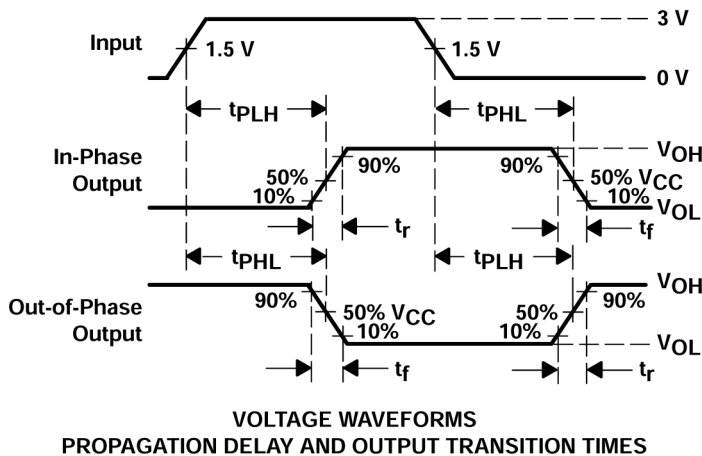
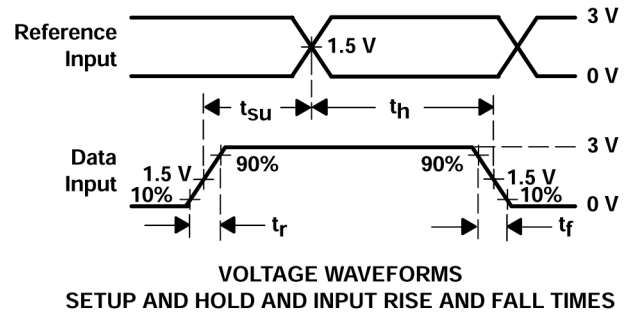
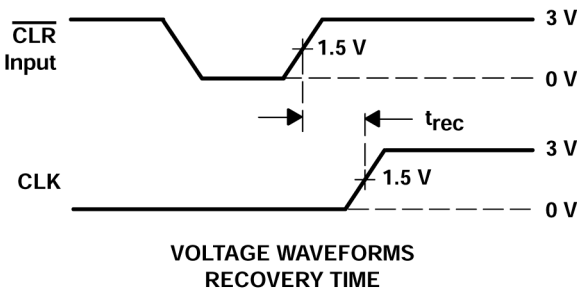
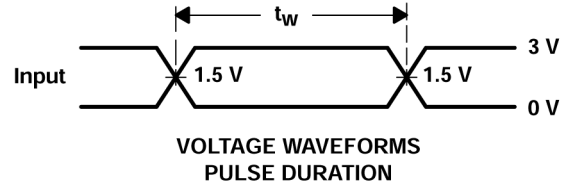
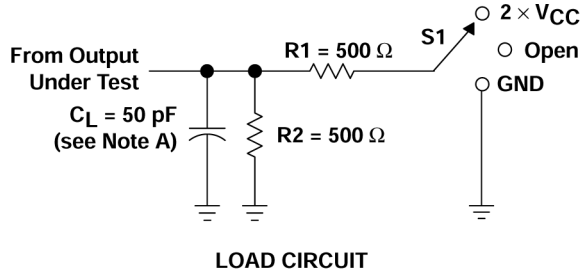
PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	CLK	Q or $\bar{Q}$	2.4	9.5	2.5	8.6	ns
$t_{PHL}$			2.4	9.5	2.5	8.6	
$t_{PLH}$	$\overline{PRE}$ or $\overline{CLR}$	Q or $\bar{Q}$	2.9	11.5	3	10.5	ns
$t_{PHL}$			3.1	12.5	3.2	11.4	

## 4.8 Operating Characteristics

 $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

PARAMETER	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	55	pF

## 5 Parameter Measurement Information



- $C_L$  includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ . Phase relationships between waveforms are arbitrary.
- For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
- The outputs are measured one at a time with one input transition per measurement.
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

图 5-1. Load Circuit and Voltage Waveforms

TEST	S1
$t_{PLH}/t_{PHL}$	Open

TEST	S1
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



## 6 Detailed Description

### 6.1 Overview

A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

### 6.2 Functional Block Diagram

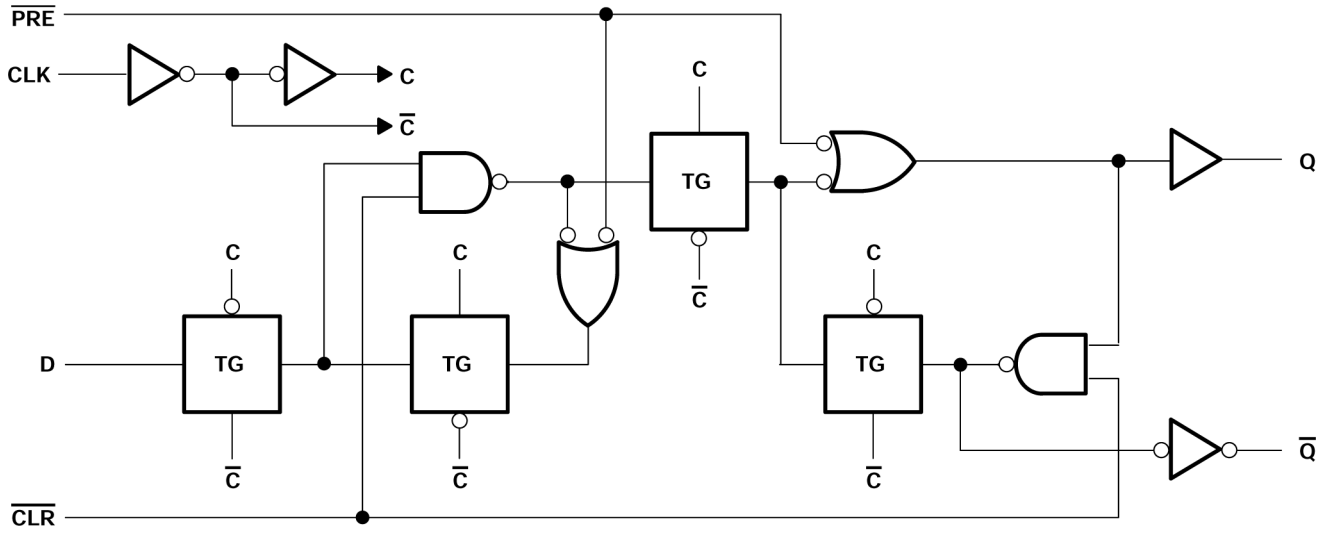


图 6-1. Logic Diagram, Each Flip-flop (Positive Logic)

### 6.3 Device Functional Modes

Function Table (Each Flip-Flop)

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>(1)</sup>	H <sup>(1)</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

- (1) This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

## 7 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [节 4.3](#). Each  $V_{CC}$  terminal should have a bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

#### 7.2.2 Layout Example

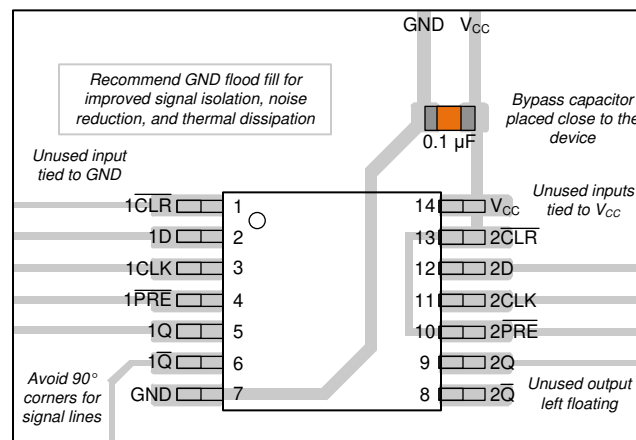


图 7-1. Example layout for the CD74ACT74

## 8 Device and Documentation Support

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54ACT74	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
CD74ACT74	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 8.3 支持资源

TI E2E™ [中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (December 2002) to Revision A (July 2024)	Page
• 添加了 <a href="#">器件信息表</a> 、 <a href="#">引脚功能表</a> 、 <a href="#">ESD 等级表</a> 、 <a href="#">热性能信息表</a> 、 <a href="#">器件功能模式</a> 、“应用和实施”部分、 <a href="#">器件和文档支持</a> 部分以及 <a href="#">机械</a> 、 <a href="#">封装和可订购信息</a> 部分.....	1
• Updated R <sub>θ</sub> JA values: D = 86 to 119.9, all values in °C/W.....	4

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54ACT74F3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54ACT74F3A	<a href="#">Samples</a>
CD74ACT74E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74ACT74E	<a href="#">Samples</a>
CD74ACT74M	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	ACT74M	
CD74ACT74M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT74M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54ACT74, CD74ACT74 :**

- Catalog : [CD74ACT74](#)
- Automotive : [CD74ACT74-Q1](#), [CD74ACT74-Q1](#)
- Military : [CD54ACT74](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

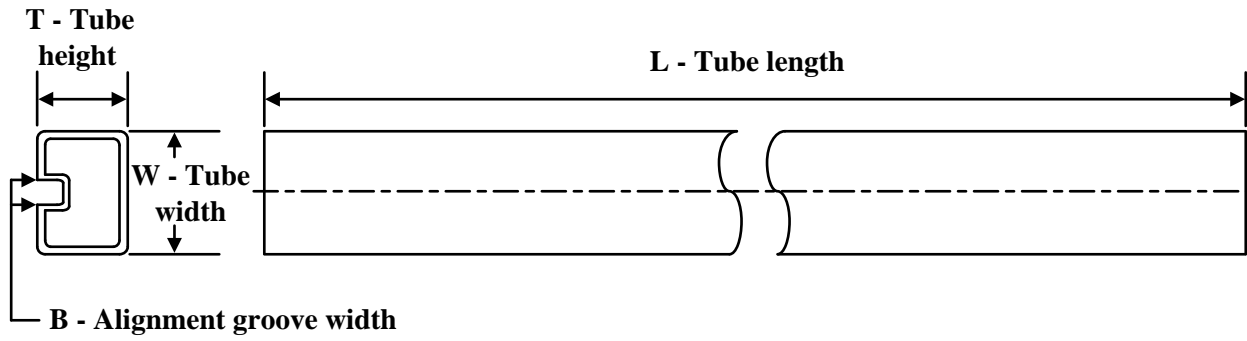

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT74M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74ACT74M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT74M96	SOIC	D	14	2500	353.0	353.0	32.0
CD74ACT74M96	SOIC	D	14	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74ACT74E	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT74E	N	PDIP	14	25	506	13.97	11230	4.32



J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G



# J0014A

# PACKAGE OUTLINE

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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