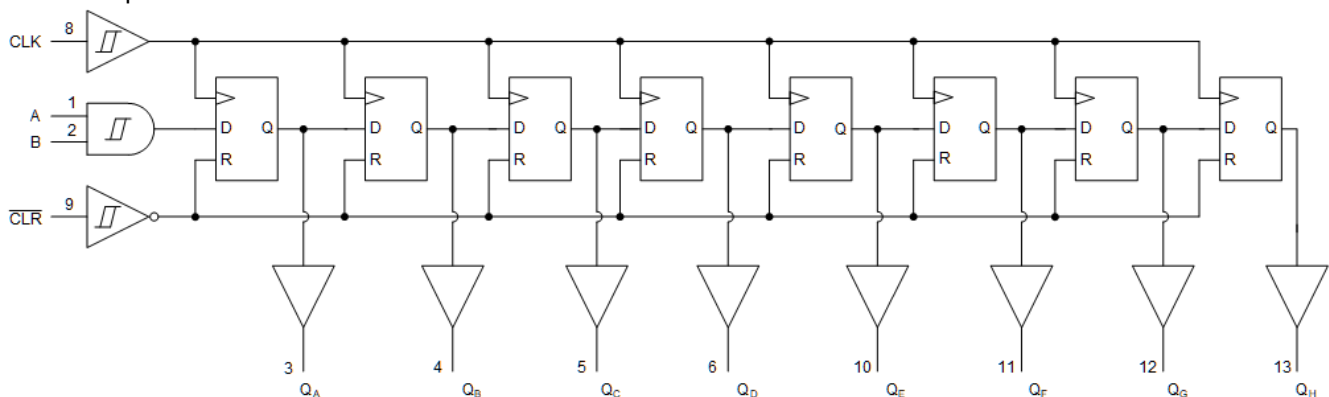


## CDx4HC164、CDx4HCT164 高速 CMOS 逻辑 8 位串行输入/并行输出移位寄存器

### 1 特性

- 缓冲输入
- 异步复位
- 当  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$  时,  $f_{MAX}$  典型值 = 60MHz
- 扇出 (过热范围)
  - 标准输出: 10 个 LSTTL 负载
  - 总线驱动器输出: 15 个 LSTTL 负载
- 宽工作温度范围:  $-55^\circ C$  至  $125^\circ C$
- 平衡的传播延迟及转换时间
- 与 LSTTL 逻辑 IC 相比, 可显著降低功耗
- HC 类型
  - 工作电压为 2V 至 6V
  - 高抗噪性: 当  $V_{CC} = 5V$  时,  $N_{IL} = 30\%$ ,  $N_{IH} = V_{CC}$  的 30%
- HCT 类型
  - 工作电压为 4.5V 至 5.5V
  - 直接 LSTTL 输入逻辑兼容性,  $V_{IL} = 0.8V$  (最大值),  $V_{IH} = 2V$  (最小值)
  - CMOS 输入兼容性, 当电压为  $V_{OL}$ 、 $V_{OH}$  时,  $I_i \leq 1\mu A$



功能方框图

### 2 说明

'HC164 和 'HCT164 是具有异步复位功能的 8 位串行输入/并行输出移位寄存器。数据在时钟 (CLK) 正边沿发生移位。复位 ( $\overline{CLR}$ ) 引脚上的低电平将移位寄存器复位, 无论输入情况如何, 所有输出均进入低电平状态。提供的两个串行数据输入 (A 和 B) 中的任何一个都可用作数据使能控制。

#### 器件信息

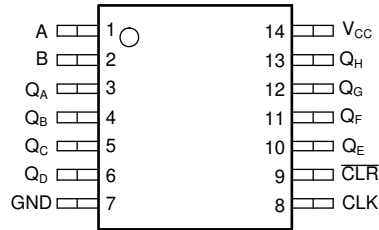
器件型号	封装 <sup>(1)</sup>	本体尺寸 (标称值)
CD74HC164M	SOIC (14)	8.65mm × 3.90mm
CD74HCT164M	SOIC (14)	8.65mm × 3.90mm
CD74HC164E	PDIP (14)	19.31mm × 6.35mm
CD74HCT164E	PDIP (14)	19.31mm × 6.35mm
CD54HC164F	CDIP (14)	19.55mm × 6.71mm

(1) 有关所有可选封装, 请参阅节 11。

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### 3 Pin Configuration and Functions



**J, D, and N Package  
14-Pin CDIP, SOIC, and PDIP  
Top View**

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	(V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> )		±20 mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	(V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )		±20 mA
I <sub>O</sub>	Continuous output current	(V <sub>O</sub> = 0 to V <sub>CC</sub> )		±25 mA
	Continuous current through V <sub>CC</sub> or GND			±50 mA
T <sub>J</sub>	Junction temperature			150 °C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 Recommended Operating Conditions

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V <sub>I</sub> , V <sub>O</sub>	Input or output voltage	0	V <sub>CC</sub>	V	
	Input rise and fall time	2 V	1000	ns	
		4.5 V	500		
		6 V	400		
T <sub>A</sub>	Temperature range	-55	125	°C	

### 4.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		D (SOIC)	N (PDIP)	UNIT
		14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	86	80	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

#### 4.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	V <sub>CC</sub> (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
V <sub>IH</sub>	High level input voltage		2	1.5		1.5		1.5		V	
			4.5	3.15		3.15		3.15			
			6	4.2		4.2		4.2			
V <sub>IL</sub>	Low level input voltage		2	0.5		0.5		0.5		V	
			4.5	1.35		1.35		1.35			
			6	1.8		1.8		1.8			
V <sub>OH</sub>	High level output voltage	I <sub>OH</sub> = -20 μA	2	1.9		1.9		1.9		V	
		I <sub>OH</sub> = -20 μA	4.5	4.4		4.4		4.4			
		I <sub>OH</sub> = -20 μA	6	5.9		5.9		5.9			
	High level output voltage	I <sub>OH</sub> = -4 mA	4.5	3.98		3.84		3.7			
		I <sub>OH</sub> = -5.2 mA	6	5.48		5.34		5.2			
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 20 μA	2	0.1		0.1		0.1		V	
		I <sub>OL</sub> = 20 μA	4.5	0.1		0.1		0.1			
		I <sub>OL</sub> = 20 μA	6	0.1		0.1		0.1			
	Low level output voltage	I <sub>OL</sub> = 4 mA	4.5	0.26		0.33		0.4			
		I <sub>OL</sub> = 5.2 mA	6	0.26		0.33		0.4			
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6	±0.1		±1		±1		μA	
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND	6	8		80		160		μA	
<b>HCT TYPES</b>											
V <sub>IH</sub>	High level input voltage		4.5 to 5.5	2		2		2		V	
V <sub>IL</sub>	Low level input voltage		4.5 to 5.5	0.8		0.8		0.8		V	
V <sub>OH</sub>	High level output voltage	I <sub>OH</sub> = -20 μA	4.5	4.4		4.4		4.4		V	
	High level output voltage	I <sub>OH</sub> = -4 μA	4.5	3.98		3.84		3.7			
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 20 μA	4.5	0.1		0.1		0.1		V	
	Low level output voltage	I <sub>OL</sub> = 4 μA	4.5	0.26		0.33		0.4			
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	±0.1		±1		±1		μA	
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	8		80		160		μA	
ΔI <sub>CC</sub> <sup>(2) (3)</sup>	Additional supply current per input pin	Date Shift-In (1,2)	4.5 to 5.5	100 108		135		147		μA	
		CLR	4.5 to 5.5	100 324		405		441		μA	
		CLK	4.5 to 5.5	100 252		315		343		μA	

(1) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

(3) Inputs held at V<sub>CC</sub> - 2.1.

## 4.5 Prerequisite for Switching Characteristics

PARAMETER		V <sub>CC</sub> (V)	25°C		– 40°C to 85°C		– 55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>									
f <sub>MAX</sub>	Maximum clock frequency	2	6	5	4	MHz			
		4.5	30	24	20	MHz			
		6	35	28	24	MHz			
t <sub>W</sub>	CLR pulse width	2	60	75	90	ns			
		4.5	12	15	18	ns			
		6	10	13	15	ns			
t <sub>w</sub>	CLK pulse width	2	80	100	120	ns			
		4.5	16	20	24	ns			
		6	14	17	20	ns			
t <sub>SU</sub>	Set-up time	2	60	75	90	ns			
		4.5	12	15	18	ns			
		6	10	13	15	ns			
t <sub>H</sub>	Hold time	2	4	4	4	ns			
		4.5	4	4	4	ns			
		6	4	4	4	ns			
t <sub>REM</sub>	CLR to clock, Removal time	2	80	100	120	ns			
		4.5	16	20	24	ns			
		6	14	17	20	ns			
<b>HCT TYPES</b>									
f <sub>MAX</sub>	Maximum clock frequency	4.5	27	22	18	MHz			
t <sub>W</sub>	CLR pulse width	6	18	23	27	ns			
t <sub>w</sub>	CLK pulse width	4.5	18	23	27	ns			
t <sub>SU</sub>	Set-up time	6	12	15	18	ns			
t <sub>H</sub>	Hold time	4.5	4	4	4	ns			
t <sub>REM</sub>	CLR to clock, Removal time	6	16	20	24	ns			

## 4.6 Switching Characteristics

 Input  $t_r$ ,  $t_f = 6\text{ns}$ .  $C_L = 50\text{pF}$  unless otherwise noted

PARAMETER		$V_{CC}$ (V)	25°C		- 40°C to 85°C	- 55°C to 125°C	UNIT
			TYP	MAX	MAX	MAX	
<b>HC TYPES</b>							
$t_{PLH}$ , $t_{PHL}$	CLK to Q	2		170	212	255	ns
		4.5	14 <sup>(3)</sup>	34	43	51	ns
		6		29	36	43	ns
$t_{PLH}$ , $t_{PHL}$	$\overline{\text{CLR}}$ to Q	2		140	175	210	ns
		4.5	11 <sup>(3)</sup>	28	35	42	ns
		6		24	30	36	ns
$t_{TLH}$ , $t_{THL}$	Output transition times	2		75		110	ns
		4.5		15		22	ns
		6		13		19	ns
$f_{MAX}$	Maximum clock frequency	5	60 <sup>(3)</sup>				ns
$C_{IN}$	Input capacitance			10	10	10	pF
$C_{PD}$	Power dissipation capacitance <sup>(1) (2)</sup>	5	47				pF
<b>HCT TYPES</b>							
$t_{PLH}$ , $t_{PHL}$	CLK to Q	4.5		36	45	54	ns
		5	15 <sup>(3)</sup>				
$t_{PLH}$ , $t_{PHL}$	$\overline{\text{CLR}}$ to Q	4.5		38	46	57	ns
		5	16 <sup>(3)</sup>				
$t_{TLH}$ , $t_{THL}$	Output Transition time	4.5		15	19	22	ns
$C_{IN}$	Input Capacitance						pF
$f_{MAX}$	Maximum clock frequency		54 <sup>(4)</sup>				MHz
$C_{PD}$	Power dissipation capacitance <sup>(1) (2)</sup>	5	49	10	10	10	pF

 (1)  $C_{PD}$  is used to determine the dynamic power consumption, per device.

 (2)  $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 + f_O)$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

 (3)  $C_L = 15\text{pF}$ .  $V_{CC} = 5$ .

 (4)  $C_L = 15\text{pF}$ .

## 5 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{MHz}$ ,  $Z_O = 50\Omega$ ,  $t_f < 6\text{ns}$ .

For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.

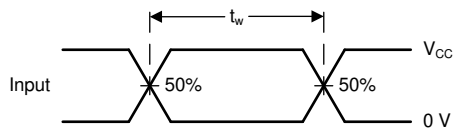


图 5-1. Voltage Waveforms, Standard CMOS Inputs Pulse Duration

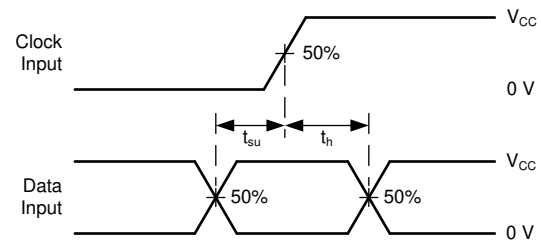


图 5-2. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times

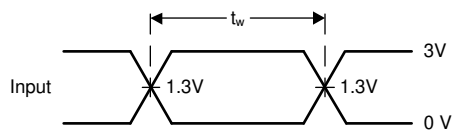


图 5-3. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration

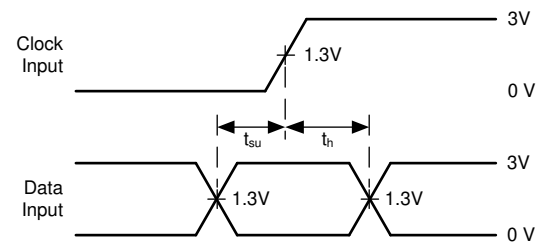


图 5-4. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times



## 6 Detailed Description

### 6.1 Overview

The ' HC164 and ' HCT164 are 8-bit, serial-in, parallel-out, shift registers with asynchronous reset. Data is shifted on the positive edge of Clock (CLK). A LOW on the RESET (CLR) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (A and B) are provided, either one can be used as a data enable control.

### 6.2 Functional Block Diagram

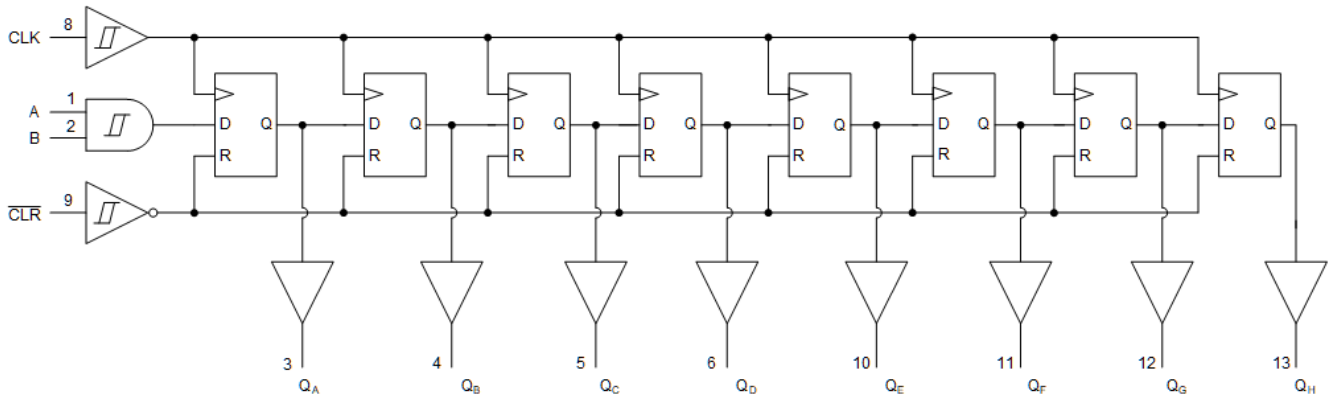


图 6-1. Functional Block Diagram

### 6.3 Device Functional Modes

Truth Table<sup>(1)</sup>

OPERATING MODE	INPUTS				OUTPUTS	
	CLR	CLK	A	B	QA	QB - QH
RESET (CLEAR)	L	X	X	X	L	L - L
Shift	H	↑	l	l	L	q <sub>A</sub> - q <sub>F</sub>
	H	↑	l	h	L	q <sub>A</sub> - q <sub>F</sub>
	H	↑	h	l	L	q <sub>A</sub> - q <sub>F</sub>
	H	↑	h	h	H	q <sub>A</sub> - q <sub>F</sub>

- (1) H = High voltage level.  
h = High voltage level one set-up time prior to the low-to-high clock transition.  
l = Low voltage level one set-up time prior to the low-to-high clock transition.  
L = Low voltage level.  
X = Don't care.  
↑ = Transition from low to high level.  
q<sub>n</sub> = Lower case letters indicate the state of the reference input clock transition.

## 7 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating, located in the [Recommended Operating Conditions](#). Each  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. TI recommends a  $0.1\ \mu\text{F}$  capacitor for this device. Paralleling multiple bypass caps is acceptable to reject different frequencies of noise. The  $0.1\ \mu\text{F}$  and  $1\ \mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for better results.

## 8 Layout

### 8.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not be left floating. In many cases, functions of digital logic devices, or parts of functions, are unused. For example, when a triple-input AND gate only uses two inputs or the buffer gates only use three of the four buffers. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Documentation Support

#### 9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

#### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

#### 9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

#### 9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (March 2022) to Revision E (March 2024)	Page
• 更新了“功能方框图”图.....	1

Changes from Revision C (August 2003) to Revision D (March 2022)	Page
• 通篇更新了编号、格式、表格、图和交叉参考，以反映当前数据表标准.....	1
• Updated naming conventions to reflect modern TI function. DS1 is now A; DS2 is now B; Q <sub>0</sub> is now Q <sub>A</sub> ; Q <sub>1</sub> is now Q <sub>B</sub> ; Q <sub>2</sub> is now Q <sub>C</sub> ; Q <sub>3</sub> is now Q <sub>D</sub> ; CP is now CLK; MR is now CLR; Q <sub>4</sub> is now Q <sub>E</sub> ; Q <sub>5</sub> is now Q <sub>F</sub> ; Q <sub>6</sub> is now Q <sub>G</sub> ; Q <sub>7</sub> is now Q <sub>H</sub> .....	3

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8970401CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8970401CA CD54HCT164F3A	<a href="#">Samples</a>
CD54HC164F	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC164F	<a href="#">Samples</a>
CD54HC164F3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8416201CA CD54HC164F3A	<a href="#">Samples</a>
CD54HCT164F3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8970401CA CD54HCT164F3A	<a href="#">Samples</a>
CD74HC164E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC164E	<a href="#">Samples</a>
CD74HC164M	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	HC164M	
CD74HC164M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC164M	<a href="#">Samples</a>
CD74HC164M96G4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC164M	<a href="#">Samples</a>
CD74HC164MT	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	HC164M	
CD74HCT164E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT164E	<a href="#">Samples</a>
CD74HCT164M	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	HCT164M	
CD74HCT164M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	(HCT164, HCT164M)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HC164, CD54HCT164, CD74HC164, CD74HCT164 :**

- Catalog : [CD74HC164](#), [CD74HCT164](#)
- Military : [CD54HC164](#), [CD54HCT164](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC164M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT164M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT164M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC164M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HCT164M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HCT164M96	SOIC	D	14	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC164E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC164E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT164E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT164E	N	PDIP	14	25	506	13.97	11230	4.32



J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

D0014A



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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