CDx4HC374 三态正边沿触发式高速 CMOS 逻辑八路 D 型触发器

1 特性

- 缓冲输入
- 通用三态输出使能控制
- 三态输出
- 总线驱动能力
- 当 V_{CC} = 5V，C_L = 15pF, T_A = 25℃ 时的传播延迟典型值（时钟到 Q）= 15ns
- 扇出（在温度范围内）
  - 标准输出：10 个 LSTTL 负载
  - 总线驱动器输出：15 个 LSTTL 负载
- 宽工作温度范围：–55℃ 至 125℃
- 平衡的传播延迟及转换时间
- 与 LSTTL 逻辑 IC 相比，功耗显著降低
- HC 类型
  - 2V 至 6V 工作电压
  - 高抗噪性：当 V_{CC} = 5V 时，N_{IL} = 30%，N_{IH} = V_{CC} 的 30%
- HCT 类型
  - 4.5V 至 5.5V 工作电压
  - 直接 LSTTL 输入逻辑兼容性，V_{IL} = 0.8V（最大值），V_{IH} = 2V（最小值）
  - CMOS 输入兼容性，当电压为 V_{OL}、V_{OH} 时，I_I ≤ 1μA

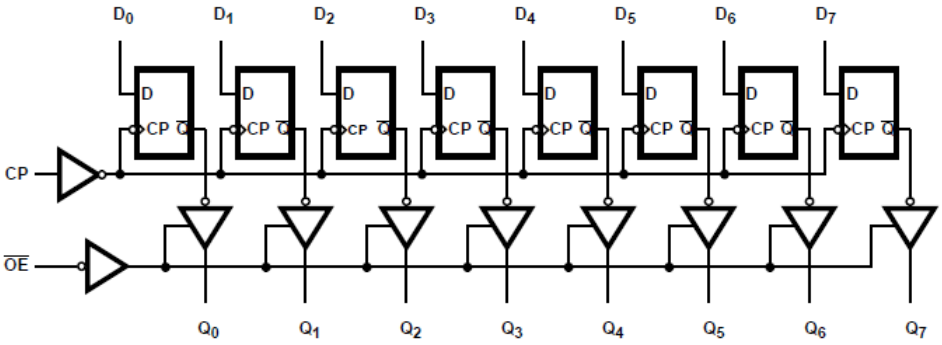
2 说明

’HC374、’HCT374、’HC574 和 ’HCT574 是八路 D 型触发器，具有三态输出，能够驱动 15 个 LSTTL 负载。八个边沿触发式触发器在时钟 (CP) 从低电平向高电平转换时将数据输入其寄存器。输出使能端 ($\overline{OE}$) 控制三态输出，不受寄存器操作的影响。当 $\overline{OE}$ 为高电平时，输出处于高阻态。374 和 574 功能相同，只是引脚排列方式不同。

器件信息

器件型号	封装[1]	封装尺寸（标称值）
CD54HC374F3A	CDIP (20)	26.92mm × 6.92mm
CD54HC574F	CDIP (20)	26.92mm × 6.92mm
CD54HCT374F3A	CDIP (20)	26.92mm × 6.92mm
CD54HCT574F	CDIP (20)	26.92mm × 6.92mm
CD74HC374M	SOIC (20)	12.80mm × 7.50mm
CD74HC574M	SOIC (20)	12.80mm × 7.50mm
CD74HCT374M	SOIC (20)	12.80mm × 7.50mm
CD74HCT574M	SOIC (20)	12.80mm × 7.50mm
CD74HC374E	PDIP (20)	25.40mm × 6.35mm
CD74HC574E	PDIP (20)	25.40mm × 6.35mm
CD74HCT374E	PDIP (20)	25.40mm × 6.35mm
CD74HCT574E	PDIP (20)	25.40mm × 6.35mm
CD74HCT574PWR	TSSOP (20)	6.50mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能图

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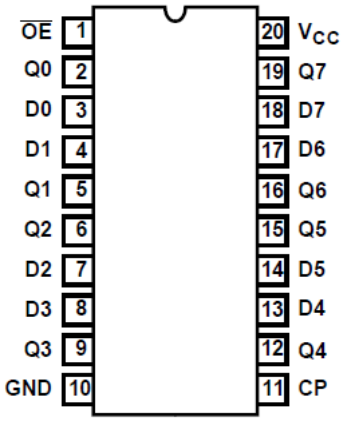
3 Revision History

注：以前版本的页码可能与当前版本的页码不同

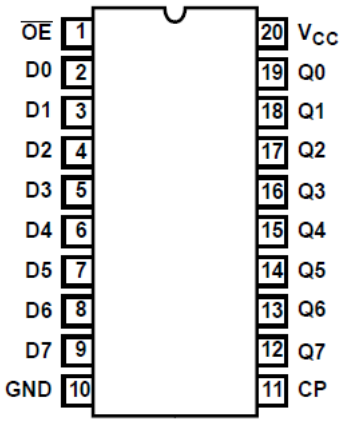
Changes from Revision D (January 2022) to Revision E (October 2022)	Page
• Increased R θ JA for packages: DW (58 to 109.1); N (69 to 84.6); PW (83 to 131.8)	4

Changes from Revision C (May 2004) to Revision D (January 2022)	Page
• 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准	1

4 Pin Configuration and Functions



HC(T) 374
J, DW, or N package
20-Pin CDIP, SOIC, or PDIP
Top View



HC(T) 574
J, DW, N, or PW package
20-Pin CDIP, SOIC, PDIP, or TSSOP
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		– 0.5	7	V
I_{IK}	Input diode current	For V_I < – 0.5 V or V_I > V_{CC} + 0.5 V		±20	mA
I_{OK}	Output diode current	For V_O < – 0.5 V or V_O > V_{CC} + 0.5 V		±20	mA
I_O	Drain current, per output	For – 0.5 V < V_O < V_{CC} + 0.5 V		±35	mA
I_O	Output source or sink current per output pin	For V_O > – 0.5 V or V_O < V_{CC} + 0.5 V		±25	mA
	Continuous current through V_{CC} or ground current			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		– 65	150	°C
	Lead temperature (Soldering 10s) (SOIC - Lead Tips Only)			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V_I, V_O	DC input or output voltage		0	V_{CC}	V
	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T_A	Temperature range		– 55	125	℃

5.3 Thermal Information

THERMAL METRIC		DW (SOIC) 20 PINS	N (PDIP) 20 PINS	PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	109.1	84.6	131.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76	72.5	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	65.3	82.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	51.5	55.3	21.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.1	65.2	82.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS[2]	V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High level output voltage CMOS loads	I_{OH} = – 20 μA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 μA	4.5	4.4			4.4		4.4		
		I_{OH} = – 20 μA	6	5.9			5.9		5.9		
	High level output voltage TTL loads	I_{OH} = – 6 mA	4.5	3.98			3.84		3.7		V
		I_{OH} = – 7.8 mA	6	5.48			5.34		5.2		
V_{OL}	Low level output voltage CMOS loads	I_{OL} = 20 μA	2			0.1		0.1		0.1	V
		I_{OL} = 20 μA	4.5			0.1		0.1		0.1	
		I_{OL} = 20 μA	6			0.1		0.1		0.1	
	Low level output voltage TTL loads	I_{OL} = 6 mA	4.5			0.26		0.33		0.4	V
		I_{OL} = 7.8 mA	6			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} or GND	6			±0.1		±1		±1	μA
I_{CC}	Quiescent device current	V_I = V_{CC} or GND	6			8		80		160	μA
V_{IL} or V_{IH}	Three-state leakage current	V_O = V_{CC}or GND	6			±0.5		±5.0		±10	μA
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage CMOS loads	I_{OH} = – 20 μA	4.5	4.4			4.4		4.4		V
	High level output voltage TTL loads	I_{OH} = – 6 mA	4.5	3.98			3.84		3.7		
V_{OL}	Low level output voltage CMOS loads	I_{OL} = 20 μA	4.5			0.1		0.1		0.1	V
	Low level output voltage TTL loads	I_{OL} = 6 mA	4.5			0.26		0.33		0.4	
I_I	Input leakage current	V_I = V_{CC} or GND	5.5			±0.1		±1		±1	μA
I_{CC}	Quiescent device current	V_I = V_{CC} or GND	5.5			8		80		160	μA
V_{IL} or V_{IH}	Three-state leakage current	V_O = V_{CC}or GND	6			±0.5		±5.0		±10	μA

5.4 Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS[2]	V_{CC} (V)	25℃			–40℃ to 85℃		–55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
ΔI_{CC} [1]	HCT374 Additional quiescent device current per input pin	D0 - D7 inputs held at V_{CC} – 2.1	4.5 to 5.5		100	108		135		147	µA
		CP input held at V_{CC} – 2.1	4.5 to 5.5		100	324		405		441	µA
		$\overline{OE}$ input held at V_{CC} – 2.1	4.5 to 5.5		100	468		585		637	µA
	HCT574 Additional quiescent device current per input pin	D0 - D7 inputs held at V_{CC} – 2.1	4.5 to 5.5		100	144		180		196	µA
		CP input held at V_{CC} – 2.1	4.5 to 5.5		100	270		337.5		367.5	µA
		$\overline{OE}$ input held at V_{CC} – 2.1	4.5 to 5.5		100	216		270		294	µA

(1) For dual-supply systems, theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specificationis 1.8mA.
(2) $V_I = V_{IH}$ or V_{IL}, unless otherwise noted.

5.5 Prerequisite for Switching Characteristics

PARAMETER		V_{CC} (V)	25℃			–40℃ to 85℃			–55℃ to 125℃			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
f_{MAX}	Maximum clock frequency	2	6			5			4			MHz
		4.5	30			25			20			
		6	35			29			23			
t_W	Clock pulse width	2	80			100			120			ns
		4.5	16			20			24			
		6	14			17			20			
t_{SU}	Setup time data to clock	2	60			75			90			ns
		4.5	12			15			18			
		6	10			13			15			
t_H	Hold time data to clock	2	5			5			5			ns
		4.5	5			5			5			
		6	5			5			5			
HCT TYPES												
f_{MAX}	Maximum clock frequency	4.5	30			25			20			MHz
t_W	Clock pulse width	4.5	16			20			24			ns
t_{SU}	Setup time data to clock	4.5	12			15			18			ns
t_H	Hold time data to clock	4.5	5			5			5			ns

5.6 Switching Characteristics

C_L = 50 pF, Input t_r, t_f = 6 ns

PARAMETER		TEST CONDITIONS	V_{CC} (V)	25℃			−40℃ to 85℃		−55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
t_{PLH}, t_{PHL}	Propagation delay Clock to output	C_L = 50 pF	2			165		205		250	ns
			4.5			33		41		50	
		C_L = 15 pF	5		15						ns
		C_L = 50 pF	6			28		35		43	
t_{PLZ}, t_{PHZ}	Output disable to Q	C_L = 50 pF	2			135		170		205	ns
			4.5			27		34		41	
		C_L = 15 pF	5		11						ns
		C_L = 50 pF	6			23		29		35	
t_{PZL}, t_{PZH}	Output enable to Q	C_L = 50 pF	2			150		190		225	ns
			4.5			30		38		45	
		C_L = 15 pF	5		12						ns
		C_L = 50 pF	6			26		33		38	
f_{MAX}	Maximum clock frequency	C_L = 15 pF	5		60						MHz
t_{THL}, t_{TLH}	Output transition time	C_L = 50 pF	2			60		75		90	ns
			4.5			12		15		18	
			6			10		13		15	
C_I	Input capacitance	C_L = 50 pF		10		10		10		10	pF
C_O	Three-state output capacitance			20		20		20		20	pF
C_{PD}	Power dissipation capacitance(1) (2)	C_L = 15 pF	5		39						pF
HCT TYPES											
t_{PHL}, t_{PLH}	Propagation delay Clock to output	C_L = 50 pF	4.5			33		41		50	ns
		C_L = 15 pF	5		15						
t_{PLZ}, t_{PHZ}	Output disable to Q	C_L = 50pF	4.5			28		35		42	ns
		C_L = 15 pF	5		11						
t_{PZL}, t_{PZH}	Output enable to Q	C_L = 50 pF	4.5			30		38		45	ns
		C_L = 15 pF	5		12						
f_{MAX}	Maximum clock frequency	C_L = 15 pF	5		60						MHz
t_{TLH}, t_{THL}	Output transition time	C_L = 50 pF	4.5			12		15		18	ns
C_I	Input capacitance	C_L = 50 pF		10		10		10		10	pF
C_O	Three-state output capacitance			20		20		20		20	pF
C_{PD}	Power dissipation capacitance(1) (2)	C_L = 15 pF	5		47						pF

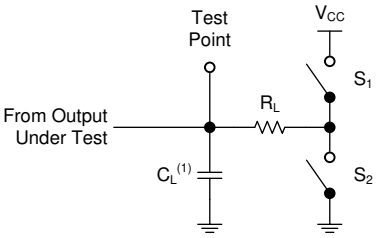
(1) C_{PD} is used to determine the dynamic power consumption, per package.
(2) $P_D = C_{PD} V_{CC}^2 f_i + \Sigma V_{CC}^2 f_O C_L$ where f_i = input frequency, f_O = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.

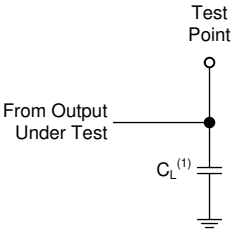
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



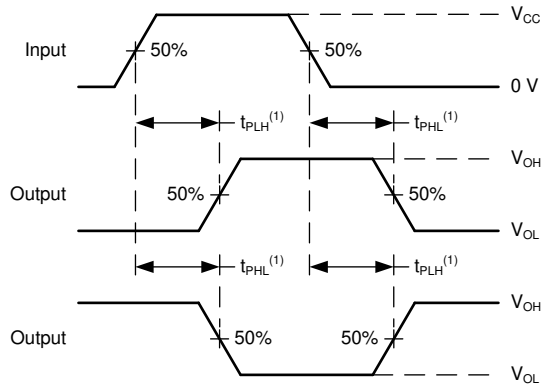
(1) C_L includes probe and test-fixture capacitance.

图 6-1. Load Circuit for 3-State Outputs



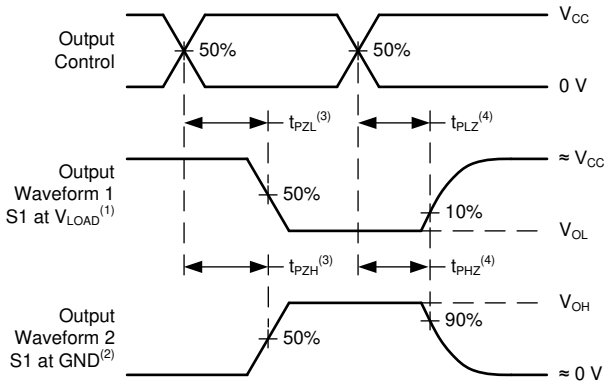
(1) C_L includes probe and test-fixture capacitance.

图 6-2. Load Circuit for Push-Pull Outputs



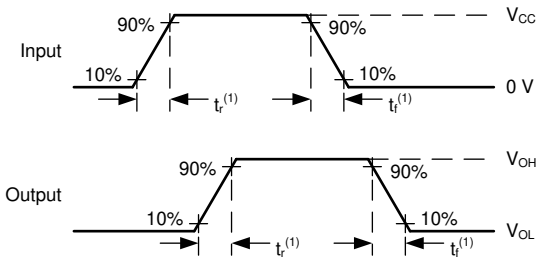
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

图 6-3. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



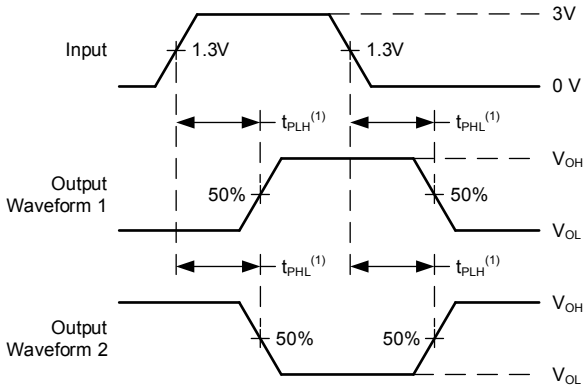
(1) S1 = CLOSED; S2 = OPEN.
(2) S1 = OPEN; s2 = CLOSED.
(3) t_{PLZ} and t_{PHZ} are the same as t_{dis}.
(4) t_{PZL} and t_{PZH} are the same as t_{en}.

图 6-4. Voltage Waveforms, Standard CMOS Inputs Propagation Delays



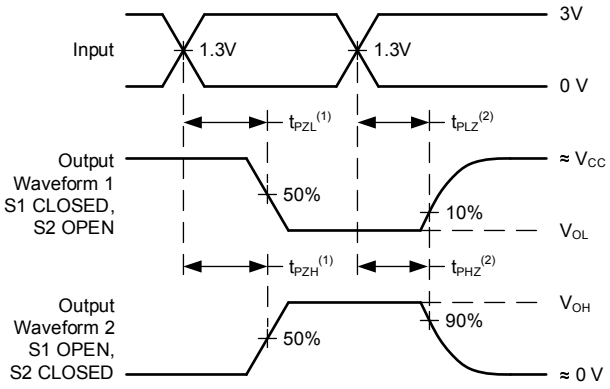
(1) The greater between t_r and t_f is the same as t_t.

图 6-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

图 6-6. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs



(1) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

(2) t_{PZL} and t_{PZH} are the same as t_{en}.

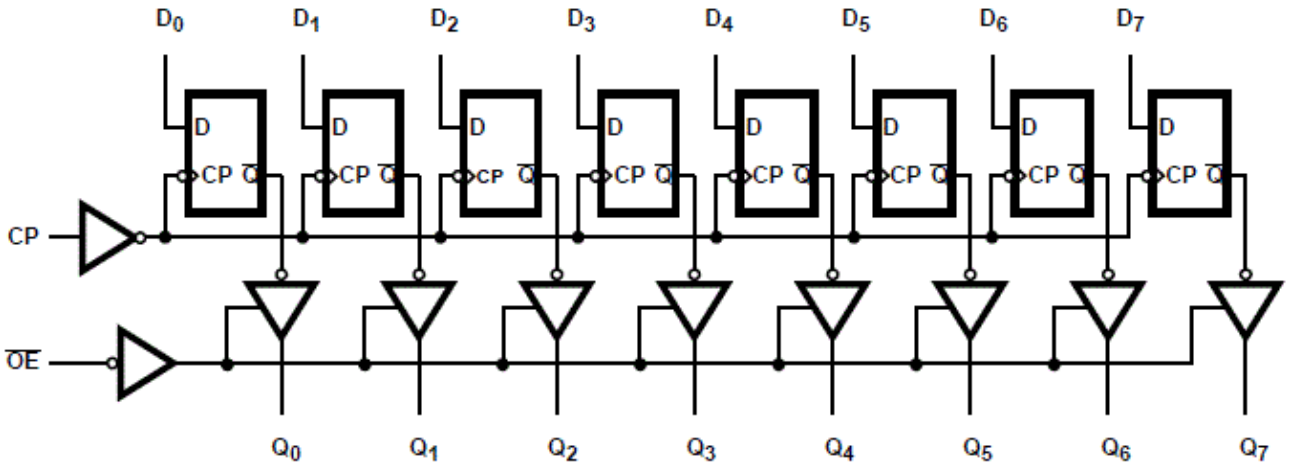
图 6-7. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays

7 Detailed Description

7.1 Overview

The ’HC374, ’HCT374, ’HC574, and ’HCT574 are octal D-type flip-flops with 3-state outputs and the capability to drive 15 LSTTL loads. The eight edge-triggered flip-flops enter data into their registers on the LOW to HIGH transition of clock (CP). The output enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state. The 374 and 574 are identical in function and differ only in their pinout arrangements.

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1. Truth Table(1)

INPUTS			OUTPUT
$\overline{OE}$	CP	Dn	Qn
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

(1) H = high level (steady state), L = low level (steady state), X = don’t care, ↑ = transition from low to high level, Q0 = the level of Q before the indicated steady-state input conditions were established, Z= high impedance state

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8974201RA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974201RA CD54HCT574F3A
CD54HC374F3A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407101RA CD54HC374F3A
CD54HC374F3A.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407101RA CD54HC374F3A
CD54HC574F	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC574F
CD54HC574F.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC574F
CD54HC574F3A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC574F3A
CD54HC574F3A.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC574F3A
CD54HCT374F3A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8550701RA CD54HCT374F3A
CD54HCT374F3A.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8550701RA CD54HCT374F3A
CD54HCT574F	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT574F
CD54HCT574F.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT574F
CD54HCT574F3A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974201RA CD54HCT574F3A
CD54HCT574F3A.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974201RA CD54HCT574F3A
CD74HC374E	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC374E
CD74HC374E.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC374E
CD74HC374M	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-55 to 125	HC374M
CD74HC374M96	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC374M
CD74HC374M96.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC374M
CD74HC374M96E4	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC374M
CD74HC574E	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC574E
CD74HC574E.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC574E
CD74HC574M	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-55 to 125	HC574M
CD74HC574M96	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC574M
CD74HC574M96.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC574M

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HCT374E	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT374E
CD74HCT374E.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT374E
CD74HCT374EE4	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT374E
CD74HCT374M	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-55 to 125	HCT374M
CD74HCT374M96	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT374M
CD74HCT374M96.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT374M
CD74HCT574E	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT574E
CD74HCT574E.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT574E
CD74HCT574M	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-55 to 125	HCT574M
CD74HCT574M96	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT574M
CD74HCT574M96.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT574M
CD74HCT574PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK574
CD74HCT574PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK574

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD54HC374, CD54HC574, CD54HCT374, CD54HCT574, CD74HC374, CD74HC574, CD74HCT374, CD74HCT574 :

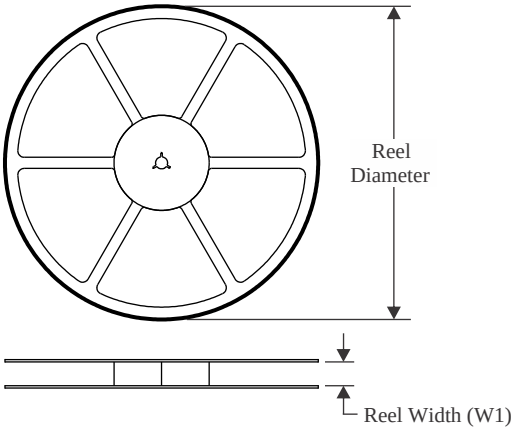
- Catalog : CD74HC374, CD74HC574, CD74HCT374, CD74HCT574
- Automotive : CD74HCT574-Q1, CD74HCT574-Q1
- Enhanced Product : CD74HCT574-EP, CD74HCT574-EP
- Military : CD54HC374, CD54HC574, CD54HCT374, CD54HCT574

NOTE: Qualified Version Definitions:

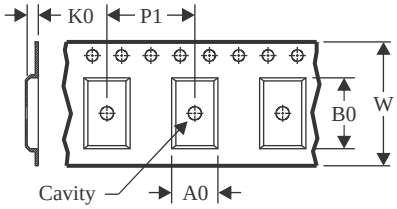
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

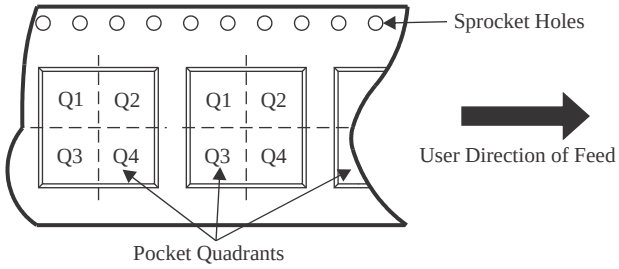


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

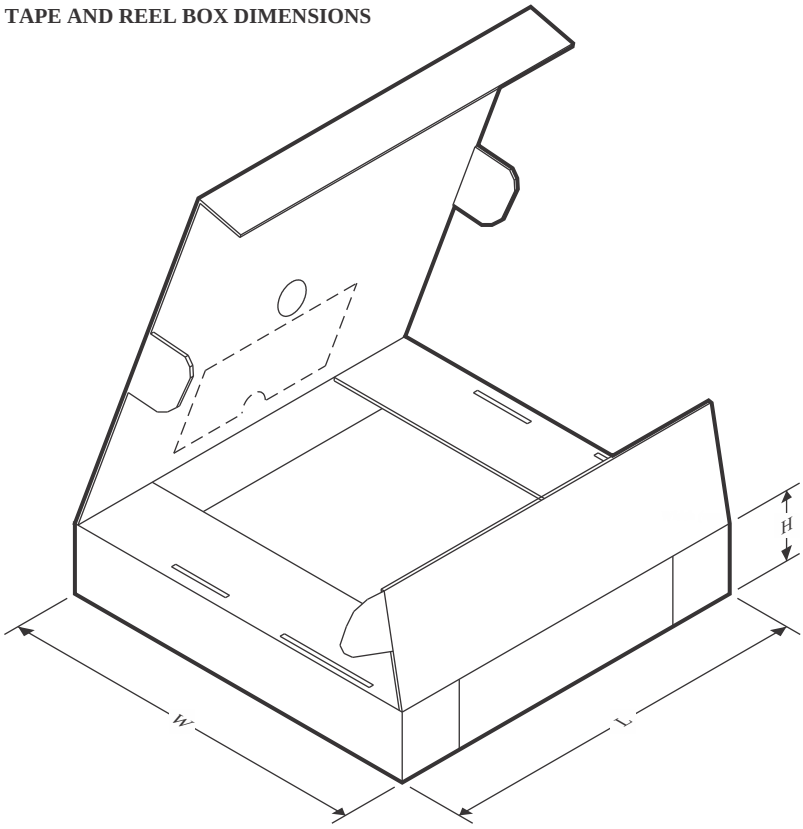
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC374M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HC574M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT374M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT574M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT574PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

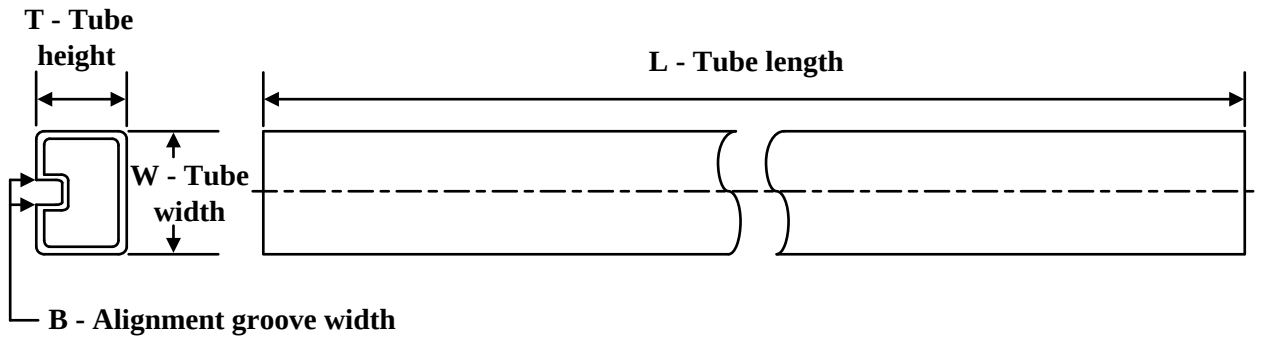
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC374M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74HC574M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74HCT374M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74HCT574M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74HCT574PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

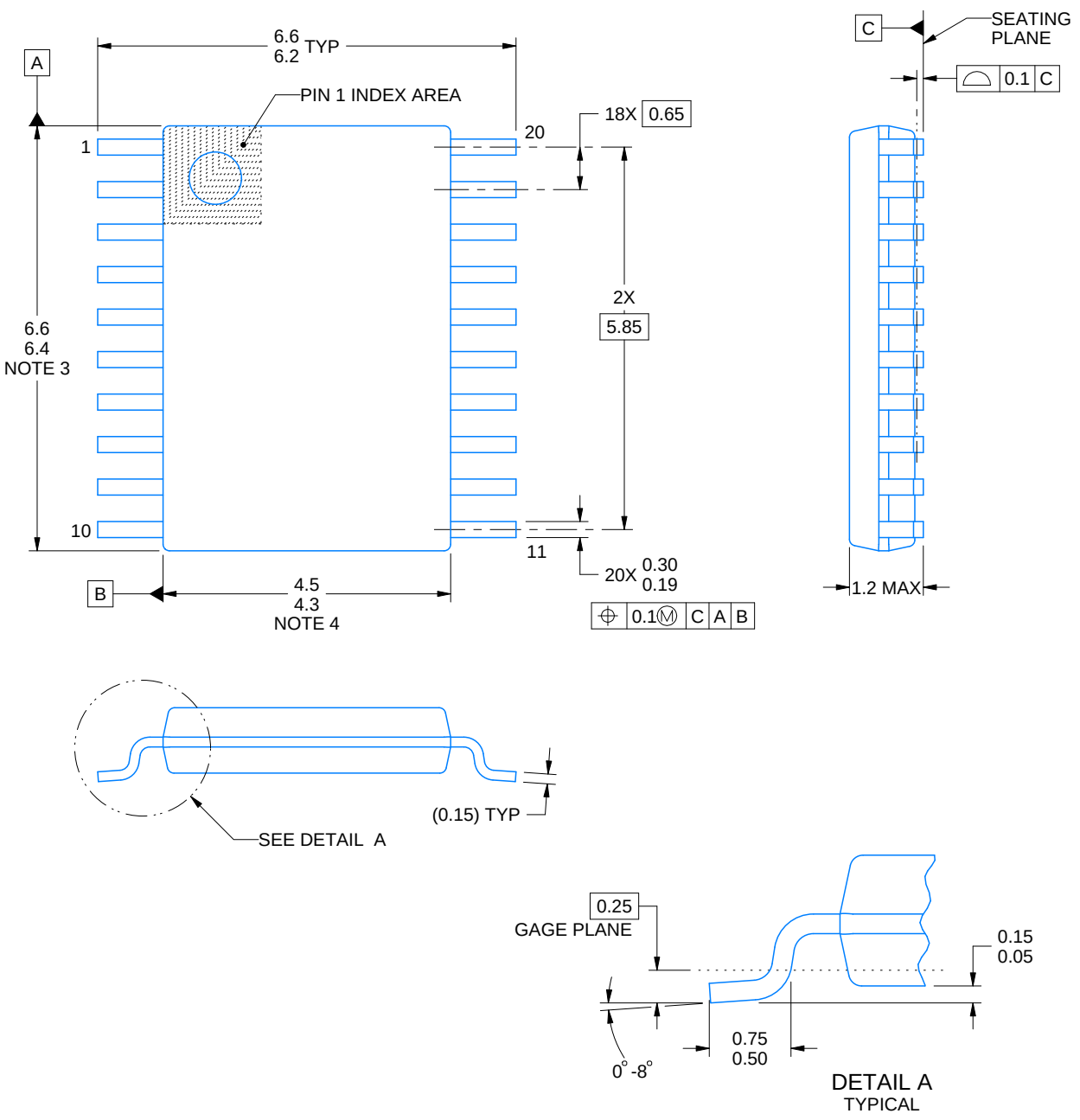
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC374E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC374E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC574E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC574E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT374E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT374E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT374EE4	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT574E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT574E.A	N	PDIP	20	20	506	13.97	11230	4.32

PACKAGE OUTLINE

PW0020A

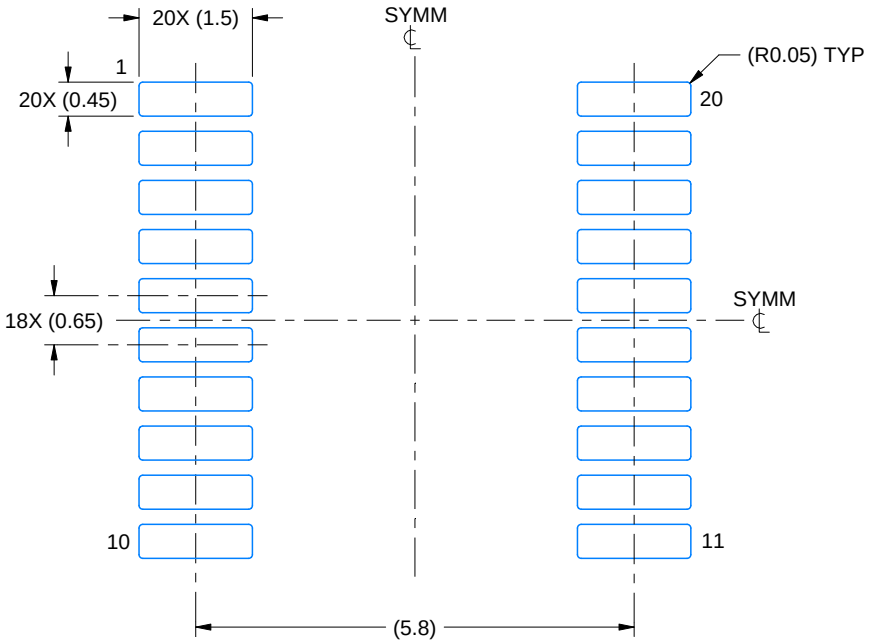
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



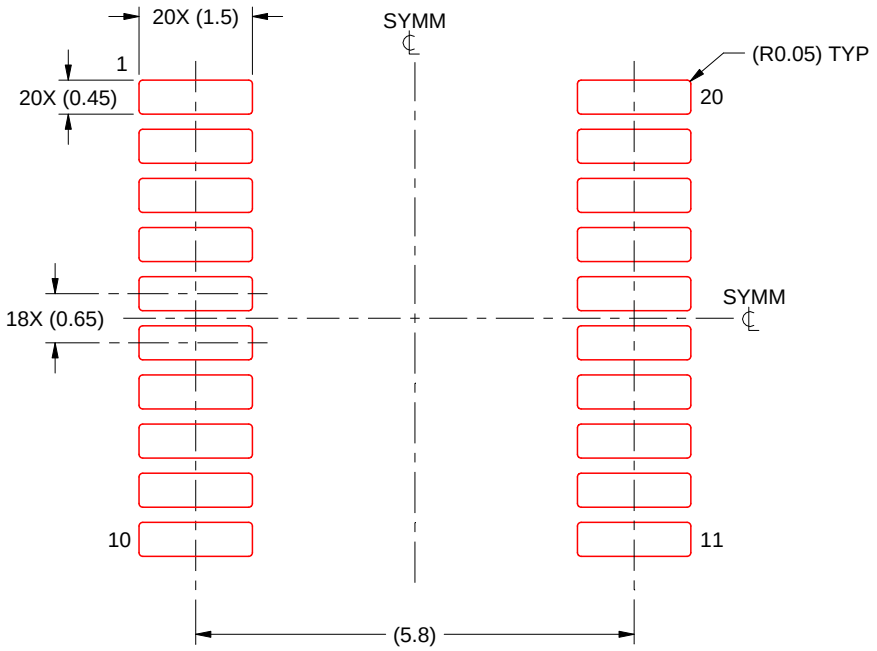
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

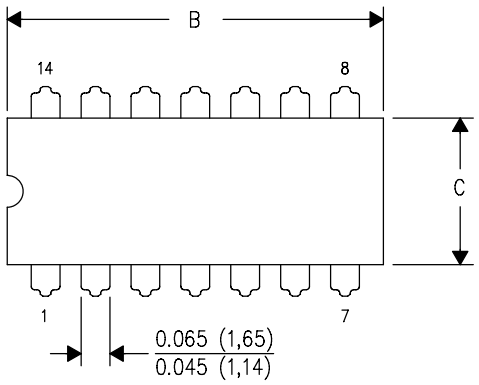
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

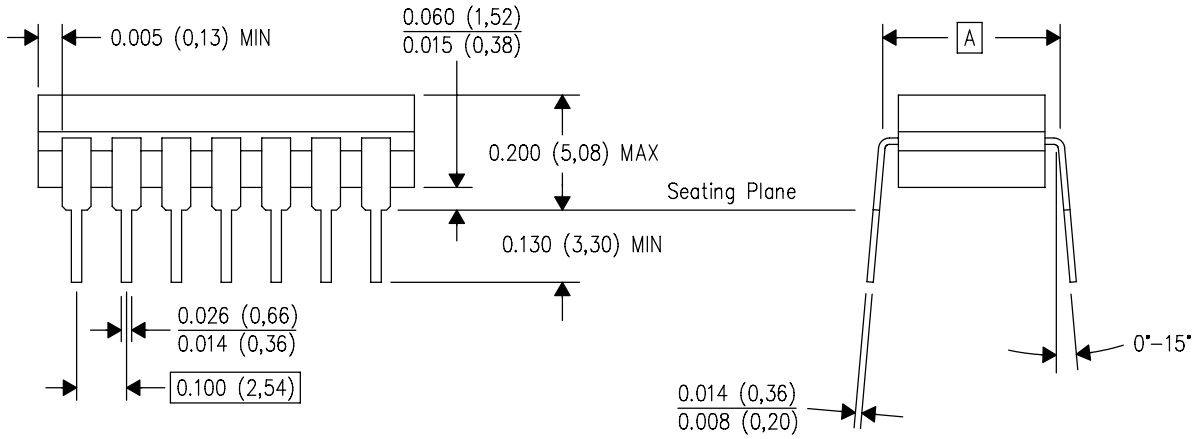
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



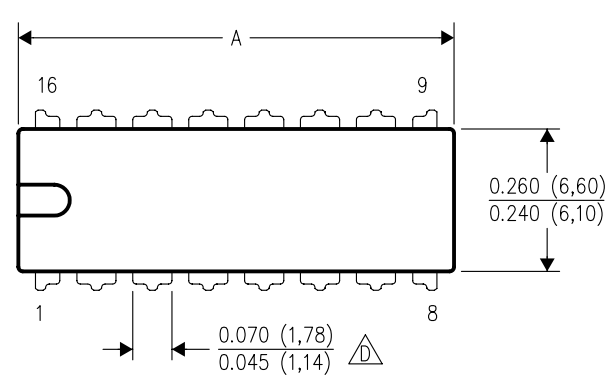
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

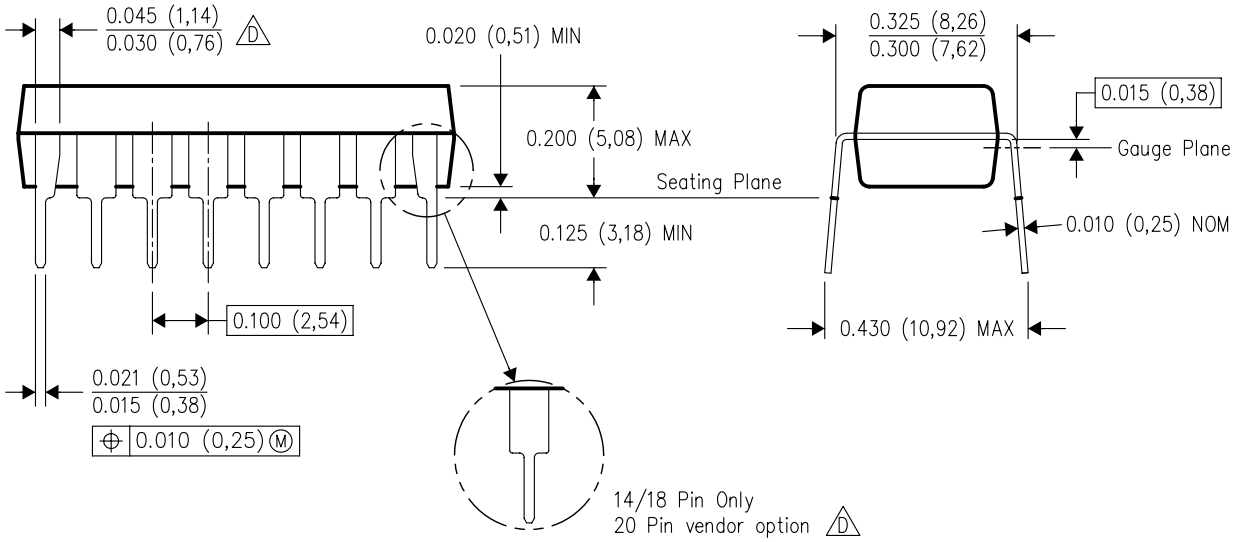
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

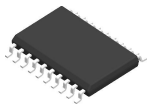


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

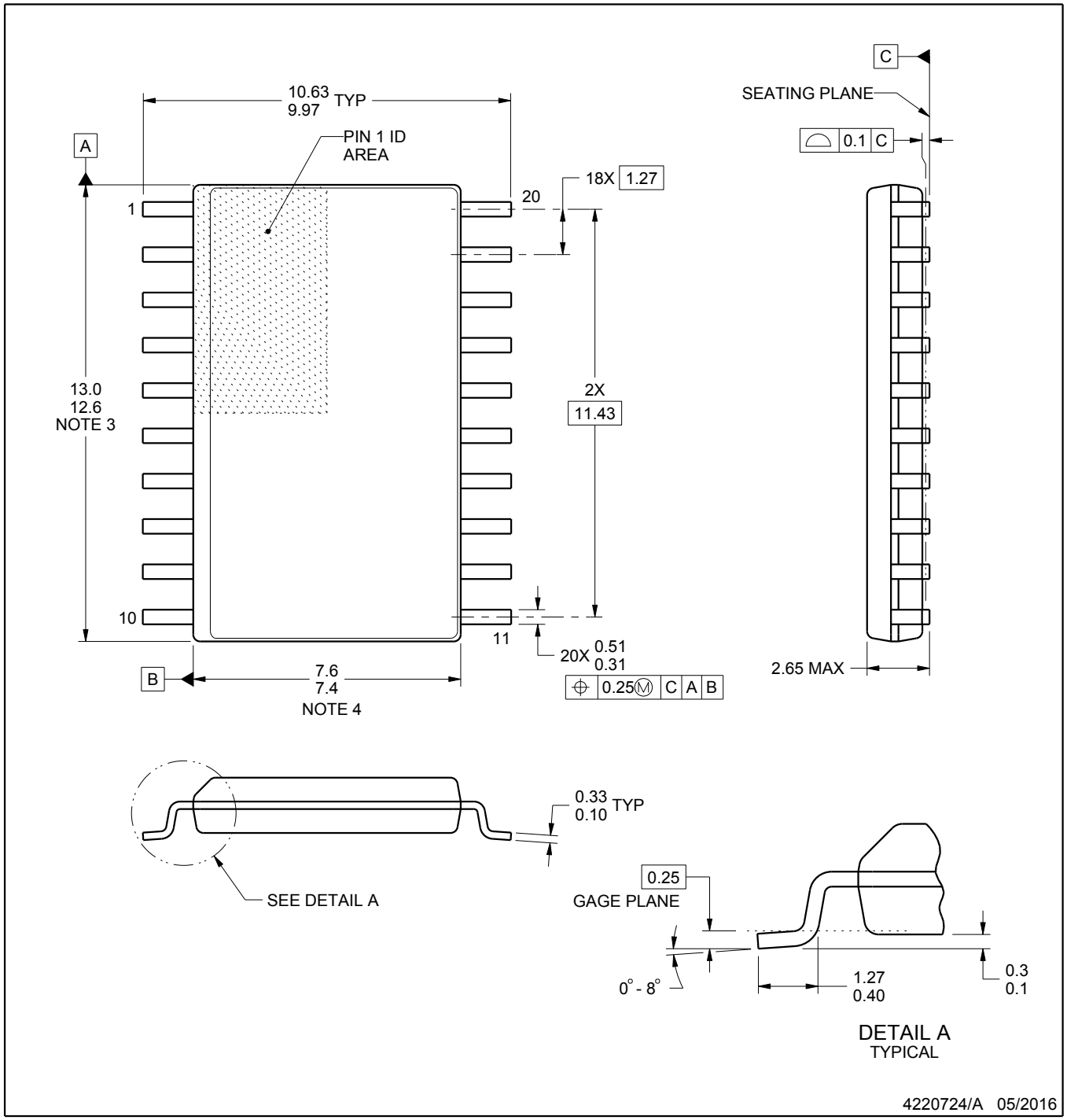


PACKAGE OUTLINE

DW0020A

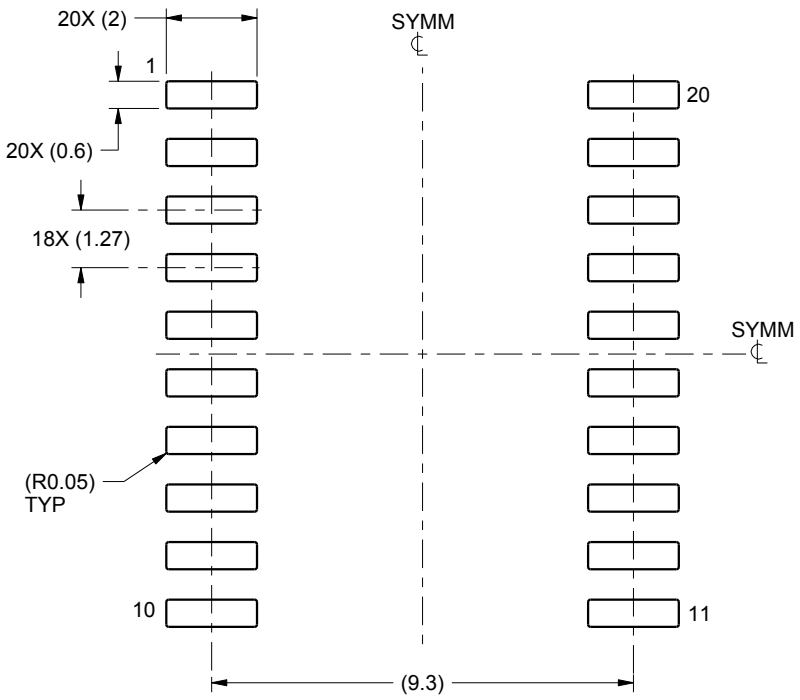
SOIC - 2.65 mm max height

SOIC

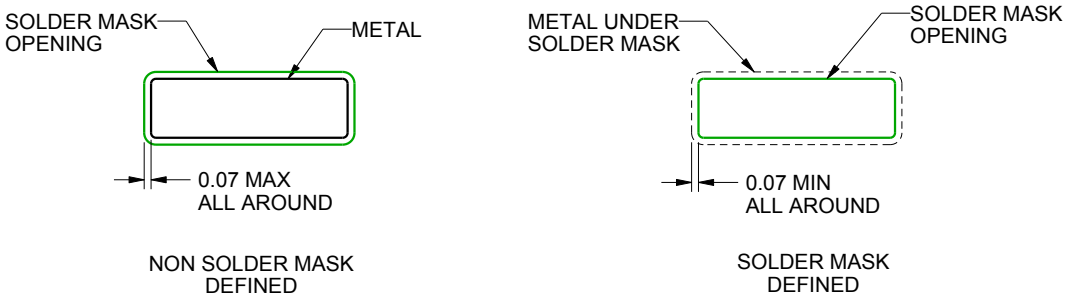


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

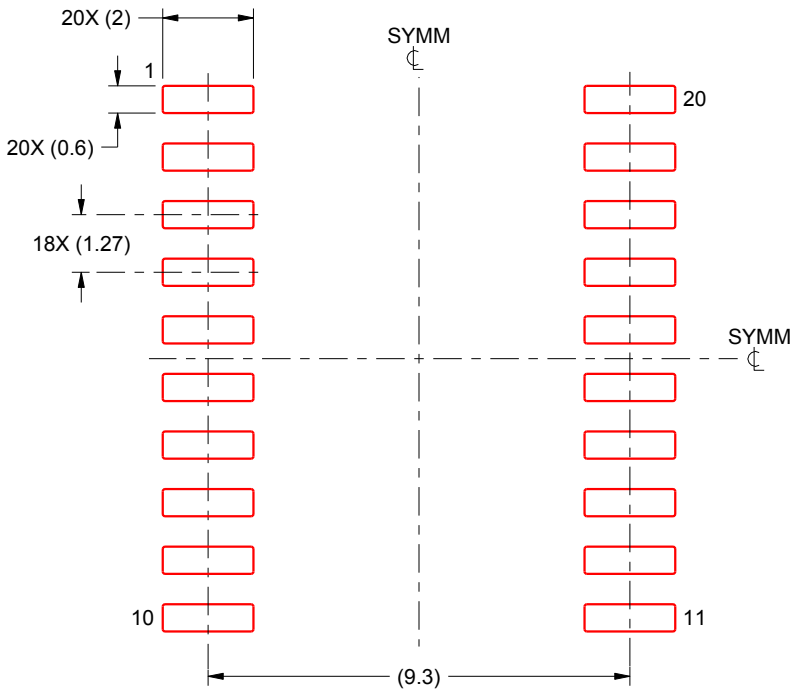


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月