

CDx4HC73 CD74HCT73 具有复位功能的负边沿触发式双路 J-K 触发器

1 特性

- 时钟输入迟滞，改进了抗扰度并增加了输入上升和下降时间
- 异步复位
- 互补输出
- 缓冲输入
- 当 $V_{CC} = 5V$,
 $C_L = 15pF$, $T_A = 25^\circ C$ 时 f_{MAX} 典型值 = 60MHz
- 扇出 (在温度范围内)
 - 标准输出：10 个 LSTTL 负载
 - 总线驱动器输出：15 个 LSTTL 负载
- 宽工作温度范围：-55°C 至 125°C
- 平衡的传播延迟及转换时间
- 与 LSTTL 逻辑 IC 相比，功耗显著降低
- HC 类型
 - 工作电压为 2 V 至 6V
 - 高抗噪性：当 $V_{CC} = 5V$ 时， $N_{IL} = 30\%$, $N_{IH} = V_{CC}$ 的 30%
- HCT 类型
 - 工作电压为 4.5V 至 5.5V
 - 直接 LSTTL 输入逻辑兼容性，
 $V_{IL} = 0.8V$ (最大值) , $V_{IH} = 2V$ (最小值)
 - CMOS 输入兼容性，当电压为 V_{OL} 、 V_{OH} 时， $I_I \leq 1\mu A$

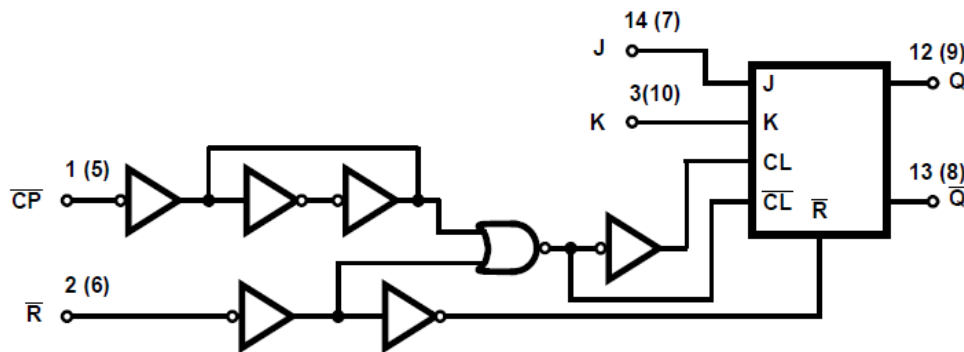
2 说明

HC73 和 CD74HCT73 采用硅栅 CMOS 技术，可实现相当于 LSTTL 器件的运行速度。具有标准 CMOS 集成电路的低功耗特性，还能够驱动 10 个 LSTTL 负载。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
CD74HC73M	SOIC (14)	8.65mm × 3.90mm
CD74HCT73M	SOIC (14)	8.65mm × 3.90mm
CD74HC73E	PDIP (14)	19.31mm × 6.35mm
CD74HCT73E	PDIP (14)	19.31mm × 6.35mm
CD54HC73F	CDIP (14)	19.55mm × 6.71mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能方框图



Table of Contents

1 特性	1	7.2 Functional Block Diagram.....	9
2 说明	1	7.3 Device Functional Modes.....	9
3 Revision History	2	8 Power Supply Recommendations	10
4 Pin Configuration and Functions	3	9 Layout	10
5 Specifications	4	9.1 Layout Guidelines.....	10
5.1 Absolute Maximum Ratings ⁽¹⁾	4	10 Device and Documentation Support	11
5.2 Recommended Operating Conditions.....	4	10.1 接收文档更新通知.....	11
5.3 Thermal Information.....	4	10.2 支持资源.....	11
5.4 Electrical Specifications.....	5	10.3 Trademarks.....	11
5.5 Prerequisite for Switching Specifications.....	6	10.4 Electrostatic Discharge Caution.....	11
5.6 Switching Specifications.....	7	10.5 术语表.....	11
6 Parameter Measurement Information	8	11 Mechanical, Packaging, and Orderable Information	11
7 Detailed Description	9		
7.1 Overview.....	9		

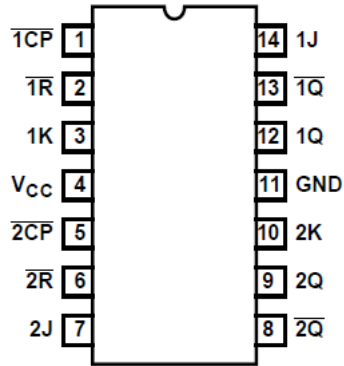
3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (January 2022) to Revision G (October 2022)	Page
• Increased R _{θJA} for packages: D (86 to 138.7); N (80 to 91).....	4

Changes from Revision E (August 2003) to Revision F (January 2022)	Page
• 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准.....	1

4 Pin Configuration and Functions



J, N, or D package
14-Pin CDIP, PDIP, or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	- 0.5	7	V
I _{IK}	Input diode current	For V _I < - 0.5 V or V _I > V _{CC} + 0.5 V		± 20 mA
I _O	Drain current, per output	For - 0.5 V < V _O < V _{CC} + 0.5 V		± 25 mA
I _{OK}	Output diode current	For V _O < - 0.5 V or V _O > V _{CC} + 0.5 V		± 20 mA
I _O	Output source or sink current per output pin	For V _O > - 0.5 V or V _O < V _{CC} + 0.5 V		± 25 mA
I _{CC}	Continuous current through V _{CC} or GND			± 50 mA
T _J	Junction temperature			±150 °C
T _{stg}	Storage temperature	- 65	150	°C

- (1) Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

5.2 Recommended Operating Conditions

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V _I , V _O	Input or output voltage	0	V _{CC}	V	
t _t	Input rise and fall time	2 V	1000	ns	
		4.5 V	500		
		6 V	400		
T _A	Temperature range	- 55	125	°C	

5.3 Thermal Information

THERMAL METRIC		D (SOIC)	N (PDIP)	UNIT
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	138.7	91	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	93.8	78.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	94.7	70.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	49.1	58.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter resistance	94.3	70.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Specifications

PARAMETER		TEST CONDITIONS ⁽²⁾	V _{CC} (V)	25°C			- 40°C to 85°C		- 55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V _{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V _{IL}	Low level input voltage		2	0.5			0.5		0.5		V
			4.5	1.35			1.35		1.35		
			6	1.8			1.8		1.8		
V _{OH}	High level output voltage	I _{OH} = - 20 μA	2	1.9			1.9		1.9		V
		I _{OH} = - 20 μA	4.5	4.4			4.4		4.4		
		I _{OH} = - 20 μA	6	5.9			5.9		5.9		
	High level output voltage	I _{OH} = - 4 mA	4.5	3.98			3.84		3.7		
		I _{OH} = - 5.2 mA	6	5.48			5.34		5.2		
V _{OL}	Low level output voltage	I _{OL} = 20 μA	2	0.1			0.1		0.1		V
		I _{OL} = 20 μA	4.5	0.1			0.1		0.1		
		I _{OL} = 20 μA	6	0.1			0.1		0.1		
	Low level output voltage	I _{OL} = 4 mA	4.5	0.26			0.33		0.4		
		I _{OL} = 5.2 mA	6	0.26			0.33		0.4		
I _I	Input leakage current	V _I = V _{CC} or GND	6	±0.1			±1		±1		mA
I _{CC}	Supply current	V _I = V _{CC} or GND	6	4			40		80		mA
HCT TYPES											
V _{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V _{IL}	Low level input voltage		4.5 to 5.5	0.8			0.8		0.8		V
V _{OH}	High level output voltage	I _{OH} = - 20 μA	4.5	4.4			4.4		4.4		V
	High level output voltage	I _{OH} = - 4 mA	4.5	3.98			3.84		3.7		
V _{OL}	Low level output voltage	I _{OL} = 20 μA	4.5	0.1			0.1		0.1		V
	Low level output voltage	I _{OL} = 4 mA	4.5	0.26			0.33		0.4		
I _I	Input leakage current	V _I = V _{CC} and GND	5.5	±0.1			±1		±1		μA
I _{CC}	Supply current	V _I = V _{CC} and GND	5.5	4			40		80		μA
Δ I _{CC} ⁽¹⁾	Additional supply current per input pin	All inputs held at V _{CC} - 2.1	4.5 to 5.5	100 108			135		147		μA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

(2) V_I = V_{IH} or V_{IL}.

5.5 Prerequisite for Switching Specifications

PARAMETER		TEST CONDITIONS	V _{CC} (V)	25°C			- 40°C to 85°C		- 55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
t _w	\overline{CP} pulse width	- C _L = 50 pF	2	80			100		120		ns
			4.5	16			20		24		
			6	14			17		20		
t _w	\overline{R} pulse width	- C _L = 50 pF	2	80			100		120		ns
			4.5	16			20		24		
			6	14			17		20		
t _{SU}	Setup time, J, K to \overline{CP}	C _L = 50 pF	2	80			100		120		ns
			4.5	16			20		24		
			6	14			17		20		
t _H	Hold time, J, K to \overline{CP}	C _L = 50 pF	2	3			3		3		ns
			4.5	3			3		3		
			6	3			3		3		
t _{REM}	Removal time	- C _L = 50 pF	2	80			100		120		ns
			4.5	16			20		24		
			6	14			17		20		
f _{MAX}	\overline{CP} frequency	C _L = 50 pF	2	6			5		4		MHz
			4.5	30			25		20		
		C _L = 15 pF	5	60							
		C _L = 50 pF	6	35			29		23		
HCT TYPES											
t _w	\overline{CP} pulse width	C _L = 50 pF	4.5	16			20		24		ns
t _w	\overline{R} pulse width	C _L = 50 pF	4.5	18			23		27		ns
t _{SU}	Setup time, J, K to \overline{CP}	C _L = 50 pF	4.5	16			20		24		ns
t _H	Hold time, J, K to \overline{CP}	C _L = 50 pF	4.5	3			3		3		ns
t _{REM}	Removal time	C _L = 50 pF	4.5	12			15		18		ns
f _{MAX}	\overline{CP} frequency	C _L = 50 pF	4.5	30			25		20		MHz
		C _L = 15 pF	5	60							

5.6 Switching Specifications

Input, t_r , $t_f = 6$ ns

PARAMETER		TEST CONDITIONS	V_{CC} (V)	25°C			- 40°C to 85°C		- 55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
t_{PLH} , t_{PHL}	Propagation delay, \overline{CP} to Q	$C_L = 50$ pF	2		160		200		240	ns	
			4.5		32		40		48		
		$C_L = 15$ pF	5		13						
		$C_L = 50$ pF	6		28		34		41		
t_{PLH} , t_{PHL}	Propagation delay, \overline{CP} to \overline{Q}	$C_L = 50$ pF	2		160		200		240	ns	
			4.5		32		40		48		
		$C_L = 15$ pF	5		13						
		$C_L = 50$ pF	6		28		34		41		
t_{PLH} , t_{PHL}	Propagation delay, \overline{R} to Q, \overline{Q}	$C_L = 50$ pF	2		145		180		220	ns	
			4.5		29		36		44		
		$C_L = 15$ pF	5		12						
		$C_L = 50$ pF	6		25		31		38		
t_{TLH} , t_{THL}	Output transition time	$C_L = 50$ pF	2		75		95	18	110	ns	
			4.5		15		19		22		
			6		13		16		19		
C_I	Input capacitance				10		10		10	pF	
C_{PD}	Power dissipation capacitance ^{(1) (2)}		5		28					pF	
HCT TYPES											
t_{PLH} , t_{PHL}	Propagation delay, \overline{CP} to Q	$C_L = 50$ pF	4.5		38		48		57	ns	
t_{PLH} , t_{PHL}	Propagation delay, \overline{CP} to \overline{Q}	$C_L = 50$ pF	4.5		36		45		54	ns	
t_{PLH} , t_{PHL}	Propagation delay, \overline{R} to Q, \overline{Q}	$C_L = 50$ pF	4.5		34		43		51	ns	
t_{TLH} , t_{THL}	Output transition time	$C_L = 50$ pF	4.5		15		19		22	ns	
C_I	Input capacitance				10		10		10	pF	
C_{PD}	Power dissipation capacitance ^{(1) (2)}		5		28					pF	

(1) C_{PD} is used to determine the dynamic power consumption, per flip-flop.

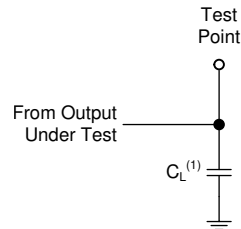
(2) $P_D = C_{PD} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 2.5 \text{ ns}$.

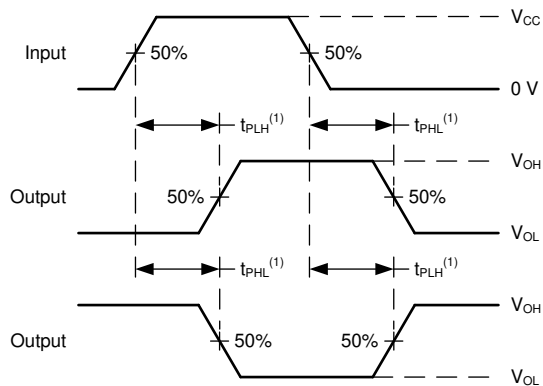
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



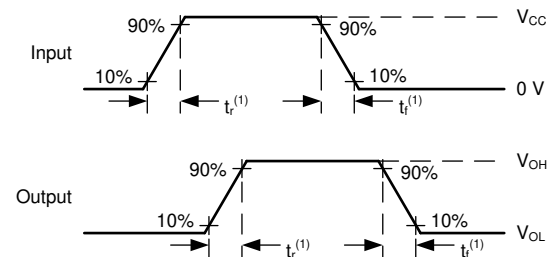
(1) C_L includes probe and test-fixture capacitance.

图 6-1. Load Circuit for Push-Pull Outputs



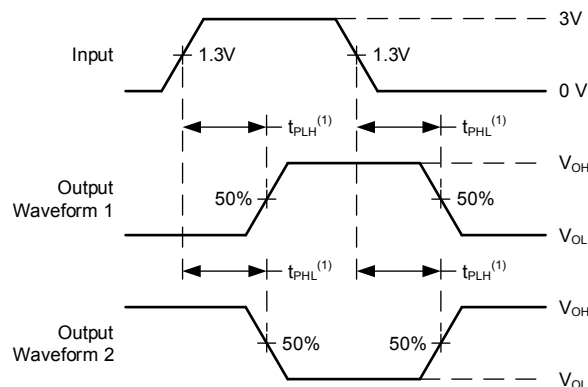
(1) The greater between t_{pLH} and t_{pHL} is the same as t_{pd} .

图 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t .

图 6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs



(1) The greater between t_{pLH} and t_{pHL} is the same as t_{pd} .

图 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

7 Detailed Description

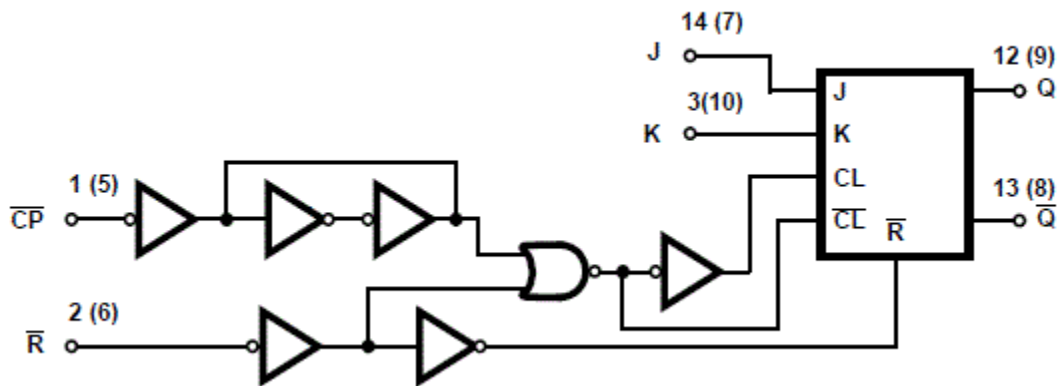
7.1 Overview

The ' HC73 and CD74HCT73 utilize silicon gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads

These flip-flops have independent J, K, Reset and Clock inputs and Q and \bar{Q} outputs. They change state on the negative-going transition of the clock pulse. Reset is accomplished asynchronously by a low level input. This device is functionally identical to the HC/HCT107 but differs in terminal assignment and in some parametric limits.

The HCT logic family is functionally as well as pin compatible with the standard LS logic family

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1. Truth Table⁽¹⁾

INPUTS				OUTPUTS	
R	CP	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	↓	L	L	No change	
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	No change	

(1) H = high level (steady state), L = low level (steady state), X = irrelevant, ↓ = high-to-low transition

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8515301CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515301CA CD54HC73F3A	Samples
CD54HC73F	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC73F	Samples
CD54HC73F3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8515301CA CD54HC73F3A	Samples
CD74HC73E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC73E	Samples
CD74HC73M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC73M	Samples
CD74HCT73E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT73E	Samples
CD74HCT73M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT73M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC73, CD74HC73 :

- Catalog : [CD74HC73](#)
- Military : [CD54HC73](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC73M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC73M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HCT73M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC73M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HC73M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HCT73M96	SOIC	D	14	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC73E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT73E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT73E	N	PDIP	14	25	506	13.97	11230	4.32

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024，德州仪器 (TI) 公司