

## DAC5672 14-Bit 275 MSPS Digital-to-Analog Converter

### 1 Features

- 14-Bit Dual Transmit Digital-to-Analog Converter (DAC)
- 275 MSPS Update Rate
- Single-Supply: 3 V to 3.6 V
- High Spurious-Free Dynamic Range (SFDR): 84 dBc at 5 MHz
- High Third-Order Two-Tone Intermodulation (IMD3): 79 dBc at 15.1 MHz and 16.1 MHz
- WCDMA Adjacent Channel Leakage Ratio (ACLR): 78 dB at Baseband
- WCDMA ACLR: 73 dB at 30.72 MHz
- Independent or Single Resistor Gain Control
- Dual or Interleaved Data
- On-Chip 1.2-V Reference
- Low Power: 330 mW
- Power-Down Mode: 9 mW
- Package: 48-Pin Thin-Quad Flat Pack (TQFP)

### 2 Applications

- Cellular Base Transceiver Station Transmit Channel
  - CDMA: W-CDMA, CDMA2000, IS-95
  - TDMA: GSM, IS-136, EDGE and UWC-136
- Medical and Test Instrumentation
- Arbitrary Waveform Generators (ARB)
- Direct Digital Synthesis (DDS)
- Cable Modem Termination System (CMTS)

### 3 Description

The DAC5672 device is a monolithic, dual-channel, 14-bit, high-speed DAC with on-chip voltage reference.

Operating with update rates of up to 275 MSPS, the DAC5672 offers exceptional dynamic performance, tight-gain, and offset matching characteristics that make the device well-suited in I/Q baseband or direct IF communication applications.

Each DAC has a high-impedance, differential-current output suitable for single-ended or differential analog-output configurations. External resistors allow scaling the full-scale output current for each DAC separately or together, typically between 2 mA and 20 mA. An accurate on-chip voltage reference is temperature-compensated and delivers a stable 1.2-V reference voltage. Optionally, an external reference may be used.

The DAC5672 has two, 14-bit, parallel input ports with separate clocks and data latches. For flexibility, the DAC5672 supports multiplexed data for each DAC on one port when operating in interleaved mode.

The DAC5672 is specifically designed for a differential transformer-coupled output with a 50-Ω doubly-terminated load. For a 20-mA full-scale output current, a 4:1 impedance ratio (resulting in an output power of 4 dBm) and 1:1 impedance ratio transformer (–2 dBm output power) are supported.

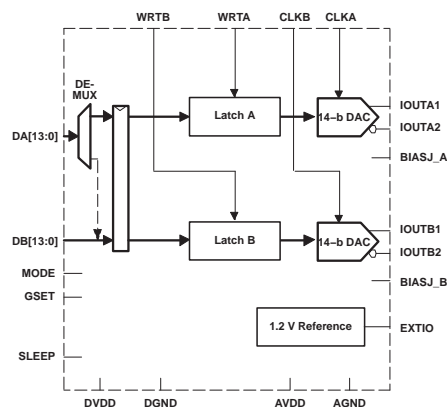
The DAC5672 is available in a 48-pin TQFP package. Pin compatibility between family members provides 12-bit (DAC5662) and 14-bit (DAC5672) resolutions. Furthermore, the DAC5672 is pin compatible to the DAC2904 and AD9767 dual DACs. The device is characterized for operation over the industrial temperature range from –40°C to 85°C.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC5672	TQFP (48)	7.00 mm x 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Functional Block Diagram



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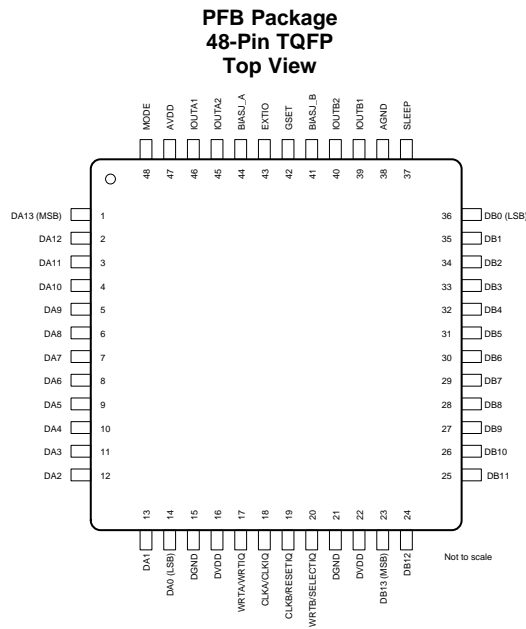
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision C (November 2010) to Revision D</b>	<b>Page</b>
• Deleted <i>Available Options</i> table .....	<b>1</b>
• Added <i>Device Information</i> table .....	<b>1</b>
• Added Temperature Coefficients Offset Drift and Gain Drift to <i>Electrical Characteristics</i> section .....	<b>1</b>
• Added <i>Feature Description</i> section .....	<b>1</b>
• Added $f_{\text{DATA}} = 200 \text{ MSPS}$ , $f_{\text{OUT}} = 1 \text{ MHz}$ to Power Supply in the <i>Electrical Characteristics</i> section .....	<b>1</b>
• Changed Dual-Bus Data Interface and Timing in <i>Programming</i> section .....	<b>1</b>
• Added 3.3 MAX and 0.8 MAX to Digital Input in <i>Electrical Characteristics</i> section .....	<b>1</b>
• Reformatted pinout diagram and pin table in <i>Pin Configuration and Functions</i> section .....	<b>3</b>
• Added <i>ESD Ratings</i> table .....	<b>5</b>
• Added <i>Recommended Operating Conditions</i> table .....	<b>5</b>
• Added <i>Thermal Information</i> table .....	<b>6</b>
• Changed formatting of <a href="#">Table 1</a> .....	<b>15</b>
• Added <i>Application Information</i> and <i>Typical Application</i> sections .....	<b>22</b>
• Added <i>Power Supply Recommendations</i> section .....	<b>24</b>
• Added <i>Layout</i> section .....	<b>25</b>

<b>Changes from Revision B (May 2009) to Revision C</b>	<b>Page</b>
• Changed the non-printing $\mu$ symbols in the Digital Input section of the <i>Electrical Characteristics</i> table (Units column) to the correct $\mu$ symbols recognized by the PDF processor .....	<b>1</b>

## 5 Pin Configuration and Functions



### Pin Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	38	I	Analog ground
AVDD	47	I	Analog supply voltage
BIASJ_A	44	O	Full-scale output current bias for DACA
BIASJ_B	41	O	Full-scale output current bias for DACB
CLKA/CLKIQ	18	I	Clock input for DACA, CLKIQ in interleaved mode
CLKB/RESETIQ	19	I	Clock input for DACB, RESETIQ in interleaved mode
DA[13:0]	1	I	Data port A. DA13 is MSB and DA0 is LSB. Internal pulldown.
	2		
	3		
	4		
	5		
	6		
	7		
	8		
	9		
	10		
	11		
	12		
	13		
	14		

**Pin Functions (continued)**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DB[13:0]	23	I	Data port B. DB13 is MSB and DB0 is LSB. Internal pulldown.
	24		
	25		
	26		
	27		
	28		
	29		
	30		
	31		
	32		
	33		
DGND	15	I	Digital ground
	21		
DVDD	16	I	Digital supply voltage
	22		
EXTIO	43	I/O	Internal reference output (bypass with 0.1 $\mu$ F to AGND) or external reference input
GSET	42	I	Gain-setting mode: H – 1 resistor, L – 2 resistors. Internal pullup.
IOUTA1	46	O	DACA current output. Full-scale with all bits of DA high.
IOUTA2	45	O	DACA complementary current output. Full-scale with all bits of DA low.
IOUTB1	39	O	DACB current output. Full-scale with all bits of DB high.
IOUTB2	40	O	DACB complementary current output. Full-scale with all bits of DB low.
MODE	48	I	Mode Select: H – Dual Bus, L – Interleaved. Internal pullup.
SLEEP	37	I	Sleep function control input: H – DAC in power-down mode, L – DAC in operating mode. Internal pulldown.
WRTA/WRTIQ	17	I	Input write signal for PORT A (WRTIQ in interleaving mode)
WRTB/SELECTIQ	20	I	Input write signal for PORT B (SELECTIQ in interleaving mode)

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	AVDD <sup>(2)</sup>	-0.5	4	V
	DVDD <sup>(3)</sup>			
Voltage between AGND and DGND		-0.5	0.5	V
Voltage between AVDD and DVDD				
Supply voltage	DA [13:0] and DB [13:0] <sup>(3)</sup>	-0.5	DVDD + 0.5	V
	MODE, SLEEP, CLKA, CLKB, WRTA, WRTB <sup>(3)</sup>	-0.5	DVDD + 0.5	V
	IOUTA1, IOUTA2, IOUTB1, IOUTB2 <sup>(2)</sup>	-1	AVDD + 0.5	V
	EXTIO, BIASJ_A, BIASJ_B, GSET <sup>(2)</sup>	-0.5	AVDD + 0.5	V
Peak input current (any input)		20		mA
Peak total input current (all inputs)		-30		mA
Operating free-air temperature range		-40	85	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Measured with respect to AGND.

(3) Measured with respect to DGND.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
<b>Supplies</b>				
AVDD	3.0	3.3	3.6	V
DVDD	3.0	3.3	3.6	V
I <sub>(AVDD)</sub> Analog supply current		75	90	mA
I <sub>(DVDD)</sub> Digital supply current		25	38	mA
<b>Analog Output</b>				
I <sub>O(FS)</sub> Full-scale output current	2		20	mA
Output voltage compliance range	-1		1.25	V
<b>Clock Interface (CLK, CLKC)</b>				
CLKINPUT Frequency			275	MHz

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DAC5672	
		PFB (TQFP)	UNIT
		48 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	64.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	16.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	27.7	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	27.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over T<sub>A</sub>, AVDD = DVDD = 3.3 V, I<sub>OUTFS</sub> = 20 mA, independent gain set mode, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DC SPECIFICATIONS</b>						
Resolution			14			Bits
<b>DC ACCURACY<sup>(1)</sup></b>						
INL	Integral nonlinearity	1 LSB = I <sub>OUTFS</sub> / 2 <sup>14</sup> , T <sub>MIN</sub> to T <sub>MAX</sub>	-4	±1.1	4	LSB
DNL	Differential nonlinearity		-3	±0.75	3	LSB
<b>ANALOG OUTPUT</b>						
Offset error		Midscale value		±0.03		%FSR
Offset mismatch		Midscale value		±0.03		%FSR
Gain error		With external reference		±0.25		%FSR
		With internal reference		±0.25		%FSR
Minimum full-scale output current <sup>(2)</sup>				2		mA
Maximum full-scale output current <sup>(2)</sup>				20		mA
Gain mismatch		With external reference	-2	0.2	2	%FSR
		With internal reference	-2	0.2	2	%FSR
Output voltage compliance range <sup>(3)</sup>			-1		1.25	V
R <sub>O</sub>	Output resistance			300		kΩ
C <sub>O</sub>	Output capacitance			5		pF
<b>REFERENCE OUTPUT</b>						
Reference voltage			1.14	1.2	1.26	V
Reference output current <sup>(4)</sup>				100		nA
<b>REFERENCE INPUT</b>						
V <sub>EXTIO</sub>	Input voltage		0.1		1.25	V
R <sub>I</sub>	Input resistance			1		MΩ
Small signal bandwidth				300		kHz
C <sub>I</sub>	Input capacitance			100		pF
<b>TEMPERATURE COEFFICIENTS</b>						
Offset drift				2	10	ppm of FSR/°C

(1) Measured differently through 50 Ω to AGND.

(2) Nominal full-scale current (I<sub>OUTFS</sub>) equals 32 times the I<sub>BIAS</sub> current

(3) The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5672 device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.

(4) Use an external buffer amplifier with high-impedance input to drive any external load.

## Electrical Characteristics (continued)

over  $T_A$ ,  $AVDD = DVDD = 3.3\text{ V}$ ,  $I_{OUTFS} = 20\text{ mA}$ , independent gain set mode, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gain drift	With external reference (DACA)		10	43	ppm of FSR/°C
	With external reference (DACB)		20	80	
	With internal reference		40	160	ppm of FSR/°C
Reference voltage drift			20		ppm /°C

## 6.6 Electrical Characteristics

over  $T_A$ ,  $AVDD = DVDD = 3.3\text{ V}$ ,  $I_{OUTFS} = 20\text{ mA}$ ,  $f_{DATA} = 200\text{ MSPS}$ ,  $f_{OUT} = 1\text{ MHz}$ , independent gain set mode, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>					
AVDD	Analog supply voltage	3	3.3	3.6	V
DVDD	Digital supply voltage	3	3.3	3.6	V
$I_{AVDD}$	Analog supply current	Including output current through load resistor	75	90	mA
		Sleep mode with clock	2.5	6	
		Sleep mode without clock	2.5		
$I_{DVDD}$	Digital supply current	$f_{DATA} = 200\text{ MSPS}$ , $f_{OUT} = 1\text{ MHz}$	25	38	mA
		Sleep mode with clock	13.4	18	
		Sleep mode without clock	0.6		
Power dissipation		$f_{DATA} = 200\text{ MSPS}$ , $f_{OUT} = 1\text{ MHz}$	330	390	mW
		Sleep mode with clock	53		
		Sleep mode without clock	9.2		
		$f_{DATA} = 275\text{ MSPS}$ , $f_{OUT} = 20\text{ MHz}$	350		
APSR	Analog power supply rejection ratio	-0.2	-0.01	0.2	%FSR/V
DPSRR	Digital power supply rejection ratio	-0.2	0	0.2	%FSR/V
$T_A$	Operating free-air temperature	-40		85	°C

## 6.7 Electrical Characteristics: AC Characteristics

AC specifications over  $T_A$ ,  $AVDD = DVDD = 3.3\text{ V}$ ,  $I_{OUTFS} = 20\text{ mA}$ , differential 1:1 impedance ratio transformer coupled output, 50- $\Omega$  doubly terminated load (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG OUTPUT</b>					
$f_{clk}$	Maximum output update rate <sup>(1)</sup>	275			MSPS
$t_s$	Output settling time to 0.1% (DAC)	Midscale transition	20		ns
$t_r$	Output rise time 10% to 90% (OUT)		1.4		ns
$t_f$	Output fall time 10% to 90% (OUT)		1.5		ns
Output noise	$I_{OUTFS} = 20\text{ mA}$		55		pA/ $\sqrt{\text{Hz}}$
	$I_{OUTFS} = 2\text{ mA}$		30		pA/ $\sqrt{\text{Hz}}$
<b>AC LINEARITY</b>					

(1)

**Electrical Characteristics: AC Characteristics (continued)**

 AC specifications over  $T_A$ ,  $AVDD = DVDD = 3.3\text{ V}$ ,  $I_{OUTFS} = 20\text{ mA}$ , differential 1:1 impedance ratio transformer coupled output, 50- $\Omega$  doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SFDR	Spurious-free dynamic range	1st Nyquist zone: $T_A = 25^\circ\text{C}$ $f_{DATA} = 50\text{ MSPS}$ $f_{OUT} = 1\text{ MHz}$ $I_{OUTFS} = 0\text{ dB}$		83		dBc
		1st Nyquist zone: $T_A = 25^\circ\text{C}$ $f_{DATA} = 50\text{ MSPS}$ $f_{OUT} = 1\text{ MHz}$ $I_{OUTFS} = -6\text{ dB}$		80		
		1st Nyquist zone: $T_A = 25^\circ\text{C}$ $f_{DATA} = 50\text{ MSPS}$ $f_{OUT} = 1\text{ MHz}$ $I_{OUTFS} = -12\text{ dB}$		79		
		1st Nyquist zone: $T_A = 25^\circ\text{C}$ $f_{DATA} = 100\text{ MSPS}$ $f_{OUT} = 5\text{ MHz}$		84		
		1st Nyquist zone, $T_A = 25^\circ\text{C}$ , $f_{DATA} = 100\text{ MSPS}$ , $f_{OUT} = 20\text{ MHz}$		79		
		1st Nyquist zone, $T_{MIN}$ to $T_{MAX}$ , $f_{DATA} = 200\text{ MSPS}$ , $f_{OUT} = 20\text{ MHz}$	68	75		
		1st Nyquist zone, $T_A = 25^\circ\text{C}$ , $f_{DATA} = 200\text{ MSPS}$ , $f_{OUT} = 41\text{ MHz}$		72		
		1st Nyquist zone, $T_A = 25^\circ\text{C}$ , $f_{DATA} = 275\text{ MSPS}$ , $f_{OUT} = 20\text{ MHz}$		74		
SNR	Signal-to-noise ratio	1st Nyquist zone, $T_A = 25^\circ\text{C}$ , $f_{DATA} = 100\text{ MSPS}$ , $f_{OUT} = 5\text{ MHz}$		77		dB
		1st Nyquist zone, $T_A = 25^\circ\text{C}$ , $f_{DATA} = 160\text{ MSPS}$ , $f_{OUT} = 20\text{ MHz}$		70		dB
ACLR	Adjacent channel leakage ratio	W-CDMA signal with 3.84-MHz bandwidth, $f_{DATA} = 61.44\text{ MSPS}$ , $IF = 15.360\text{ MHz}$		75		dB
		W-CDMA signal with 3.84-MHz bandwidth, $f_{DATA} = 122.88\text{ MSPS}$ , $IF = 30.72\text{ MHz}$		73		dB
		W-CDMA signal with 3.84-MHz bandwidth, $f_{DATA} = 61.44\text{ MSPS}$ , baseband		78		dB
		W-CDMA signal with 3.84-MHz bandwidth, $f_{DATA} = 122.88\text{ MSPS}$ , baseband		78		dB
IMD3	Third-order two-tone intermodulation	Each tone at $-6\text{ dBFS}$ , $T_A = 25^\circ\text{C}$ , $f_{DATA} = 200\text{ MSPS}$ , $f_{OUT} = 45.4\text{ MHz}$ and $46.4\text{ MHz}$		65		dBc
		Each tone at $-6\text{ dBFS}$ , $T_A = 25^\circ\text{C}$ , $f_{DATA} = 100\text{ MSPS}$ , $f_{OUT} = 15.1\text{ MHz}$ and $16.1\text{ MHz}$		79		dBc
IMD	Four-tone intermodulation	Each tone at $-12\text{ dBFS}$ , $T_A = 25^\circ\text{C}$ , $f_{DATA} = 100\text{ MSPS}$ , $f_{OUT} = 15.6, 15.8, 16.2,$ and $16.4\text{ MHz}$		79		dBc
		Each tone at $-12\text{ dBFS}$ , $T_A = 25^\circ\text{C}$ , $f_{DATA} = 165\text{ MSPS}$ , $f_{OUT} = 68.8, 69.6, 71.2,$ and $72\text{ MHz}$		61		dBc
		Each tone at $-12\text{ dBFS}$ , $T_A = 25^\circ\text{C}$ , $f_{DATA} = 165\text{ MSPS}$ , $f_{OUT} = 19, 19.1, 19.3,$ and $19.4\text{ MHz}$		73		dBc



## Electrical Characteristics: AC Characteristics (continued)

AC specifications over  $T_A$ ,  $AVDD = DVDD = 3.3\text{ V}$ ,  $I_{OUTFS} = 20\text{ mA}$ , differential 1:1 impedance ratio transformer coupled output, 50- $\Omega$  doubly terminated load (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Channel isolation	$T_A = 25^\circ\text{C}$ , $f_{\text{DATA}} = 165\text{ MSPS}$ , $f_{\text{OUT}}(\text{CH1}) = 20\text{ MHz}$ , $f_{\text{OUT}}(\text{CH2}) = 21\text{ MHz}$		95		dBc

## 6.8 Electrical Characteristics: Digital Characteristics

Digital specifications over  $T_A$ ,  $AVDD = DVDD = 3.3\text{ V}$ ,  $I_{OUTFS} = 20\text{ mA}$ , (unless otherwise noted)

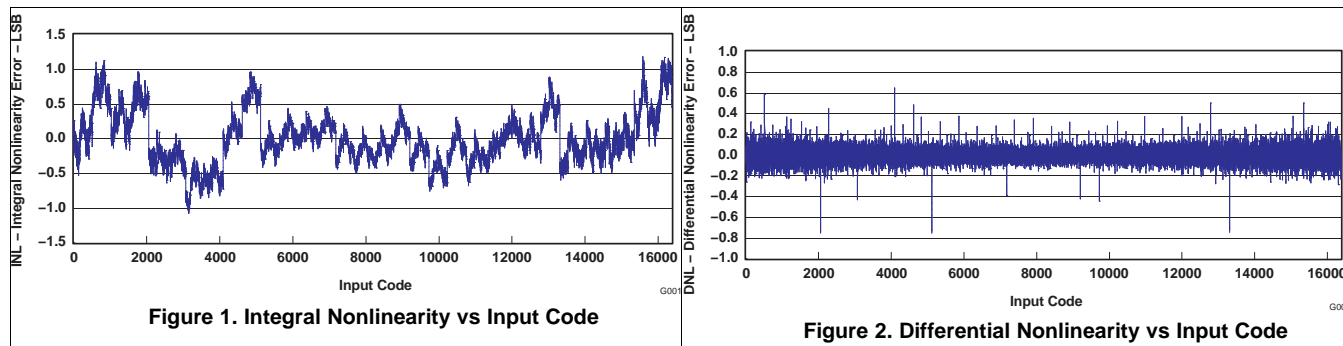
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DIGITAL INPUT</b>					
$V_{IH}$	High-level input voltage	2		3.3	V
$V_{IL}$	Low-level input voltage	0		0.8	V
$I_{IH}$	High-level input current		$\pm 50$	0.8	$\mu\text{A}$
$I_{IL}$	Low-level input current		$\pm 10$		$\mu\text{A}$
$I_{IH}(\text{GSET})$	High-level input current, GSET pin		7		$\mu\text{A}$
$I_{IL}(\text{GSET})$	Low-level input current, GSET pin		-80		$\mu\text{A}$
$I_{IH}(\text{MODE})$	High-level input current, MODE pin		-30		$\mu\text{A}$
$I_{IL}(\text{MODE})$	Low-level input current, MODE pin		-80		$\mu\text{A}$
$C_I$	Input capacitance		5		pF

## 6.9 Switching Characteristics

digital specifications over  $T_A$ ,  $AVDD = DVDD = 3.3\text{ V}$ ,  $I_{OUTFS} = 20\text{ mA}$ , (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{su}$	Dual bus mode	1			ns
	Single-bus interleaved mode		0.5		
$t_h$	Dual bus mode	1			ns
	Single-bus interleaved mode		0.5		
$t_{LPH}$	Dual bus mode		1		ns
	Single-bus interleaved mode				
$t_{LAT}$	Dual bus mode	4		4	clk
	Single-bus interleaved mode	4		4	
$t_{PD}$	Dual bus mode		1.5		ns
	Single-bus interleaved mode		1.5		

## 6.10 Typical Characteristics



Typical Characteristics (continued)

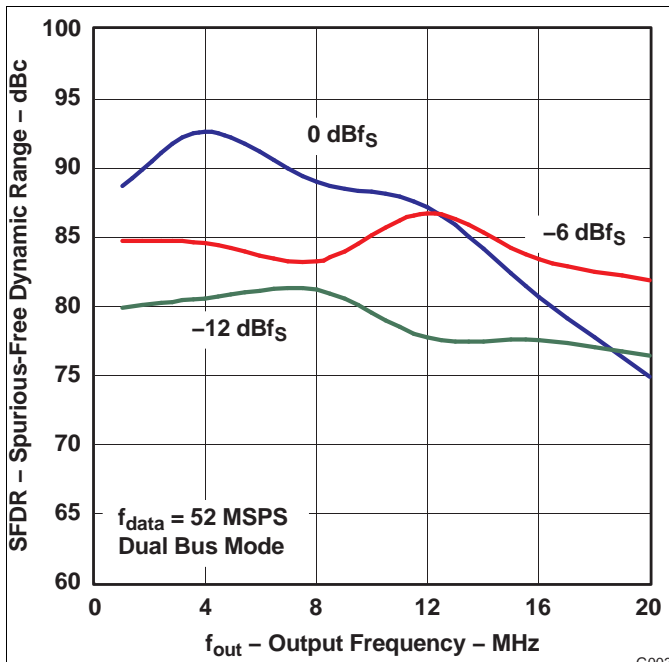


Figure 3. Spurious-Free Dynamic Range vs Output Frequency

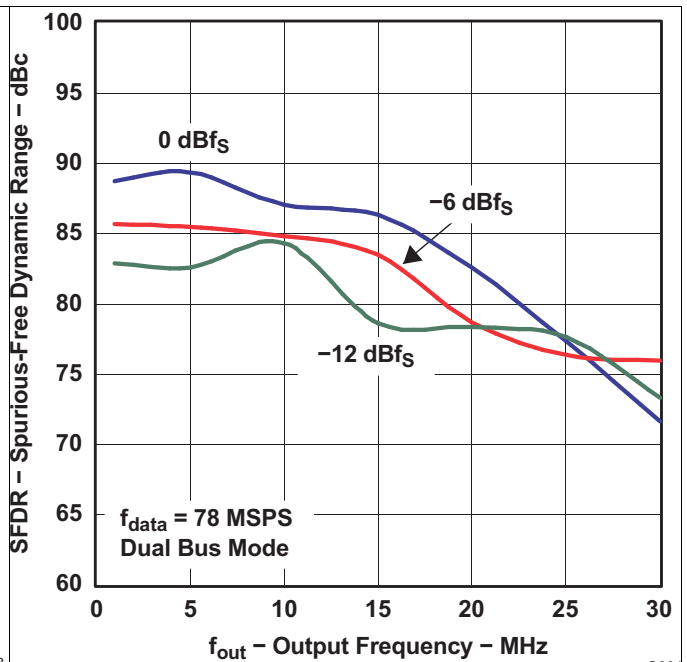


Figure 4. Spurious-Free Dynamic Range vs Output Frequency

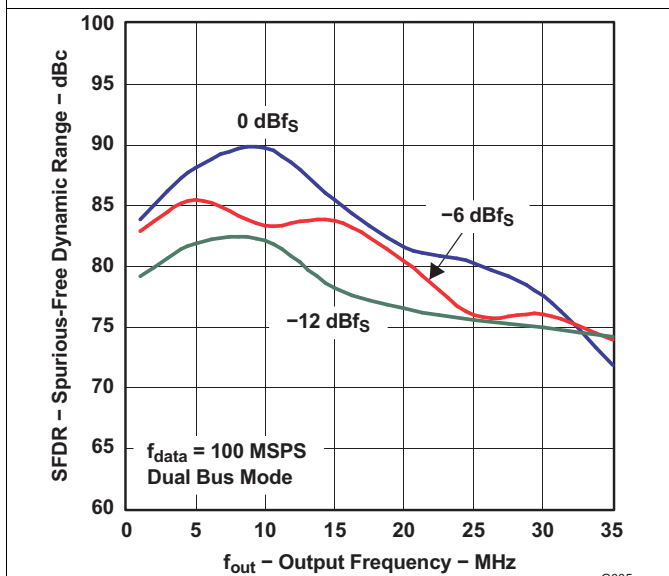


Figure 5. Spurious-Free Dynamic Range vs Output Frequency

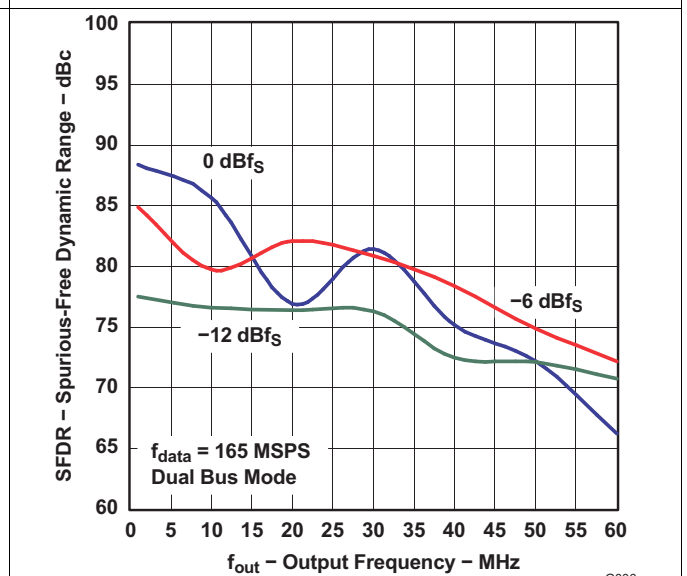
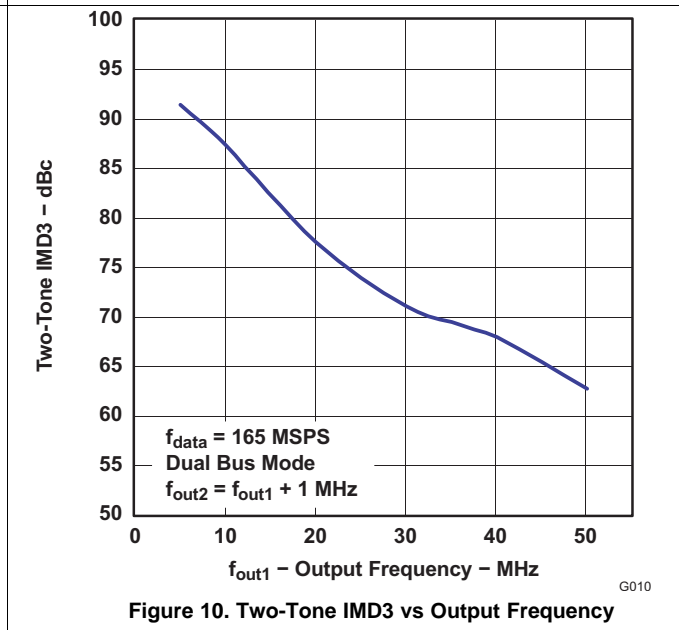
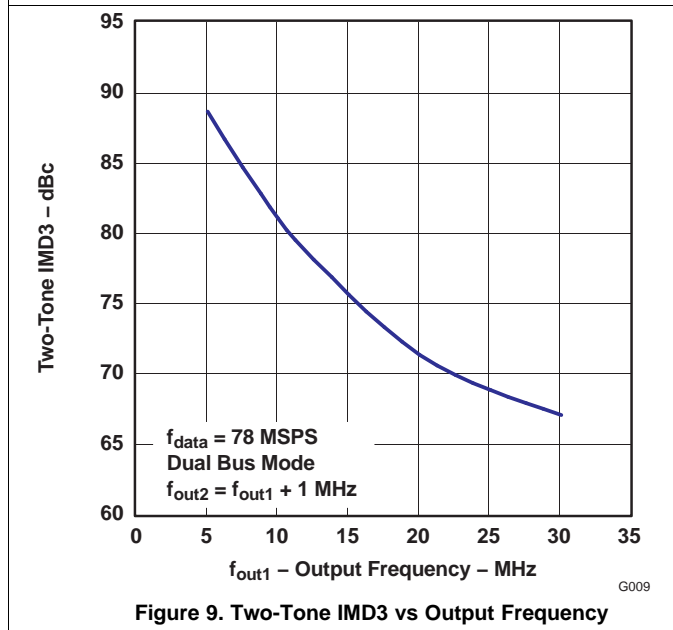
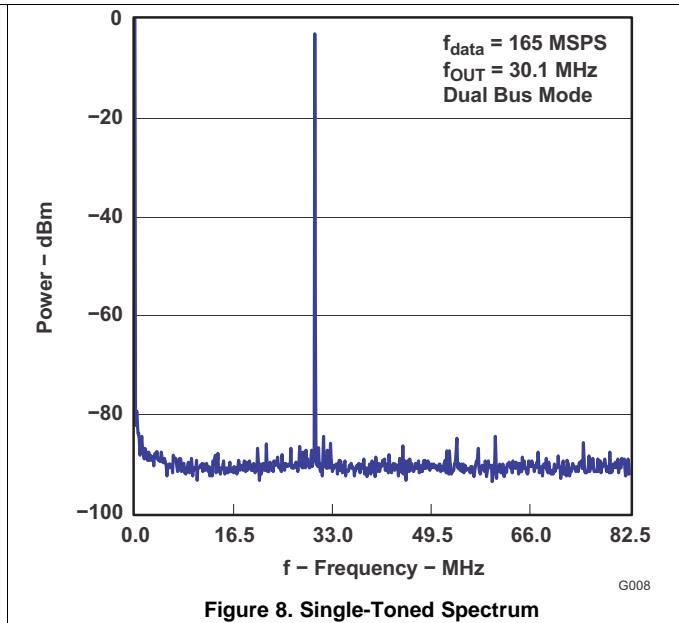
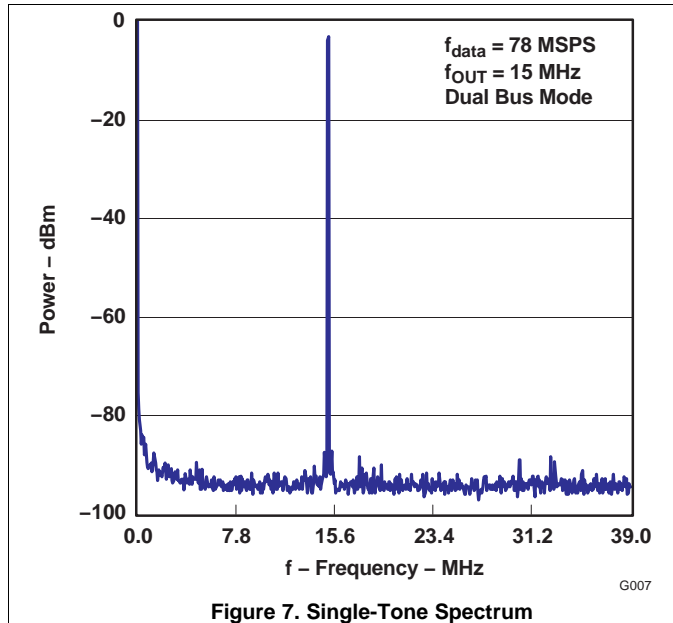
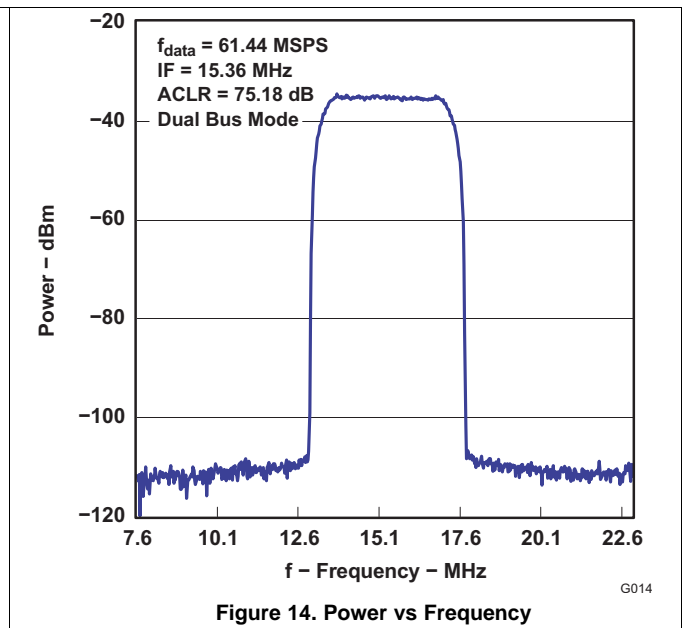
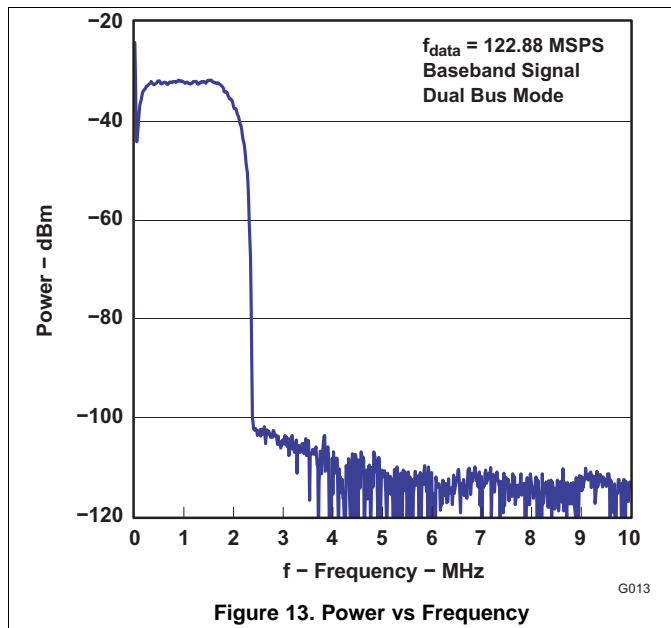
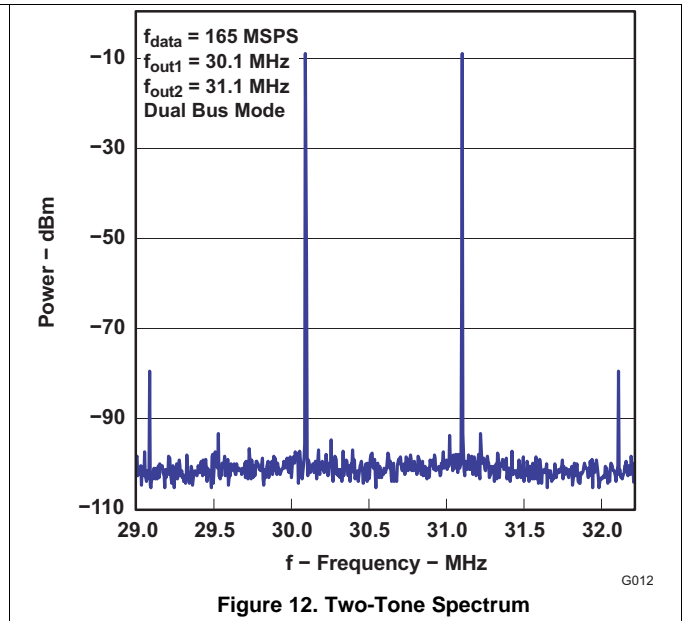
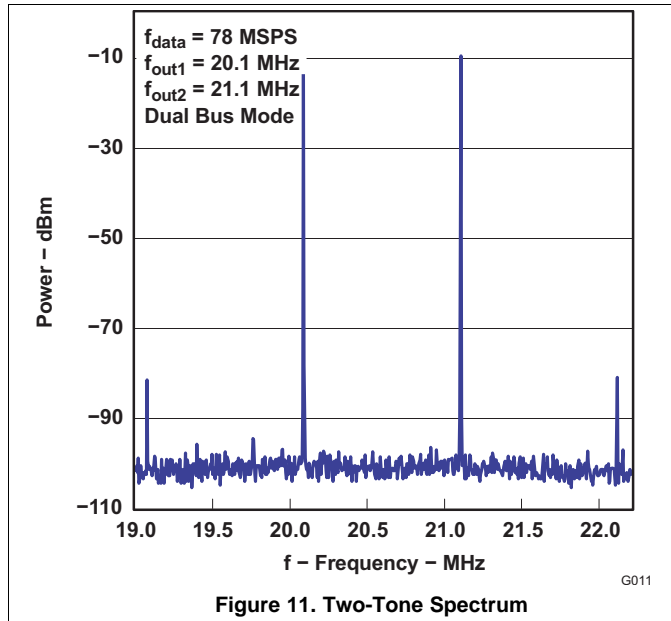


Figure 6. Spurious-Free Dynamic Range vs Output Frequency

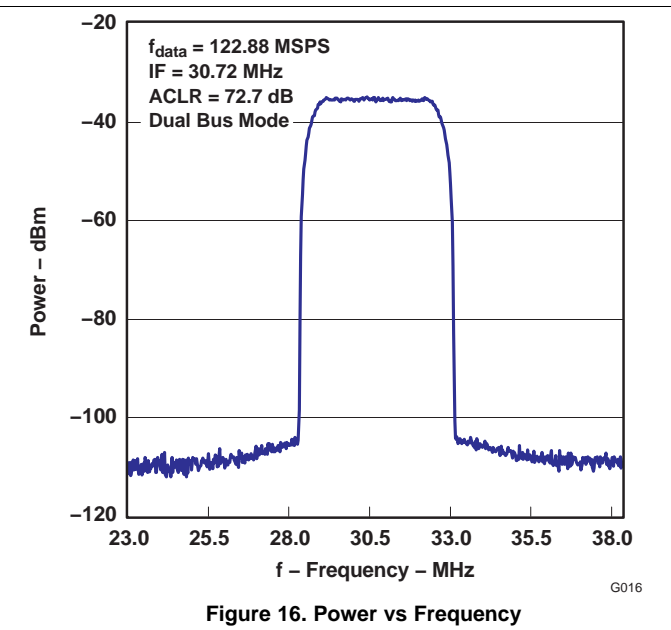
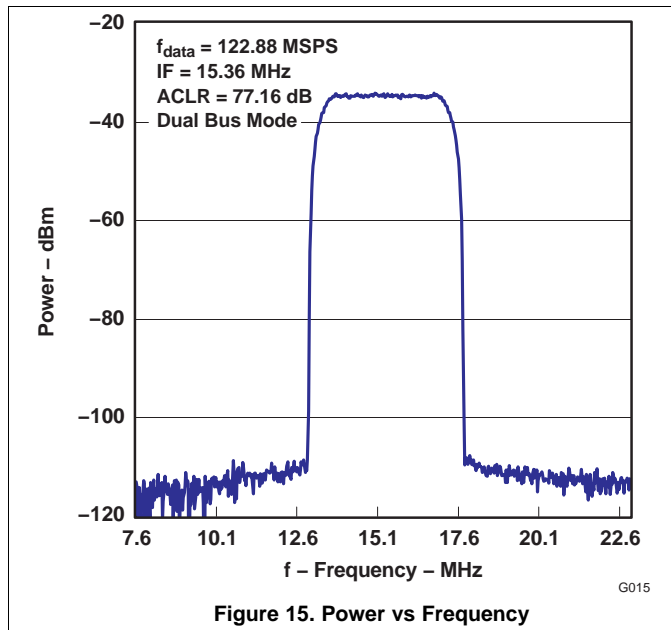
Typical Characteristics (continued)



**Typical Characteristics (continued)**



Typical Characteristics (continued)



## 7 Detailed Description

### 7.1 Overview

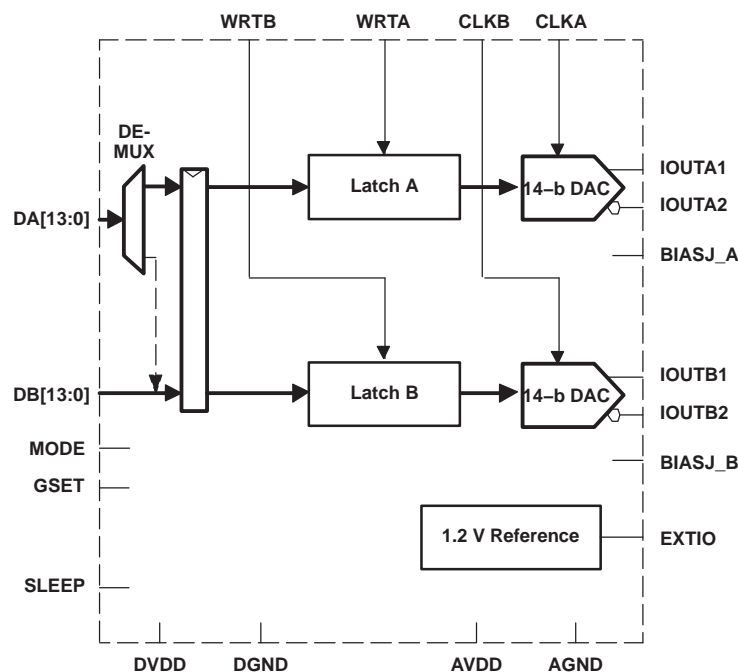
The architecture of the DAC5672 uses a current steering technique to enable fast switching and high update rate. The core element within the monolithic DAC is an array of segmented current sources that are designed to deliver a full-scale output current of up to 20 mA. An internal decoder addresses the differential current switches each time the DAC is updated and a corresponding output current is formed by steering all currents to either output summing node, IOUT1 or IOUT2. The complementary outputs deliver a differential output signal, which improves the dynamic performance through reduction of even-order harmonics, common-mode signals (noise), and double the peak-to-peak output signal swing by a factor of two, as compared to single-ended operation.

The segmented architecture results in a significant reduction of the glitch energy and improves the dynamic performance (SFDR) and DNL. The current outputs maintain a very high output impedance of greater than 300 k $\Omega$ .

When pin 42 (GSET) is high (simultaneous gain set mode), the full-scale output current for DACs is determined by the ratio of the internal reference voltage (1.2 V) and an external resistor ( $R_{SET}$ ) connected to BIASJ\_A. When GSET is low (independent gain set mode), the full-scale output current for each DAC is determined by the ratio of the internal reference voltage (1.2 V) and separate external resistors ( $R_{SET}$ ) connected to BIASJ\_A and BIASJ\_B. The resulting  $I_{REF}$  is internally multiplied by a factor of 32 to produce an effective DAC output current that can range from 2 mA to 20 mA, depending on the value of  $R_{SET}$ .

The DAC5672 is split into a digital and an analog portion, each of which is powered through its own supply pin. The digital section includes edge-triggered input latches and the decoder logic, while the analog section comprises both the current source array with its associated switches, and the reference circuitry.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Input Interfaces

The DAC5672 features two operating modes selected by the MODE pin, as shown in Table 1.

- For dual-bus input mode, the device essentially consists of two separate DACs. Each DAC has its own separate data input bus, clock input, and data write signal (data latch-in).
- In single-bus interleaved mode, the data must be presented interleaved at the A-channel input bus. The B-channel input bus is not used in this mode. The clock and write input are now shared by both DACs.

Table 1. Operating Modes

MODE PIN	BUS INPUT
MODE pin connected to DGND	Single-bus interleaved mode, clock and write input equal for both DACs
MODE pin connected to DVDD	Dual-bus mode, DACs operate independently

#### 7.3.2 Dual-Bus Data Interface and Timing

In dual-bus mode, the MODE pin is connected to DVDD. The two converter channels within the DAC5672 consist of two independent, 14-bit, parallel data ports. Each DAC channel is controlled by its own set of write (WRTA, WRTB) and clock (CLKA, CLKB) lines. The WRTA, WRTB lines control the channel input latches and the CLKA, CLKB lines control the DAC latches. The data is first loaded into the input latch by a rising edge of the WRTA, WRTB line.

The internal data transfer requires a correct sequence of write and clock inputs, since essentially two clock domains having equal periods (but possibly different phases) are input to the DAC5672. The DAC5672 is defined by a minimum requirement of the time between the rising edge of the clock and the rising edge of the write inputs. The rising edge of CLKA, CLKB must occur at the same time or before the rising edge of the WRTA, WRTB signal. A minimum delay of 2 ns must be maintained if the rising edge of the clock occurs after the rising edge of the write. Note that these conditions are satisfied when the clock and write inputs are connected externally. Note that all specifications were measured with the WRTA, WRTB and CLKA, CLKB lines connected together.

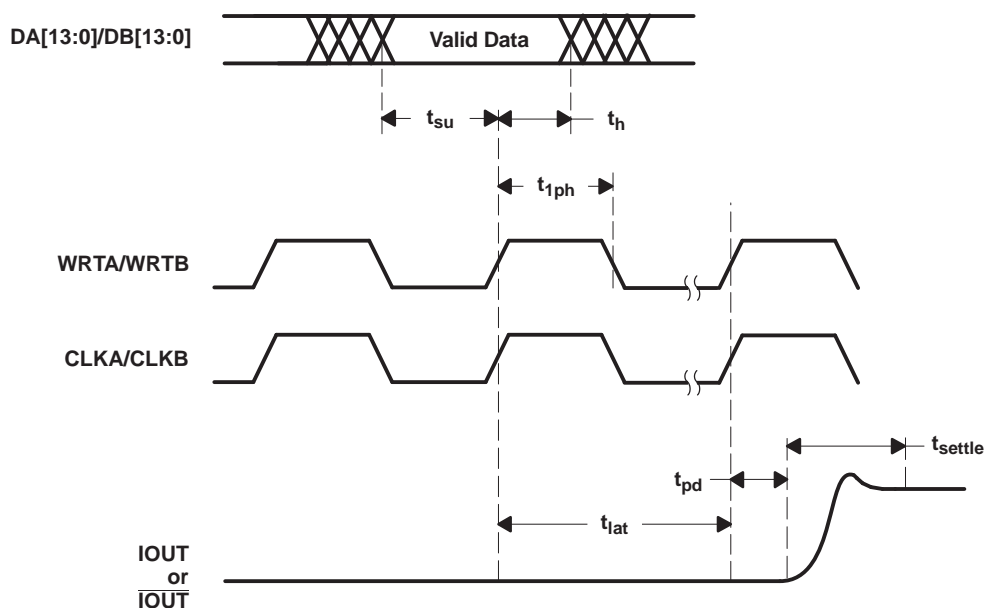


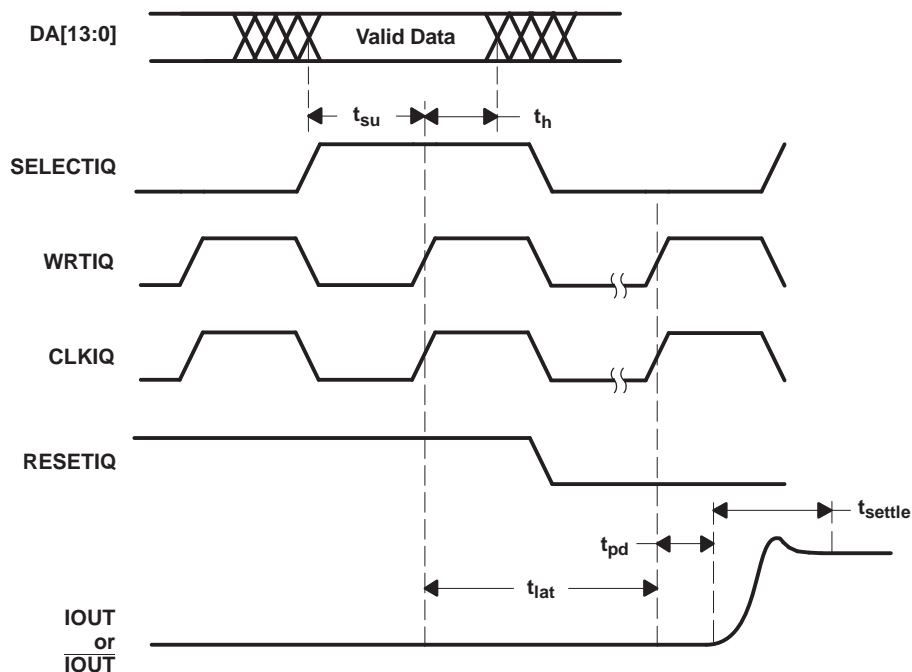
Figure 17. Dual-Bus Mode Operation

### 7.3.3 Single-Bus Interleaved Data Interface and Timing

In single-bus interleaved mode, the MODE pin is connected to DGND. Figure 18 shows the timing diagram. In interleaved mode, the A- and B-channels share the write input (WRTIQ) and update clock (CLKIQ and internal CLKDACIQ). Multiplexing logic directs the input word at the A-channel input bus to either the A-channel input latch (SELECTIQ is high) or to the B-channel input latch (SELECTIQ is low). When SELECTIQ is high, the data value in the B-channel latch is retained by presenting the latch output data to its input again. When SELECTIQ is low, the data value in the A-channel latch is retained by presenting the latch output data to its input.

In interleaved mode, the A-channel input data rate is twice the update rate of the DAC core. As in dual-bus mode, it is important to maintain a correct sequence of write and clock inputs. The edge-triggered flip-flops latch the A- and B-channel input words on the rising edge of the write input (WRTIQ). This data is presented to the A- and B-DAC latches on the following falling edge of the write inputs. The DAC5672 clock input is divided by a factor of two before it is presented to the DAC latches.

Correct pairing of the A- and B-channel data is done by RESETIQ. In interleaved mode, the clock input CLKIQ is divided by two, which would translate to a non-deterministic relation between the rising edges of the CLKIQ and CLKDACIQ. RESETIQ ensures, however, that the correct position of the rising edge of CLKDACIQ with respect to the data at the input of the DAC latch is determined. CLKDACIQ is disabled (low) when RESETIQ is high.



**Figure 18. Single-Bus Interleaved Mode Operation**

## 7.4 Device Functional Modes

### 7.4.1 DAC Transfer Function

Each of the DACs in the DAC5672 has a set of complementary current outputs, IOU1 and IOU2. The full-scale output current,  $I_{OUTFS}$ , is the summation of the two complementary output currents:

$$I_{OUTFS} = I_{OUT1} + I_{OUT2} \quad (1)$$

The individual output currents depend on the DAC code and can be expressed as:

$$I_{OUT1} = I_{OUTFS} \times \left( \frac{\text{Code}}{16384} \right) \quad (2)$$

$$I_{OUT2} = I_{OUTFS} \times \left( \frac{16383 - \text{Code}}{16384} \right) \quad (3)$$



## Device Functional Modes (continued)

where Code is the decimal representation of the DAC data input word. Additionally,  $I_{OUTFS}$  is a function of the reference current  $I_{REF}$ , which is determined by the reference voltage and the external setting resistor ( $R_{SET}$ ).

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \quad (4)$$

In most cases, the complementary outputs drive resistive loads or a terminated transformer. A signal voltage develops at each output according to:

$$V_{OUT1} = I_{OUT1} \times R_{LOAD} \quad (5)$$

$$V_{OUT2} = I_{OUT2} \times R_{LOAD} \quad (6)$$

The value of the load resistance is limited by the output compliance specification of the DAC5672. To maintain specified linearity performance, the voltage for  $I_{OUT1}$  and  $I_{OUT2}$  must not exceed the maximum allowable compliance range.

The total differential output voltage is:

$$V_{OUTDIFF} = V_{OUT1} - V_{OUT2} \quad (7)$$

$$V_{OUTDIFF} = \frac{(2 \times \text{Code} - 16383)}{16384} \times I_{OUTFS} \times R_{LOAD} \quad (8)$$

### 7.4.2 Analog Outputs

The DAC5672 provides two complementary current outputs,  $I_{OUT1}$  and  $I_{OUT2}$ . The simplified circuit of the analog output stage representing the differential topology is shown in Figure 19. The output impedance of  $I_{OUT1}$  and  $I_{OUT2}$  results from the parallel combination of the differential switches, along with the current sources and associated parasitic capacitances.

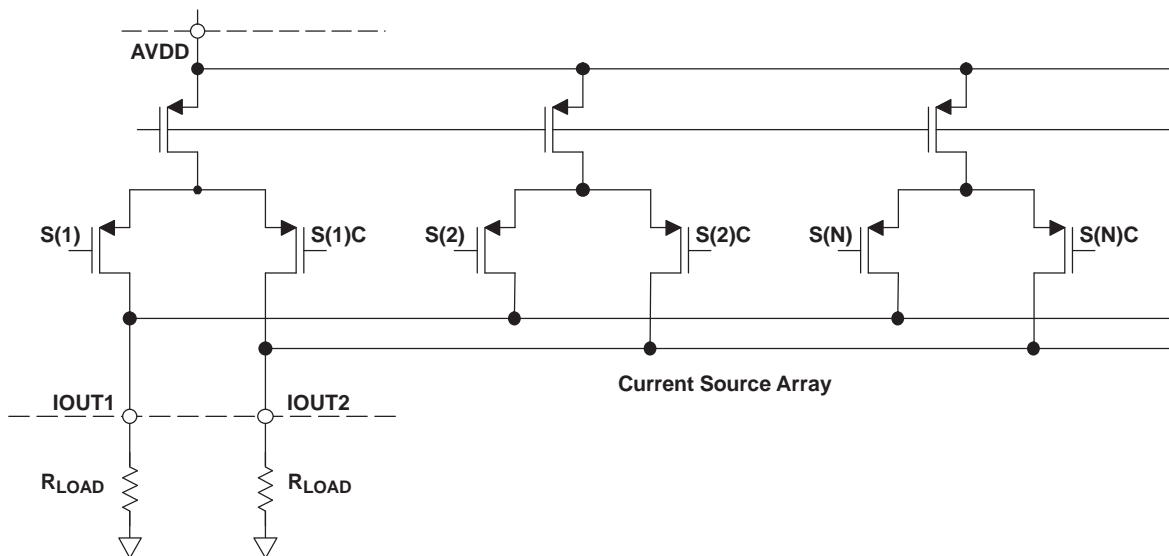


Figure 19. Analog Outputs

The signal voltage swing that may develop at the two outputs,  $I_{OUT1}$  and  $I_{OUT2}$ , is limited by a negative and positive compliance. The negative limit of  $-1$  V is given by the breakdown voltage of the CMOS process and exceeding it compromises the reliability of the DAC5672 (or even causes permanent damage). With the full-scale output set to 20 mA, the positive compliance equals 1.2 V. Note that the compliance range decreases to about 1 V for a selected output current of  $I_{OUTFS} = 2$  mA. Care must be taken that the configuration of DAC5672 does not exceed the compliance range to avoid degradation of the distortion performance and integral linearity.

### Device Functional Modes (continued)

Best distortion performance is typically achieved with the maximum full-scale output signal limited to approximately  $0.5 V_{PP}$ . This is the case for a  $50\text{-}\Omega$  doubly-terminated load and a  $20\text{-mA}$  full-scale output current. A variety of loads can be adapted to the output of the DAC5672 by selecting a suitable transformer while maintaining optimum voltage levels at IOUT1 and IOUT2. Furthermore, using the differential output configuration in combination with a transformer is instrumental for achieving excellent distortion performance. Common-mode errors, such as even-order harmonics or noise, can be substantially reduced. This is particularly the case with high output frequencies.

For those applications requiring the optimum distortion and noise performance, it is recommended to select a full-scale output of  $20\text{ mA}$ . A lower full-scale range of  $2\text{ mA}$  may be considered for applications that require low power consumption, but can tolerate a slight reduction in performance level.

#### 7.4.3 Output Configurations

The current outputs of the DAC5672 allow for a variety of configurations. As mentioned previously, utilizing the converter's differential outputs yield the best dynamic performance. Such a differential output circuit may consist of an RF transformer or a differential amplifier configuration. The transformer configuration is ideal for most applications with ac coupling, while op amps are suitable for a dc-coupled configuration.

The single-ended configuration may be considered for applications requiring a unipolar output voltage. Connecting a resistor from either one of the outputs to ground converts the output current into a ground-referenced voltage signal. To improve on the dc linearity by maintaining a virtual ground, an I-to-V or op-amp configuration may be considered.

#### 7.4.4 Differential With Transformer

Using an RF transformer provides a convenient way of converting the differential output signal into a single-ended signal while achieving excellent dynamic performance. The appropriate transformer must be carefully selected based on the output frequency spectrum and impedance requirements.

The differential transformer configuration has the benefit of significantly reducing common-mode signals, thus improving the dynamic performance over a wide range of frequencies. Furthermore, by selecting a suitable impedance ratio (winding ratio) the transformer can provide optimum impedance matching while controlling the compliance voltage for the converter outputs.

Figure 20 and Figure 21 show  $50\text{-}\Omega$  doubly-terminated transformer configurations with 1:1 and 4:1 impedance ratios, respectively. Note that the center tap of the primary input of the transformer has to be grounded to enable a dc-current flow. Applying a  $20\text{-mA}$  full-scale output current would lead to a  $0.5\text{-}V_{PP}$  output for a 1:1 transformer and a  $1\text{-}V_{PP}$  output for a 4:1 transformer. In general, the 1:1 transformer configuration will have slightly better output distortion, but the 4:1 transformer will have 6 dB higher output power.

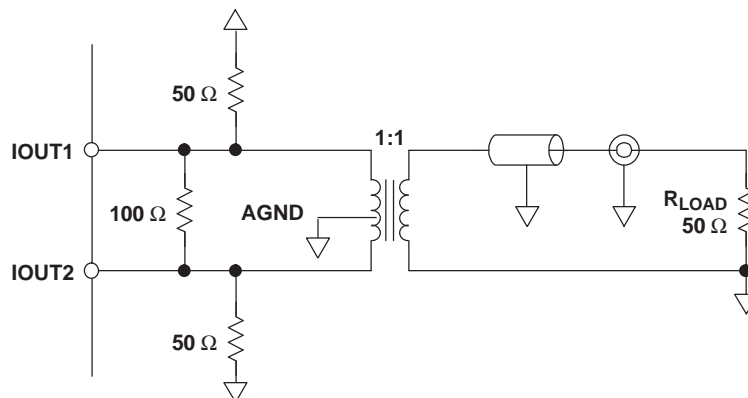


Figure 20. Driving a Doubly-Terminated  $50\text{-}\Omega$  Cable Using a 1:1 Impedance Ratio Transformer

## Device Functional Modes (continued)

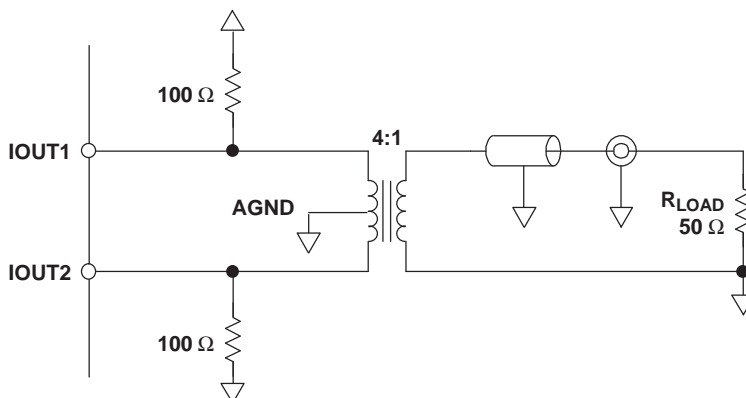


Figure 21. Driving a Doubly-Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

### 7.4.5 Single-Ended Configuration

Figure 22 shows the single-ended output configuration, where the output current  $I_{OUT1}$  flows into an equivalent load resistance of 25 Ω. Node IOUT2 must be connected to AGND or terminated with a resistor of 25 Ω to AGND. The nominal resistor load of 25 Ω gives a differential output swing of 1 V<sub>PP</sub> when applying a 20-mA full-scale output current.

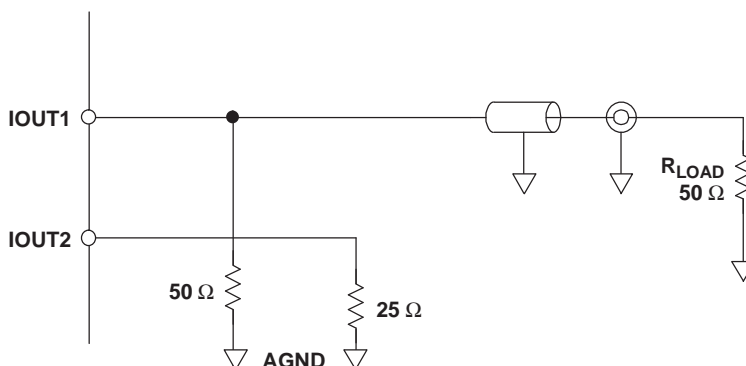


Figure 22. Driving a Doubly-Terminated 50-Ω Cable Using a Single-Ended Output

### 7.4.6 Reference Operation

#### 7.4.6.1 Internal Reference

The DAC5672 has an on-chip reference circuit which comprises a 1.2-V bandgap reference and two control amplifiers, one for each DAC. The full-scale output current,  $I_{OUTFS}$ , of the DAC5672 is determined by the reference voltage,  $V_{REF}$ , and the value of resistor  $R_{SET}$ .  $I_{OUTFS}$  can be calculated by:

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \quad (9)$$

The reference control amplifier operates as a V-to-I converter producing a reference current,  $I_{REF}$ , which is determined by the ratio of  $V_{REF}$  and  $R_{SET}$  (see Equation 9). The full-scale output current,  $I_{OUTFS}$ , results from multiplying  $I_{REF}$  by a fixed factor of 32.

Using the internal reference, a 2-kΩ resistor value results in a full-scale output of approximately 20 mA. Resistors with a tolerance of 1% or better should be considered. Selecting higher values, the output current can be adjusted from 20 mA down to 2 mA. Operating the DAC5672 at lower than 20-mA output currents may be desirable for reasons of reducing the total power consumption, improving the distortion performance, or observing the output compliance voltage limitations for a given load condition.

## Device Functional Modes (continued)

It is recommended to bypass the EXTIO pin with a ceramic chip capacitor of 0.1  $\mu\text{F}$  or more. The control amplifier is internally compensated and its small signal bandwidth is approximately 300 kHz.

### 7.4.6.2 External Reference

The internal reference can be disabled by simply applying an external reference voltage into the EXTIO pin, which in this case functions as an input. The use of an external reference may be considered for applications that require higher accuracy and drift performance or to add the ability of dynamic gain control.

While a 0.1- $\mu\text{F}$  capacitor is recommended to be used with the internal reference, it is optional for the external reference operation. The reference input, EXTIO, has a high input impedance (1 M $\Omega$ ) and can easily be driven by various sources. Note that the voltage range of the external reference must stay within the compliance range of the reference input.

### 7.4.6.3 Gain Setting Option

The full-scale output current on the DAC5672 can be set two ways: either for each of the two DAC channels independently or for both channels simultaneously. For the independent gain set mode, the GSET pin (pin 42) must be low (that is, connected to AGND). In this mode, two external resistors are required — one RSET connected to the BIASJ\_A pin (pin 44) and the other to the BIASJ\_B pin (pin 41). In this configuration, the user has the flexibility to set and adjust the full-scale output current for each DAC independently, allowing for the compensation of possible gain mismatches elsewhere within the transmit signal path.

Alternatively, bringing the GSET pin high (that is, connected to AVDD), the DAC5672 switches into the simultaneous gain set mode. Now the full-scale output current of both DAC channels is determined by only one external R<sub>SET</sub> resistor connected to the BIASJ\_A pin. The resistor at the BIASJ\_B pin may be removed; however, this is not required since this pin is not functional in this mode and the resistor has no effect on the gain equation.

### 7.4.6.4 Sleep Mode

The DAC5672 features a power-down function which can reduce the total supply current to approximately 3.1 mA over the specified supply range if no clock is present. Applying a logic high to the SLEEP pin initiates the power-down mode, while a logic low enables normal operation. When left unconnected, an internal active pulldown circuit enables the normal operation of the converter.

## 7.5 Programming

### 7.5.1 Digital Inputs and Timing

#### 7.5.1.1 Digital Inputs

The data input ports of the DAC5672 accept a standard positive coding with data bits DA13 and DB13 being the most significant bits (MSB). The converter outputs support a clock rate of up to 275 MSPS. The best performance is typically achieved with a symmetric duty cycle for write and clock; however, the duty cycle may vary as long as the timing specifications are met. Similarly, the setup and hold times may be chosen within their specified limits.

All digital inputs of the DAC5672 are CMOS compatible. [Figure 23](#) and [Figure 24](#) show schematics of the equivalent CMOS digital inputs of the DAC5672. The pullup and pulldown circuitry is approximately equivalent to 100 k $\Omega$ . The 14-bit digital data input follows the offset positive binary coding scheme. The DAC5672 is designed to operate with a digital supply (DVDD) of 3 V to 3.6 V.

Programming (continued)

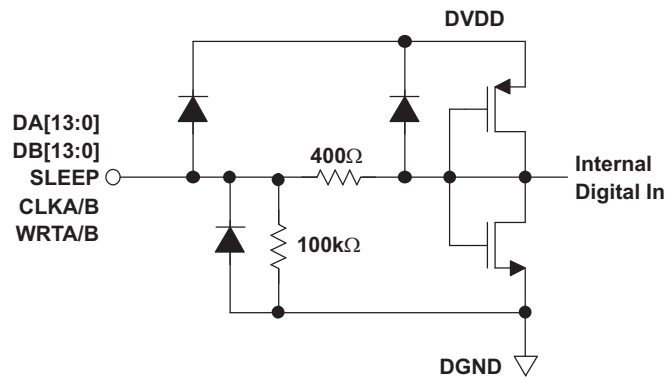


Figure 23. CMOS/TTL Digital Equivalent Input With Internal Pulldown Resistor

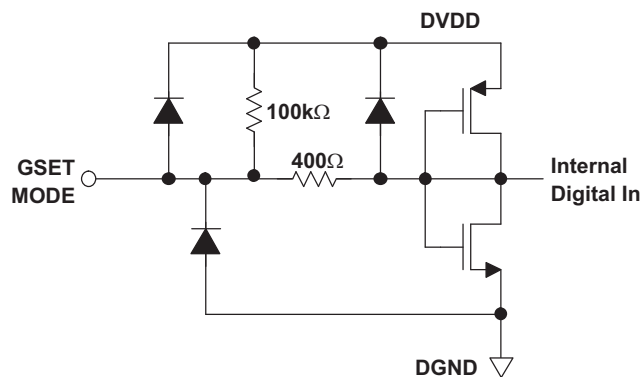


Figure 24. CMOS/TTL Digital Equivalent Input With Internal Pullup Resistor

## 8 Application and Implementation

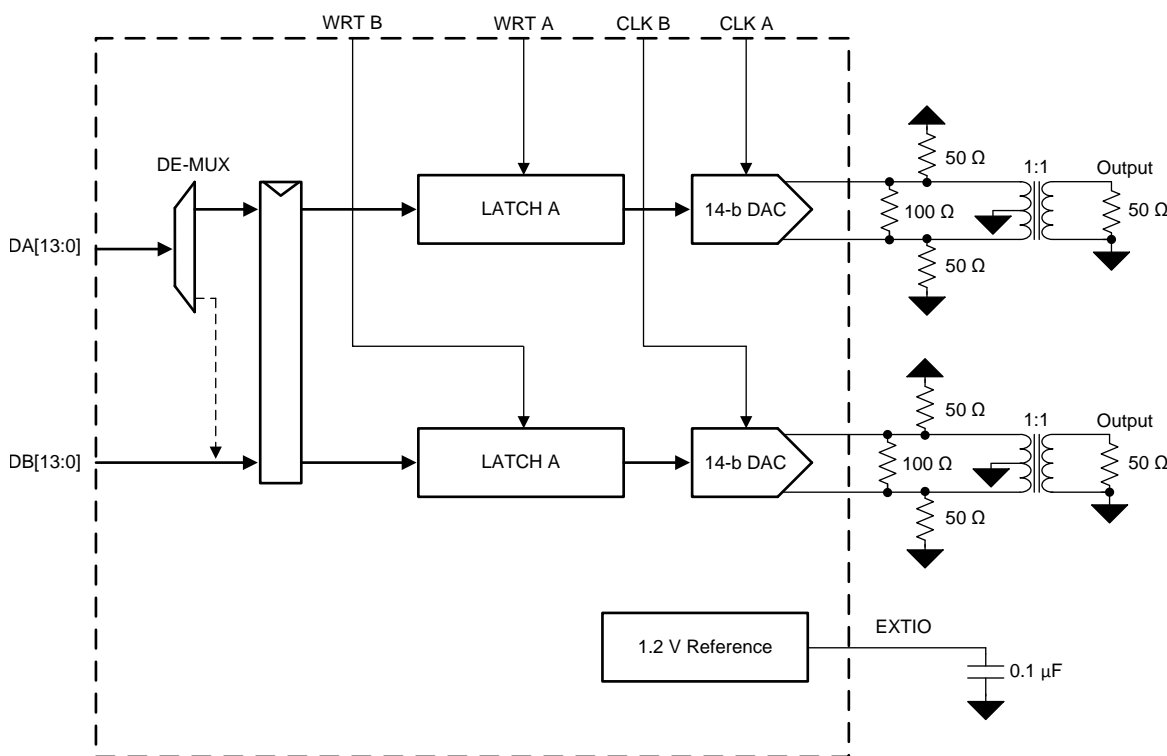
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

### 8.2 Typical Application

A typical application for the DAC5672 is as dual or single carrier transmitter. The DAC is provided with some input digital baseband signal and it outputs an analog carrier. A typical configuration is described below.



**Figure 25. Typical Application Schematic**

- Clock rate = 122.88 MHz
- Input data = WCDMA with IF frequency at 30.72 MHz
- AVDD= DVDD = 3.3 V

#### 8.2.1 Design Requirements

The requirements for this design were to generate a single WCDMA signal at an intermediate frequency of 30.72 MHz. The ACLR needs to be better than 72 dBc.

#### 8.2.2 Detailed Design Procedure

The single carrier signal with an intermediate frequency of 30.72 MHz must be created in the digital processor at a sample rate of 122.88 Msps for DAC. These 14 bit samples are placed on the 14b CMOS input port of the DAC.

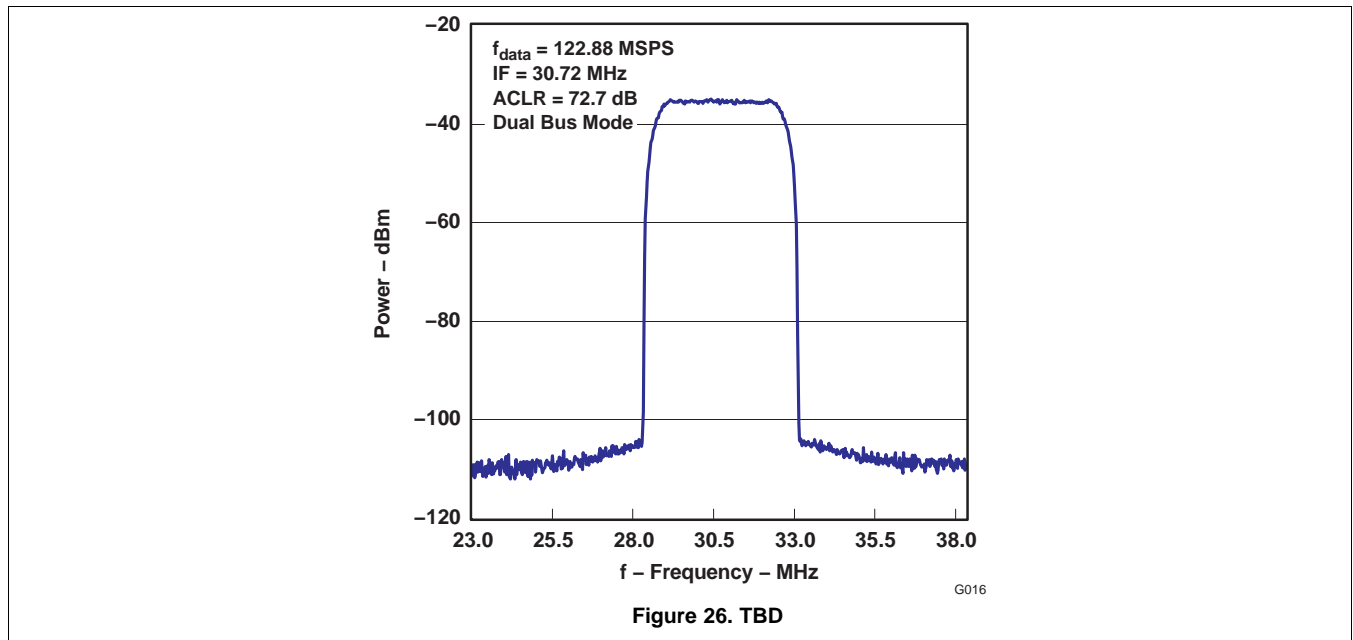
**Typical Application (continued)**

A CMOS DAC clock must be generated from a clock source at 122.88 MHz. This must be provided to the CLK pin of the DAC.

The IOUTA and IOUTB differential connections must be connected to a transformer to provide a single ended output. A typical 1:1 impedance transformer is used on the device EVM. The DAC5672EVM provides a good reference for this design example.

**8.2.3 Application Curves**

This spectrum analyzer plot shows the ACLR for the transformer output single carrier signal with intermediate frequency of 30.72 MHz. The results meet the system requirements for a minimum of 72 dBc ACLR.



## 9 Power Supply Recommendations

It is recommended that the device be powered with the nominal supply voltages as indicated in the [Recommended Operating Conditions](#).

In most instances the best performance is achieved with LDO supplies. However the supplies may be driven with direct outputs from a DC-DC switcher as long as the noise performance of the switcher is acceptable.



## 10 Layout

### 10.1 Layout Guidelines

The DAC5672 EVM layout should be used as a reference for the layout to obtain the best performance. A sample layout is shown in Figure 27 through Figure 30. Some important layout recommendations are:

1. Use a single ground plane. Keep the digital and analog signals on distinct separate sections of the board. This may be virtually divided down the middle of the device package when doing placement and layout.
2. Keep the analog outputs as far away from the switching clocks and digital signals as possible. This will keep coupling from the digital circuits to the analog outputs to a minimum.
3. Decoupling caps should be kept close to the power pins of the device.

### 10.2 Layout Example

The EVM is constructed on a 4-layer, 5.1-inch x 4.8-inch, 0.062-inch thick PCB using FR-4 material. Figure 27 through Figure 30 show the PCB layout for the EVM.

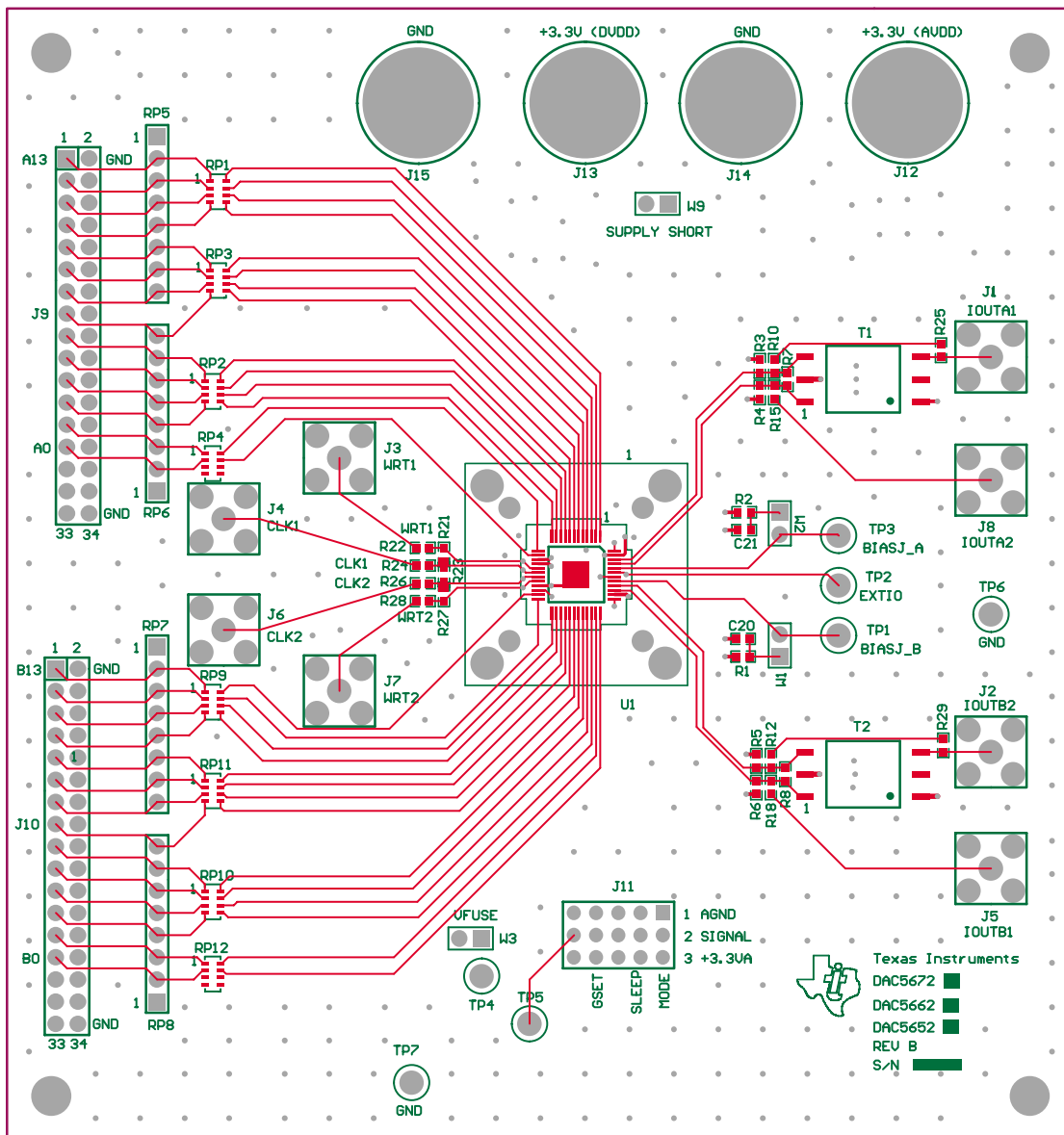
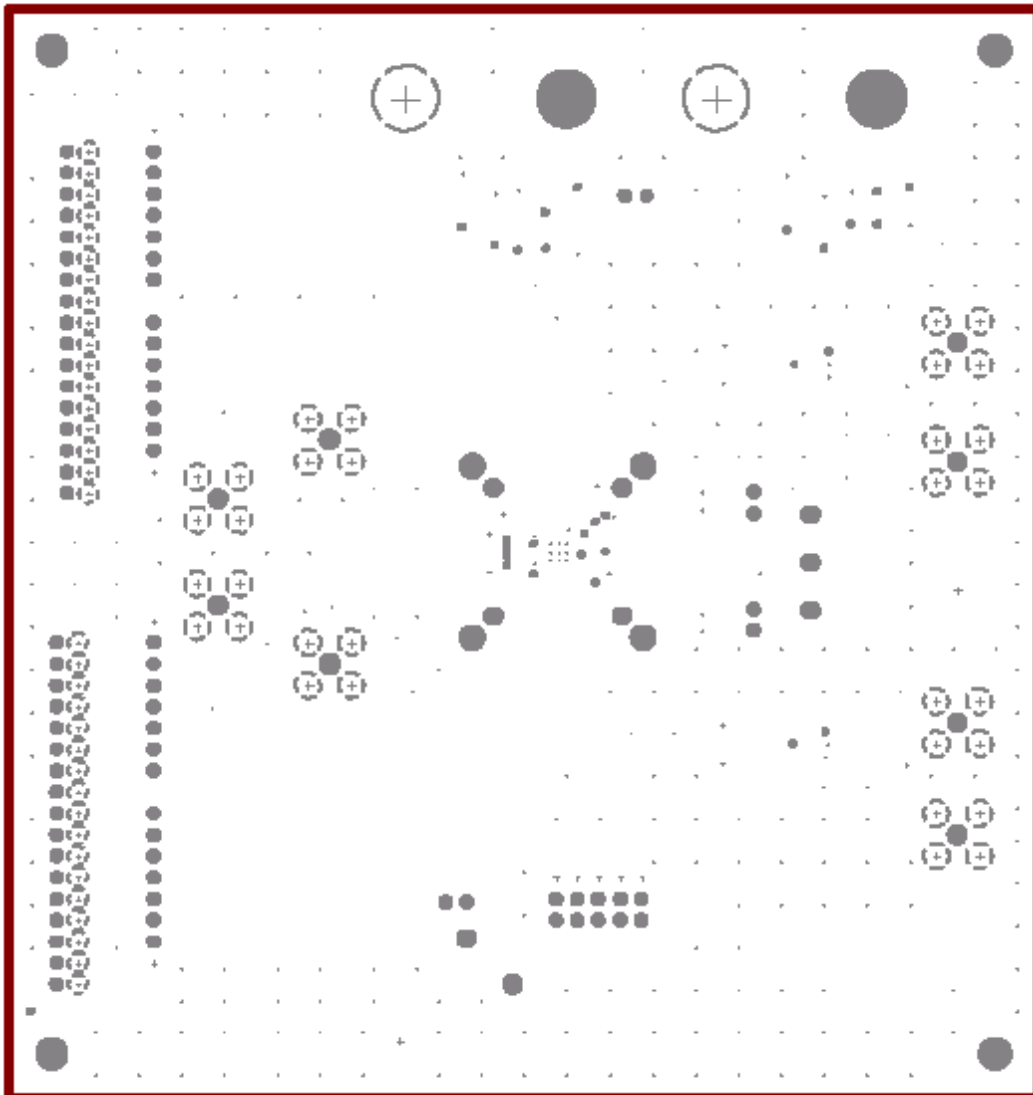


Figure 27. Top Layer 1

**Layout Example (continued)**



**Figure 28. Ground Plane Layer 2**

Layout Example (continued)

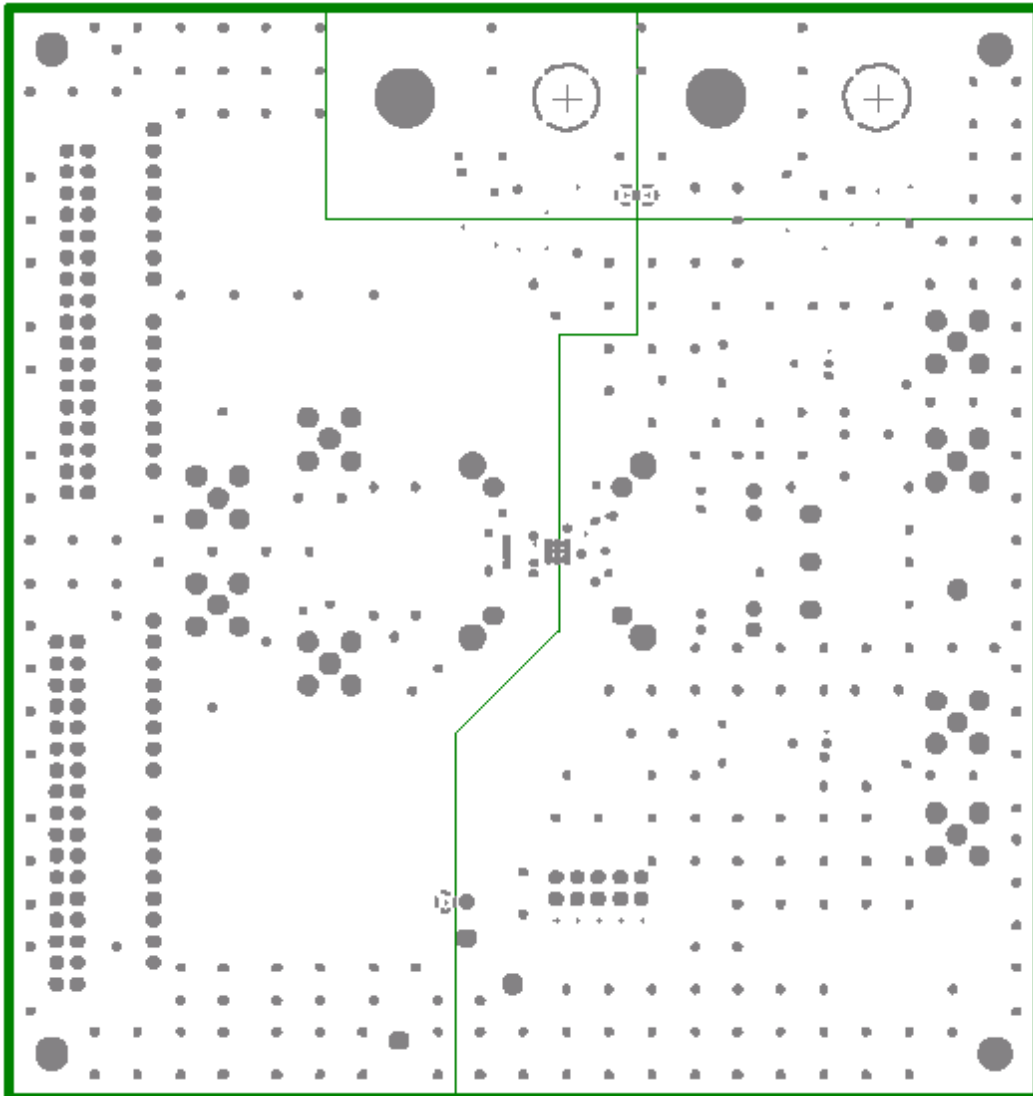
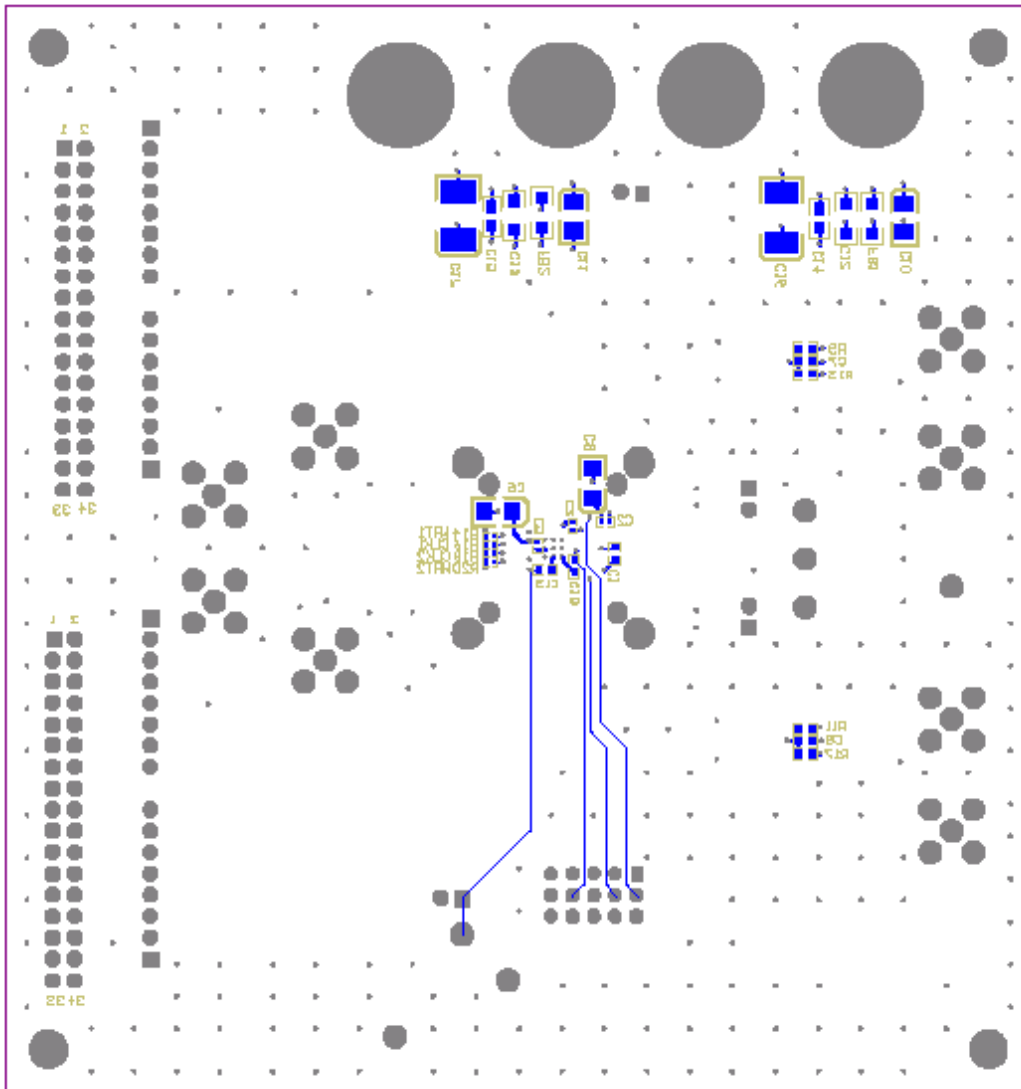


Figure 29. Power Plane Layer 3

**Layout Example (continued)**



**Figure 30. Bottom Layer 4**

## 11 Device and Documentation Support

### 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 Trademarks

E2E is a trademark of Texas Instruments.

### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">DAC5672IPFB</a>	Active	Production	TQFP (PFB)   48	250   JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5672I
DAC5672IPFB.A	Active	Production	TQFP (PFB)   48	250   JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5672I
DAC5672IPFBG4	Active	Production	TQFP (PFB)   48	250   JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5672I
DAC5672IPFBG4.A	Active	Production	TQFP (PFB)   48	250   JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5672I
<a href="#">DAC5672IPFBR</a>	Active	Production	TQFP (PFB)   48	1000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5672I
DAC5672IPFBR.A	Active	Production	TQFP (PFB)   48	1000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC5672I

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF DAC5672 :**

- Enhanced Product : [DAC5672-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

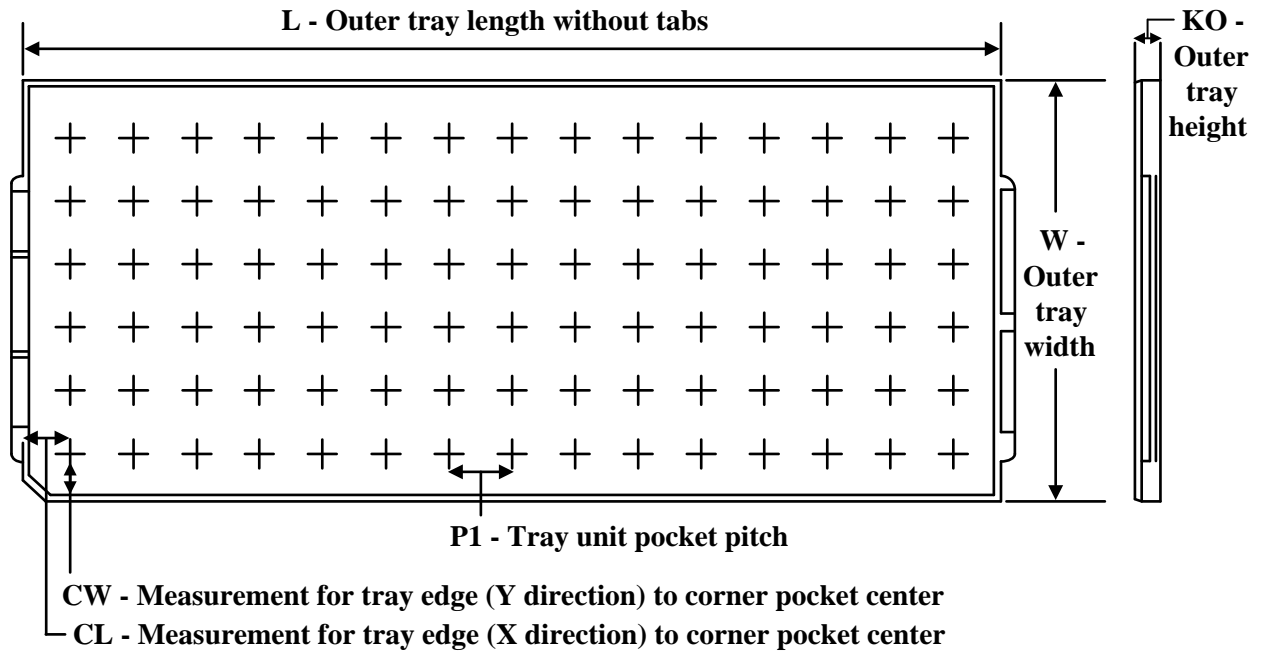
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5672IPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5672IPFBR	TQFP	PFB	48	1000	367.0	367.0	38.0

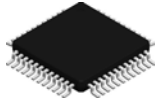
**TRAY**


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DAC5672IPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25
DAC5672IPFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25
DAC5672IPFBG4	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25
DAC5672IPFBG4.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.5	11.25

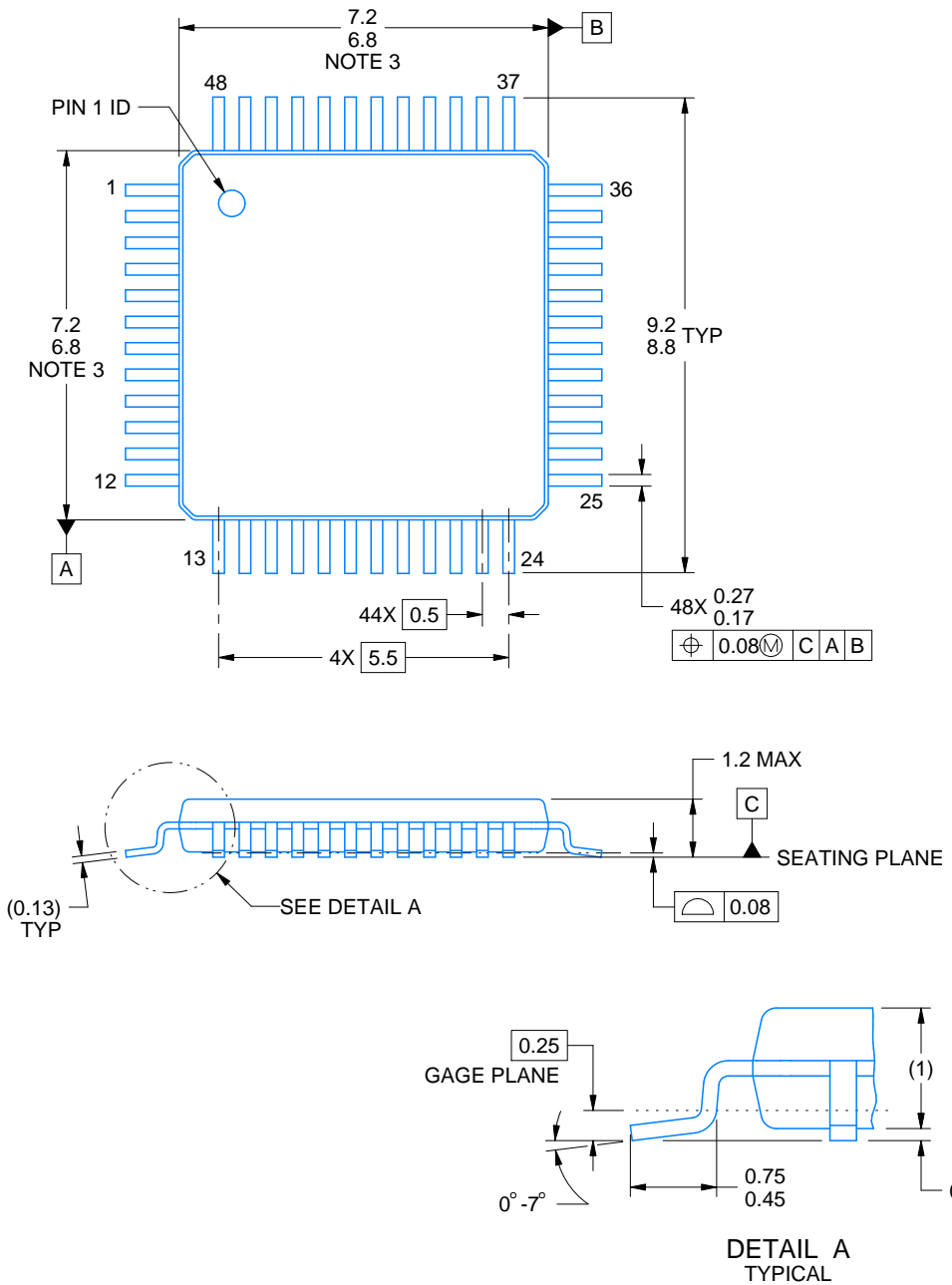
PFB0048A



PACKAGE OUTLINE

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



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NOTES:

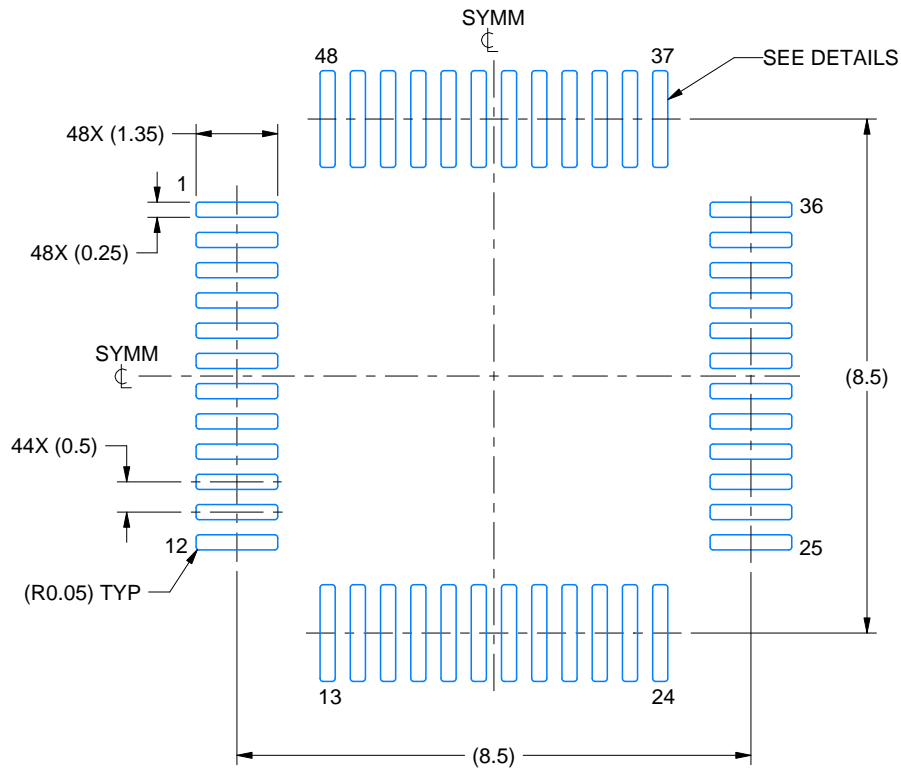
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

# EXAMPLE BOARD LAYOUT

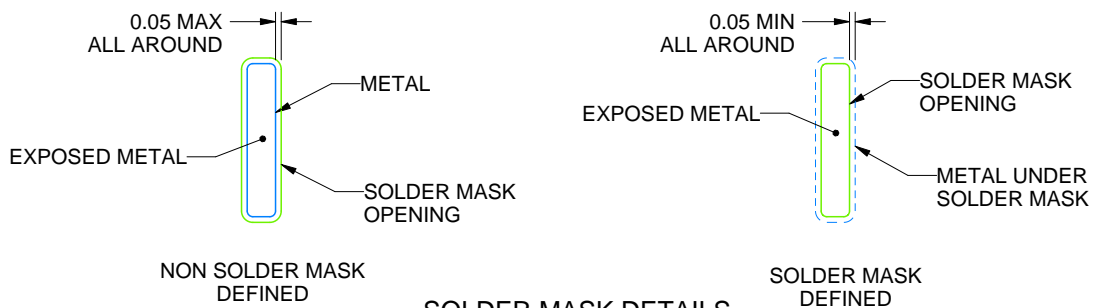
PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

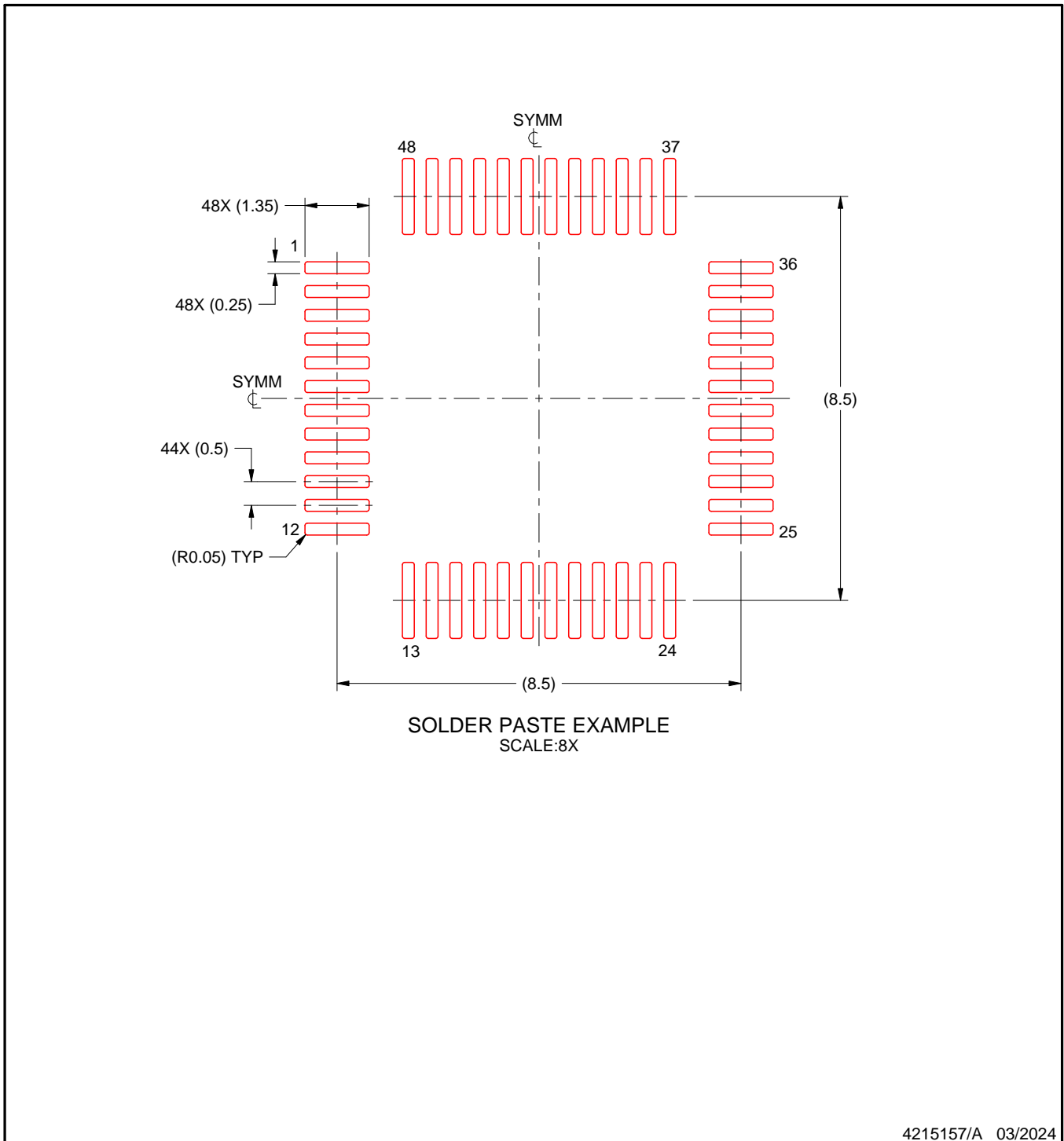
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025