



DAC7614

Quad, Serial Input, 12-Bit, Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW POWER: 20mW
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 10µs to 0.012%
- 12-BIT LINEARITY AND MONOTONICITY: -40°C to +85°C
- USER SELECTABLE RESET TO MID-SCALE OR ZERO-SCALE
- SECOND-SOURCE for DAC8420
- SMALL 20-LEAD SSOP PACKAGE

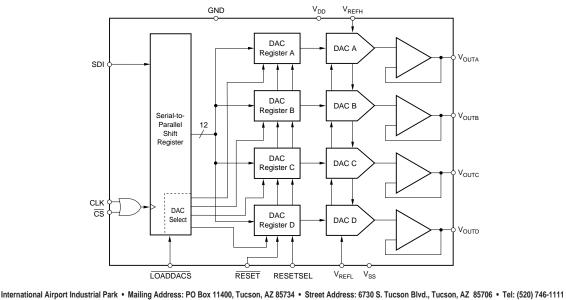
DESCRIPTION

The DAC7614 is a quad, serial input, 12-bit, voltage output digital-to-analog converter (DAC) with guaranteed 12-bit monotonic performance over the -40° C to $+85^{\circ}$ C temperature range. An asynchronous reset clears all registers to either mid-scale ($800_{\rm H}$) or zeroscale ($000_{\rm H}$), selectable via the RESETSEL pin. The device can be powered from a single +5V supply or from dual +5V and -5V supplies.

APPLICATIONS

- ATE PIN ELECTRONICS
- PROCESS CONTROL
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS

Low power and small size makes the DAC7614 ideal for process control, data acquisition systems, and closed-loop servo-control. The device is available in 16-pin plastic DIP, 16-lead SOIC, or 20-lead SSOP packages, and is guaranteed over the -40°C to +85°C temperature range.



SPECIFICATIONS

At T_A = -40°C to +85°C, V_{DD} = +5V, V_{SS} = -5V, V_{REFH} = +2.5V, and V_{REFL} = -2.5V, unless otherwise noted.

	DAC7614E, P, U			7614EB, P	B, UB	
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$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		±2			±1	LSB ⁽²⁾
Differential Linearity Error Monotonicity $V_{SS} = 0V \text{ or } -5V$ 12Zero-Scale Error Zero-Scale DriftCode = 000_H 12Zero-Scale Matching ⁽³⁾ Full-Scale ErrorCode = $00A_H, V_{SS} = 0V$ $V_{SS} = 0V$ 2Zero-Scale Matching ⁽³⁾ Code = $00A_H, V_{SS} = 0V$ $V_{SS} = 0V$ 2Zero-Scale ErrorCode = $00A_H, V_{SS} = 0V$ $V_{SS} = 0V$ 2Zero-Scale Matching ⁽³⁾ Vss = 0V $V_{SS} = 0V$ 2Power Supply RejectionCode = FFF _H , V_{SS} = 0V $V_{SS} = 0V$ 2ANALOG OUTPUT Voltage Output ⁽⁴⁾ V_{SS} = 0V or -5V $V_{SS} = 0V$ V_{REFL} -1.25 No Clauge Capacitance Short-Circuit DurationNo Oscillation-1.25REFERENCE INPUT VREFL Input RangeV_{SS} = 0V or -5V $V_{SS} = 0V$ 0 0 $V_{SS} = 0V or -5V00VREFL Input RangeV_{SS} = 0V or -5VV_{SS} = 0V00V_{SS} = 0V or -2.50DYNAMIC PERFORMANCESetting Time(6)To \pm 0.012\%Full-Scale StepOn Any Other DAC, R_L = 2k\OmegaBandwidth: 0Hz to 1MHzTTL-40I_{H_L} \le 10\muA-0.32.4DIGITAL INPUT/OUTPUTLogic LevelsV_{H} I_{H_H} \le 10\muA2.4-0.3-0.32.5POWER SUPPLY REQUIREMENTSV_{DD}If V_{SS} \neq 0V-5.25-5.25IsIf V_{SS} \neq 0V-5.25$		±2			±1	LSB
Monotonicity Zero-Scale Error12Zero-Scale Drift Zero-Scale DriftCode = 000_{H} 12Zero-Scale Drift Zero-Scale Matching ⁽³⁾ Code = FFF_{H} 12Full-Scale Error Full-Scale ErrorCode = $00A_{H}$, $V_{SS} = 0V$ $V_{SS} = 0V$ 2ero-Scale DriftZero-Scale Drift Zero-Scale Matching ⁽³⁾ Code = FFF_{H} , $V_{SS} = 0V$ $V_{SS} = 0V$ 2ero-Scale Matching ⁽³⁾ Power Supply RejectionVoltage Output ⁽⁴⁾ $V_{SS} = 0V$ or $-5V$ $V_{SS} = 0V$ V_{REFL} -1.25 ANALOG OUTPUT Voltage Output ⁽⁴⁾ Voltage = 0V or $-5V$ V_{REFL} V_{REFL} -1.25 V_{REFL} -1.25 Code a pacitiance Short-Circuit DurationNo Oscillation V_{REFL} -1.25 V_{REFL} -1.25 REFERNCE INPUT V_{REFL} Input Range $V_{SS} = 0V$ or $-5V$ V_{REFL} Input Range $V_{SS} = 0V$ or -2.5 0 V_{REFL} -2.5 DYNAMIC PERFORMANCE Setting Time ⁽⁵⁾ Channel-to-Channel CrosstalkTo $\pm 0.012\%$ Full-Scale Step On Any Other DAC, $R_L = 2k\Omega$ Bandwidth: OHz to 1MHz $TTL-4$ -0.3 Data Format $TTL-4$ -0.3 S DIGITAL INPUT/OUTPUT Logic Levels V_{H} V_{H} V_{IL} $ I_{IL} \le 10\muA$ -0.3 Data Format 2.4 -5.25 POWER SUPPLY REQUIREMENTS V_{DD} V_{SS} $If V_{SS} \neq 0V$ -5.25 -5.21		±1			±1	LSB
Zero-Scale ErrorCode = 000_H Zero-Scale DriftZero-Scale Matching ⁽³⁾ Full-Scale ErrorCode = $00A_H, V_{SS} = 0V$ Zero-Scale Matching ⁽³⁾ V_{SS} = 0VZero-Scale DriftV_{SS} = 0VZero-Scale Matching ⁽³⁾ V_{SS} = 0VVal-Scale ErrorCode = FFF _H , V_{SS} = 0VFull-Scale Matching ⁽³⁾ V_{SS} = 0V or -5VPower Supply RejectionV_{SS} = 0V or -5VANALOG OUTPUTV_{SS} = 0V or -5VVoluput CurrentNo OscillationShort-Circuit CurrentNo OscillationShort-Circuit DurationV_{SS} = 0V or -5VV_REFL Input RangeV_{SS} = 0V or -5VV_REFL Input RangeV_{SS} = 0V or -2.5DYNAMIC PERFORMANCETo ±0.012%Setting Time ⁽⁶⁾ To ±0.012%Channel-to-Channel CrosstalkTo ±0.012%PUITAL INPUT/OUTPUTInput Anny Other DAC, $R_L = 2k\Omega$ Logic LevelsV _H V _H I _H $\leq 10\muA$ 2.4V _{IL} V _H I _L $\leq 10\muA$ 2.4V _{SS} $\neq 0V$ V _{RE} SPOWER SUPPLY REQUIREMENTSIf $V_{SS} \neq 0V$ V _{DD} V _{SS} V _{DD} If $V_{SS} \neq 0V$ V _{SS} -2.2			*			Bits
Zero-Scale Drift Zero-Scale Matching ⁽³⁾ Full-Scale ErrorCode = FFF _H Code = FFF _H Full-Scale Matching ⁽³⁾ Zero-Scale DriftCode = 00A _H , V _{SS} = 0V V _{SS} = 0V Zero-Scale Matching ⁽³⁾ Zero-Scale Matching ⁽³⁾ Zero-Scale Matching ⁽³⁾ Code = 00A _H , V _{SS} = 0V V _{SS} = 0VFull-Scale Error Full-Scale Matching ⁽³⁾ Code = FFF _H , V _{SS} = 0V V _{SS} = 0VFull-Scale Matching ⁽³⁾ Power Supply RejectionV _{SS} = 0V or -5V V _{SS} = 0V or -5VANALOG OUTPUT Voltage Output ⁽⁴⁾ Short-Circuit Durrent Short-Circuit DurationV _{SS} = 0V or -5V V _{SS} = 0V or -5V V _{SS} = 0V or -5VREFERENCE INPUT V _{REFL} Input Range V _{REFL} Input Range V _{SS} = 0V or -5V V _{REFL} Input Range V _{SS} = 0V or -2.5V V _{REFL} 1.25 O 0 V _{SS} = 0V or -5V V _{SS} = 0V or -2.5DYNAMIC PERFORMANCE Setting Time ⁽⁶⁾ Channel-to-Channel Crosstalk V _H Logic Levels V _H Logic Levels V _H Logic Levels V _H N _L N _H N _L = 10µA Logic Levels V _H N _L S S S N _{DD} V _{SS} S S N _{DD} N _{SS} TTL-4 10µA Logic A, 2, 4 Logic Levels V _H I I _L < 10µA Logic Levels V _{DD} V _{SS} S N _{DD} N _{SS} TTL-4 LOGIC LEVENCE S LINC LINCENCE S LINCENCE S Company LINCENCE S Company LINCENCE S Company LINCENCE Company LINCENCE Company LINCENCE Company LINCENCE Company LINCENCE Company LINCENCE Company LINCENCE Company LINCENCE Company LINCENCE Company LINCENCE Company LINCENCE Company LINCENCE Company LINCENCE Company LINCENCE Company LINCENCE Company LINCENCE C		±4			*	LSB
Full-Scale ErrorCode = FFF _H Full-Scale Matching(3)Code = 00A _H , V _{SS} = 0VZero-Scale Drift $V_{SS} = 0V$ Zero-Scale Matching(3) $V_{SS} = 0V$ Pull-Scale Matching(3) $V_{SS} = 0V$ Power Supply Rejection $V_{SS} = 0V$ ANALOG OUTPUT $V_{SS} = 0V$ or $-5V$ Voltage Output(4) $V_{SS} = 0V$ or $-5V$ Output CurrentNo OscillationShort-Circuit DurationNo OscillationREFERENCE INPUT $V_{SS} = 0V$ or $-5V$ V _{REFL} Input Range $V_{SS} = 0V$ or $-5V$ VREFL Input Range $V_{SS} = -5V$ Otyput Neise VoltageTo $\pm 0.012\%$ Channel-to-Channel CrosstalkFull-Scale StepOn Any Other DAC, $R_L = 2k\Omega$ Bandwidth: 0Hz to 1MHzDIGITAL INPUT/OUTPUTInput A 2.4Logic Levels V_{H} V_{IH} $ I_{H_H} \leq 10\muA$ 2.4 V_{IL} V_{DD} If $V_{SS} \neq 0V$ V_{SS} If $V_{SS} \neq 0V$ V_{SS} -2.5	2	5		*	*	ppm/°C
Full-Scale ErrorCode = FFF _H Full-Scale Matching(3)Code = 00A _H , V _{SS} = 0VZero-Scale Drift $V_{SS} = 0V$ Zero-Scale Matching(3) $V_{SS} = 0V$ Pull-Scale Matching(3) $V_{SS} = 0V$ Power Supply Rejection $V_{SS} = 0V$ ANALOG OUTPUT $V_{SS} = 0V$ or $-5V$ Voltage Output(4) $V_{SS} = 0V$ or $-5V$ Output CurrentNo OscillationShort-Circuit DurationNo OscillationREFERENCE INPUT $V_{SS} = 0V$ or $-5V$ V _{REFL} Input Range $V_{SS} = 0V$ or $-5V$ VREFL Input Range $V_{SS} = -5V$ Otyput Neise VoltageTo $\pm 0.012\%$ Channel-to-Channel CrosstalkFull-Scale StepOn Any Other DAC, $R_L = 2k\Omega$ Bandwidth: 0Hz to 1MHzDIGITAL INPUT/OUTPUTInput A 2.4Logic Levels V_{H} V_{IH} $ I_{H_H} \leq 10\muA$ 2.4 V_{IL} V_{DD} If $V_{SS} \neq 0V$ V_{SS} If $V_{SS} \neq 0V$ V_{SS} -2.5		±2			±1	LSB
Full-Scale Matching(3) Zero-Scale ErrorCode = $00A_{H}$, $V_{SS} = 0V$ $V_{SS} = 0V$ $V_{SS} = 0V$ Zero-Scale Drift $V_{SS} = 0V$ $V_{SS} = 0V$ Zero-Scale Matching(3) $V_{SS} = 0V$ Full-Scale Matching(3) $V_{SS} = 0V$ Power Supply Rejection $V_{SS} = 0V$ ANALOG OUTPUT Voltage Output(4) $V_{SS} = 0V$ or $-5V$ Voltage Output(4) $V_{SS} = 0V$ or $-5V$ Output Current Short-Circuit CurrentNo OscillationShort-Circuit Duration $V_{SS} = 0V$ or $-5V$ VREFL Input Range $V_{SS} = 0V$ or $-5V$ VREFL Input Range $V_{SS} = 0V$ or $-5V$ VREFL Input Range $V_{SS} = 0V$ or $-5V$ Output Noise VoltageTo $\pm 0.012\%$ Bandwidth: 0Hz to 1MHzDIGITAL INPUT/OUTPUT Logic FamilyI $I_{HH} \le 10\muA$ Logic Family $ I_{H} \le 10\muA$ Logic Levels V_{IL} V_{IL} I $I_{VSS} \neq 0V$ V_{SS} If $V_{SS} \neq 0V$ V_{SS} If $V_{SS} \neq 0V$ V_{DD} I_{TZ} V_{DD} I_{TZ} V_{DD} I_{TZ}		±4			*	LSB
Zero-Scale ErrorCode $= 00A_{H}, V_{SS} = 0V$ $V_{SS} = 0V$ $V_{SS} = 0V$ Zero-Scale Drift $V_{SS} = 0V$ $V_{SS} = 0V$ Zero-Scale Matching(3)Code $= FFF_{H}, V_{SS} = 0V$ $V_{SS} = 0V$ Full-Scale ErrorCode $= FFF_{H}, V_{SS} = 0V$ $V_{SS} = 0V$ Power Supply Rejection $V_{SS} = 0V$ or $-5V$ V_{REFL} ANALOG OUTPUT Voltage Output (4) $V_{SS} = 0V$ or $-5V$ V_{REFL} Voltage Output Current Short-Circuit DurationNo OscillationShort-Circuit Duration $V_{SS} = 0V$ or $-5V$ $V_{SS} = 0V$ REFERENCE INPUT V_{REFL Input Range $V_{SS} = 0V$ or $-5V$ $V_{SS} = 0V$ $V_{SS} = 0V$ VREFL Input Range $V_{SS} = 0V$ or $-5V$ $V_{SS} = 0V$ Output Nange $V_{SS} = 0V$ or $-5V$ $V_{SS} = 0V$ DYNAMIC PERFORMANCE Setting Time(5)To $\pm 0.012\%$ $Channel-to-Channel CrosstalkDIGITAL INPUT/OUTPUTLogic FamilyBandwidth: 0Hz to 1MHzDIGITAL INPUT/OUTPUTLogic FamilyI III \leq 10\muALogic LevelsV_{IL}V_{IL}VIH I_{H1} \leq 10\muA2.4V_{IL}= 0.33Data FormatSPOWER SUPPLY REQUIREMENTSV_{DD}If V_{SS} \neq 0VVasI_{SS}If V_{SS} \neq 0VVasI_{SS}= 0.21$		±2			±1	LSB
Zero-Scale Drift $V_{SS} = 0V$ $V_{SS} = 0V$ Full-Scale Error $V_{SS} = 0V$ $V_{SS} = 0V$ Full-Scale Matching(3)Code = FFF _H , $V_{SS} = 0V$ $V_{SS} = 0V$ V_{REFL} -1.25 Power Supply Rejection $V_{SS} = 0V$ or $-5V$ V_{REFL} V_{REFL} -1.25 ANALOG OUTPUT Voltage Output Current Short-Circuit Current Short-Circuit Duration $V_{SS} = 0V$ or $-5V$ $V_{SS} = 0V$ or $-5V$ $V_{SS} = 0V$ or $-5V$ $V_{SS} = 0V$ or $-5V$ $V_{SS} = 0V$ or $-5V$ V_{REFL} Input Range $V_{SS} = 0V$ or $-5V$ $V_{SS} = 0V$ or -2.5 DYNAMIC PERFORMANCE Settling Time(5) Channel-to-Channel CrosstalkTo $\pm 0.012\%$ Full-Scale Step On Any Other DAC, $R_L = 2k\Omega$ Bandwidth: 0Hz to 1MHzDIGITAL INPUT/OUTPUT Logic Family U_{IL} $ I_{IH} \le 10\muA$ $ I_{L} \le 10\muA$ Digita Linput Requirements V_{IL} $ I_{H} \le 10\muA$ $ I_{L} \le 10\muA$ POWER SUPPLY REQUIREMENTS V_{DD} V_{SS} If $V_{SS} \ne 0V$ -5.25 V_{DD} V_{SS} $ I_{FV}_{SS} \ne 0V$ -5.25		±8			*	LSB
Zero-Scale Matching(3) $V_{SS} = 0V$ Code = FFF _H , $V_{SS} = 0V$ V $_{SS} = 0V$ Full-Scale ErrorCode = FFF _H , $V_{SS} = 0V$ $V_{SS} = 0V$ Power Supply Rejection $V_{SS} = 0V$ or $-5V$ ANALOG OUTPUT Voltage Output(4) $V_{SS} = 0V$ or $-5V$ Uptut CurrentOutput Current Short-Circuit DurationNo OscillationREFERENCE INPUT V_{REFL $V_{SS} = 0V$ or $-5V$ $V_{SS} = 0V$ $V_{REFL} + 1.25$ 0 -2.5 DYNAMIC PERFORMANCE Settling Time(5)To $\pm 0.012\%$ Full-Scale Step On Any Other DAC, $R_L = 2k\Omega$ Bandwidth: 0Hz to 1MHzDIGITAL INPUT/OUTPUT Logic Levels V_{IL} $ I_{IH} \le 10\muA$ -0.3 Data FormatPOWER SUPPLY REQUIREMENTS V_{DD} If $V_{SS} \neq 0V$ V_{DD} 4.75 -5.25	5	10		*	*	ppm/°C
Full-Scale ErrorCode = FFF_H, V_{SS} = 0VFull-Scale Matching(3) $V_{SS} = 0V$ Power Supply Rejection $V_{SS} = 0V$ ANALOG OUTPUT $V_{SS} = 0V \text{ or } -5V$ V_{REFL} Voltage Output(4) $V_{SS} = 0V \text{ or } -5V$ V_{REFL} Output CurrentNo Oscillation -1.25 Load CapacitanceNo Oscillation V_{REFL} Short-Circuit Duration $V_{SS} = 0V \text{ or } -5V$ V_{REFL} VREFH Input Range $V_{SS} = 0V \text{ or } -5V$ V_{REFL} V_REFL Input Range $V_{SS} = 0V \text{ or } -5V$ 0 V_{REFL} Input Range $V_{SS} = -5V$ -2.5 DYNAMIC PERFORMANCETo $\pm 0.012\%$ 0 Settling Time ⁽⁵⁾ To $\pm 0.012\%$ -2.5 Output Noise VoltageBandwidth: 0Hz to 1MHz $TTL-4$ DIGITAL INPUT/OUTPUTBandwidth: 0Hz to 1MHz -0.3 Logic Levels V_{H} $ I_{H} \le 10\muA$ -0.3 V_{IL} V_{IL} $ I_{UL} \le 10\muA$ -0.3 Data FormatS S -5.25 V_{DD} $I_{SS} \ne 0V$ -5.25	-	±4			±2	LSB
Full-Scale Matching(3) Power Supply Rejection $V_{SS} = 0V$ ANALOG OUTPUT Voltage Output(4) Output Current Load Capacitance Short-Circuit Duration $V_{SS} = 0V \text{ or } -5V$ V_{REFL} -1.25REFERENCE INPUT VREFH Input Range VREFL Input Range $V_{SS} = 0V \text{ or } -5V$ $V_{REFL} + 1.25$ 0VREFL Input Range VREFL Input Range $V_{SS} = 0V \text{ or } -5V$ $V_{REFL} + 1.25$ 0DYNAMIC PERFORMANCE Settling Time(5)To $\pm 0.012\%$ Full-Scale Step On Any Other DAC, $R_L = 2k\Omega$ Daniel-to-Channel CrosstalkTo $\pm 0.012\%$ Full-Scale StepDIGITAL INPUT/OUTPUT Logic LevelsI I _{IH} $\leq 10\muA$ 2.4 -0.3VIH VIL I _{IL} $\leq 10\muA$ 2.4 -0.3POWER SUPPLY REQUIREMENTS VDD ISSIf $V_{SS} \neq 0V$ 4.75 -5.25VDD ISSIf $V_{SS} \neq 0V$ -2.5		±8			*	LSB
Power Supply RejectionVANALOG OUTPUT Voltage Outputt40 $V_{SS} = 0V \text{ or } -5V$ V_{REFL} -1.25Output Current Load CapacitanceNo Oscillation-1.25Short-Circuit Current Short-Circuit DurationNo Oscillation-1.25 REFERENCE INPUT V _{REFL} Input Range $V_{SS} = 0V \text{ or } -5V$ $V_{REFL} + 1.25$ 0 V_{REFL} Input Range $V_{SS} = 0V \text{ or } -5V$ $V_{REFL} + 1.25$ DYNAMIC PERFORMANCE Settling Time ⁽⁵⁾ To $\pm 0.012\%$ Full-Scale Step On Any Other DAC, $R_L = 2k\Omega$ Output Noise VoltageBandwidth: 0Hz to 1MHz DIGITAL INPUT/OUTPUT Logic LevelsInput Sign 2.04 VIHV _{IL} Input Sign 2.04 VIH $V_{IL} \leq 10\muA$ VD V _{SS} If $V_{SS} \neq 0V$ -0.3 S POWER SUPPLY REQUIREMENTS V _{DD} If $V_{SS} \neq 0V$ -5.25IbD IsSIf $V_{SS} \neq 0V$ -5.25		0 ±4			±2	LSB
ANALOG OUTPUT Voltage Output(4) $V_{SS} = 0V \text{ or } -5V$ V_{REFL} -1.25Output Current Load CapacitanceNo Oscillation-1.25Short-Circuit Current 	30	÷ '		*		ppm/V
Voltage Output(4) Output Current Load Capacitance $V_{SS} = 0V \text{ or } -5V$ V_{REFL} -1.25Load Capacitance Short-Circuit Current Short-Circuit DurationNo Oscillation-1.25 REFERENCE INPUT V_{REFL} Input Range V_{REFL} Input Range $V_{SS} = 0V \text{ or } -5V$ $V_{REFL} +1.25$ $V_{SS} = 0V$ 0 V_{REFL} Input Range $V_{SS} = -5V$ $V_{SS} = 0V$ 0 V_{REFL} Input Range $V_{SS} = -5V$ -2.5 0 DYNAMIC PERFORMANCE Settling Time(5) Channel-to-Channel CrosstalkTo $\pm 0.012\%$ Full-Scale Step On Any Other DAC, $R_L = 2k\Omega$ -10.012% Channel-to Channel CrosstalkDIGITAL INPUT/OUTPUT Logic Levels V_{IL} Bandwidth: 0Hz to 1MHz -10.3 CompanyDIGITAL INPUT/OUTPUT Logic Family Logic Levels -0.3 SSPOWER SUPPLY REQUIREMENTS V_{DD} V_{SS} If $V_{SS} \neq 0V$ -5.25 -5.25 V_{DD} V_{SS} If $V_{SS} \neq 0V$ -5.25 V_{DD} V_{SS} -2.1 -2.1						PP
Output Current Load CapacitanceInter- Inter- Inter- No OscillationInter- Inte		V	*		*	v
Load CapacitanceNo OscillationShort-Circuit CurrentNo OscillationREFERENCE INPUT $V_{SS} = 0V \text{ or } -5V$ V_{REFL} Input Range $V_{SS} = 0V \text{ or } 0$ V_{REFL} Input Range $V_{SS} = 0V$ V_{REFL} Input Range $V_{SS} = -5V$ V_{REFL} Input Range $V_{SS} = -5V$ DYNAMIC PERFORMANCETo $\pm 0.012\%$ Settling Time ⁽⁵⁾ To $\pm 0.012\%$ Channel-to-Channel CrosstalkFull-Scale StepOutput Noise VoltageBandwidth: 0Hz to 1MHzDIGITAL INPUT/OUTPUTInput AngleLogic Levels V_{IH} V_{IL} $ I_{H} \le 10\muA$ 2.4 -0.3 Data FormatSPOWER SUPPLY REQUIREMENTSIf $V_{SS} \ne 0V$ V_{DD} If $V_{SS} \ne 0V$ V_{SS} $If V_{SS} \ne 0V$ I_{SS} -2.1		V _{REFH} +1.25	*		*	
Short-Circuit Current Short-Circuit DurationV SS $V_{SS} = 0V$ or $-5V$ V 	100	+1.20	*	*	*	mA pF
Short-Circuit DurationREFERENCE INPUT $V_{SS} = 0V \text{ or } -5V$ $V_{REFL} + 1.25$ V_{REFL} Input Range $V_{SS} = 0V$ 0 V_{REFL} Input Range $V_{SS} = 0V$ 0 V_{REFL} Input Range $V_{SS} = -5V$ -2.5 DYNAMIC PERFORMANCE To $\pm 0.012\%$ -2.5Settling Time ⁽⁵⁾ To $\pm 0.012\%$ -2.5Channel-to-Channel CrosstalkFull-Scale Step-2.5Output Noise VoltageBandwidth: 0Hz to 1MHz-2.4DIGITAL INPUT/OUTPUTLogic FamilyTTL-0Logic Levels V_{IH} $ I_{H} \le 10\mu A$ -0.3Data FormatSSPOWER SUPPLY REQUIREMENTSIf $V_{SS} \ne 0V$ -5.25 V_{DD} If $V_{SS} \ne 0V$ -5.25 I_{DD} Is-2.1	+5, -15			*		-
REFERENCE INPUT V_{REFH} Input Range $V_{SS} = 0V$ or $-5V$ $V_{REFL}+1.25$ V_{REFL} Input Range $V_{SS} = 0V$ 0 V_{REFL} Input Range $V_{SS} = 0V$ 0 V_{REFL} Input Range $V_{SS} = 0V$ 0 V_{REFL} Input Range $V_{SS} = -5V$ -2.5 DYNAMIC PERFORMANCE To $\pm 0.012\%$ -2.5Settling Time ⁽⁵⁾ To $\pm 0.012\%$ Channel-to-Channel CrosstalkChannel-to-Channel CrosstalkFull-Scale StepOn Any Other DAC, $R_L = 2k\Omega$ Output Noise VoltageBandwidth: 0Hz to 1MHzTTL-0 DIGITAL INPUT/OUTPUT Logic LevelsTTL-0Logic Levels $ I_{H} \le 10\muA$ -0.3Data FormatSS POWER SUPPLY REQUIREMENTS If $V_{SS} \ne 0V$ -5.25 V_{DD} If $V_{SS} \ne 0V$ -5.25 I_{DD} I_{SS} If $V_{SS} \ne 0V$ -2.1				*		mA
$\begin{array}{cccc} V_{REFH} \mbox{ Input Range} & V_{SS} = 0V \mbox{ or } -5V & 0 \\ V_{REFL} \mbox{ Input Range} & V_{SS} = 0V & 0 \\ V_{REFL} \mbox{ Input Range} & V_{SS} = 0V & -2.5 \\ \hline \mathbf{DYNAMIC PERFORMANCE} & & & & & & \\ Settling Time^{(5)} & To \pm 0.012\% & & & & \\ Channel-to-Channel Crosstalk & Full-Scale Step & 0n Any Other DAC, R_L = 2K\Omega & & & \\ Output Noise Voltage & Bandwidth: 0Hz to 1MHz & & & \\ \hline \mathbf{DiGITAL INPUT/OUTPUT} & & & & & \\ Logic Levels & & & & & \\ V_{IH} & & I_{IH} \leq 10\mu A & 2.4 & \\ V_{IL} & & I_{IL} \leq 10\mu A & -0.3 & \\ \hline \mathbf{POWER SUPPLY REQUIREMENTS} & & & & & \\ V_{DD} & & & & & \\ V_{DD} & & & & \\ V_{DD} & & & & \\ V_{DD} & & & & \\ V_{SS} & & & & \\ If V_{SS} \neq 0V & -5.25 & \\ I_{DD} & & & \\ I_{SS} & & & & & \\ \end{array}$	Indefinite			*		
$\begin{array}{c c} V_{\text{REFL}} \mbox{ Input Range} & V_{\text{SS}} = 0V & 0 \\ V_{\text{REFL}} \mbox{ Input Range} & V_{\text{SS}} = -5V & -2.5 \\ \hline \mbox{DYNAMIC PERFORMANCE} \\ \mbox{Settling Time}^{(5)} & To \pm 0.012\% \\ \mbox{Channel-to-Channel Crosstalk} & Full-Scale Step \\ \mbox{Output Noise Voltage} & Bandwidth: 0Hz to 1MHz \\ \hline \mbox{DiGITAL INPUT/OUTPUT} \\ \mbox{Logic Levels} & & & \\ V_{1H} & I_{1H} \leq 10\mu\text{A} & 2.4 \\ V_{1L} & I_{1L} \leq 10\mu\text{A} & -0.3 \\ \hline \mbox{Data Format} & & & \\ \hline \mbox{POWER SUPPLY REQUIREMENTS} \\ V_{DD} & & & \\ V_{DD} & & & \\ V_{DD} & & & \\ If V_{SS} \neq 0V & -5.25 \\ I_{DD} & & \\ I_{SS} & & & & \\ \end{array}$						
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		+2.5	*		*	V
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		V _{REFH} -1.25	*		*	V
Settling Time (5)To $\pm 0.012\%$ Channel-to-Channel CrosstalkFull-Scale StepOutput Noise VoltageOn Any Other DAC, $R_L = 2k\Omega$ DIGITAL INPUT/OUTPUTBandwidth: 0Hz to 1MHzLogic FamilyTTL-0Logic LevelsTTL-0V _{IH} $ I_{H} \le 10\muA$ 2.4V _{IL} $ I_{IL} \le 10\muA$ -0.3Data FormatSPOWER SUPPLY REQUIREMENTSIf $V_{SS} \ne 0V$ -5.25 I_{DD} If $V_{SS} \ne 0V$ -5.25 I_{DD} -2.1		V _{REFH} -1.25	*		*	V
$\begin{array}{c c} \mbox{Channel Crosstalk} & \mbox{Full-Scale Step} \\ \mbox{On Any Other DAC, } R_L = 2k\Omega \\ \mbox{DidITAL INPUT/OUTPUT} \\ \mbox{Logic Family} & \mbox{TTL-0} \\ \mbox{Logic Levels} & \mbox{V}_{IH} & I_{IH} \leq 10\mu\text{A} & 2.4 \\ \mbox{V}_{IL} & \mbox{I} I_{IL} \leq 10\mu\text{A} & -0.3 \\ \mbox{Data Format} & \mbox{S} \\ \hline \end{tabular}$						
$\begin{array}{c c} & On Any Other DAC, R_L = 2k\Omega\\ Bandwidth: 0Hz to 1MHz \end{array} \\ \hline \begin{tabular}{lllllllllllllllllllllllllllllllllll$	5	10		*	*	μs
Output Noise VoltageBandwidth: 0Hz to 1MHzDIGITAL INPUT/OUTPUTTTL-0Logic FamilyTTL-0Logic Levels $ I_{IH} \le 10\muA$ V_{IH} $ I_{IL} \le 10\muA$ V_{IL} $ I_{IL} \le 10\muA$ Data FormatSPOWER SUPPLY REQUIREMENTS V_{DD} 4.75 V_{SS} If $V_{SS} \ne 0V$ I_{SS} -2.1	0.1			*		LSB
DigitAL INPUT/OUTPUTTTL-0Logic FamilyTTL-0Logic Levels $ I_{IH} \le 10\mu A$ 2.4 V_{IL} $ I_{L} \le 10\mu A$ -0.3Data FormatSPOWER SUPPLY REQUIREMENTSVDD4.75 V_{SS} If $V_{SS} \ne 0V$ -5.25 I_{DD} If $V_{SS} \ne 0V$ -2.1						
$ \begin{array}{c c c c c c c } Logic Family & & TTL-0 \\ Logic Levels & & & & & \\ V_{IH} & & & & & I_{IH} \leq 10 \mu A & & 2.4 \\ V_{IL} & & & & I_{IL} \leq 10 \mu A & & -0.3 \\ \hline Data Format & & & & & \\ \hline \textbf{POWER SUPPLY REQUIREMENTS} & & & & & \\ V_{DD} & & & & & & \\ V_{DD} & & & & & & \\ V_{SS} & & & & If \ V_{SS} \neq 0V & & -5.25 \\ I_{DD} & & & & & \\ I_{SS} & & & & & & & -2.1 \\ \end{array} $	40			*		nV/√Hz
$\begin{array}{c c c c c c c c } \mbox{Logic Levels} & & & & & & & & & & & & & & & & & & &$						
$ \begin{array}{c c} V_{IH} & & \ I_{IH} \leq 10 \mu A & 2.4 \\ V_{IL} & & \ I_{IL} \leq 10 \mu A & -0.3 \\ \hline \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$	Compatible	CMOS			*	
V_{IL} $ I_{IL} \le 10\mu A$ -0.3Data FormatSPOWER SUPPLY REQUIREMENTS4.75 V_{DD} 4.75 V_{SS} If $V_{SS} \ne 0V$ I_{SS} -2.1						
Data FormatSPOWER SUPPLY REQUIREMENTS4.75 V_{DD} 4.75 V_{SS} If $V_{SS} \neq 0V$ I_{DD} -5.25 I_{SS} -2.1		V _{DD} +0.3	*		*	V
POWER SUPPLY REQUIREMENTS4.75 V_{DD} 4.75 V_{SS} If $V_{SS} \neq 0V$ I_{DD} -5.25 I_{SS} -2.1		0.8	*		*	V
V_{DD} 4.75 V_{SS} If $V_{SS} \neq 0V$ -5.25 I_{DD} -2.1	traight Bina	ary		*		
V_{SS} If $V_{SS} \neq 0V$ -5.25 I_{DD} I_{SS} -2.1						
V_{SS} If $V_{SS} \neq 0V$ -5.25 I_{DD} I_{SS} -2.1		5.25	*		*	V
I _{DD} I _{SS} –2.1		-4.75	*		*	V
I _{SS} –2.1	1.5	1.9		*	*	mA
	-1.6		*	*		mA
VSS = 0V	15	20		*	*	mW
V _{SS} = 0V	7.5	10		*	*	mW
TEMPERATURE RANGE				1		
Specified Performance -40		+85	*		*	°C

* Specification same as grade to the left.

NOTES: (1) If $V_{SS} = 0V$, specification applies at code 00A_H and above. (2) LSB means Least Significant Bit, with V_{REFH} equal to +2.5V and V_{REFL} equal to -2.5V, one LSB is 1.22mV. (3) All DAC outputs will match within the specified error band. (4) Ideal output voltage, does not take into account zero or full-scale error. (5) If $V_{SS} = -5V$, full-scale step from code 000_H to FFF_H or vice-versa. If $V_{SS} = 0V$, full-scale positive step from code 000_H to FFF_H and negative step from code FFF_H to 00A_H.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

V_{DD} to V_{SS}	–0.3V to +11V
V _{DD} to GND	–0.3V to +5.5V
V _{REFL} to V _{SS}	–0.3V to (V _{DD} – V _{SS})
V _{DD} to V _{REFH}	0.3V to (V _{DD} - V _{SS})
V _{REFH} to V _{REFL}	–0.3V to (V _{DD} – V _{SS})
Digital Input Voltage to GND	–0.3V to V _{DD} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

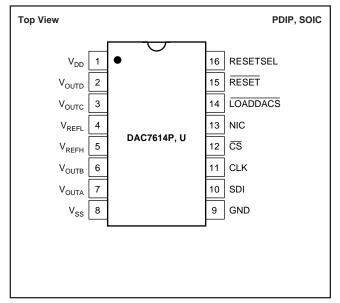
PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER ⁽²⁾	TRANSPORT MEDIA
DAC7614P	±2	±1	16-Pin DIP	180	–40°C to +85°C	DAC7614P	Rails
DAC7614PB	±1	"	"	"	"	DAC7614PB	Rails
DAC7614U	<u>+2</u>	±1	16-Lead SOIC	211	–40°C to +85°C	DAC7614U	Rails
"	"	"	"	"		DAC7614U/1K	Tape and Reel
DAC7614UB	±1 "	±1 "	16-Lead SOIC "	211	–40°C to +85°C "	DAC7614UB DAC7614UB/1K	Rails Tape and Reel
DAC7614E	<u>+2</u>	±1	20-Lead SSOP	334	–40°C to +85°C	DAC7614E	Rails
	"	"	"	"	"	DAC7614E/1K	Tape and Reel
DAC7614EB	±1	±1	20-Lead SSOP	334	−40°C to +85°C	DAC7614EB	Rails
"	"	"	"	"	"	DAC7614EB/1K	Tape and Reel

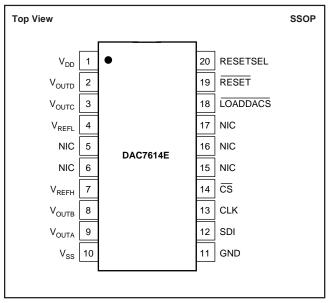
NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DAC7614EB/1K" will get a single 1000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.



PIN CONFIGURATION—P, U Packages



PIN CONFIGURATION—E Package



PIN DESCRIPTIONS—P, U Packages

PIN	LABEL	DESCRIPTION
1	V _{DD}	Positive Analog Supply Voltage, +5V nominal.
2	V _{OUTD}	DAC D Voltage Output
3	V _{OUTC}	DAC C Voltage Output
4	V _{REFL}	Reference Input Voltage Low. Sets minimum out- put voltage for all DACs.
5	V _{REFH}	Reference Input Voltage High. Sets maximum out- put voltage for all DACs.
6	V _{OUTB}	DAC B Voltage Output
7	V _{OUTA}	DAC A Voltage Output
8	V_{SS}	Negative Analog Supply Voltage, 0V or –5V nomi- nal.
9	GND	Ground
10	SDI	Serial Data Input
11	CLK	Serial Data Clock
12	CS	Chip Select Input
13	NIC	Not Internally Connected.
14	LOADDACS	The selected DAC register becomes transparent when LOADDACS is LOW. It is in the latched state when LOADDACS is HIGH.
15	RESET	Asynchronous Reset Input. Sets all DAC registers to either zero-scale (000_H) or mid-scale (800_H) when LOW. RESETSEL determines which code is active.
16	RESETSEL	When LOW, a LOW on $\overrightarrow{\text{RESET}}$ will cause all DAC registers to be set to code 000 _H . When RESETSEL is HIGH, a LOW on RESET will set the registers to code 800 _H .

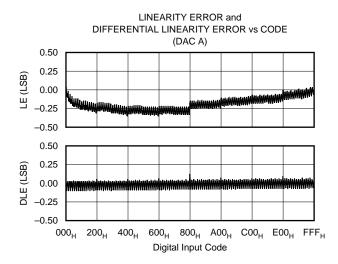
PIN DESCRIPTIONS—E Package

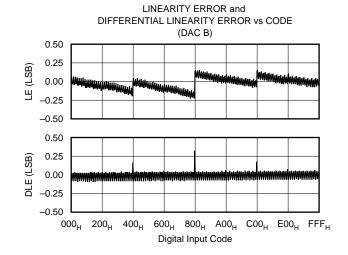
PIN	LABEL	DESCRIPTION
1	V _{DD}	Positive Analog Supply Voltage, +5V nominal.
2	V _{OUTD}	DAC D Voltage Output
3	V _{OUTC}	DAC C Voltage Output
4	V _{REFL}	Reference Input Voltage Low. Sets minimum out- put voltage for all DACs.
5	NIC	Not Internally Connected.
6	NIC	Not Internally Connected.
7	V _{REFH}	Reference Input Voltage High. Sets maximum out- put voltage for all DACs.
8	V _{OUTB}	DAC B Voltage Output.
9	V _{OUTA}	DAC A Voltage Output.
10	V_{SS}	Negative Analog Supply Voltage, 0V or –5V nomi- nal.
11	GND	Ground
12	SDI	Serial Data Input
13	CLK	Serial Data Clock
14	CS	Chip Select Input
15	NIC	Not Internally Connected.
16	NIC	Not Internally Connected.
17	NIC	Not Internally Connected.
18	LOADDACS	The selected DAC register becomes transparent when LOADDACS is LOW. It is in the latched state when LOADDACS is HIGH.
19	RESET	Asynchronous Reset Input. Sets all DAC registers to either zero-scale (000_H) or mid-scale (800_H) when LOW. RESETSEL determines which code is active.
20	RESETSEL	When LOW, a LOW on $\overline{\text{RESET}}$ will cause all DAC registers to be set to code 000_{H} . When RESETSEL is HIGH, a LOW on $\overline{\text{RESET}}$ will set the registers to code 800_{H} .

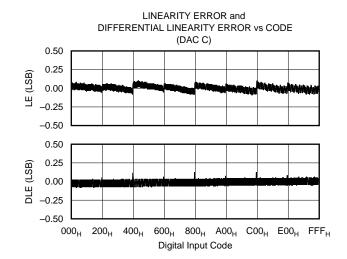
DAC7614

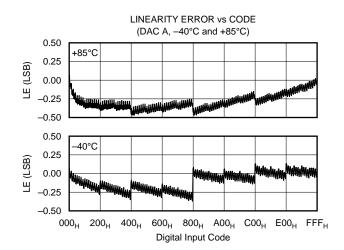
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$

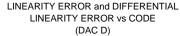
At $T_A = +25^{\circ}C$, $V_{DD} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +2.5V$, and $V_{REFL} = 0V$, representative unit, unless otherwise specified.

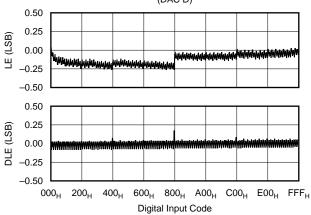


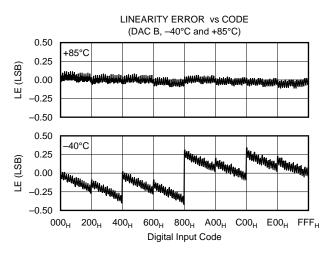








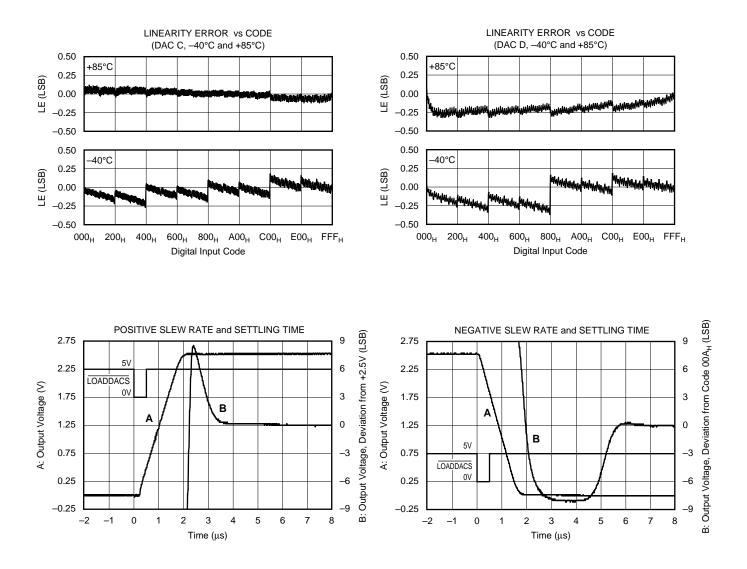






TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (CONT)

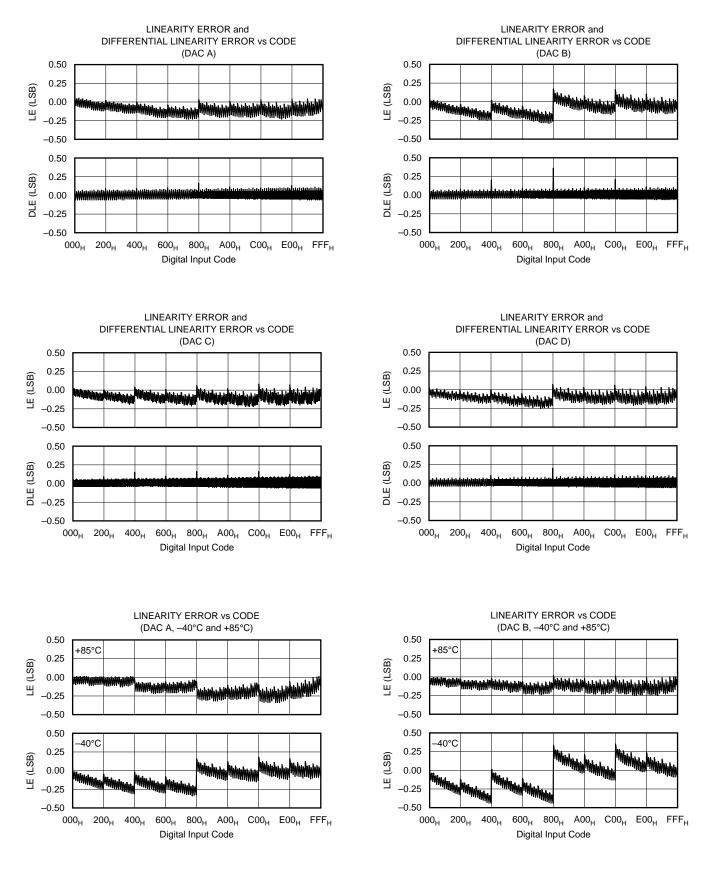
At $T_A = +25^{\circ}C$, $V_{DD} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +2.5V$, and $V_{REFL} = 0V$, representative unit, unless otherwise specified.





TYPICAL PERFORMANCE CURVES: $V_{SS} = -5V$

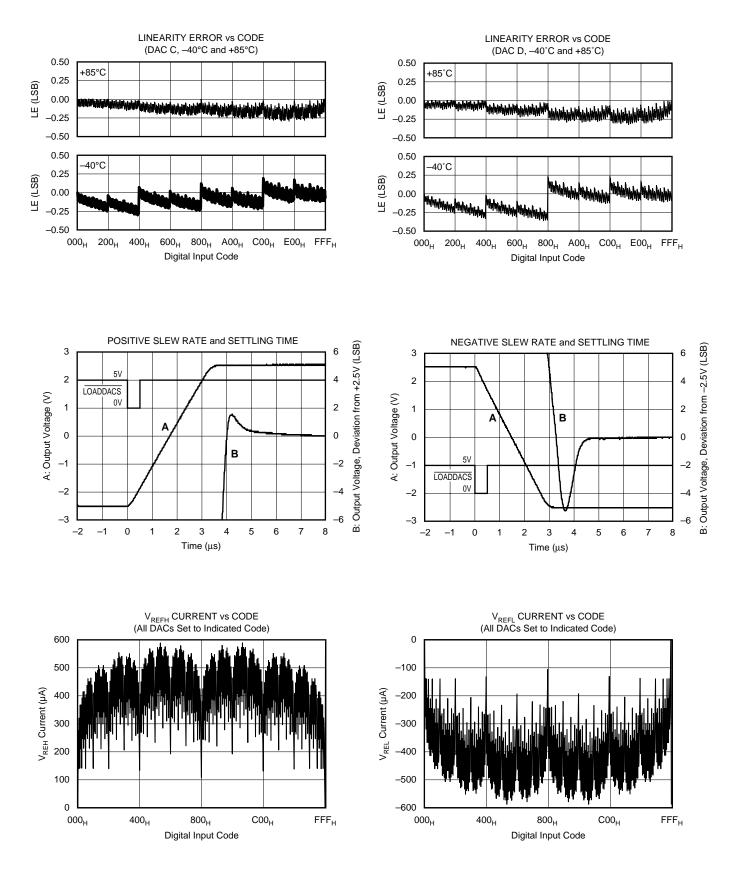
At $T_A = +25^{\circ}$ C, $V_{DD} = +5$ V, $V_{SS} = -5$ V, $V_{REFH} = +2.5$ V, and $V_{REFL} = -2.5$ V, representative unit, unless otherwise specified.



DAC7614

TYPICAL PERFORMANCE CURVES: $V_{SS} = -5V$ (CONT)

At $T_A = +25^{\circ}$ C, $V_{DD} = +5$ V, $V_{SS} = -5$ V, $V_{REFH} = +2.5$ V, and $V_{REFL} = -2.5$ V, representative unit, unless otherwise specified.





THEORY OF OPERATION

The DAC7614 is a quad, serial input, 12-bit, voltage output DAC. The architecture is a classic R-2R ladder configuration followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network and output op amp, but all share the reference voltage inputs. The minimum voltage output ("zero-scale") and maximum voltage output ("full-scale") are set by external voltage references (V_{REFL}) and V_{REFH} , respectively). The digital input is a 16-bit serial word that contains the 12-bit DAC code and a 2-bit address code that selects one of the four DACs (the two remaining bits are unused). The converter can be powered from a single +5V supply or a dual $\pm 5V$ supply. Each device offers a reset function which immediately sets all DAC output voltages and internal registers to either zero-scale (code 000_H) or mid-scale (code $800_{\rm H}$). The reset code is selected by the state of the RESETSEL pin (LOW = 000_{H} , HIGH = 800_{H}). See Figures 1 and 2 for the basic operation of the DAC7614.

ANALOG OUTPUTS

When $V_{SS} = -5V$ (dual supply operation), the output amplifier can swing to within 2.25V of the supply rails, over the -40°C to +85°C temperature range. With $V_{SS} = 0V$ (single-supply operation), the output can swing to ground. Note that the settling time of the output op amp will be longer with voltages very near ground. Also, care must be taken when measuring the zero-scale error when $V_{SS} = 0V$. If the output amplifier has a negative offset, the output voltage may not change for the first few digital input codes (000_H, 001_H, 002_H, etc.) since the output voltage cannot swing below ground.

The behavior of the output amplifier can be critical in some applications. Under short-circuit conditions (DAC output shorted to ground), the output amplifier can sink a great deal more current than it can source. See the Specifications table for more details concerning short-circuit current.

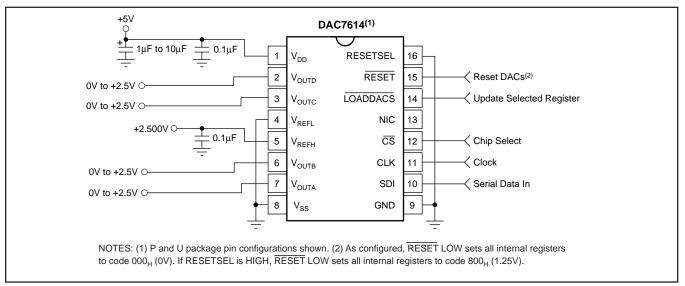


FIGURE 1. Basic Single-Supply Operation of the DAC7614.

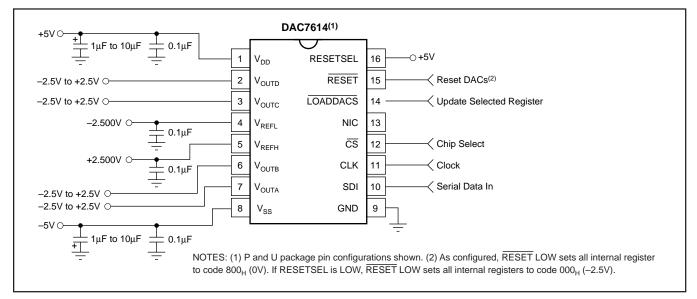


FIGURE 2. Basic Dual-Supply Operation of the DAC7614.



DAC7614

REFERENCE INPUTS

The reference inputs, V_{REFL} and V_{REFH} , can be any voltage between $V_{SS} + 2.25V$ and $V_{DD} - 2.25V$ provided that V_{REFH} is at least 1.25V greater than V_{REFL} . The minimum output of each DAC is equal to $V_{REFL} - 1LSB$ plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to V_{REFH} plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of -4.75V to -5.25V. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the reference inputs depends on the DAC output voltages and can vary from a few microamps to approximately 0.6 milliamp. Bypassing the reference voltage or voltages with a 0.1μ F capacitor placed as close as possible to the DAC7614 package is strongly recommended.

DIGITAL INTERFACE

Figure 3 and Table I provide the basic timing for the DAC7614. The interface consists of a serial clock (CLK), serial data (SDI), and a load DAC signal ($\overline{\text{LOADDACS}}$). In addition, a chip select ($\overline{\text{CS}}$) input is available to enable serial communication when there are multiple serial devices. An

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t _{DS}	Data Valid to CLK Rising	25			ns
t _{DH}	Data Held Valid after CLK Rises	20			ns
t _{CH}	CLK HIGH	30			ns
t _{CL}	CLK LOW	50			ns
t _{CSS}	CS LOW to CLK Rising	55			ns
t _{CSH}	CLK HIGH to $\overline{\text{CS}}$ Rising	15			ns
t _{LD1}	LOADDACS HIGH to CLK Rising	40			ns
t _{LD2}	CLK Rising to LOADDACS LOW	15			ns
t _{LDDW}	LOADDACS LOW Time	45			ns
t _{RSSH}	RESETSEL Valid to RESET LOW	25			ns
t _{RSTW}	RESET LOW Time	70			ns
t _S	Settling Time	10			μs

TABLE I. Timing Specifications ($T_A = -40^{\circ}C$ to $+85^{\circ}C$).

asynchronous reset input ($\overline{\text{RESET}}$) is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state.

The DAC code and address are provided via a 16-bit serial interface as shown in Figure 3. The first two bits select the DAC register that will be updated when LOADDACS goes LOW (see Table II). The next two bits are not used. The last 12 bits is the DAC code which is provided, most significant bit first.

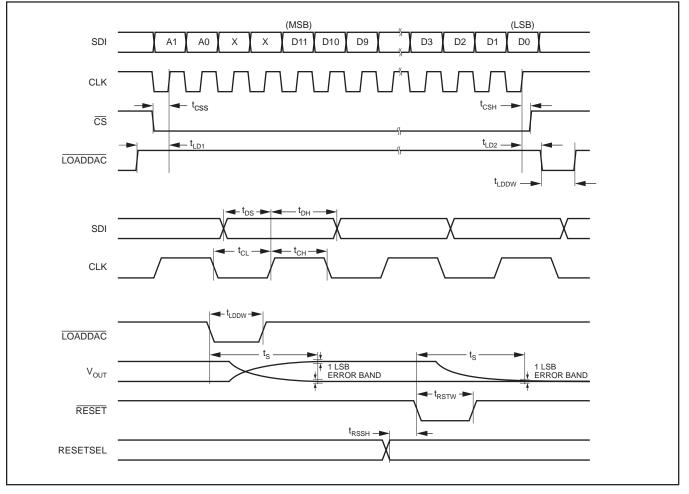


FIGURE 3. DAC7614 Timing.

A1	A0		RESET	SELECTED DAC REGISTER	STATE OF SELECTED DAC REGISTER
L(1)	L	L	н	А	Transparent
L	н	L	Н	В	Transparent
н	L	L	Н	С	Transparent
н	н	L	Н	D	Transparent
X ⁽²⁾	Х	н	н	NONE	(All Latched)
Х	Х	Х	L	ALL	Reset ⁽³⁾

NOTES: (1) L = Logic LOW. (2) X = Don't Care. (3) Resets to either <u>000H</u> or 800_H, per the RESETSEL state (LOW = 000_H, HIGH = 800_H). When $\overrightarrow{\text{RESET}}$ rises, all registers that are in their latched state retain the reset value.

TABLE II. Control Logic Truth Table.

CS ⁽¹⁾	CLK ⁽¹⁾	LOADDACS	RESET	SERIAL SHIFT REGISTER
H ⁽²⁾	X ⁽³⁾	н	н	No Change
L ⁽⁴⁾	L	н	н	No Change
L	∱(5)	н	н	Advanced One Bit
\uparrow	L	н	н	Advanced One Bit
H ⁽⁶⁾	х	L ⁽⁷⁾	н	No Change
H ⁽⁶⁾	Х	н	L ⁽⁸⁾	No Change

NOTES: (1) \overrightarrow{CS} and CLK are interchangeable. (2) H = Logic HIGH. (3) X = Don't Care. (4) L = Logic LOW (5) = Positive Logic Transition. (6) A HIGH value is suggested in order to avoid a "false clock" from advancing the shift register and changing the shift register. (7) If data is clocked into the serial register while LOADDACS is LOW, the selected DAC register will change as the shift register bits "flow" through A1 and A0. This will corrupt the data in each DAC register that has been erroneously selected. (8) RESET LOW causes no change in the contents of the serial shift register.

TABLE III. Serial Shift Register Truth Table.

Note that $\overline{\text{CS}}$ and CLK are combined with an OR gate and the output controls the serial-to-parallel shift register internal to the DAC7614 (see the block diagram on the front of this data sheet). These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when $\overline{\text{CS}}$ rises at the end of a serial transfer. If CLK is LOW when $\overline{\text{CS}}$ rises, the OR gate will provide a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong DAC.

If both \overline{CS} and CLK are used, then \overline{CS} should rise only when CLK is HIGH. If not, then either \overline{CS} or CLK can be used to operate the shift register. See Table III for more information.

Digital Input Coding

The DAC7614 input data is in Straight Binary format. The output voltage is given by the following equation:

$$V_{OUT} = V_{REFL} + \frac{(V_{REFH} - V_{REFL}) \bullet N}{4096}$$

where N is the digital input code (in decimal). This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.



LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. As the DAC7614 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it will be to achieve good performance from the converter.

Because the DAC7614 has a single ground pin, all return currents, including digital and analog return currents, must flow through the GND pin. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system (see Figure 4). The power applied to V_{DD} (as well as V_{SS} , if not grounded) should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a +5V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 1µF to 10µF and 0.1µF capacitors shown in Figure 4 are strongly recommended. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a "Pi" filter made up of inductors and capacitors—all designed to essentially lowpass filter the +5V supply, removing the high frequency noise (see Figure 4).

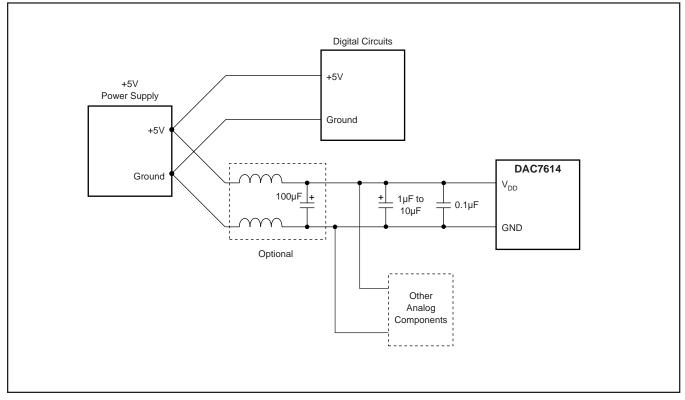


FIGURE 4. Suggested Power and Ground Connections for a DAC7614 Sharing a +5V Supply with a Digital System.





PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
							(6)				
DAC7614E	ACTIVE	SSOP	DB	20	70	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7614E	Samples
DAC7614E/1K	ACTIVE	SSOP	DB	20	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7614E	Samples
DAC7614EB	ACTIVE	SSOP	DB	20	70	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7614E B	Samples
DAC7614EB/1K	ACTIVE	SSOP	DB	20	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7614E	Samples
DAC7614U	ACTIVE	SOIC	DW	16	40	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7614U	Samples
DAC7614U/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7614U	Samples
DAC7614UB	ACTIVE	SOIC	DW	16	40	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7614U B	Samples
DAC7614UB/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7614U	Samples
DAC7614UBG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7614U B	Samples
DAC7614UG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7614U	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



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PACKAGE OPTION ADDENDUM

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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Texas

*All dimensions are nominal

STRUMENTS

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7614E/1K	SSOP	DB	20	1000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
DAC7614EB/1K	SSOP	DB	20	1000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
DAC7614U/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
DAC7614UB/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1



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PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7614E/1K	SSOP	DB	20	1000	356.0	356.0	35.0
DAC7614EB/1K	SSOP	DB	20	1000	356.0	356.0	35.0
DAC7614U/1K	SOIC	DW	16	1000	356.0	356.0	35.0
DAC7614UB/1K	SOIC	DW	16	1000	356.0	356.0	35.0

TEXAS INSTRUMENTS

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TUBE



- B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
DAC7614E	DB	SSOP	20	70	530	10.5	4000	4.1
DAC7614EB	DB	SSOP	20	70	530	10.5	4000	4.1
DAC7614U	DW	SOIC	16	40	507	12.83	5080	6.6
DAC7614UB	DW	SOIC	16	40	507	12.83	5080	6.6
DAC7614UBG4	DW	SOIC	16	40	507	12.83	5080	6.6
DAC7614UG4	DW	SOIC	16	40	507	12.83	5080	6.6

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