DS90C187 低功耗、1.8V 双像素 FPD-Link (LVDS) 串行器

1 特性

- 185MHz 下的典型功耗为 100mW（SIDO 模式）
- 驱动 QXGA 和 WQXGA 类显示器
- 三种工作模式：
  - 单输入像素、单输出像素 (SISO)：最大频率为 105MHz
  - 单输入像素、双输出像素 (SIDO)：最大频率为 185MHz
  - 双输入像素、双输出像素 (DIDO)：105MHz
- 支持 24 位 RGB、48 位 RGB
- 可选的低功耗模式支持 18 位 RGB、36 位 RGB
- 支持 3D+C、4D+C、6D+C、6D+2C、8D+C 和 8D+2C LVDS 配置
- 与 FPD-Link 解串器兼容
- 由 1.8V 单电源供电
- 直接与 1.8V LVCMOS 连接
- 睡眠模式下的功耗低于 1mW
- 与扩频时钟兼容
- 小型 7mm × 7mm × 0.9mm 92 引脚双行 VQFN 封装

2 应用

- 摄像头监控系统 (CMS)
- 汽车音响主机
- 智能后视镜
- 仪表组

3 说明

DS90C187 是一款低功耗串行器，该器件用于便携式电池供电，能够减小主机 GPU 与显示器之间的 RGB 接口的尺寸。

DS90C187 串行器旨在支持主机与平板显示器之间频率为 60Hz、分辨率高达 QXGA (2048x1536) 的双像素数据传输。该发送器可将高达 48 位（双像素 24 位颜色）的 1.8V LVCMOS 数据转换成双通道 4 数据 + 时钟 (4D+C) 宽度更低的接口 LVDS 兼容数据流。

DS90C187 支持 3 种工作模式。

- 在单输入像素/单输出像素模式下，该器件能够以 60Hz 的频率驱动高达 SXGA+ (1400x1050) 的分辨率。在该模式下，该器件可以将一组 24 位的 RGB 数据转换成单通道 4D+C LVDS 数据流。
- 在单输入像素/双输出像素模式下，该器件能够以 60Hz 的频率驱动高达 WUXGA+ (1920x1440) 的分辨率。在该配置下，该器件可以提供单像素到双像素的转换，将一组 24 位 RGB 数据转换成双通道 4D+C LVDS 数据流，其频率是像素时钟频率的一半。

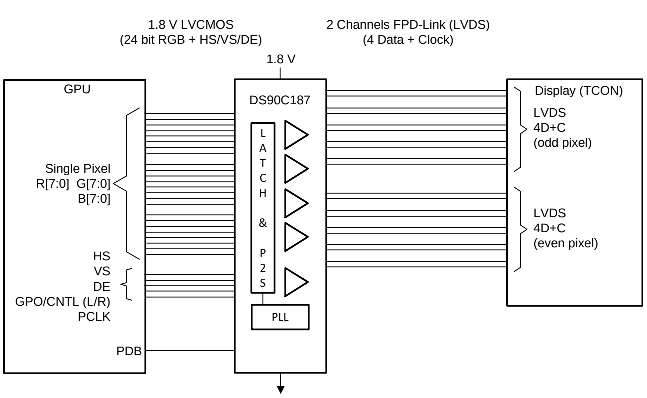
在双输入像素/双输出像素模式下，该器件能够以 60Hz 的频率下驱动高达 QXGA 2048x1536 的分辨率，或者以 30Hz 的频率驱动高达 QSXGA 2560x2048 的分辨率。在该模式下，该器件可以 2 通道 24 位 RGB 数据转换成 2 通道 4D+C LVDS 数据流。 对于所有模式，该器件都支持 18bpp 和 24bpp 颜色。

器件信息[(1)]

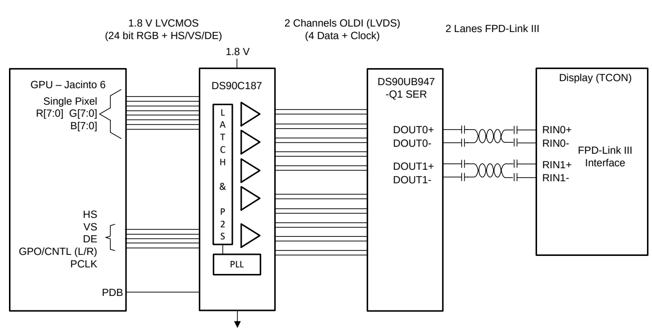
器件型号	封装	封装尺寸（标称值）
DS90C187	VQFN-MR (92)	7.00mm × 7.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用



典型应用



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (April 2013) to Revision C — **Page**

- 添加了*器件信息* 表、*器件比较* 表、*ESD 额定值* 表、*特性 说明部分*，*器件功能模式*，*应用和实施部分*，*电源相关建议部分*，*布局部分*，*器件和文档支持部分以及机械、封装和可订购信息部分*。 ... 1
- Added Start Up / Phase Lock Loop Set Time timing diagram ... 9
- Added content to the *Power Up Sequence* section ... 26

Changes from Revision A (April 2013) to Revision B — **Page**

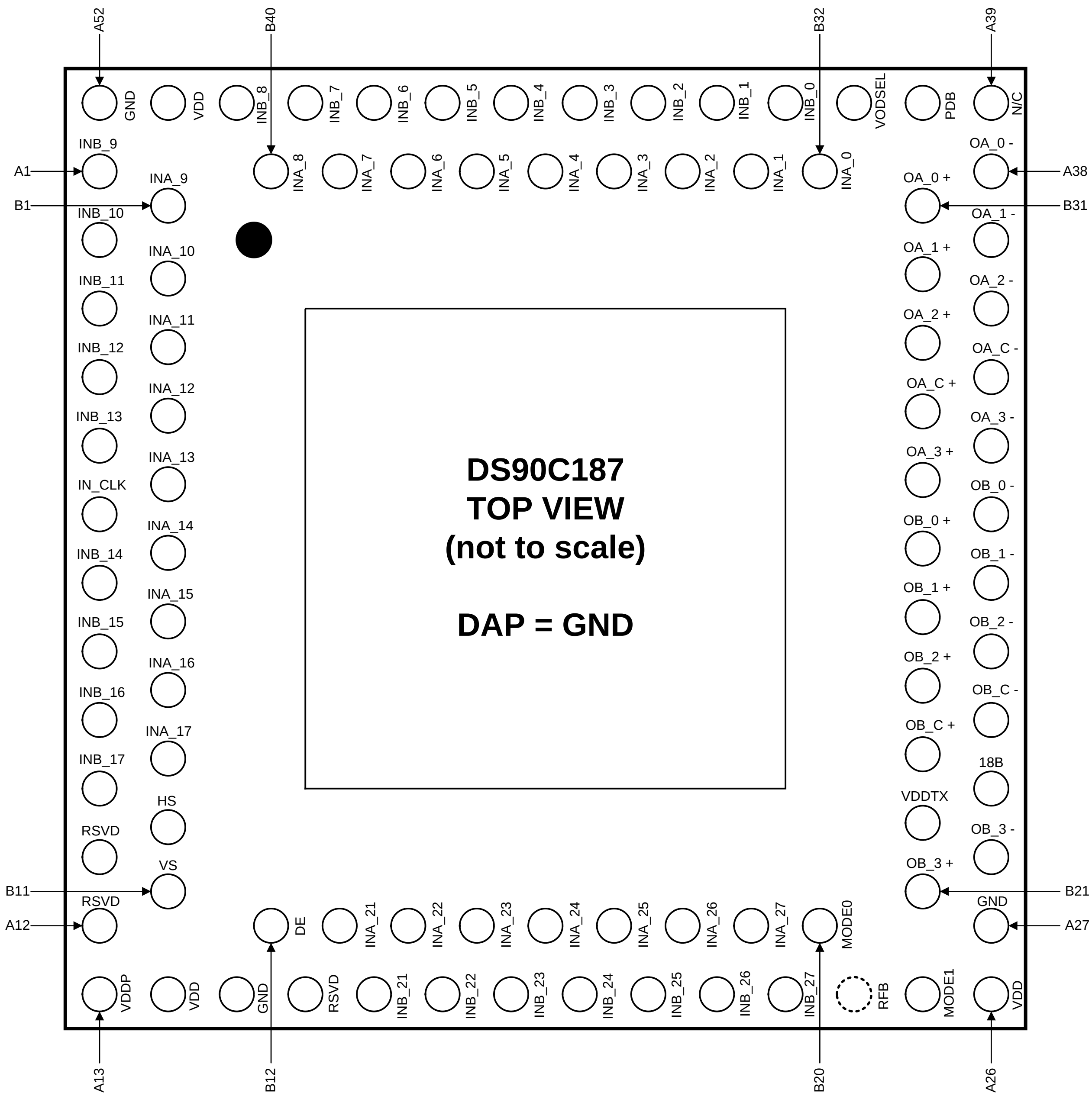
- 已将美国国家半导体数据表的版面布局更改为 TI 格式 ... 1

5 （说明 （续））

DS90C187 采用小型 92 引脚双行 VQFN 封装并 采用 1.8V 单电源，以实现最低的功率耗散。

6 Pin Configuration and Functions

NLA Package
92-Pin VQFN-MR
Top View



DS90C187 Pin Descriptions — Serializer

NAME	PIN NO.	I/O	DESCRIPTION
1.8-V LVCMOS VIDEO INPUTS			
INA_[27:21] INA_[17:9] NA_[8:0]	B19-B13, B9-B1, B40-B32	I	Channel A Data Inputs Typically consists of 8 Red, 8 Green, 8 Blue and a general purpose or L/R control bit. Includes pull down.
INB_[27:21] INB_[17:14], INB_[13:9] INB_[8:0	A23-A17, A10-A7, A5-A1, A50-A42	I	Channel B Data Inputs Typically consists of 8 Red, 8 Green, 8 Blue and a general purpose or L/R control bit. Includes pull down.
HS (INA_18), VS (INA_19), DE (INA_20)	B10, B11 B12	I	Video Control Signal Inputs - HS = Horizontal Sync, VS = Vertical SYNC, and DE = Data Enable
IN_CLK	A6	I	Pixel Input Clock Includes pull down.
1.8-V LVCMOS CONTROL INPUTS			
MODE0, MODE1	B20, A25	I	Mode Control Input (MODE0) 00 = Single In / Single Out 01 = Single In / Dual Out 10 = Dual In / Dual Out 11 = Reserved Includes pull down.
RFB	A24	I	Rising / Falling Clock Edge Select Input - 0 = Falling Edge, 1 = Rising Edge Includes pull down.
PDB	A40	I	Power Down (Sleep) Control Input - 0 = Sleep (Power Down mode), 1 = device active (enabled) Includes pull down.
18B	A29	I	18 bit / 24 bit Control Input - 0 = 24 bit mode, 1 = 18 bit mode Includes pull down.
VODSEL	A41	I	VOD Level Select Input - 0 = Low swing, 1 = Normal swing Includes pull down.
N/C	A39	I	**no connect pin — leave open**
RSVD	A11, A12, A16	I	**Reserved - Tie to Ground.**
LVDS OUTPUTS			
OA_C+ OA_C-	B28, A35	O	Channel A LVDS Output Clock — Expects 100 Ω DC load.
OA_[3:0]+, OA_[3:0]-	B27, B29-B31 A34, A36-A38	O	Channel A LVDS Output Data — Expects 100 Ω DC load.
OB_C+, OB_C-	B23, A30	O	Channel B LVDS Output Clock — Expects 100 Ω DC load.
OB_[3:0]+, OB_[3:0]-	B21, B24-B26 A28, A16-A33	O	Channel B LVDS Output Data — Expects 100 Ω DC load.
POWER AND GROUND			
V_{DDTX}	B22	P	Power supply for LVDS Drivers, 1.8V.
V_{DD}	A14, A26, A51	P	Power supply pin for core, 1.8V.
V_{DDP}	A13	P	Power supply pin for PLL, 1.8V.
GND	A15, A27, A52	G	Ground pins.
DAP	DAP	G	**Connect DAP to Ground plane.**

7 Specifications

7.1 Absolute Maximum Ratings

See (1)

	MIN	MAX	UNIT
Supply Voltage (V_{CC})	−0.3	2.5	V
LVCMOS Input Voltage	−0.3	VDD + 0.3	V
LVDS Driver Output Voltage	−0.3	3.6	V
LVDS Output Short-Circuit Duration	Continuous		
Junction Temperature		150	°C
Storage Temperature (T_{stg})	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1250	
		Machine model	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. **[Following sentence optional; see the wiki.]** Manufacturing with less than 500-V HBM is possible with the necessary precautions. **[Following sentence optional; see the wiki.]** Pins listed as ±XXX V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. **[Following sentence optional; see the wiki.]** Manufacturing with less than 250-V CDM is possible with the necessary precautions. **[Following sentence optional; see the wiki.]** Pins listed as ±YYY V may actually have higher performance.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage	1.71	1.80	1.89	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Differential Load Impedance	80	100	120	Ω
Supply Noise Voltage			<90	mV_{p-p}

7.4 Thermal Information

THERMAL METRIC (1)		DS90C187 NLA (VQFN-MR) 92 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	35.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		°C/W
ψ_{JT}	Junction-to-top characterization parameter		°C/W
ψ_{JB}	Junction-to-board characterization parameter		°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Above +22°C

7.5 Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS DC SPECIFICATIONS					

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High Level Input Voltage			$0.65V_{DD}$		V_{DD}	V
V_{IL}	Low Level Input Voltage			GND		$0.35V_{DD}$	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DD} = 1.71 V to 1.89 V		–10	±1	+10	µA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω 图 3	VODSEL = V_{IH}	160 (320)	300 (600)	450 (900)	mV (mV_{P-P})
			VODSEL = V_{IL}	110 (220)	180 (360)	300 (600)	mV (mV_{P-P})
ΔV_{OD}	Change in V_{OD} between Complimentary Output States	R_L = 100Ω 图 3				50	mV
V_{OS}	Offset Voltage	R_L = 100Ω 图 3		0.8	0.9	1.0	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States	R_L = 100Ω 图 3				50	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = GND, VODSEL = V_{DD}		-45	−35	−25	mA
SUPPLY CURRENT							
IDDT1	Serializer Worst Case Supply Current (includes load current)	Checkerboard pattern, R_L = 100 Ω, 18B = V_{IL}, VODSEL = V_{IH}, V_{DD} = 1.89 V, 图 1	f = 105 MHz, MODE[1:0] = 00 (SISO)		60	85	mA
IDDT2			f = 185 MHz, MODE[1:0] = 01 (SIDO)		95	140	mA
IDDT3			f = 105 MHz, MODE[1:0] = 10 (DIDO)		100	150	mA
IDDTP	Serializer Supply Current PRBS-7	MODE[1:0] = 01 (SIDO), f = 150 MHz, R_L = 100 Ω, PRBS-7 Pattern 图 12	18B = V_{IL}, VODSEL = V_{IL}, VDD = 1.8		55		mA
			18B = V_{IL}, VODSEL = V_{IH}, VDD = 1.8		75		mA
			18B = V_{IH}, VODSEL = V_{IL}, VDD = 1.8		49		mA
			18B = V_{IH}, VODSEL = V_{IH}, VDD = 1.8		65		mA
IDDTG	Serializer Supply Current 16 Grayscale	MODE[1:0] = 01 (SIDO), f = 150 MHz, R_L = 100 Ω, 16 Grayscale Pattern	18B = V_{IL}, VODSEL = V_{IL}, VDD = 1.8		53		mA
			18B = V_{IL}, VODSEL = V_{IH}, VDD = 1.8		71		mA
			18B = V_{IH}, VODSEL = V_{IL}, VDD = 1.8		48		mA
			18B = V_{IH}, VODSEL = V_{IH}, VDD = 1.8		63		mA
IDDZ	Power Down Supply Current	PDB = GND			18	200	µA

7.6 Recommended Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER			MIN	TYP	MAX	UNIT
TCIT	IN_CLK Transition Time 图 5	MODE[1:0] = 00 or 10	1	T	4	ns
		MODE[1:0] = 01	1		2	ns
TCIP	IN_CLK Period 图 6	MODE[1:0] = 00 or 10	9.53	T	40	ns
		MODE[1:0] = 01	5.40	T	20	ns
TCIH	IN_CLK High Time	See 图 6	0.35T	0.5T	0.65T	ns
TCIL	IN_CLK Low Time	See 图 6	0.35T	0.5T	0.65T	ns
TXIT	INA_x & INB_x Transition Time	See 图 5	1.5		0.3T	ns

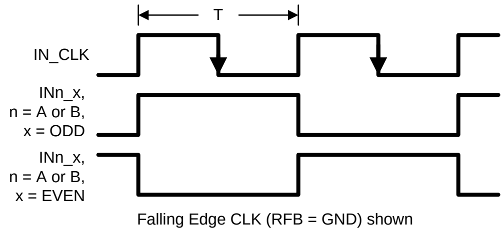
7.7 Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER			MIN	TYP	MAX	UNIT
TSTC	INn_x Setup to IN_CLK	See 图 6	0			ns
THTC	INn_x Hold from IN_CLK	See 图 6	2.5			ns
LLHT	LVDS Low-to-High Transition Time 图 4 (1)			0.18	0.5	ns
LHLT	LVDS High-to-Low Transition Time 图 4 (1)			0.18	0.5	ns
TBIT	LVDS Output Bit Width	MODE[1:0] = 00, or 10		1/7 TCIP		ns
		MODE[1:0] = 01		2/7 TCIP		ns
TPPOS0	Transmitter Output Pulse Positions Normalized for Bit 0	See 图 9		1		UI
TPPOS1	Transmitter Output Pulse Positions Normalized for Bit 1	See 图 9		2		UI
TPPOS2	Transmitter Output Pulse Positions Normalized for Bit 2	See 图 9		3		UI
TPPOS3	Transmitter Output Pulse Positions Normalized for Bit 3	See 图 9		4		UI
TPPOS4	Transmitter Output Pulse Positions Normalized for Bit 4	See 图 9		5		UI
TPPOS5	Transmitter Output Pulse Positions Normalized for Bit 5	See 图 9		6		UI
TPPOS6	Transmitter Output Pulse Positions Normalized for Bit 6	See 图 9		7		UI
ΔTPPOS	Variation in Transmitter Pulse Position (Bit 6 — Bit 0)	See 图 9		±0.06		UI
TCCS	LVDS Channel to Channel Skew			110		ps
TJCC	Jitter Cycle-to-Cycle	MODE0, MODE1 = 0, f = 105 MHz, (1)		0.028	0.035	UI
TPLLS	Phase Lock Loop Set (Enable Time)	图 7			1	ms
TPDD	Powerdown Delay	图 8 (2)			100	ns
TSD	Latency Delay	MODE0 = 0, MODE1 = 1 or 0 图 10 (1)		2*TCIP + 10.54	2*TCIP + 13.96	ns
TLAT	Latency Delay for Single Pixel In / Dual Pixel Out Mode	MODE0 = 1, MODE1 = 0 图 10 (1)		9*TCIP + 4.19	9*TCIP + 6.36	ns

(1) Parameter is ensured by characterization and is not tested at final test.
(2) Parameter is ensured by design and is not tested at final test.

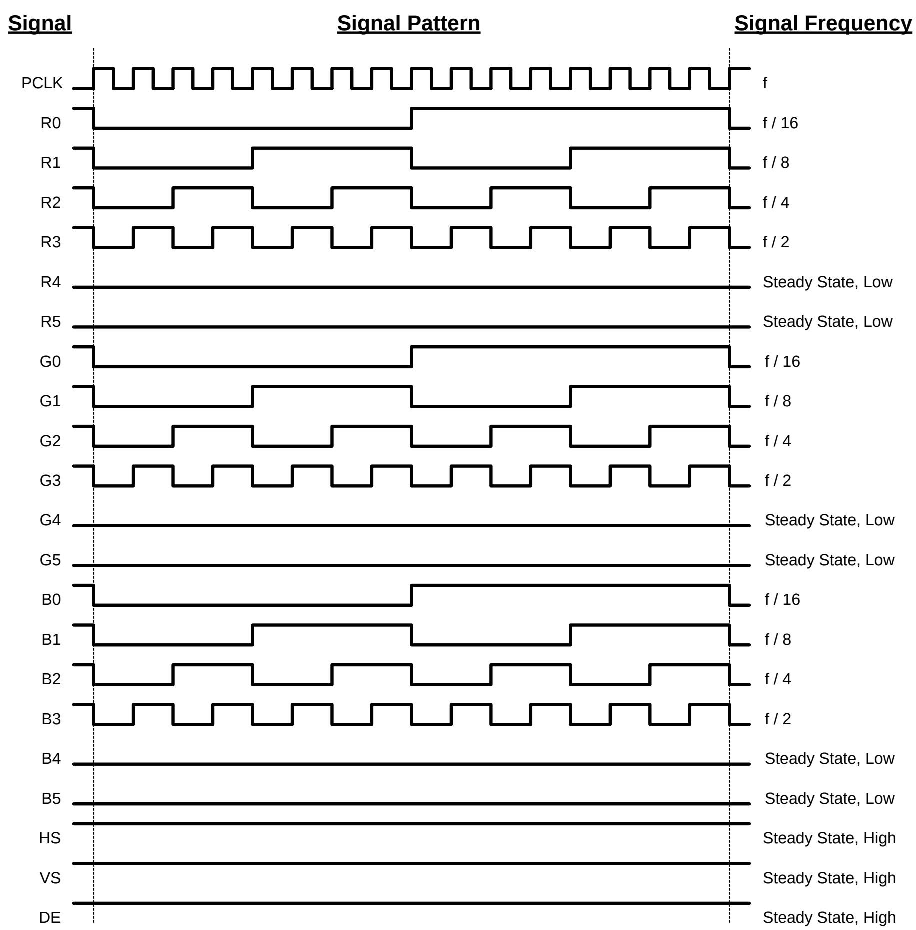
7.8 AC Timing Diagrams



A. The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVCMOS/ I/O.

B. 图 1 and 图 2 show a falling edge data strobe (IN_CLK).

图 1. Checker Board Test Pattern



A. The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVCMOS/ I/O.

B. Recommended pin to signal mapping for 18 bits per pixel, customer may choose to define differently. The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

C. 图 2 shows a falling edge data strobe (IN_CLK).

图 2. "16 Gray Scale" Test Pattern (Falling Edge Clock shown)

AC Timing Diagrams (接下页)

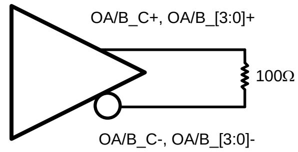


图 3. DS90C187 (Transmitter) LVDS Output Load

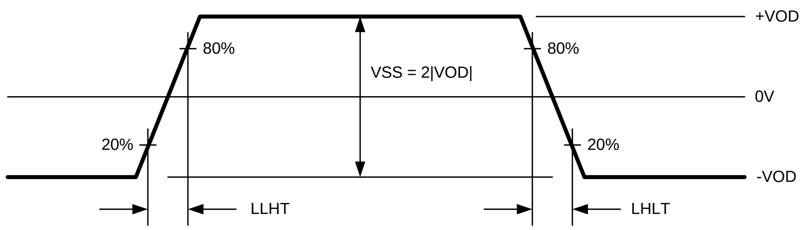


图 4. LVDS Output Transition Times

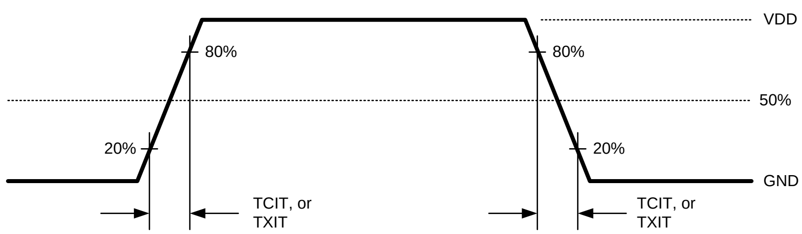


图 5. LVCMOS Input Transition Times

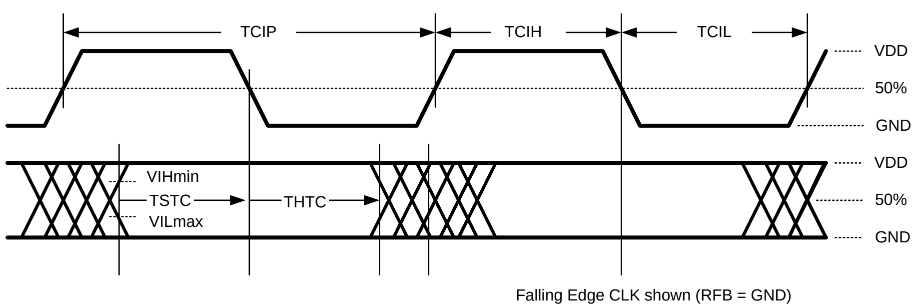


图 6. LVCMOS Input Setup/Hold and Clock High/Low Times (Falling Edge Strobe)

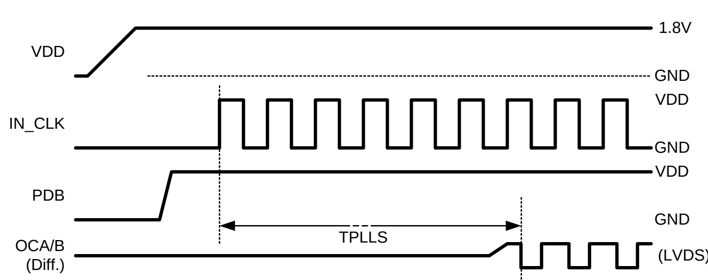


图 7. Start Up / Phase Lock Loop Set Time

AC Timing Diagrams (接下页)

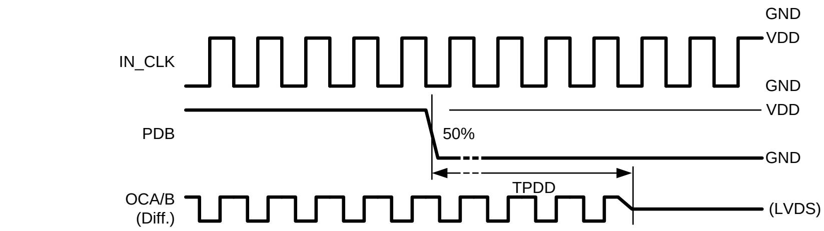


图 8. Sleep Mode / Power Down Delay

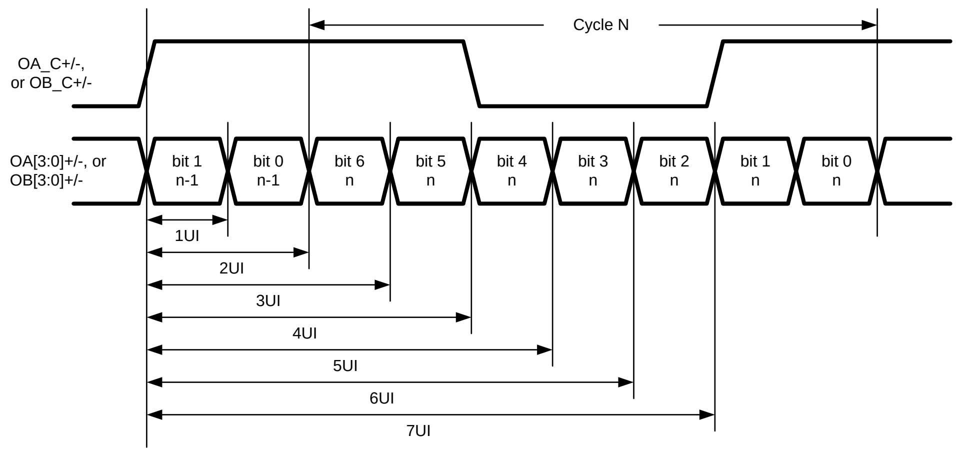


图 9. LVDS Serial Bit Positions

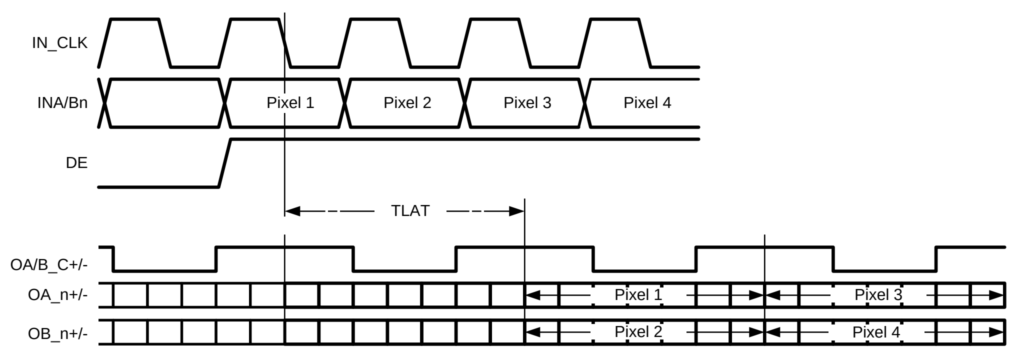


图 10. Single In Dual Out Mode Timing and Latency

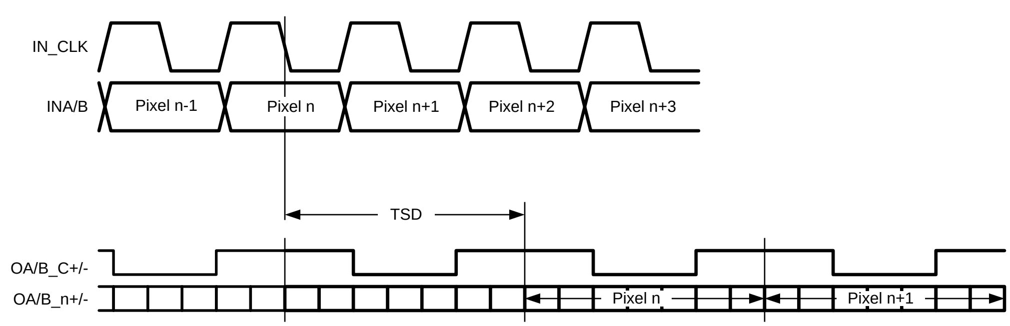


图 11. Single In Single Out / Dual In Dual Out Latency

7.9 Typical Characteristics

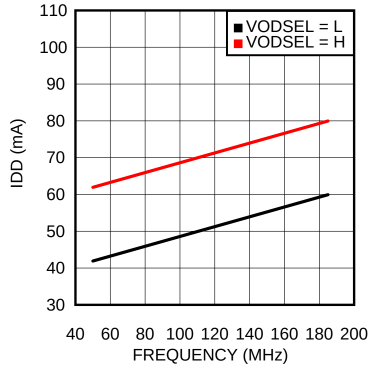


图 12. Typ Current Draw — Single In/Dual Out Mode — PRBS-7 Data Pattern

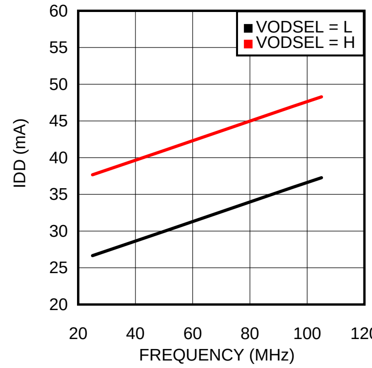


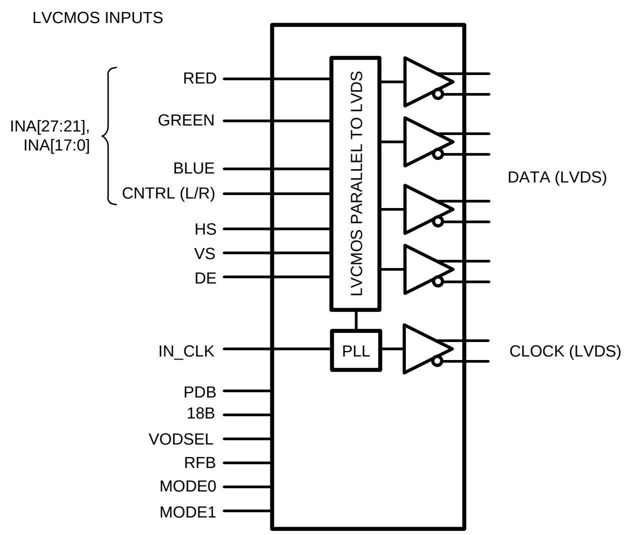
图 13. Typ Current Draw — Single In/Single Out Mode — PRBS-7 Data Pattern

8 Detailed Description

8.1 Overview

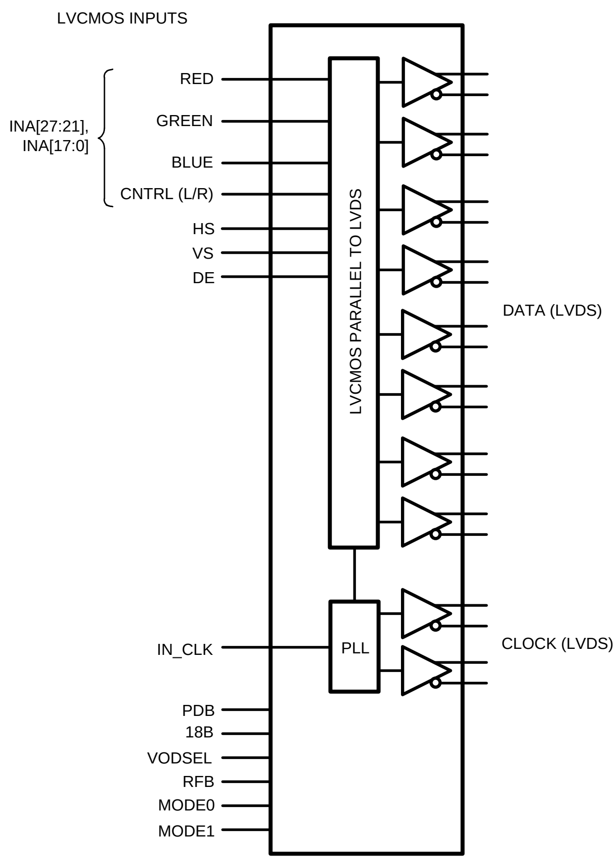
DS90C187 converts a wide parallel LVCMOS input bus into banks of FPD-Link LVDS data. The device can be configured to support RGB-888 (24-bit color) or RGB-666 (18 bit color) in three main configurations: single pixel in / single pixel out; single pixel in / dual pixel out; dual pixel in / dual pixel out. The DS90C187 has several power saving features including: selectable VOD, 18 bit / 24 bit mode select, and a power down pin control.

8.2 Functional Block Diagrams



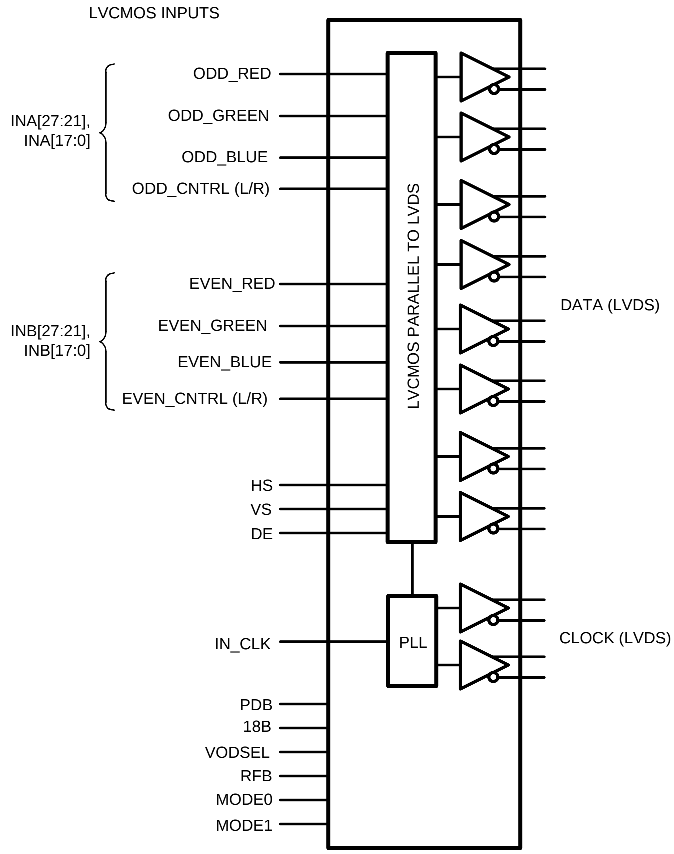
DS90C187 – SERIALIZER
Single Pixel In / Single Pixel Out
(SISO)

Functional Block Diagrams (接下页)



DS90C187 – SERIALIZER
Single Pixel In / Dual Pixel Out (SIDO)

Functional Block Diagrams (接下页)



DS90C187 – SERIALIZER
Dual Pixel In / Dual Pixel Out (SIDO)

8.3 Device Functional Modes

8.3.1 Device Configuration

The MODE0 and MODE1 pins are used to configure the DS90C187 into the three main operation modes as shown in the table below.

表 1. Mode Configurations

MODE1	MODE0	CONFIGURATION
0	0	Single Pixel Input, Single Pixel Output (SISO)
0	1	Single Pixel Input, Dual Pixel Output (SIDO)
1	0	Dual Pixel Input, Dual Pixel Output (DIDO)
1	1	RESERVED

8.3.2 Single Pixel Input / Single Pixel Output

When MODE0 and MODE1 are both set to low, data from INA_[27:0], HS, VS and DE is serialized and driven out on OA_[3:0]+/- with OA_C+/-. If 18B_MODE is LOW, then OA_3+/- is powered down and the corresponding LVCMOS input signals are ignored.

In this configuration IN_CLK can range from 25 MHz to 105 MHz, resulting in a total maximum payload of 700 Mbps (28 bits * 25MHz) to 2.94 Gbps (28 bits * 105 MHz). Each LVDS driver will operate at a speed of 7 bits per input clock cycle, resulting in a serial line rate of 175 Mbps to 735 Mbps. OA_C+/- will operate at the same rate as IN_CLK with a duty cycle ratio of 57:43.

8.3.3 Single Pixel Input / Dual Pixel Output

When MODE0 is HIGH and MODE1 is LOW, data from INA_[27:0], HS, VS and DE is serialized and driven out on OA_[3:0]+/- and OB_[3:0]+/- with OA_C+/- and OB_C+/-. If 18B_MODE is LOW, then OA_3+/- and OB_3+/- are powered down and the corresponding LVCMOS input signals are ignored. The input LVCMOS data is split into odd and even pixels starting with the odd (first) pixel outputs OA_[3:0]+/- and then the even (second) pixel outputs OB_[3:0]+/-. The splitting of the data signals starts with DE (data enable) transitioning from logic LOW to HIGH indicating active data (see 图 10). **The number of clock cycles during blanking must be an EVEN number.** This configuration will allow the user to interface with two FPD-Link receivers or other dual pixel inputs.

In this configuration IN_CLK can range from 50 MHz to 185 MHz, resulting in a total maximum payload of 1.4 Gbps (28 bits * 50 MHz) to 5.18 Gbps (28 bits * 185 MHz). Each LVDS driver will operate at a speed of 7 bits per 2 input clock cycles, resulting in a serial line rate of 175 Mbps to 647.5 Mbps. OA_C+/- and OA_B+/- will operate at ½ the rate as IN_CLK with a duty cycle ratio of 57:43.

1. Disable the clock and data.
2. Toggle PDB to Low and then High.
3. After PDB settles reset the data pattern and enable the clock and data.

8.3.4 Dual Pixel Input / Dual Pixel Output

When MODE0 is LOW and MODE1 is set to HIGH, data from INA_[27:0], HS, VS and DE is serialized and driven out on OA_[3:0]+/- with OA_C+/-, while data from INB_[27:0], HS, VS and DE is serializer and driven out on OB_[3:0]+/- with OB_C+/-. If 18B_MODE is LOW, then OA_3+/- and OB_3+/- is powered down and the corresponding LVCMOS input signals are ignored.

In this configuration IN_CLK can range from 25 MHz to 105 MHz, resulting in a total maximum payload of 1.325 Gbps (53 bits * 25 MHz) to 5.565 Gbps (53 bits * 105 MHz). Each LVDS driver will operate at a speed of 7 bits per input clock cycle, resulting in a serial line rate of 175 Mbps to 735 Mbps. OA_C+/- and OB_C+/- will operate at the same rate as IN_CLK with a duty cycle ratio of 57:43.

8.3.5 Pixel Clock Edge Select (RFB)

The RFB pin determines the edge that the input LVCMOS data is latched on. If RFB is HIGH, input data is latched on the RISING EDGE of the pixel clock (IN_CLK). If RFB is LOW, the input data is latched on the FALLING EDGE of the pixel clock. Note: This can be set independently of receiver’s output clock strobe.

表 2. Pixel Clock Edge

RFB	Result
0	FALLING edge
1	RISING edge

8.3.6 Power Management

The DS90C187 has several features to assist with managing power consumption. The device can be configured through the MODE0 and MODE1 control pins to enable only the required number of LVDS drivers for each application. The 18B_MODE pin allows the DS90C187 to power down the unused LVDS driver(s) for RGB-666 (18 bit color) applications for an additional level of power management. If no clock is applied to the IN_CLK pin, the DS90C187 will enter a low power state. To place the DS90C187 in its lowest power state, the device can be powered down by driving the PDB pin to LOW.

8.3.7 Sleep Mode (PDB)

The DS90C187 provides a power down feature. When the device has been powered down, current draw through the supply pins is minimized and the PLL is shut down. The LVDS drivers are also powered down with their outputs pulled to GND through 100-Ω resistors (not tri-stated).

表 3. Power Down Select

PDB	Result
0	SLEEP Mode (default)
1	ACTIVE (enabled)

8.3.8 LVDS Outputs

The DS90C187's LVDS drivers are compatible with ANSI/TIA/EIA-644-A LVDS receivers. The LVDS drivers can output a power saving low V_{OD}, or a high V_{OD} to enable longer trace and cable lengths by configuring the VODSEL pin.

表 4. VOD Select

VODSEL	Result
0	±220 mV (440 mVpp)
1	±340 mV (680 mVpp)

Any unused LVDS outputs that are not powered down or put into TRI-STATE® due to the MODE0, MODE1, or 18B pins should be externally terminated differentially with a 100 ohm resistor. For example, when driving a timing controller (TCON) that only requires an 8D + C LVDS interface, rather than 8D + 2C, the unused clock line should be terminated near the package of the DS90C187. For more information regarding the output state of unused LVDS drivers, refer to the next section, 18 bit / 24 bit Color Mode (18B). For more information regarding the electrical characteristics of the LVDS outputs, refer to the LVDS DC Characteristics and LVDS Switching Specifications.

8.3.9 18 bit / 24 bit Color Mode (18B)

The 18B pin can be used to further save power by powering down the 4th LVDS driver in each used bank when the application requires only 18 bit color or 3D+C LVDS. Set the 18B pin to logic HIGH to TRI-STATE® OA_3+/- and OB_3+/- (if the device is configured for dual pixel output). For 24 bit color applications this pin should be set to logic LOW. Note that the power down function takes priority over the TRI-STATE® function. So if the device is configured for 18 bit color Single Pixel In/Single Pixel Out, LVDS channel OB_3+/- will be powered down and not TRI-STATE®. If an LVDS driver is powered down, each output terminal is pulled low by a 100 ohm resistor to ground.

表 5. Color DepthConfigurations

18B	Result
0	24bpp, LVDS 4D+C or 8D+2C
1	18bpp, LVDS 3D+C or 6D+2C

8.3.10 LVCMOS Inputs

The DS90C187 has two banks of 24 data inputs, one set of video control signal (HS, VS and DE) inputs and several device configuration LVCMOS pins. All LVCMOS input pins are designed for 1.8 V LVCMOS logic. All LVCMOS inputs, including clock, data and configuration pins, have an internal pull down resistor to set a default state. If any inputs are unused, they can be left as no connect (NC) or connected to ground.

8.4 Programming

8.4.1 LVDS Interface / TFT Color Data Recommended Mapping

Different color mapping options exist. Check with the color mapping of the Deserializer / TCON device that is used to ensure compatible mapping for the application. The DS90C187 supports three modes of operation for single and dual pixel applications supporting either 24bpp or 18bpp color depths.

Programming (接下页)

In the Dual Pixel / 24bpp mode, eight LVDS data lines are provided along with two LVDS clock lines (8D+2C). The Deserializer may utilize one or two clock lines. The 53 bit interface typically assigns 24 bits to RGB for the odd pixel, 24 bits to RGB for the even pixel, 3 bits for the video control signals (HS, VS and DE), 1 bit for odd pixel and 1 bit for even pixel which can be ignored or used for general purpose data, control or L/R signaling.

A reduced width input interface is also supported with a Single-to-Dual Pixel conversion where the data is presented at double rate (same clock edge, 2X speed, see) and the DE transition is used to flag the first pixel. Also note in both 8D+2C configurations, the three video control signals are sent over **both** the A and B outputs. The DES / TCON may recover one set, or both depending upon its implementation. The Dual Pixel / 24bpp 8D+2C LVDS Interface Mapping is shown in .

A Dual Pixel / 18bpp mode is also supported. In this configuration OA3 and OB3 LVDS output channels are placed in TRI-STATE® to save power. Their respective inputs are ignored. (图 15)

In the Single Pixel / 24bpp mode, four LVDS data lines are provided along with a LVDS clock line (4D+C). The 28 bit interface typically assigns 24 bits to RGB color data, 3 bits to video control (HS, VS and DE) and one spare bit can be ignored, used for L/R signaling or function as a general purpose bit. The Single Pixel / 24bpp 4D+C LVDS Interface Mapping is shown in .

A Single Pixel / 18bpp mode is also supported. In this configuration the OA3 LVDS output channel is placed in TRI-STATE® to save power. Its respective inputs are ignored. (图 17)

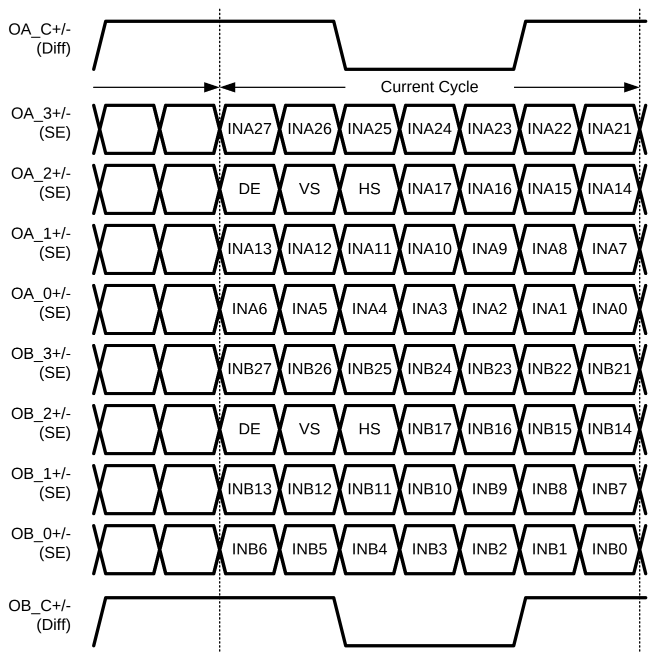


图 14. Dual Pixel / 24bpp LVDS Mapping

Programming (接下页)

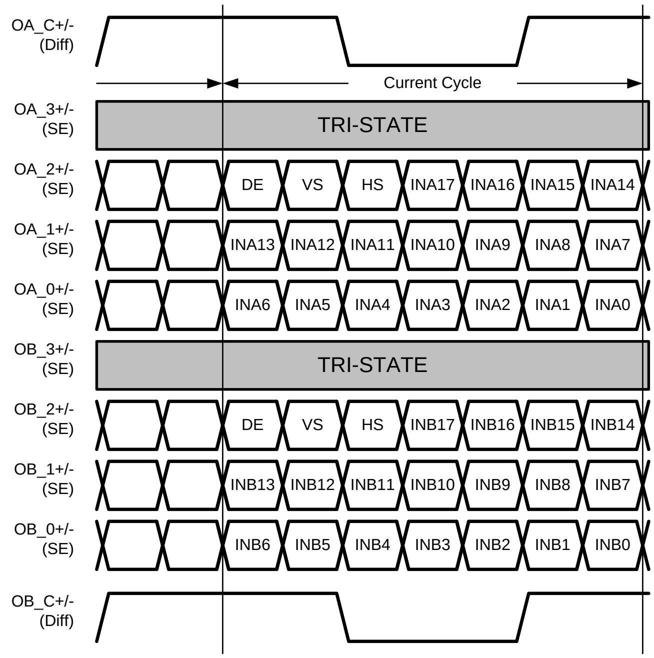


图 15. Dual Pixel / 18bpp LVDS Mapping

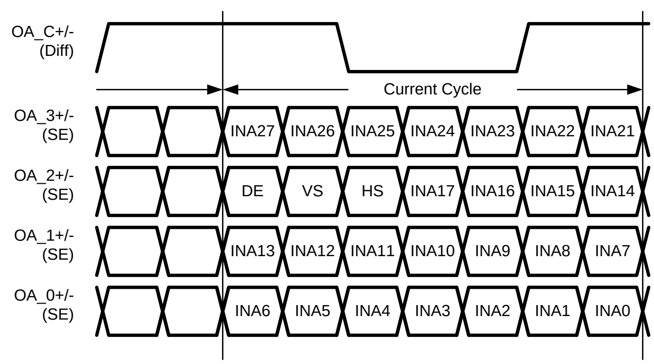


图 16. Single Pixel / 24bpp LVDS Mapping

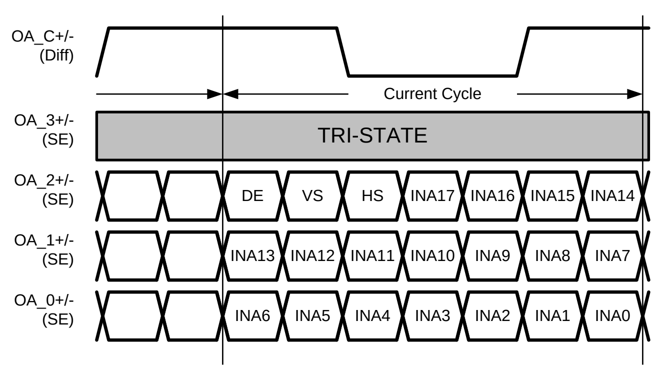


图 17. Single Pixel / 18bpp LVDS Mapping

Programming (接下页)

8.4.1.1 Color Mapping Information

A defacto color mapping is shown next. Different color mapping options exist. Check with the color mapping of the Deserializer / TCON device that is used to ensure compatible mapping for the application.

表 6. Single Pixel Input / 24bpp / MSB on CH3

DS90C187 Input	Color Mapping	Note
INA_22	R7	MSB
INA_21	R6	
INA_5	R5	
INA_4	R4	
INA_3	R3	
INA_2	R2	
INA_1	R1	
INA_0	R0	LSB
INA_24	G7	MSB
INA_23	G6	
INA_11	G5	
INA_10	G4	
INA_9	G3	
INA_8	G2	
INA_7	G1	
INA_6	G0	LSB
INA_26	B7	MSB
INA_25	B6	
INA_17	B5	
INA_16	B4	
INA_15	B3	
INA_14	B2	
INA_13	B1	
INA_12	B0	
DE	DE	Data Enable*
VS	VS	Vertical Sync
HS	HS	Horizontal Sync
INA_27	GP	General Purpose

表 7. Single Pixel Input / 24bpp / LSB on CH3

DS90C187 Input	Color Mapping	Note
INA_5	R7	MSB
INA_4	R6	
INA_3	R5	
INA_2	R4	
INA_1	R3	
INA_0	R2	
INA_22	R1	
INA_21	R0	LSB
INA_11	G7	MSB
INA_10	G6	
INA_9	G5	

表 7. Single Pixel Input / 24bpp / LSB on CH3 (接下页)

DS90C187 Input	Color Mapping	Note
INA_8	G4	
INA_7	G3	
INA_6	G2	
INA_24	G1	
INA_23	G0	LSB
INA_17	B7	MSB
INA_16	B6	
INA_15	B5	
INA_14	B4	
INA_13	B3	
INA_12	B2	
INA_26	B1	
INA_25	B0	
DE	DE	Data Enable*
VS	VS	Vertical Sync
HS	HS	Horizontal Sync
INA_27	GP	General Purpose

表 8. Single Pixel Input / 18bpp

DS90C187 Input	Color Mapping	Note
INA_5	R5	MSB
INA_4	R4	
INA_3	R3	
INA_2	R2	
INA_1	R1	
INA_0	R0	LSB
INA_11	G5	MSB
INA_10	G4	
INA_9	G3	
INA_8	G2	
INA_7	G1	
INA_6	G0	LSB
INA_17	B5	MSB
INA_16	B4	
INA_15	B3	
INA_14	B2	
INA_13	B1	
INA_12	B0	
DE	DE	Data Enable*
VS	VS	Vertical Sync
HS	HS	Horizontal Sync

表 9. Dual Pixel Input / 24bpp

DS90C187 Input	Color Mapping	Note
INA_22	O_R7	MSB
INA_21	O_R6	
INA_5	O_R5	

表 9. Dual Pixel Input / 24bpp (接下页)

DS90C187 Input	Color Mapping	Note
INA_4	O_R4	
INA_3	O_R3	
INA_2	O_R2	
INA_1	O_R1	
INA_0	O_R0	LSB
INA_24	O_G7	MSB
INA_23	O_G6	
INA_11	O_G5	
INA_10	O_G4	
INA_9	O_G3	
INA_8	O_G2	
INA_7	O_G1	
INA_6	O_G0	LSB
INA_26	O_B7	MSB
INA_25	O_B6	
INA_17	O_B5	
INA_16	O_B4	
INA_15	O_B3	
INA_14	O_B2	
INA_13	O_B1	
INA_12	O_B0	
INB_22	E_R7	
INB_21	E_R6	
INB_5	E_R5	
INB_4	E_R4	
INB_3	E_R3	
INB_2	E_R2	
INB_1	E_R1	
INB_0	E_R0	
INB_24	E_G7	
INB_23	E_G6	
INB_11	E_G5	
INB_10	E_G4	
INB_9	E_G3	
INB_8	E_G2	
INB_7	E_G1	
INB_6	E_G0	
INB_26	E_B7	
INB_25	E_B6	
INB_17	E_B5	
INB_16	E_B4	
INB_15	E_B3	
INB_14	E_B2	
INB_13	E_B1	
INB_12	E_B0	
DE	DE	Data Enable*
VS	VS	Vertical Sync

表 9. Dual Pixel Input / 24bpp (接下页)

DS90C187 Input	Color Mapping	Note
HS	HS	Horizontal Sync
INA_27	GP	General Purpose
INB_27	GP	General Purpose

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS90C187 is a Low Power Bridge for automotive application that reduces the size of the RGB interface between the host GPU and the Display. It is designed to support single pixel data transmission between Host and Flat Panel Display up to QXGA (2048x1536) at 60 Hz resolutions. The transmitter converts up to 24 bits (Single Pixel 24 bit color) of 1.8-V LVCMOS data into two channels of 4 data + clock (4D+C) reduced width interface LVDS compatible data streams.

9.2 Typical Application

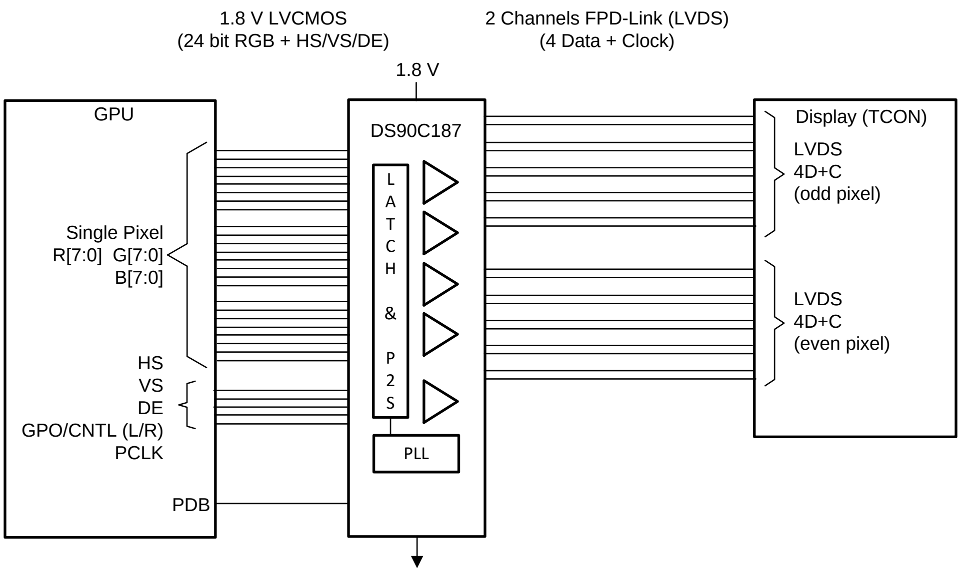


图 18. Single Pixel In Dual Pixel Out (SIDO) Mode

9.2.1 Design Requirements

The DS90C187 is used to convert 24-bit color to two channels of LVDS datastreams.

表 10. Design Parameters

DESIGN PARAMETER	VALUE
Supply	1.8V
Display Driven	SXGA+, WUXGA+
Pixel Depth	24 bits

9.2.2 Detailed Design Procedure

9.2.2.1 LVDS Interconnect Guidelines

Refer to the *AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008) and *Transmission Line RAPIDESIGNER Operation and Applications Guide* (SNLA035) for full details.

- Use 100-Ω coupled differential pairs
- Use differential connectors when above 500 Mbps
- Minimize skew within the pair
- Use the S/2S/3S rule in spacings
  - S = space between the pairs
  - 2S = space between pairs
  - 3S = space to LVCMOS signals
- Place ground vias next to signal vias when changing between layers
- When a signal changes reference planes, place a bypass cap and vias between the new and old reference plane

For more tips and detailed suggestions regarding high speed board layout principles, see the LVDS Owner's Manual at http://www.ti.com/lvds

9.2.3 Application Curves

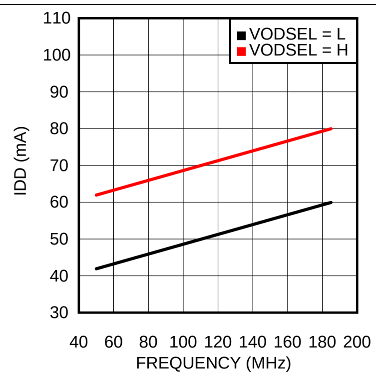


图 19. Typical Current Draw - Single In/Dual Out Mode - PRBS-7 Data Pattern

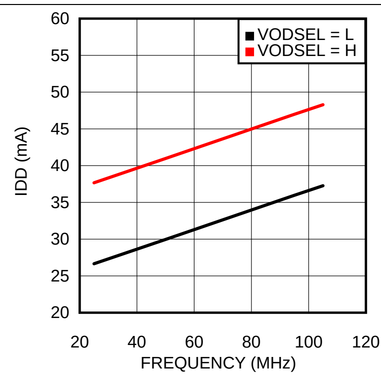


图 20. Typical Current Draw - Single In/Single Out Mode - PRBS-7 Data Pattern

10 Power Supply Recommendations

10.1 Power Up Sequence

The V_{DD} power supply pins do not require a specific power on sequence and can be powered on in any order. However, the PDB pin should only be set to logic HIGH once the power sent to all supply pins is stable. Active data inputs should not be applied to the DS90C187 until all of the input power pins have been powered on, settled to the recommended operating voltage and the PDB pin has be set to logic HIGH.

The user experience can be impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended:

Power up sequence (DS90C187 PDB input initially LOW):

1. Ramp up LCD power (maybe 0.5ms to 10ms) but keep backlight turned off.
2. Toggle DS90C187 power down pin to PDB = V_{DD}.
3. Enable clock and wait for additional 0-200ms to ensure display noise won't occur.
4. Enable video source output; start sending black video data.
5. Send >1ms of black video data; this allows the DS90C187 to be phase locked, and the display to show black data first.
6. Start sending true image data.
7. Enable backlight.

Power Down sequence (DS90C187 PDB input initially HIGH):

1. Disable LCD backlight; wait for the minimum time specified in the LCD data sheet for the backlight to go low.
2. Video source output data switch from active video data to black image data (all visible pixel turn black); drive this for >2 frame times.
3. Set DS90C187 power down pin to PDB = GND.
4. Disable the video output of the video source.
5. Remove power from the LCD panel for lowest system power.

The DS90C187 is highly sensitive to the VDD input. Even small levels on the VDD pin prior to full power up should be avoided. The user should additionally take care to not drive or pull up the CMOS inputs to the device prior to device power up so as to ensure proper power on behavior.

10.2 Power Supply Filtering

The DS90C187 has several power supply pins at 1.8 V. It is important that these pins all be connected and properly bypassed. Bypassing should consist of at least one 0.1μF capacitor placed on each pin, with an additional 4.7 μF - 22 μF capacitor placed on the PLL supply pin (VDDP). 0.01 μF capacitors are typically recommended for each pin. Additional filtering including ferrite beads may be necessary for noisy systems. It is recommended to place a 0 ohm resistor at the bypass capacitors that connect to each power pin to allow for additional filtering if needed. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50 μF — 100 μF range.

11 Layout

11.1 Layout Guidelines

Circuit board layout and stack-up for the LVDS devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. This practice is easier to implement in dense pcbs with many layers and may not be practical in simpler boards. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with vias on both ends of the capacitor.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency. Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

For more information on the VQFN package, refer to the *AN-1187 Leadless Leadframe Package (LLP)* application note (SNOA401).

11.2 Layout Example

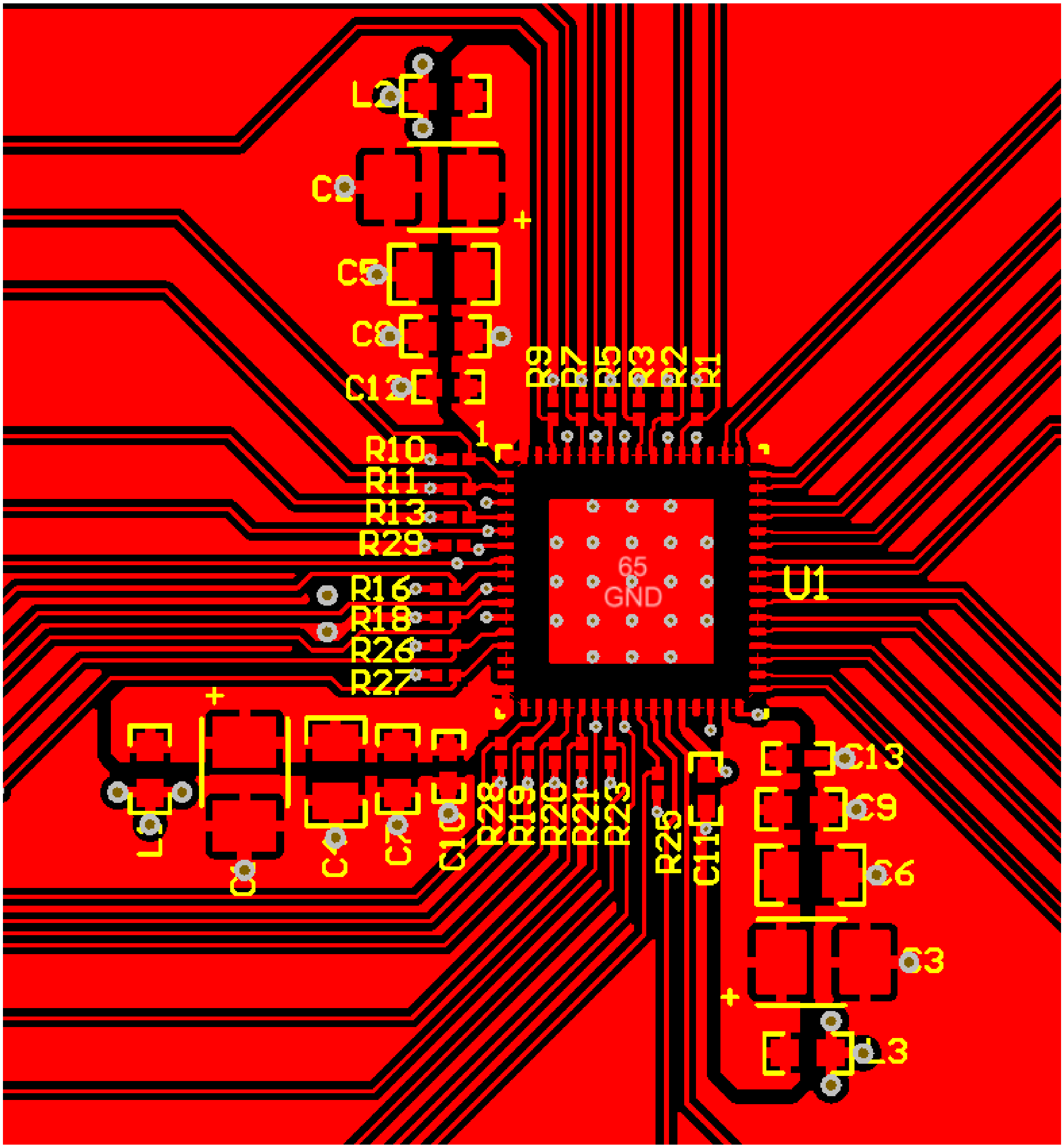


图 21. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- *《LVDS 用户手册》*(SNLA187)
- *《AN-1108 通道链路 PCB 和互连设计指南》*(SNLA008)
- *《传输线路 RAPIDESIGNER 操作和 应用 指南》*(SNLA035)
- *《AN-1187 无引线框架封装 (LLP)》*(SNOA401)

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。***此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90C187LF/NOPB	ACTIVE	VQFN-MR	NLA	92	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-10 to 70	90C187LF	Samples
DS90C187LFE/NOPB	ACTIVE	VQFN-MR	NLA	92	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-10 to 70	90C187LF	Samples
DS90C187LFX/NOPB	ACTIVE	VQFN-MR	NLA	92	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-10 to 70	90C187LF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

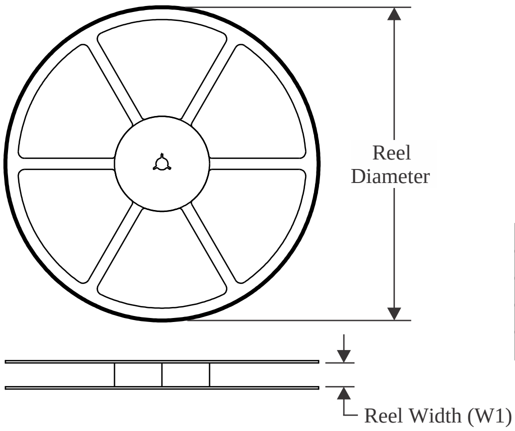
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

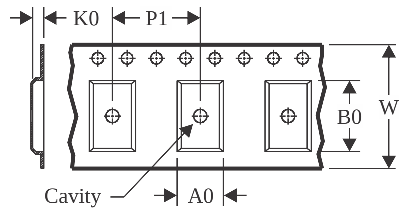
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

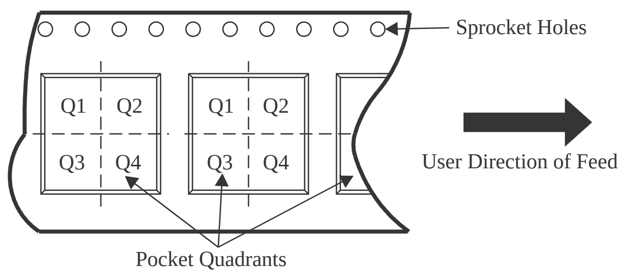


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

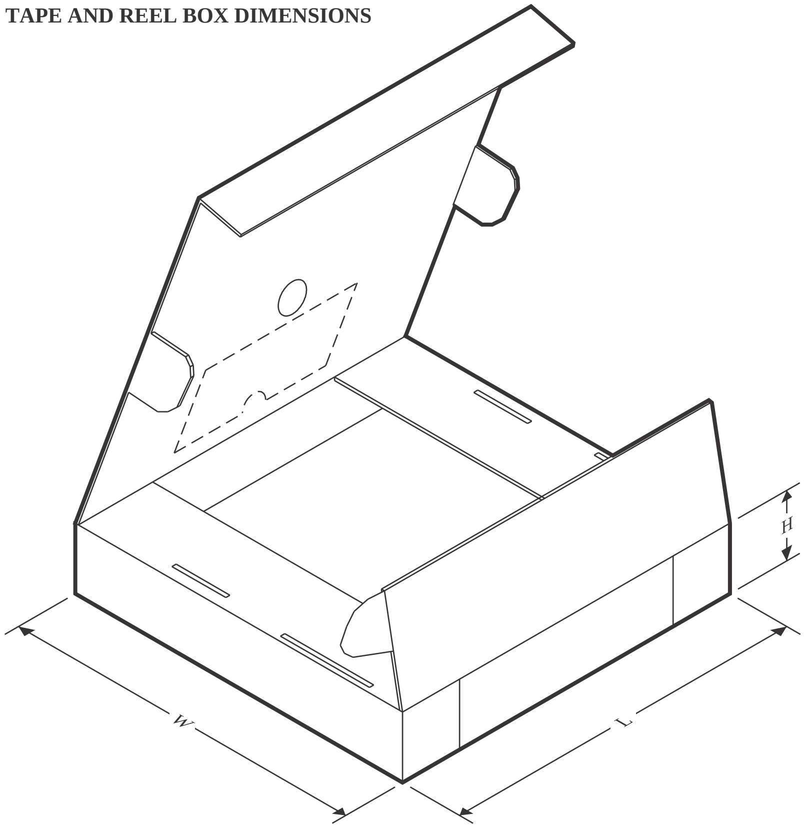
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90C187LF/NOPB	VQFN-MR	NLA	92	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90C187LFE/NOPB	VQFN-MR	NLA	92	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90C187LFX/NOPB	VQFN-MR	NLA	92	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

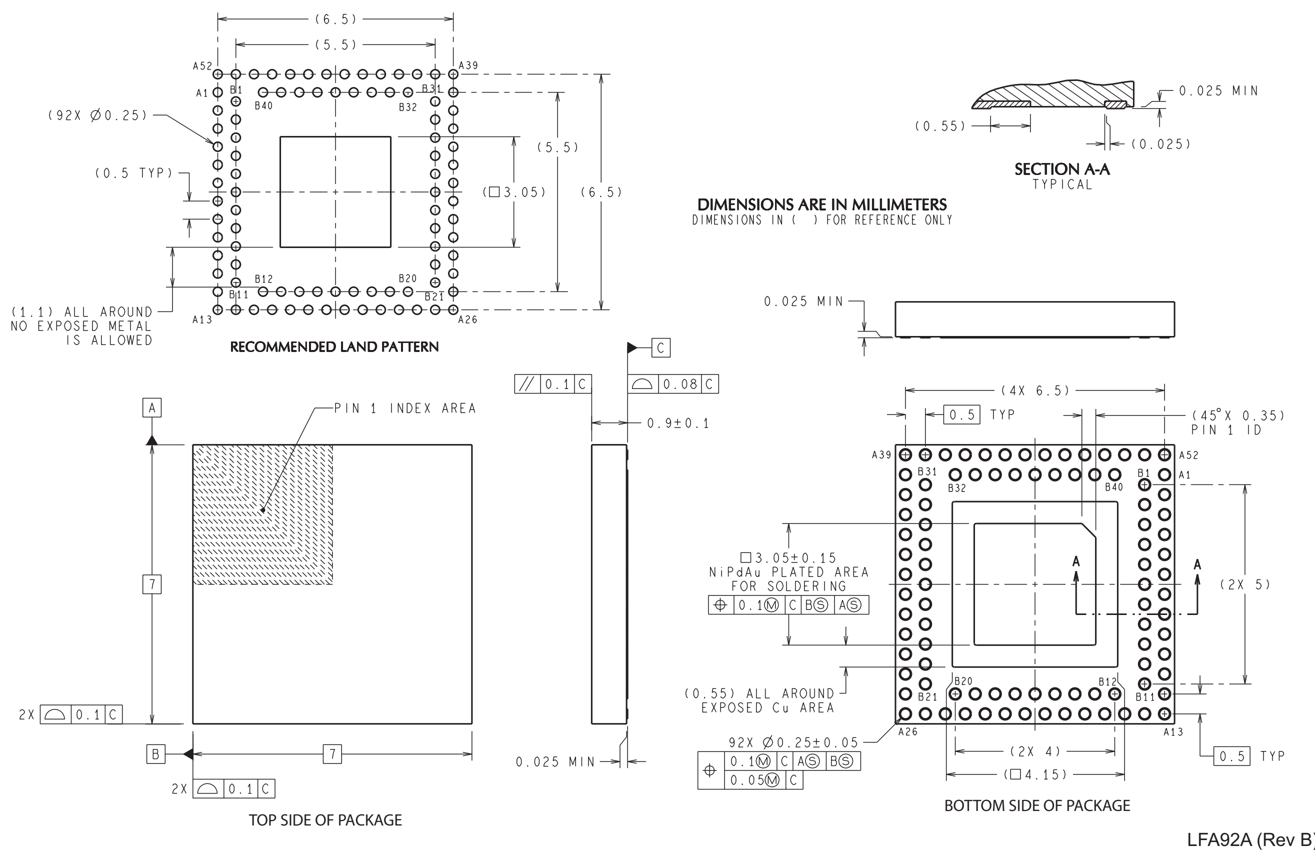
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90C187LF/NOPB	VQFN-MR	NLA	92	1000	356.0	356.0	36.0
DS90C187LFE/NOPB	VQFN-MR	NLA	92	250	208.0	191.0	35.0
DS90C187LFX/NOPB	VQFN-MR	NLA	92	2500	356.0	356.0	36.0

NLA0092A



(6.5)
(5.5)
(92X Ø0.25)
(0.5 TYP)
(□3.05)
(5.5)
(6.5)
(1.1) ALL AROUND NO EXPOSED METAL IS ALLOWED
RECOMMENDED LAND PATTERN
SECTION A-A
TYPICAL
0.025 MIN
(0.55)
(0.025)
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
PIN 1 INDEX AREA
0.9±0.1
0.025 MIN
TOP SIDE OF PACKAGE
(4X 6.5)
0.5 TYP
(45° X 0.35) PIN 1 ID
□3.05±0.15 NiPdAu PLATED AREA FOR SOLDERING
(2X 5)
(0.55) ALL AROUND EXPOSED Cu AREA
92X Ø0.25±0.05
(2X 4)
(□4.15)
BOTTOM SIDE OF PACKAGE
LFA92A (Rev B)

重要声明和免责声明