LM9036Q Ultra-Low Quiescent Current Voltage Regulator

Check for Samples: LM9036Q

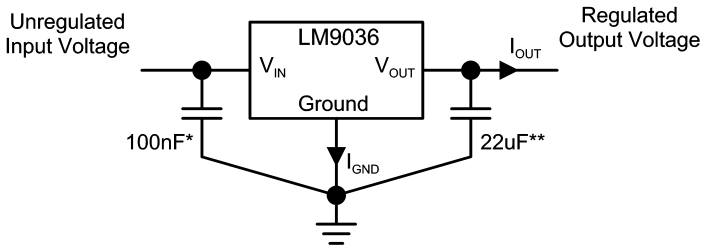
FEATURES

- **AEC-Q100 Grade 1 Qualified (-40°C to 125°C)**
- **Ultra Low Ground Pin Current (I_{GND} ≤ 25µA for I_{OUT} = 0.1mA)**
- **Fixed 5V, 3.3V, 50mA Output**
- **Output Tolerance ±5% Over Line, Load, and Temperature**
- **Dropout Voltage Typically 200mV @ I_{OUT} = 50mA**
- **−45V Reverse Transient Protection**
- **Internal Short Circuit Current Limit**
- **Internal Thermal Shutdown Protection**
- **40V Operating Voltage Limit**

DESCRIPTION

The LM9036Q ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 25µA Ground Pin current at a 0.1mA load, the LM9036Q is ideally suited for automotive and other battery operated systems. The LM9036Q retains all of the features that are common to low dropout regulators including a low dropout PNP pass device, short circuit protection, reverse battery protection, and thermal shutdown. The LM9036Q has a 40V maximum operating voltage limit, a −40°C to +125°C operating temperature range, and ±5% output voltage tolerance over the entire output current, input voltage, and temperature range.

Typical Application



* Required if regulator is located more than 2″ from power supply filter capacitor.

** Required for stability. Must be rated over intended operating temperature range. Effective series resistance (ESR) is critical, see Electrical Characteristics. Locate capacitor as close as possible to the regulator output and ground pins. Capacitance may be increased without bound.

Connection Diagram

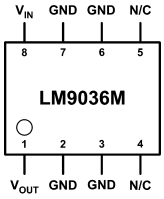


Figure 1. See Package Number D0008A
Top View

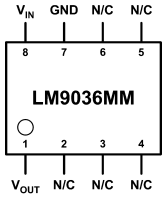


Figure 2. See Package Number DGK0008A
Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Input Voltage (Survival)	+55V, −45V
ESD Susceptibility (3)	±1.9kV
Power Dissipation (4)	Internally limited
Junction Temperature (T_{Jmax})	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 100pF discharge through a 1.5kΩ resistor.
(4) The maximum power dissipation is a function of T_{Jmax}, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM9036Q will go into thermal shutdown.

Operating Ratings

Operating Temperature Range	−40°C to +125°C
Maximum Input Voltage (Operational)	40V
SOIC-8 (D0008A) θ_{JA} (1)(2)	140°C/W
SOIC-8 (D0008A) θ_{JC}	45°C/W
VSSOP-8 (DGK0008A) θ_{JA} (1)	200°C/W

(1) Typical θ_{JA} with 1 square inch of 2 oz. copper pad area directly under the ground tab.
(2) Worst case (Free Air) per EIA / JESD51-3.

Electrical Characteristics - LM9036Q-5.0

V_{IN} = 14V, I_{OUT} = 10 mA, T_J = 25°C, unless otherwise specified. **Boldface** limits apply over entire operating temperature range

Parameter	Conditions	Min (1)	Typical (2)	Max (1)	Units
Output Voltage (V_{OUT})		4.80	5.00	5.20	V
	5.5V ≤ V_{IN} ≤ 26V, 0.1mA ≤ I_{OUT} ≤ 50mA (3)	**4.75**	**5.00**	**5.25**	
Quiescent Current (I_{GND})	I_{OUT} = 0.1mA, 8V ≤ V_{IN} ≤ 24V		20	25	µA
	I_{OUT} = 1mA, 8V ≤ V_{IN} ≤ 24V		50	100	
	I_{OUT} = 10mA, 8V ≤ V_{IN} ≤ 24V		0.3	0.5	mA
	I_{OUT} = 50mA, 8V ≤ V_{IN} ≤ 24V		2.0	2.5	
Line Regulation (Δ V_{OUT})	6V ≤ V_{IN} ≤ 40V, I_{OUT} = 1mA		10	30	mV
Load Regulation (Δ V_{OUT})	0.1mA ≤ I_{OUT} ≤ 5mA		10	30	mV
	5mA ≤ I_{OUT} ≤ 50mA		10	30	mV
Dropout Voltage (Δ V_{OUT})	I_{OUT} = 0.1mA		0.05	0.10	V
	I_{OUT} = 50mA		0.20	0.40	V
Short Circuit Current (I_{SC})	V_{OUT} = 0V	65	120	250	mA
Ripple Rejection (PSRR)	V_{ripple} = 1V_{rms}, F_{ripple} = 120Hz	−40	−60		dB
Output Bypass Capacitance (C_{OUT})	0.3Ω ≤ ESR ≤ 8Ω 0.1mA ≤ I_{OUT} ≤ 50mA	10	22		µF

(1) Tested limits are specified to AOQL (Average Outgoing Quality Level) and 100% tested.
(2) Typicals are at 25°C (unless otherwise specified) and represent the most likely parametric norm.
(3) To ensure constant junction temperature, pulse testing is used.

Electrical Characteristics - LM9036Q-3.3

V_{IN} = 14V, I_{OUT} = 10 mA, T_J = 25°C, unless otherwise specified. **Boldface** limits apply over entire operating temperature range

Parameter	Conditions	Min (1)	Typical (2)	Max (1)	Units
Output Voltage (V_{OUT})		3.168	3.30	3.432	V
	5.5V ≤ V_{IN} ≤ 26V, 0.1mA ≤ I_{OUT} ≤ 50mA (3)	**3.135**	**3.30**	**3.465**	
Quiescent Current (I_{GND})	I_{OUT} = 0.1mA, 8V ≤ V_{IN} ≤ 24V		20	25	µA
	I_{OUT} = 1mA, 8V ≤ V_{IN} ≤ 24V		50	100	
	I_{OUT} = 10mA, 8V ≤ V_{IN} ≤ 24V		0.3	0.5	mA
	I_{OUT} = 50mA, 8V ≤ V_{IN} ≤ 24V		2.0	2.5	
Line Regulation (Δ V_{OUT})	6V ≤ V_{IN} ≤ 40V, I_{OUT} = 1mA		10	30	mV
Load Regulation (Δ V_{OUT})	0.1mA ≤ I_{OUT} ≤ 5mA		10	30	mV
	5mA ≤ I_{OUT} ≤ 50mA		10	30	mV
Dropout Voltage (Δ V_{OUT})	I_{OUT} = 0.1mA		0.05	0.10	V
	I_{OUT} = 50mA		0.20	0.40	V
Short Circuit Current (I_{SC})	V_{OUT} = 0V	65	120	250	mA
Ripple Rejection (PSRR)	V_{ripple} = 1V_{rms}, F_{ripple} = 120Hz	−40	−60		dB
Output Bypass Capacitance (C_{OUT})	0.3Ω ≤ ESR ≤ 8Ω 0.1mA ≤ I_{OUT} ≤ 50mA	22	33		µF

(1) Tested limits are specified to AOQL (Average Outgoing Quality Level) and 100% tested.
(2) Typicals are at 25°C (unless otherwise specified) and represent the most likely parametric norm.
(3) To ensure constant junction temperature, pulse testing is used.

Typical Performance Characteristics

Dropout Voltage

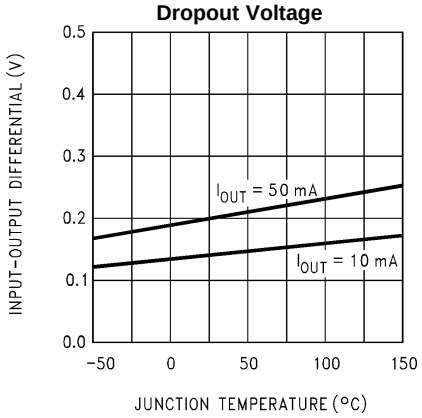


Figure 3.

Quiescent Current

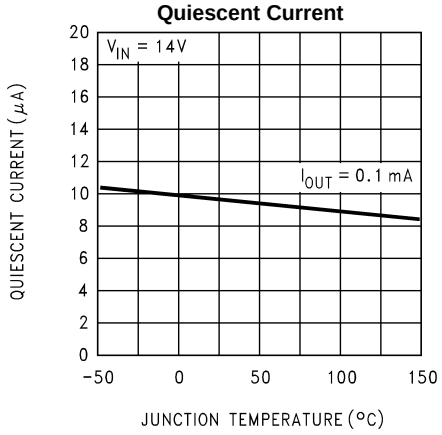


Figure 4.

Quiescent Current

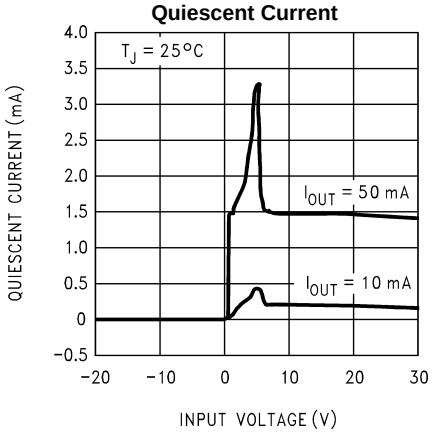


Figure 5.

Quiescent Current

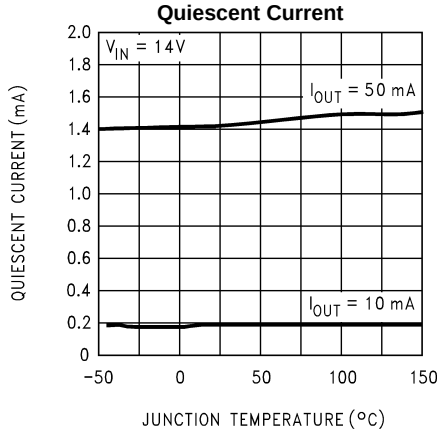


Figure 6.

Peak Output Current

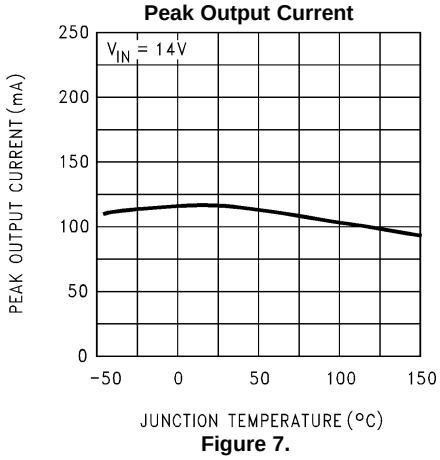


Figure 7.

APPLICATIONS INFORMATION

Unlike other PNP low dropout regulators, the LM9036Q remains fully operational to 40V. Owing to power dissipation characteristics of the package, full output current cannot be ensured for all combinations of ambient temperature and input voltage.

The junction to ambient thermal resistance θ_{JA} rating has two distinct components: the junction to case thermal resistance rating θ_{JC}; and the case to ambient thermal resistance rating θ_{CA}. The relationship is defined as: $\theta_{JA} = \theta_{JC} + \theta_{CA}$.

While the LM9036Q has an internally set thermal shutdown point of typically 150°C, this is intended as a safety feature only. Continuous operation near the thermal shutdown temperature should be avoided as it may have a negative affect on the life of the device.

The LM9036Q maintains regulation to 55V, it will not withstand a short circuit above 40V because of safe operating area limitations in the internal PNP pass device. Above 55V the LM9036Q will break down with catastrophic effects on the regulator and possibly the load as well. Do not use this device in a design where the input operating voltage may exceed 40V, or where transients are likely to exceed 55V.

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	5

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM9036QM-3.3/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6QM-3
LM9036QM-3.3/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6QM-3
LM9036QM-5.0/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6QM-5
LM9036QM-5.0/NOPB.B	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6QM-5
LM9036QMM-3.3/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	KDBQ
LM9036QMM-3.3/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	KDBQ
LM9036QMM-5.0/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	KDAQ
LM9036QMM-5.0/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	KDAQ
LM9036QMMX-3.3/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	KDBQ
LM9036QMMX-5.0/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	KDAQ
LM9036QMX-3.3/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6QM-3
LM9036QMX-3.3/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6QM-3
LM9036QMX-5.0/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6QM-5
LM9036QMX-5.0/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6QM-5

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

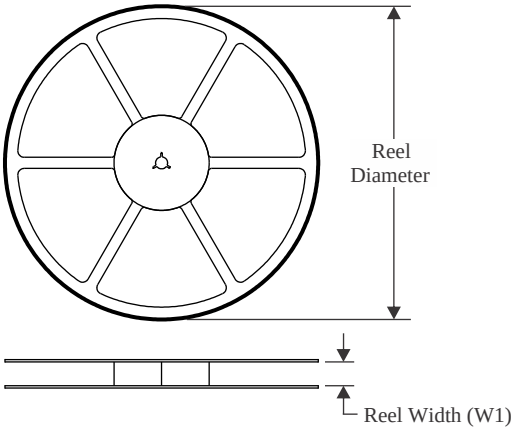
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

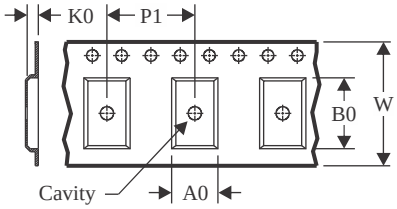
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

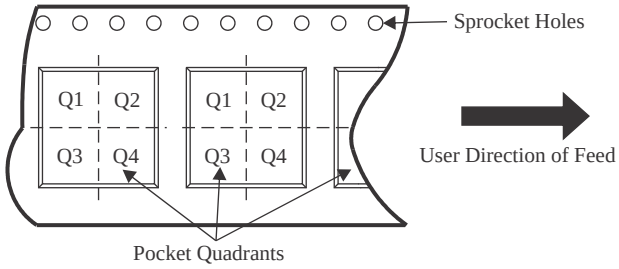


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

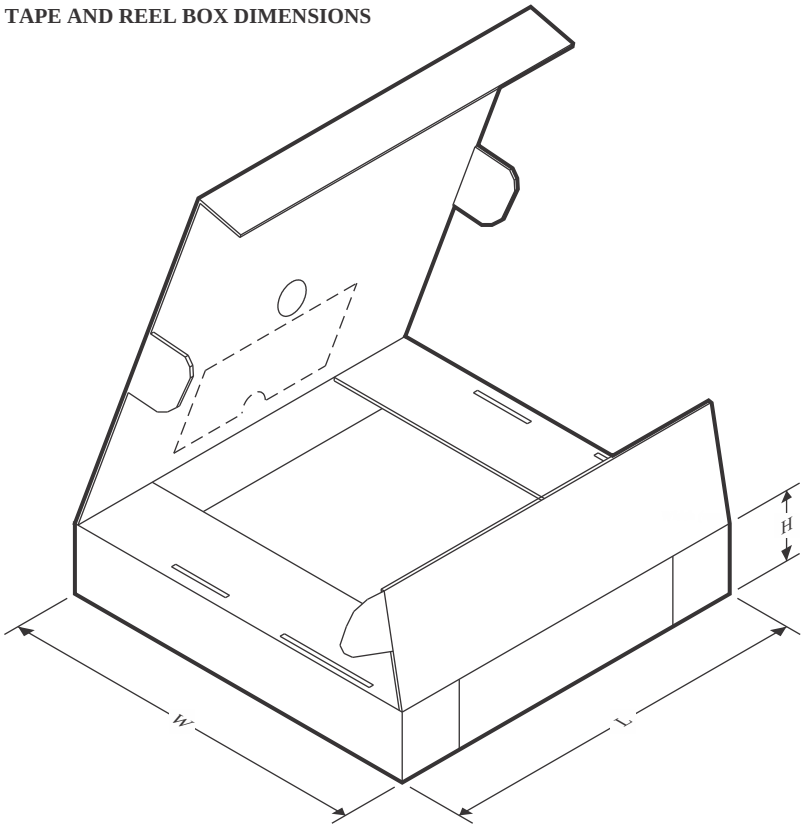
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM9036QMM-3.3/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036QMM-5.0/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036QMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036QMMX-5.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036QMX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM9036QMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

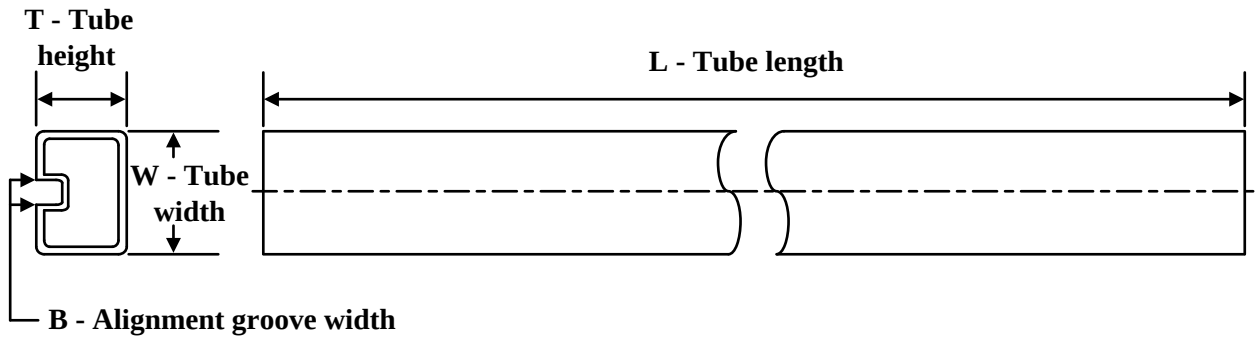
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM9036QMM-3.3/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM9036QMM-5.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM9036QMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM9036QMMX-5.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM9036QMX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM9036QMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

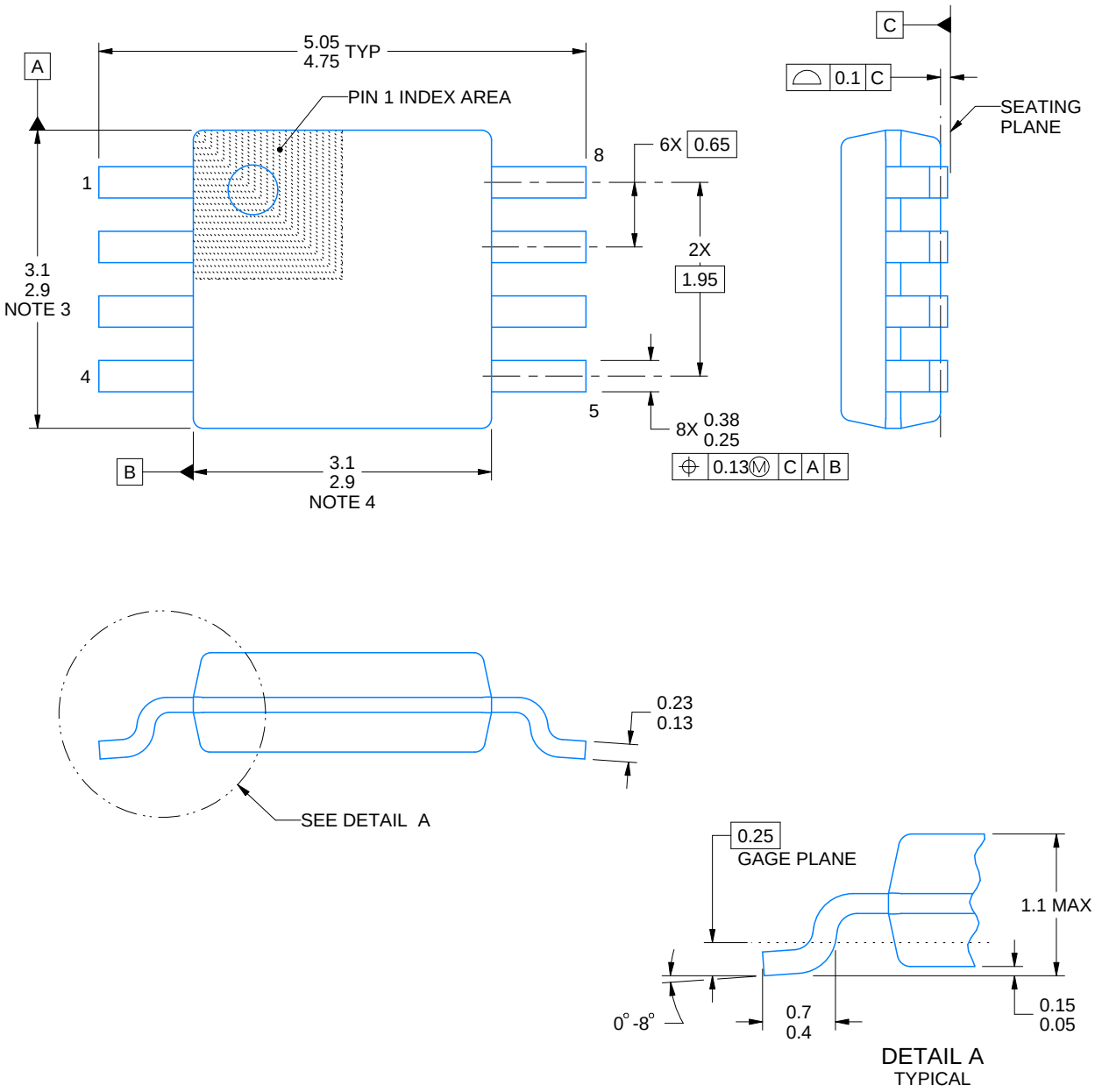
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM9036QM-3.3/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM9036QM-3.3/NOPB.B	D	SOIC	8	95	495	8	4064	3.05
LM9036QM-5.0/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM9036QM-5.0/NOPB.B	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

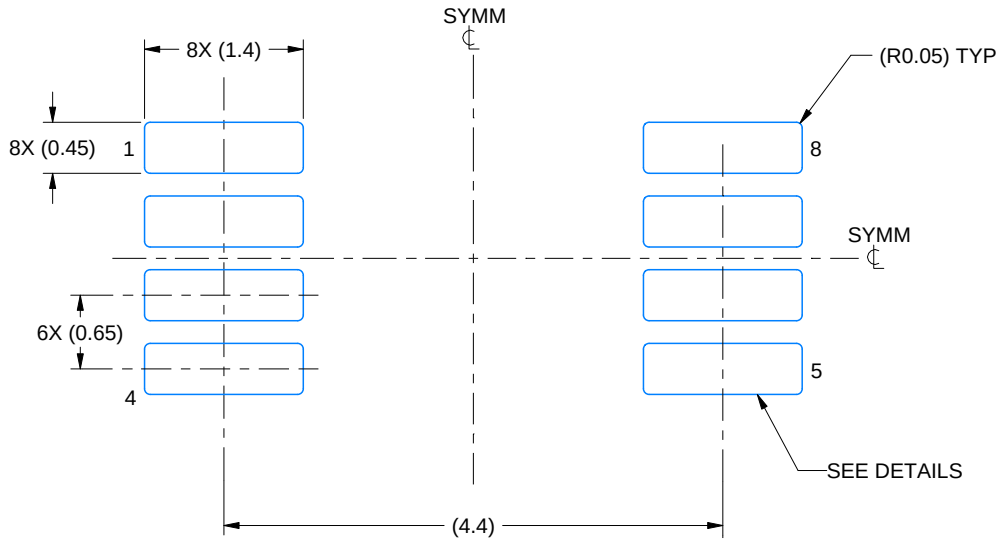
SMALL OUTLINE PACKAGE



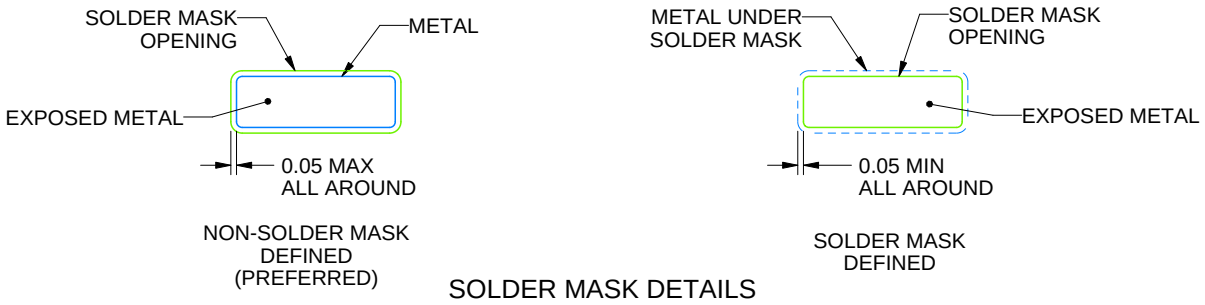
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

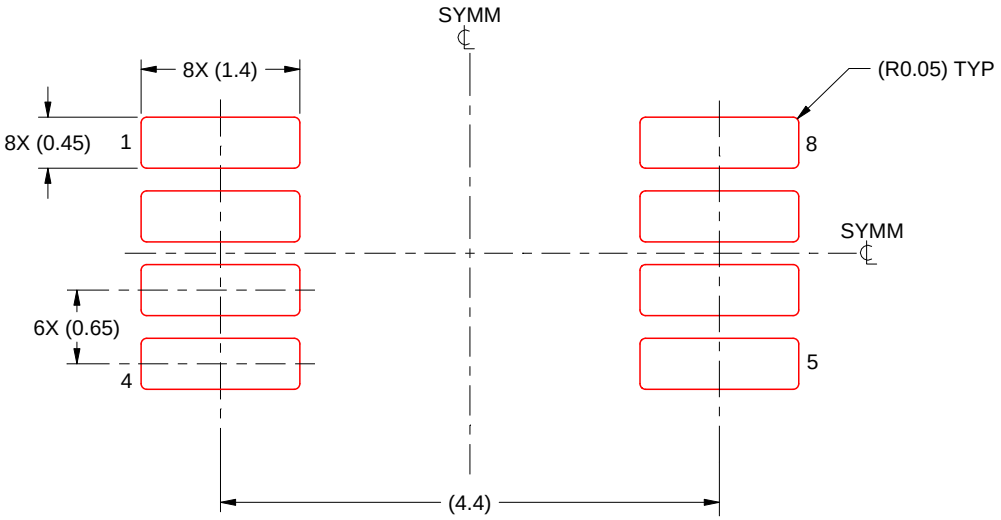


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

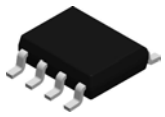


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

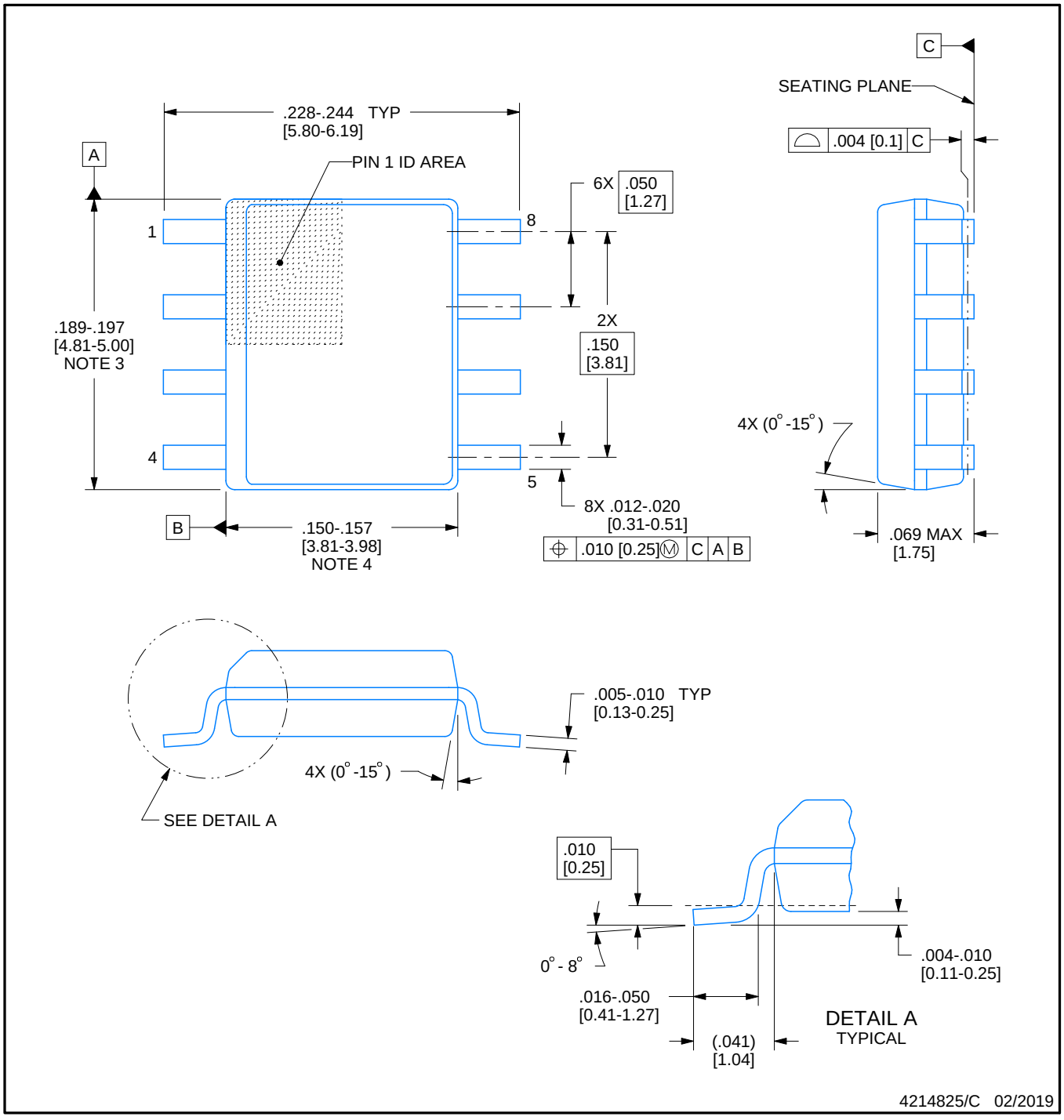


PACKAGE OUTLINE

D0008A

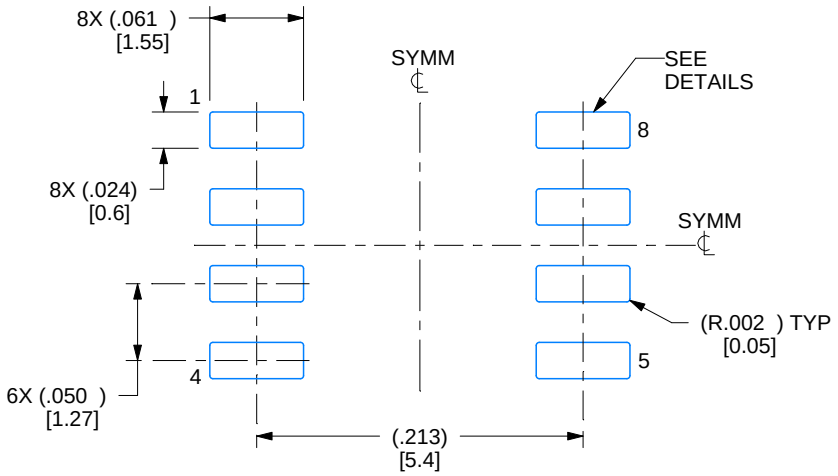
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

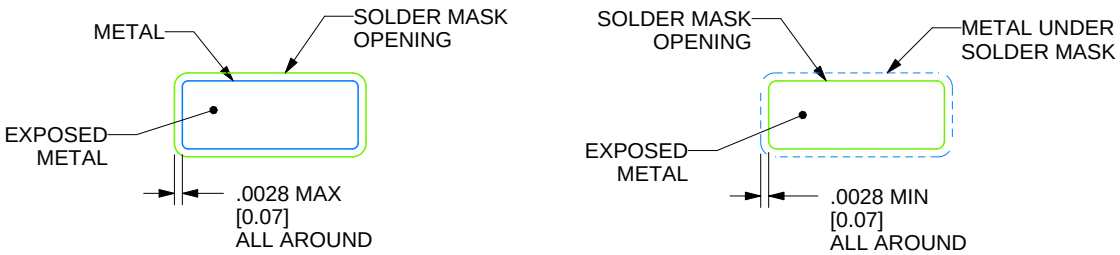


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

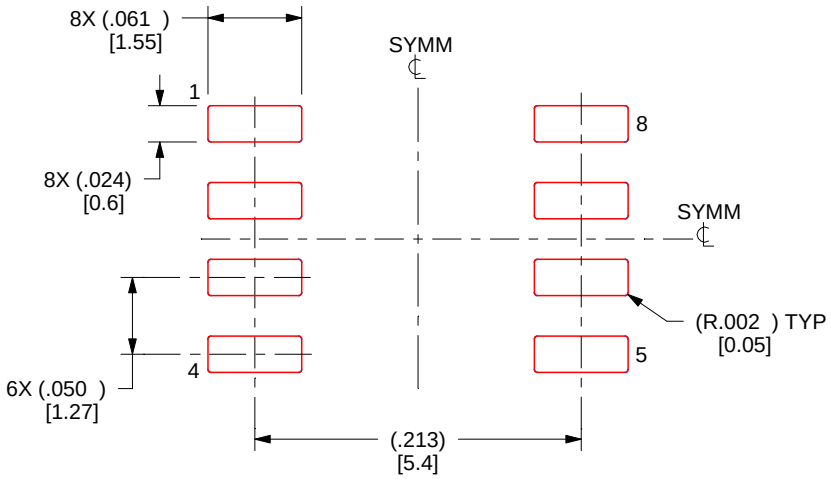
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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