

## LMC603x CMOS 双通道运算放大器

### 1 特性

- 适用于  $2k\Omega$  和  $600\Omega$  负载
- 高压增益：126dB,  $2k\Omega$
- 低失调电压漂移： $2.3\mu V/^\circ C$
- 超低输入偏置电流：40fA
- 输入共模范围包括  $V^-$
- 可由标准 5V 和 15V 电源供电
- $I_Q = 375\mu A$ /放大器；与  $V^+$  无关
- 低噪声： $22nV/\sqrt{Hz}$
- 压摆率： $1.1V/\mu s$
- 性能优于 TLC272

### 2 应用

- 高阻抗缓冲器或前置放大器
- 电流/电压转换器
- 长期积分器
- 采样保持电路
- 医疗仪器

### 3 说明

双通道 LMC6032 和四通道 LMC6034 (LMC603x) 是 CMOS 运算放大器，可由单电源或双电源供电。器件性能特性包括输入共模范围（包括接地）、低输入偏置电流以及为实际负载（例如  $2k\Omega$  和  $600\Omega$ ）提供的高压增益。

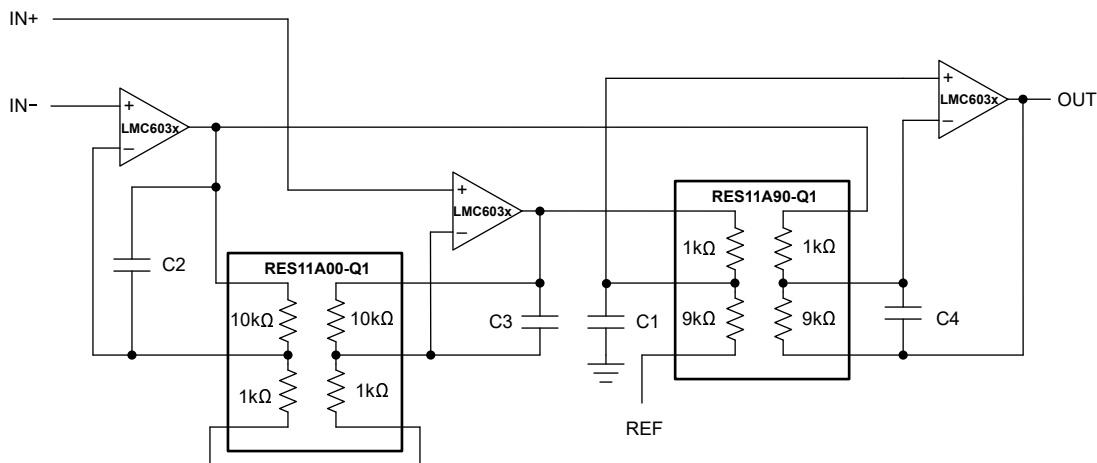
该芯片采用 TI 先进的 CMOS 工艺制造而成。

有关更高性能特性，请参阅 OPA928。

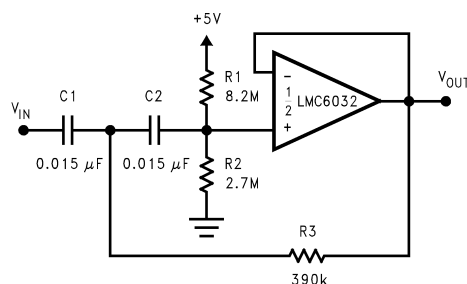
#### 器件信息

器件型号	通道	封装 <sup>(1)</sup>
LMC6032	双	D (SOIC, 8)
		P (PDIP, 8)
LMC6034	四通道	D (SOIC, 14)
		P (PDIP, 14)

(1) 如需更多信息，请参阅节 9。



典型应用：仪表放大器和 RES11A



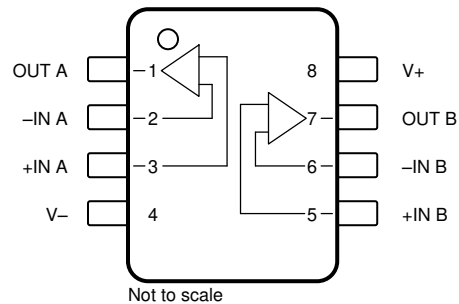
典型应用：10Hz 高通滤波器



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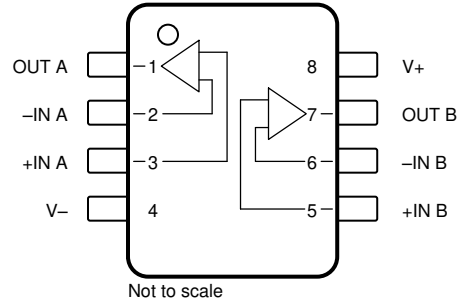
## 4 Pin Configuration and Functions



LMC6032 D Package, 8-Pin SOIC, and P Package, 8-Pin PDIP (Top View)

表 4-1. Pin Functions: LMC6032

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
- IN A	2	Input	Inverting input, channel A
+IN B	5	Input	Noninverting input, channel B
- IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V -	4	Power	Negative (lowest) power supply



**LMC6034 D Package, 14-Pin SOIC, and P Package, 14-Pin PDIP (Top View)**

**表 4-2. Pin Functions: LMC6034**

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
- IN A	2	Input	Inverting input, channel A
- IN B	6	Input	Inverting input, channel B
- IN C	9	Input	Inverting input, channel C
- IN D	13	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V+	4	Power	Positive (highest) power supply
V-	11	Power	Negative (lowest) power supply

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		MIN	MAX	UNIT
Differential input voltage		±Supply voltage		V
Supply voltage, $V_S = (V+) - (V-)$	Single supply	0	16	V
	Dual supply		±8	
Output short circuit	To V+		See <sup>(2)</sup>	mA
	To V-		See <sup>(3)</sup>	
Signal input pins	Voltage	(V-) - 0.3	(V+) + 0.3	V
	Current		±5	mA
Output pin current			±18	mA
Power supply pin	Current		35	mA
Power dissipation		See <sup>(4)</sup>		
Temperature	Operating, $T_A$	- 40	150	°C
	Junction, $T_J$		150	
	Storage, $T_{stg}$	- 65	150	
	Lead (soldering, 10 sec.)		260	

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- Do not connect output to V+, when V+ is greater than 13V or reliability will be adversely affected.
- The maximum power dissipation is a function of  $T_{J(max)}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(max)} - T_A) / \theta_{JA}$ .

### 5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V

- JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$	Single supply	4.75		15.5	V
	Dual supply	±2.375		±7.75	
Specified temperature		- 40		85	°C
Power dissipation				See <sup>(2)</sup>	

- Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the *Electrical Characteristics*. The ensured specifications apply only for the test conditions listed.
- For operating at elevated temperatures the device must be derated based on the thermal resistance  $\theta_{JA}$  with  $P_D = (T_J - T_A) / \theta_{JA}$ . All numbers apply for packages soldered directly into a printed circuit board.

### 5.4 Thermal Information LMC6032

THERMAL METRIC <sup>(1)</sup>		LMC6032		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	101	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 5.5 Thermal Information LMC6034

THERMAL METRIC <sup>(1)</sup>		LMC6034		UNIT
		D (SOIC)	P (PDIP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115	85	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.6 Electrical Characteristics

at  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$  ( $V_- = 0\text{V}$ ),  $V_{CM} = 1.5\text{V}$ ,  $V_{OUT} = V_S / 2$ , and  $R_L = 1\text{M}\Omega$  connected to  $V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>							
$V_{OS}$	Input offset voltage				$\pm 1$	$\pm 9$	mV
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$				$\pm 11$	
$dV_{OS}/dT$	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			$\pm 2.3$		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	Positive, $5\text{V} \leq V_+ \leq 15\text{V}$		63	83	dB	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	60			
		Negative, $-5\text{V} \leq V_+ \leq -10\text{V}$		74	94		
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	70			
<b>INPUT BIAS CURRENT</b>							
$I_B$	Input bias current				$\pm 40$		fA
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$				$\pm 200$	pA
$I_{OS}$	Input offset current				$\pm 10$		fA
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$				$\pm 100$	pA
<b>NOISE</b>							
$e_n$	Input voltage noise density	$f = 1\text{kHz}$			22		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input current noise density	$f = 1\text{kHz}$			4		$\text{fA}/\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$f = 10\text{kHz}$ , $G = -10\text{V/V}$ , $R_L = 2\text{k}\Omega$ , $V_O = 8V_{pp}$ , $V_S = \pm 5\text{V}$			0.2		%
<b>INPUT VOLTAGE</b>							
$V_{CM}$	Common-mode voltage range	To positive rail, $5\text{V} \leq V_S \leq 15\text{V}$ , $\text{CMRR} > 50\text{dB}$		$(V_+) - 2.3$	$(V_+) - 1.9$	V	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$(V_+) - 2.6$			
		To negative rail, $5\text{V} \leq V_S \leq 15\text{V}$ , $\text{CMRR} > 50\text{dB}$		$(V_-) - 0.4$	$(V_-) - 0.1$		
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$(V_-)$			
CMRR	Common-mode rejection ratio	$V_S = 15\text{V}$ , $0\text{V} < V_{CM} < 12\text{V}$		63	83	dB	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	60			
<b>INPUT IMPEDANCE</b>							
$R_{IN}$	Input resistance				$> 1$		$\text{T}\Omega$
<b>OPEN-LOOP GAIN</b>							
$A_{OL}$	Open-loop voltage gain	Sourcing, $V_S = 15\text{V}$ , $V_{CM} = 7.5\text{V}$ , $7.5\text{V} < V_O < 11.5\text{V}$ , $R_L = 2\text{k}\Omega$		200	2000	V/mV	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	100			
		Sinking, $V_S = 15\text{V}$ , $V_{CM} = 7.5\text{V}$ , $2.5\text{V} < V_O < 7.5\text{V}$ , $R_L = 2\text{k}\Omega$		90	500		
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	40			
		Sourcing, $V_S = 15\text{V}$ , $V_{CM} = 7.5\text{V}$ , $7.5\text{V} < V_O < 11.5\text{V}$ , $R_L = 600\Omega$		100	1000		
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	75			
		Sinking, $V_S = 15\text{V}$ , $V_{CM} = 7.5\text{V}$ , $2.5\text{V} < V_O < 7.5\text{V}$ , $R_L = 600\Omega$		50	250		
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	20			
<b>FREQUENCY RESPONSE</b>							
GBW	Gain bandwidth product				1.4		MHz
SR	Slew rate <sup>(1)</sup>	$V_S = 15\text{V}$ , $10\text{V}$ step		0.8	1.1	V/ $\mu\text{s}$	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	0.4			
$\theta_m$	Phase margin				50		$^\circ$
	Crosstalk	Dual and quad channel, $V_S = 15\text{V}$ , $R_L = 10\text{k}\Omega$ to $7.5\text{V}$ , $f = 1\text{kHz}$ , $V_O = 13V_{pp}$			130		dB

## 5.6 Electrical Characteristics (续)

at  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$  ( $V_- = 0\text{V}$ ),  $V_{\text{CM}} = 1.5\text{V}$ ,  $V_{\text{OUT}} = V_S / 2$ , and  $R_L = 1\text{M}\Omega$  connected to  $V_S / 2$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
<b>OUTPUT</b>							
$V_O$	Voltage output swing	Positive rail $V_S = 5\text{V}$ , $R_L = 2\text{k}\Omega$ to mid-supply	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4.20	4.87	V	
		Negative rail $V_S = 5\text{V}$ , $R_L = 2\text{k}\Omega$ to mid-supply	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4.00	0.10		0.25
		Positive rail $V_S = 5\text{V}$ , $R_L = 600\Omega$ to mid-supply	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	4.00	4.61		
		Negative rail $V_S = 5\text{V}$ , $R_L = 600\Omega$ to mid-supply	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	3.80	0.30		0.63
		Positive rail $V_S = 15\text{V}$ , $R_L = 2\text{k}\Omega$ to mid-supply	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	13.50	14.63		
		Negative rail $V_S = 15\text{V}$ , $R_L = 2\text{k}\Omega$ to mid-supply	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	13.00	0.26		0.45
		Positive rail $V_S = 15\text{V}$ , $R_L = 600\Omega$ to mid-supply	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	12.50	13.90		
		Negative rail $V_S = 15\text{V}$ , $R_L = 600\Omega$ to mid-supply	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	12.00	0.79		1.45
$I_{\text{SC}}$	Short-circuit current	Sourcing $V_S = 5\text{V}$ , $V_O = 0\text{V}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	13	22	mA	
		Sinking $V_S = 5\text{V}$ , $V_O = 5\text{V}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	9	21		
		Sourcing $V_S = 15\text{V}$ , $V_O = 0\text{V}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	23	40		
		Sinking $V_S = 15\text{V}$ , $V_O = 13\text{V}^{(2)}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	15	39		
<b>POWER SUPPLY</b>							
$I_Q$	Quiescent current per amplifier	$V_O = 1.5\text{V}$	LMC6032	375	800	$\mu\text{A}$	
			LMC6032, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		950		
			LMC6034	375	675		
			LMC6034, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		750		

- Specification limit established from device population bench system measurements across multiple lots. Number specified is the slower of either the positive or negative slew rates.
- Do not connect output to  $V_+$ , when  $V_+$  is greater than 13V or reliability can be adversely affected.

### Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 7.5\text{V}$ ,  $V_{\text{OUT}} = \text{mid-supply}$ , and  $R_L > 1\text{M}\Omega$  (unless otherwise noted)

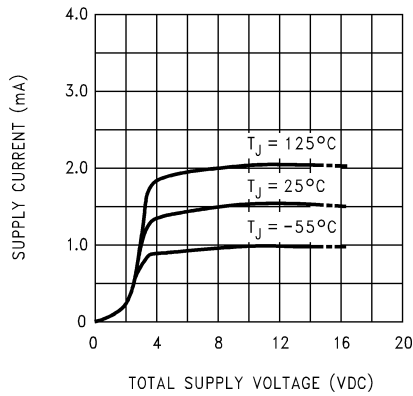


图 5-1. Supply Current vs Supply Voltage

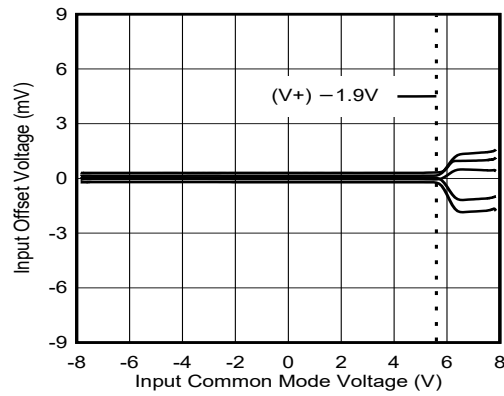


图 5-2. Offset Voltage vs Input Common-Mode Voltage

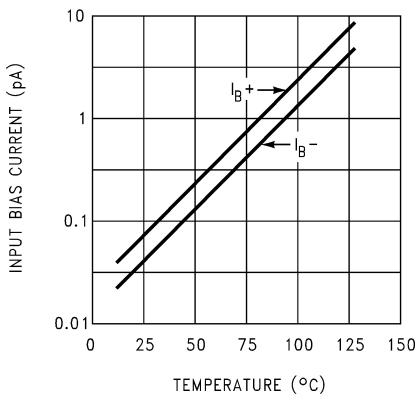


图 5-3. Input Bias Current

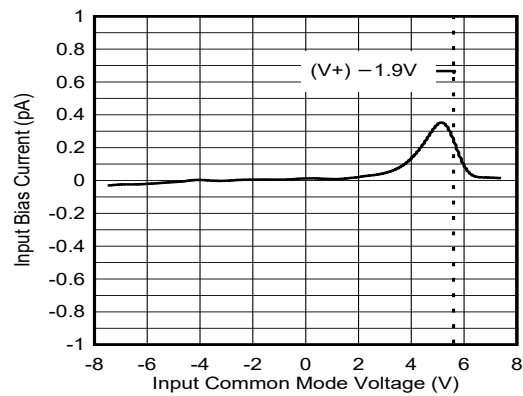


图 5-4. Input Bias Current vs Input Common-Mode Voltage

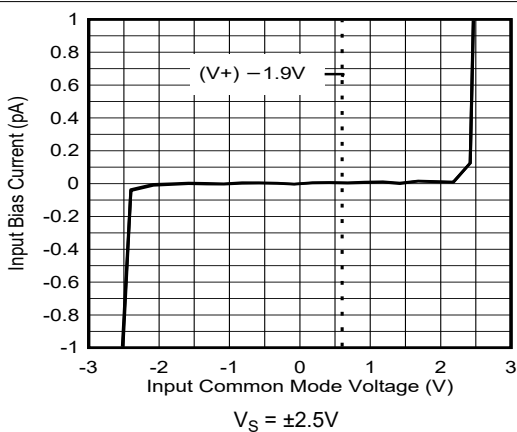


图 5-5. Input Bias Current vs Input Common-Mode Voltage

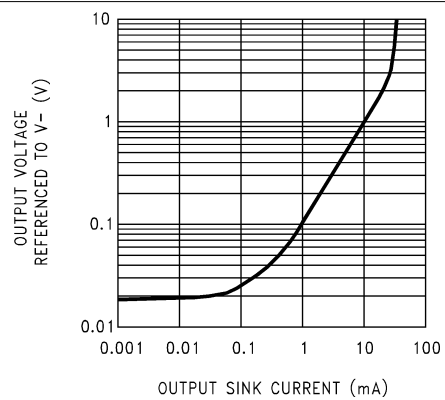


图 5-6. Output Characteristics Current Sinking



### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 7.5\text{V}$ ,  $V_{OUT} = \text{mid-supply}$ , and  $R_L > 1\text{M}\Omega$  (unless otherwise noted)

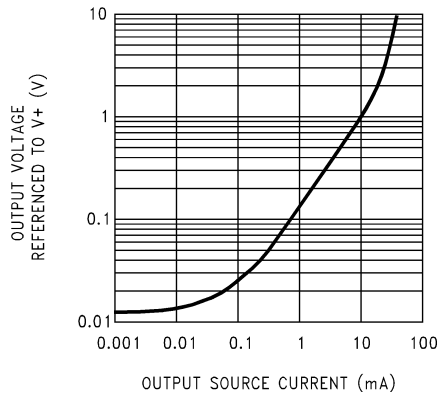


图 5-7. Output Characteristics Current Sourcing

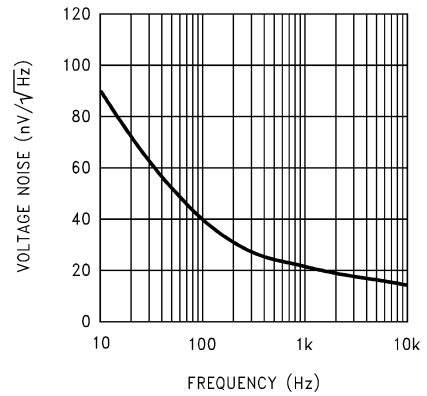


图 5-8. Input Voltage Noise vs Frequency

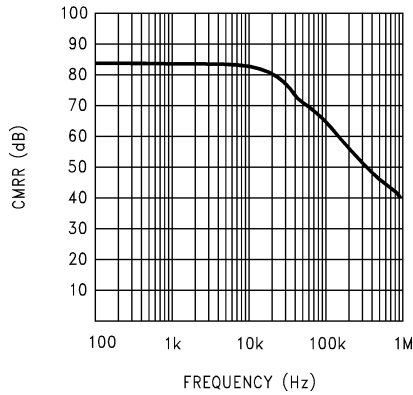


图 5-9. CMRR vs Frequency

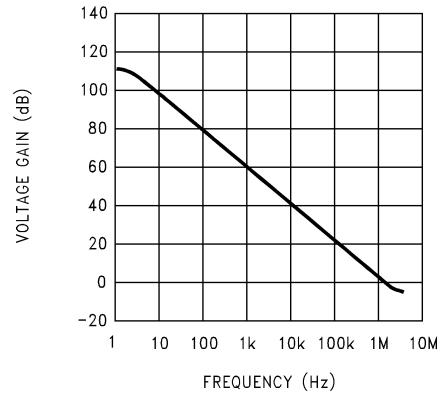


图 5-10. Open-Loop Frequency Response

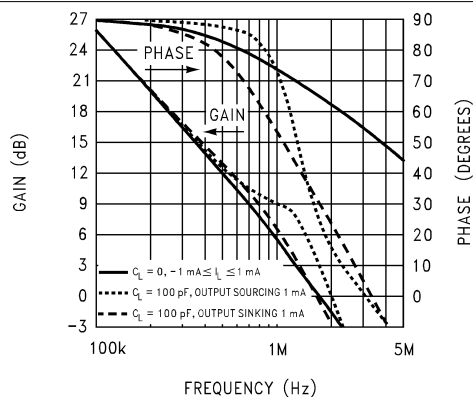


图 5-11. Frequency Response vs Capacitive Load

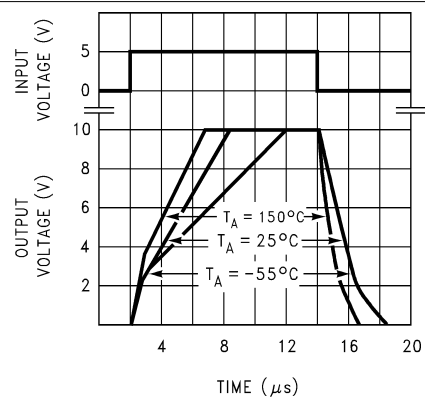


图 5-12. Noninverting Large-Signal Pulse Response

### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 7.5\text{V}$ ,  $V_{OUT} = \text{mid-supply}$ , and  $R_L > 1\text{M}\Omega$  (unless otherwise noted)

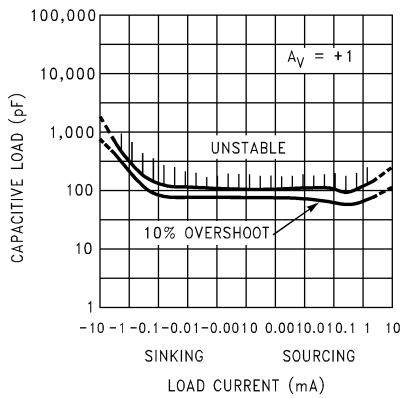


图 5-13. Stability vs Capacitive Load

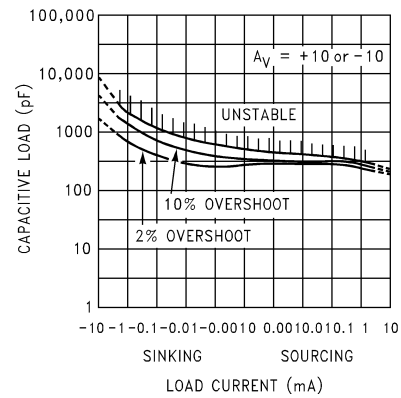


图 5-14. Stability vs Capacitive Load

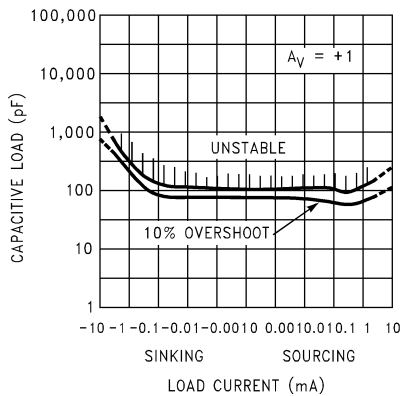
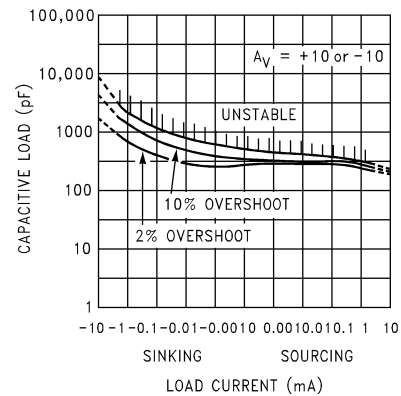


图 5-15. Stability vs Capacitive Load



Avoid resistive loads of less than  $500\Omega$  because these loads can cause instability.

图 5-16. Stability vs Capacitive Load

## 6 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 6.1 Application Information

#### 6.1.1 Amplifier Topology

The topology chosen for the LMC603x, shown in 图 6-1, is unconventional compared to general-purpose op amps. The LMC603x incorporates novel op-amp design that enables a wide input common-mode range and rail-to-rail output swing even when driving a large load. The input common-mode range includes ground, making the LMC603x an excellent choice for single-supply applications. While the LMC603x supports both a wide supply and common-mode voltage range, large input common-mode voltage can cause a degradation of input bias current performance.

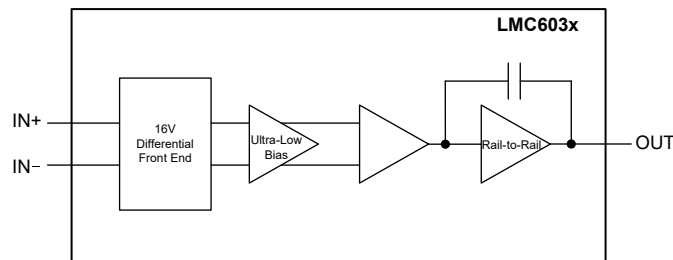


图 6-1. LMC603x Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600 Ω load. The gain while sinking is greater than most CMOS op amps as a result of the additional gain stage; however, under heavy load (600 Ω), the gain can be reduced as indicated in 节 5.6.

#### 6.1.2 Compensating Input Capacitance

The high input resistance of the LMC603x op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit can be especially sensitive to the printed circuit board (PCB) layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and ac ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, and so on) and the feedback resistors create a pole in the feedback path. In 图 6-2, the frequency of this pole is:

$$f_p = \frac{1}{2\pi C_S R_P} \quad (1)$$

where  $C_S$  is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, and so on, and  $R_P$  is the parallel combination of  $R_F$  and  $R_{IN}$ . This formula, as well as all the following formulas, apply to inverting and noninverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole can be quite high, since  $C_S$  is generally less than 10pF. If the frequency of the feedback pole is much greater than the *ideal* closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of  $C_S$ ), the pole has a negligible effect on stability, as only a small amount of phase shift is added.

However, if the feedback pole is less than approximately 6 to 10 times the *ideal* -3dB frequency, add a feedback capacitor,  $C_F$ , between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier low-frequency noise gain: To maintain stability, a feedback capacitor is probably needed if:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S} \quad (2)$$

where

- $\left(\frac{R_F}{R_{IN}} + 1\right)$  is the amplifier low-frequency noise gain.
- GBW is the amplifier gain bandwidth product.

An amplifier low-frequency noise gain is represented by the following formula:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \quad (3)$$

regardless of whether the amplifier is being used in an inverting or noninverting mode. A feedback capacitor is more likely to be needed when the noise gain is low, the feedback resistor is large, or both.

If the previous condition is met (indicating a feedback capacitor is probably be needed), and the noise gain is large enough that  $\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S}$ , the following value of feedback capacitor is recommended:

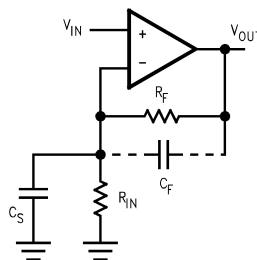
$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)} \quad (4)$$

If  $\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S}$ , the feedback capacitor is:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}} \quad (5)$$

These capacitor values are usually significantly smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F} \quad (6)$$



$C_S$  consists of the amplifier input capacitance plus any stray capacitance from the circuit board and socket.  $C_F$  compensates for the pole caused by  $C_S$  and the feedback resistor.

**图 6-2. General Operational Amplifier Circuit**

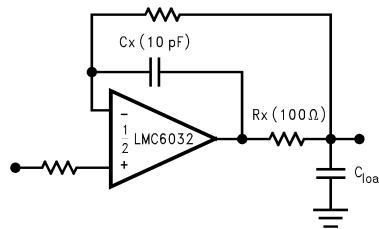
Using the smaller capacitors give much higher bandwidth with little degradation of transient response. Using a somewhat larger feedback capacitor can be necessary in any of the above cases to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the

noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a PCB stray capacitance can be larger or smaller than the breadboard capacitance, so the actual preferred value for  $C_F$  can be different from the one estimated using the breadboard. In most cases, check the value of  $C_F$  on the actual circuit, starting with the computed value.

### 6.1.3 Capacitive Load Tolerance

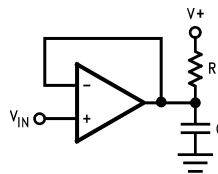
Like many other op amps, the LMC603x can oscillate when applied a load that appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See also [节 Typical Characteristics](#).

The load capacitance interacts with the op amp output resistance to create an additional pole. If this pole frequency is sufficiently low, the op amp phase margin is degraded so that the amplifier is no longer stable at low gains. [图 6-3](#) shows that the addition of a small resistor ( $50\ \Omega$  to  $100\ \Omega$ ) in series with the op amp output, and a capacitor ( $5\text{pF}$  to  $10\text{pF}$ ) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. In all cases, the output can ring heavily when the load capacitance is near the threshold for oscillation.



**图 6-3. Rx, Cx Improve Capacitive Load Tolerance**

Capacitive load driving capability is enhanced by using a pullup resistor to  $V^+$  ([图 6-4](#)). Typically, a pullup resistor conducting  $500\ \mu\text{A}$  or more significantly improves capacitive load responses. The value of the pullup resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. The open-loop gain of the amplifier can also be affected by the pullup resistor (see [节 5.6](#)).



**图 6-4. Compensating for Large Capacitive Loads with a Pullup Resistor**

### 6.1.4 Bias Current Testing

The test method of 图 6-5 is appropriate for bench-testing bias current with reasonable accuracy. To understand the circuit operation, first close switch S2 momentarily. When S2 is opened, then:

$$I_{b-} = \frac{dV_{OUT}}{dt} \times C_2 \quad (7)$$

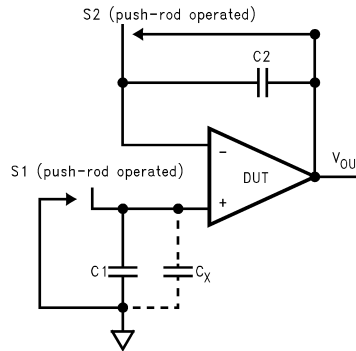


图 6-5. Simple Input Bias Current Test Circuit

A recommended capacitor for C2 is a 5pF or 10pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of  $I_{b-}$ , the leakage of the capacitor and socket must be taken into account. Leave switch S2 shorted most of the time, or else the dielectric absorption of the capacitor C2 can cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted), then:

$$I_{b+} = \frac{dV_{OUT}}{dt} \times (C_1 + C_x) \quad (8)$$

where  $C_x$  is the stray capacitance at the + input.

## 6.2 Typical Applications

### Typical Single-Supply Applications

Additional single-supply applications ideas are found in the [LM358](#) data sheet. The LMC603x is pin-for-pin compatible with the LM358 and offers greater bandwidth and input resistance over the LM358. These features can improve the performance of many existing single-supply applications. Be aware, however, the supply voltage range of the LMC603x is smaller than that of the LM358.

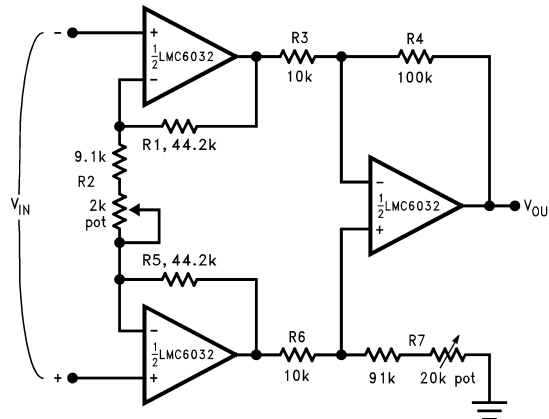


图 6-6. Instrumentation Amplifier

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

If  $R1 = R5$ ,  $R3 = R6$ , and  $R4 = R7$ , then  $A_V = 100$  for circuit shown.

Use low-drift resistors for good CMRR performance over temperature. Matching of  $R3$  to  $R6$  and  $R4$  to  $R7$  affects CMRR. Gain is adjusted through  $R2$ . CMRR is adjusted through  $R7$ . An improved circuit can be designed using the [RES11A-Q1](#), low-drift, precision, matched resistor pairs. 图 6-7 shows how a precise gain of 99 is easily implemented. The capacitors are optional and are used to improve noise performance, if needed.

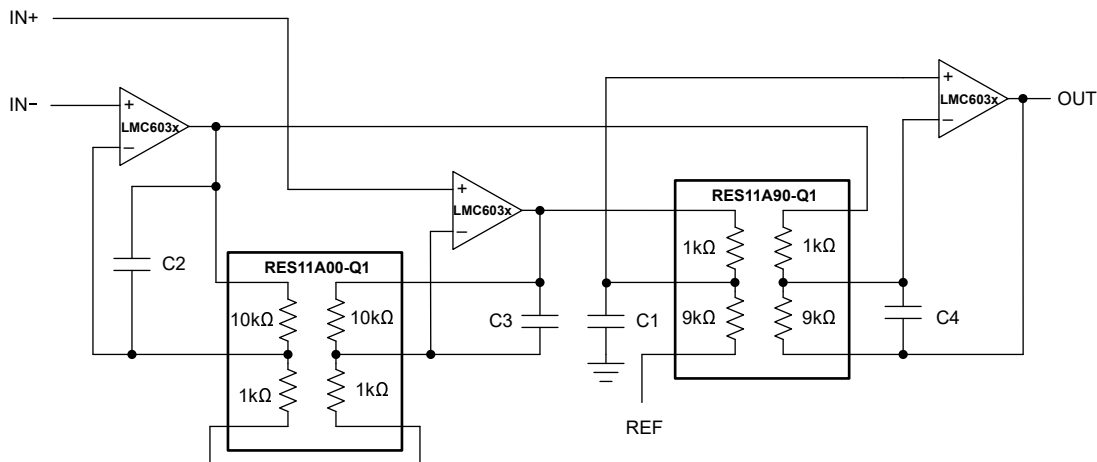
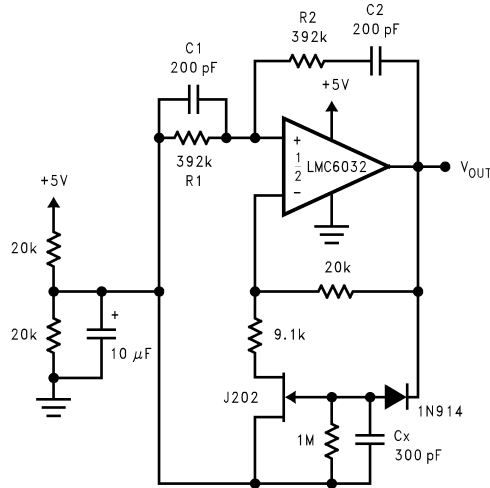


图 6-7. Improved Instrumentation Amplifier With RES11A



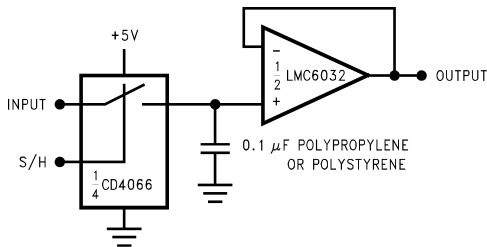
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2 \pi RC$$

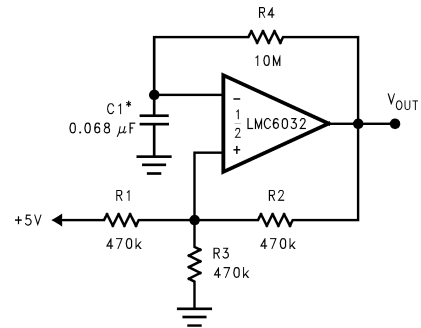
where  $R = R1 = R2$  and  $C = C1 = C2$ .

**图 6-8. Sine-Wave Oscillator**

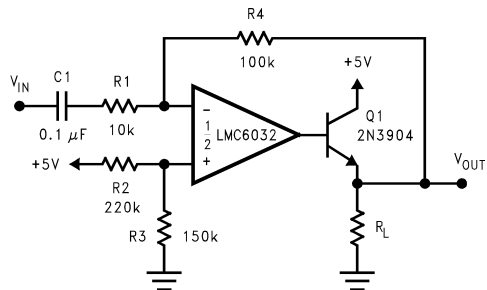
This circuit, as shown, oscillates at 2.0kHz with a peak-to-peak output swing of 4.0V.



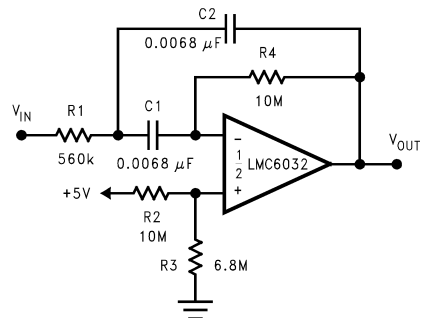
**图 6-9. Low-Leakage Sample-and-Hold**



**图 6-10. 1Hz Square-Wave Oscillator**



**图 6-11. Power Amplifier**



$$f_0 = 10\text{Hz}, Q = 2.1, \text{gain} = -8.8$$

**图 6-12. 10Hz Bandpass Filter**



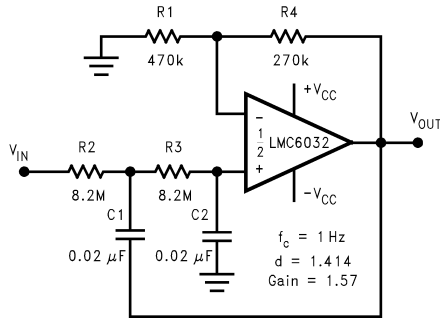
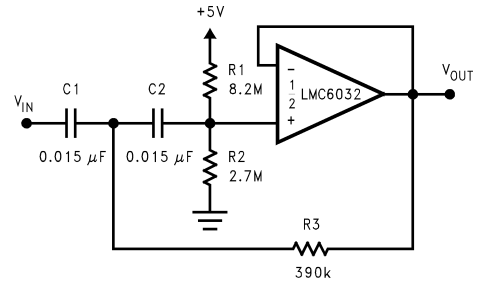
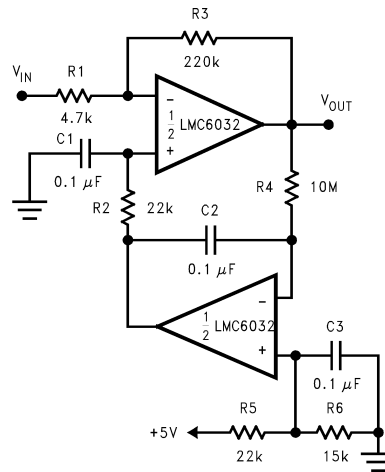


图 6-13. 1Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



$f_c = 10\text{Hz}$ ,  $d = 0.895$ , gain = 1, 2dB pass-band ripple

图 6-14. 10Hz High-Pass Filter



Gain = -46.8 Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1mV).

图 6-15. High-Gain Amplifier With Offset Voltage Reduction

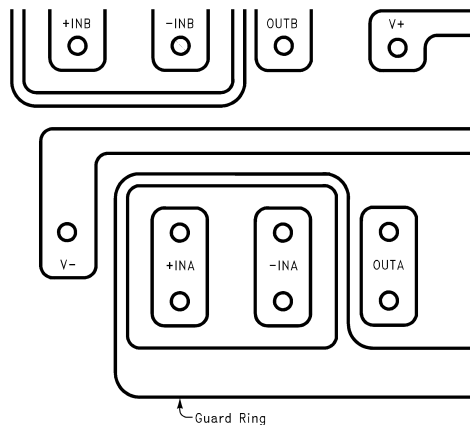
## 6.3 Layout

### 6.3.1 Layout Guidelines

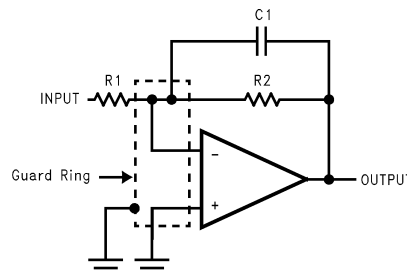
#### 6.3.1.1 Printed Circuit Board Layout for High-Impedance Work

Generally, any circuit that operates with less than 1000pA of leakage current requires special layout of the printed circuit board (PCB). To take advantage of the ultra-low bias current of the LMC603x, typically less than 40fA, an excellent layout is essential. Fortunately, the techniques for obtaining low leakages are quite simple. Foremost, do not ignore the surface leakage of the PCB, even though the leakage can sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage can be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC603x inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so on, connected to the op amp inputs. See [图 6-16](#). To have a significant effect, place guard rings on both the top and bottom of the PCB. This PCB foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of  $10^{12} \Omega$ , which is normally considered a very large resistance, can leak 5pA if the trace were a 5V bus adjacent to the pad of an input. This causes a 100 times degradation from the LMC603x actual performance. However, if a guard ring is held within 5mV of the inputs, then even a resistance of  $10^{11} \Omega$  causes only 50fA of leakage current, or perhaps a minor (2:1) degradation of the amplifier performance. See [图 6-17](#), [图 6-18](#), [图 6-19](#) for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see [图 6-20](#).



**图 6-16. Example of Guard Ring in PCB Layout**



**图 6-17. Inverting Amplifier Guard-Ring Connections**

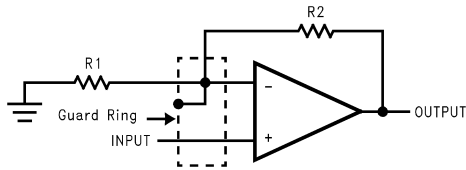


图 6-18. Noninverting Amplifier Guard-Ring Connections

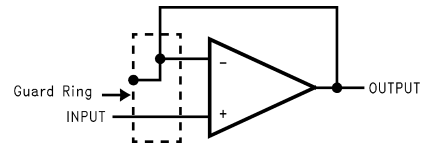


图 6-19. Follower Guard-Ring Connections

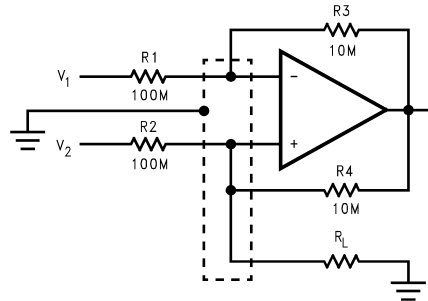
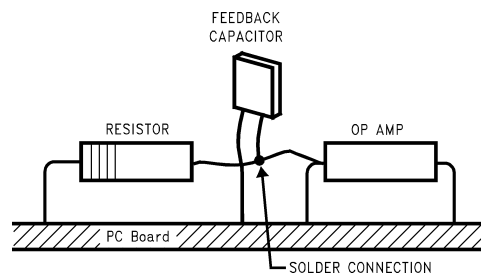


图 6-20. Howland Current-Pump Guard-Ring Connections

Be aware that when laying out a PCB for the sake of just a few circuits is inappropriate, there is another technique which is even better than a guard ring on a PCB. Do not insert the amplifier input pin into the board at all, but bend the pin up in the air and use only air as an insulator. Air is an excellent insulator. In this case you forgo some of the advantages of PCB construction, but the advantages of air are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See 图 6-21.



Input pins are lifted out of PCB and soldered directly to components. All other pins connected to the PCB.

图 6-21. Air Wiring

## 7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 7.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 7.2 支持资源

TI E2E™ [中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### Trademarks

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### 7.3 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 7.4 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 8 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (March 2013) to Revision D (February 2024)	Page
• 添加了 LMC6034 和相关信息.....	1
• 将 $I_Q$ 从 $400\ \mu\text{A}$ 更改为 $375\ \mu\text{A}$ ，以与 <i>特性</i> 中的 <i>电气特性</i> 匹配.....	1
• 将 <i>特性</i> 中的高压增益从 12dB 更改为 126dB (拼写错误).....	1
• 向 <i>特性</i> 中添加了低噪声并删除了低失真.....	1
• 向 <i>说明</i> 中添加了 OPA928 高性能基准.....	1
• Added <i>Pin Configuration and Functions</i> .....	2
• Added <i>Thermal Information</i> .....	5
• Changed parameter names to conform with new standards in <i>Electrical Characteristics</i> .....	6
• Changed input current noise specification from $0.0002\text{pA}/\sqrt{\text{Hz}}$ to $4\text{fA}/\sqrt{\text{Hz}}$ in <i>Electrical Characteristics</i> .....	6
• Changed total harmonic distortion specification from 0.01% to 0.2% in <i>Electrical Characteristics</i> .....	6
• Updated conditions in the header of <i>Typical Characteristics</i> .....	8
• Added input offset voltage vs common mode voltage and input bias current vs common mode voltage.....	8
• Updated description and circuit topology diagram in <i>Amplifier Topology</i> .....	11
• Added new instrumentation amplifier circuit using the RES11A to <i>Typical Applications</i> .....	15

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<b>Changes from Revision B (March 2013) to Revision C (March 2013)</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format.....	<a href="#">15</a>

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## **9 Mechanical, Packaging, and Orderable Information**

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6032IMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	LMC6032IM	<a href="#">Samples</a>
LMC6032IN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LMC6032IN	<a href="#">Samples</a>
LMC6034IM/NOPB	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	LMC6034IM	
LMC6034IMX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC6034IM	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

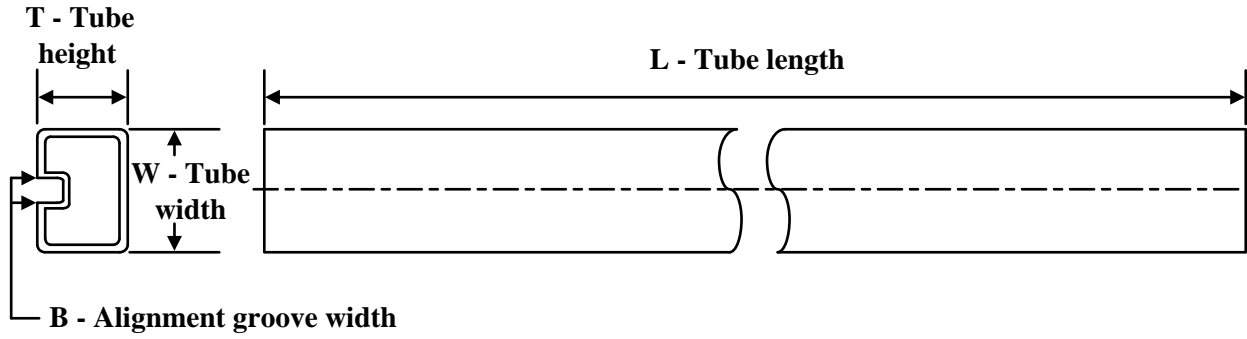
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6032IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6032IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMC6034IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6032IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6032IMX/NOPB	SOIC	D	8	2500	353.0	353.0	32.0
LMC6034IMX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LMC6032IN/NOPB	P	PDIP	8	40	502	14	11938	4.32
LMC6032IN/NOPB	P	PDIP	8	40	506	13.97	11230	4.32



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

D0014A



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

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9. Board assembly site may have different recommendations for stencil design.

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