LMH6552 1.5-GHz Fully Differential Amplifier

1 Features

- 1.5-GHz −3 dB Small Signal Bandwidth at A_V = 1
- 1.25-GHz −3 dB Large Signal Bandwidth at A_V = 1
- 800-MHz Bandwidth at A_V = 4
- 450-MHz 0.1 dB Flatness
- 3800-V/µs Slew Rate
- 10-ns Settling Time to 0.1%
  - −90 dB THD at 20 MHz
  - −74 dB THD at 70 MHz
- 20-ns Enable/Shutdown Pin
- 5-V to 12-V Operation

2 Applications

- Differential ADC Driver
- Video Over Twisted Pair
- Differential Line Driver
- Single End to Differential Converter
- High-Speed Differential Signaling
- IF/RF Amplifier
- Level Shift Amplifier
- SAW Filter Buffer/Driver

3 Description

The LMH6552 device is a high-performance, fully differential amplifier designed to provide the exceptional signal fidelity and wide large-signal bandwidth necessary for driving 8-bit to 14-bit high-speed data acquisition systems. Using TI's proprietary differential current mode input stage architecture, the LMH6552 allows operation at gains greater than unity without sacrificing response flatness, bandwidth, harmonic distortion, or output noise performance.

With external gain set resistors and integrated common mode feedback, the LMH6552 can be configured as either a differential input to differential output or single-ended input to differential output gain block. The LMH6552 can be AC- or DC-coupled at the input which makes it suitable for a wide range of applications, including communication systems and high-speed oscilloscope front ends. The performance of the LMH6552 driving an ADC14DS105 device is 86 dBc SFDR and 74 dBc SNR up to 40 MHz.

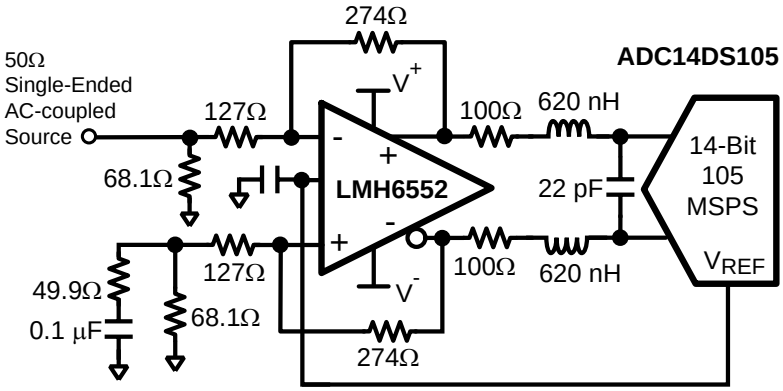
The LMH6552 is available in an 8-pin SOIC package as well as a space-saving, thermally enhanced 8-pin WSON package for higher performance.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6552	SOIC (8)	4.90 mm × 3.91 mm
	WSON (8)	3.00 mm × 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (January 2015) to Revision J — **Page**

- Changed footnote 4 in *Electrical Characteristics: ±5 V* table ... 5
- Changed Miscellaneous Performance, *Enable Voltage Threshold* parameter minimum specification in *Electrical Characteristics: ±5 V* table ... 6
- Changed footnote 4 in *Electrical Characteristics: ±2.5 V* table ... 7
- Changed minimum specifications of Miscellaneous Performance, *Enable Voltage Threshold* and *Disable Voltage Threshold* parameters in *Electrical Characteristics: ±2.5 V* table ... 8
- Added *Community Resources* section ... 31

Changes from Revision H (March 2013) to Revision I — **Page**

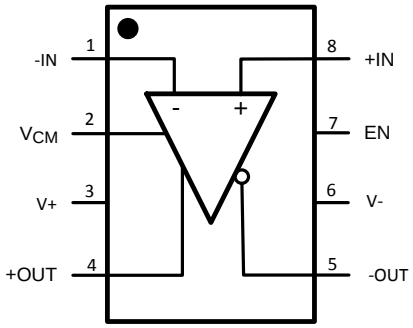
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision G (March 2013) to Revision H — **Page**

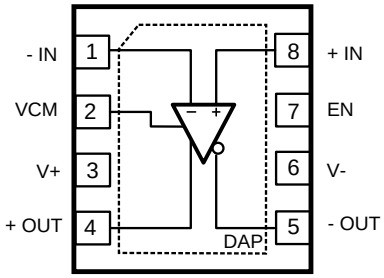
- Changed layout of National Data Sheet to TI format ... 27

5 Pin Configuration and Functions

D Package
8 Pins
Top View



NGS Package
8 Pins
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
EN	7	Enable
-IN	1	Negative Input
+IN	8	Positive Input
-OUT	5	Negative Output
+OUT	4	Positive Output
V-	6	Negative Supply
V+	3	Positive Supply
VCM	2	Output Common Mode Control
DAP	DAP	Die Attach Pad (See *Thermal Considerations* for more information)

6 Specifications

6.1 Absolute Maximum Ratings (1) (2)

	MIN	MAX	UNIT
Supply Voltage		13.2	V
Common Mode Input Voltage		$\pm V_S$	V
Maximum Input Current (pins 1, 2, 7, 8)		30	mA
Maximum Output Current (pins 4, 5)		(3)	mA
Maximum Junction Temperature		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specifications see SNOA549
(3) The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See *Power Dissipation* for more details.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	
	Machine model (MM)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Operating Temperature Range (1)	−40		+85	°C
Total Supply Voltage	4.5		12	V

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

6.4 Thermal Information

THERMAL METRIC (1)		LMH6552		UNIT
		D	NGS	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	58	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: ±5 V

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +5 V, V^- = −5 V, A_V= 1, V_{CM} = 0 V, R_F = R_G = 357 Ω, R_L = 500 Ω, for single ended in, differential out.(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
AC PERFORMANCE (DIFFERENTIAL)						
SSBW	Small Signal −3-dB Bandwidth (2)	V_{OUT} = 0.2 V_{PP}, A_V = 1, R_L = 1 kΩ		1500		MHz
		V_{OUT} = 0.2 V_{PP}, A_V = 1		1000		
		V_{OUT} = 0.2 V_{PP}, A_V = 2		930		
		V_{OUT} = 0.2 V_{PP}, A_V = 4		810		
		V_{OUT} = 0.2 V_{PP}, A_V = 8		590		
LSBW	Large Signal −3 dB Bandwidth	V_{OUT} = 2 V_{PP}, A_V = 1, R_L = 1 kΩ		1250		MHz
		V_{OUT} = 2 V_{PP}, A_V = 1		950		
		V_{OUT} = 2 V_{PP}, A_V = 2		820		
		V_{OUT} = 2 V_{PP}, A_V = 4		740		
		V_{OUT} = 2 V_{PP}, A_V = 8		590		
	0.1-dB Bandwidth	V_{OUT} = 0.2 V_{PP}, A_V = 1		450		MHz
	Slew Rate	4-V Step, A_V = 1		3800		V/µs
	Rise, Fall Time, 10%-90%	2-V Step		600		ps
	0.1% Settling Time	2-V Step		10		ns
	Overdrive Recovery Time	V_{IN} = 1.8-V to 0-V Step, A_V = 5 V/V		6		ns
DISTORTION AND NOISE RESPONSE						
HD2	2nd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800 Ω		–92		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800 Ω		–74		
HD3	3rd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800 Ω		–93		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800 Ω		–84		
IMD3	Two-Tone Intermodulation	f ≥ 70 MHz, Third-Order Products, V_{OUT} = 2-V_{PP} Composite		–87		dBc
	Input Noise Voltage	f ≥ 1 MHz		1.1		nV/√Hz
	Input Noise Current	f ≥ 1 MHz		19.5		pA/√Hz
	Noise Figure (See Figure 46)	50-Ω System, A_V = 9, 10 MHz		10.3		dB
INPUT CHARACTERISTICS						
I_{BI}	Input Bias Current (4)			60	110	µA
$I_{Boffset}$	Input Bias Current Differential (3)	V_{CM} = 0 V, V_{ID} = 0 V, $I_{Boffset}$ = (I_B^- - I_B^+)/2		2.5	18	µA
CMRR	Common Mode Rejection Ratio (3)	DC, V_{CM} = 0 V, V_{ID} = 0 V		80		dBc
R_{IN}	Input Resistance	Differential		15		Ω
C_{IN}	Input Capacitance	Differential		0.5		pF
CMVR	Input Common Mode Voltage Range	CMRR > 38 dB	±3.5	±3.8		V

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See *Overview* for information on temperature de-rating of this device. Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values can vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

(4) $I_{Boffset}$ is referred to a differential output offset voltage by the following relationship: $V_{OD(offset)}$ = I_{BI}*2R_F.

Electrical Characteristics: ±5 V (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +5 V, V^- = −5 V, A_V= 1, V_{CM} = 0 V, R_F = R_G = 357 Ω, R_L = 500 Ω, for single ended in, differential out.(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
OUTPUT PERFORMANCE						
	Output Voltage Swing (3)	Differential Output	14.8	15.4		V_{PP}
I_{OUT}	Linear Output Current (3)	V_{OUT} = 0 V	±70	±80		mA
I_{SC}	Short Circuit Current	One Output Shorted to Ground V_{IN} = 2 V Single Ended (5)		±141		mA
	Output Balance Error	ΔV_{OUT} Common Mode / ΔV_{OUT} Differential, ΔV_{OD} = 1 V, f < 1 MHz		–60		dB
MISCELLANEOUS PERFORMANCE						
Z_T	Open Loop Transimpedance	Differential		108		dBΩ
PSRR	Power Supply Rejection Ratio	DC, (V^+ - $\|V^-\|$) = ±1 V		80		dB
I_S	Supply Current (3)	R_L = ∞	19	22.5	25 **28**	mA
	Enable Voltage Threshold		3			V
	Disable Voltage Threshold				2.0	V
	Enable/Disable time			15		ns
I_{SD}	Disable Shutdown Current			500	600	µA
OUTPUT COMMON MODE CONTROL CIRCUIT						
	Common Mode Small Signal Bandwidth	V_{IN^+} = V_{IN^-} = 0		400		MHz
	Slew Rate	V_{IN^+} = V_{IN^-} = 0		607		V/µs
V_{OSCM}	Input Offset Voltage	Common Mode, V_{ID} = 0, V_{CM} = 0		1.5	±16.5	mV
	Input Bias Current	(6)		–3.2	±8	µA
	Voltage Range		±3.7	±3.8		V
	CMRR	Measure V_{OD}, V_{ID} = 0 V		80		dB
	Input Resistance			200		kΩ
	Gain	$\Delta V_{O,CM}$ / ΔV_{CM}	0.995	1.0	1.012	V/V

(5) Limit short circuit current in duration to no more than 10 seconds. See *Power Dissipation* for more details.
(6) Negative input current implies current flowing out of the device.

6.6 Electrical Characteristics: ±2.5 V

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +2.5 V, V^- = −2.5 V, A_V = 1, V_{CM} = 0 V, R_F = R_G = 357 Ω, R_L = 500 Ω, for single ended in, differential out.(1)

PARAMETER		TEST CONDITIONS	MIN (2)	TYP (3)	MAX (2)	UNIT
SSBW	Small Signal −3-dB Bandwidth (2)	V_{OUT} = 0.2 V_{PP}, A_V = 1, R_L = 1 kΩ		1100		MHz
		V_{OUT} = 0.2 V_{PP}, A_V = 1		800		
		V_{OUT} = 0.2 V_{PP}, A_V = 2		740		
		V_{OUT} = 0.2 V_{PP}, A_V = 4		660		
		V_{OUT} = 0.2 V_{PP}, A_V = 8		498		
LSBW	Large Signal −3 dB Bandwidth	V_{OUT} = 2 V_{PP}, A_V = 1, R_L = 1 kΩ		820		MHz
		V_{OUT} = 2 V_{PP}, A_V = 1		690		
		V_{OUT} = 2 V_{PP}, A_V = 2		620		
		V_{OUT} = 2 V_{PP}, A_V = 4		589		
		V_{OUT} = 2 V_{PP}, A_V = 8		480		
	0.1 dB Bandwidth	V_{OUT} = 0.2 V_{PP}, A_V = 1		300		MHz
	Slew Rate	2-V Step, A_V = 1		2100		V/µs
	Rise/Fall Time, 10% to 90%	2-V Step		700		ps
	0.1% Settling Time	2-V Step		10		ns
	Overdrive Recovery Time	V_{IN} = 0.7-V to 0-V Step, A_V = 5 V/V		6		ns
DISTORTION AND NOISE RESPONSE						
HD2	2nd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800 Ω		-82		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800 Ω		-65		
HD3	3rd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800 Ω		-79		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800 Ω		-67		
IMD3	Two-Tone Intermodulation	f ≥ 70 MHz, Third-Order Products, V_{OUT} = 2-V_{PP} Composite		−77		dBc
	Input Noise Voltage	f ≥ 1 MHz		1.1		nV/√Hz
	Input Noise Current	f ≥ 1 MHz		19.5		pA/√Hz
	Noise Figure (See Figure 46)	50-Ω System, A_V = 9, 10 MHz		10.2		dB
INPUT CHARACTERISTICS						
I_{BI}	Input Bias Current (4)			54	90	µA
$I_{Boffset}$	Input Bias Current Differential (3)	V_{CM} = 0 V, V_{ID} = 0 V, $I_{Boffset}$ = (I_{B^-} - I_{B^+})/2		2.3	18	µA
CMRR	Common-Mode Rejection Ratio (3)	DC, V_{CM} = 0 V, V_{ID} = 0 V		75		dBc
R_{IN}	Input Resistance	Differential		15		Ω
C_{IN}	Input Capacitance	Differential		0.5		pF
CMVR	Input Common Mode Range	CMRR > 38 dB	±1.0	±1.3		V
OUTPUT PERFORMANCE						
	Output Voltage Swing (3)	Differential Output	5.6	6.0		V_{PP}
I_{OUT}	Linear Output Current (3)	V_{OUT} = 0 V	±55	±65		mA
I_{SC}	Short Circuit Current	One Output Shorted to Ground, V_{IN} = 2 V Single Ended (5)		±131		mA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See *Overview* for information on temperature de-rating of this device." Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values can vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) $I_{Boffset}$ is referred to a differential output offset voltage by the following relationship: $V_{OD(offset)}$ = I_{BI}*2R_F.
(5) Limit short circuit current in duration to no more than 10 seconds. See *Power Dissipation* for more details.

Electrical Characteristics: ±2.5 V (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +2.5 V, V^- = −2.5 V, A_V = 1, V_{CM} = 0 V, R_F = R_G = 357 Ω, R_L = 500 Ω, for single ended in, differential out.(1)

PARAMETER		TEST CONDITIONS	MIN (2)	TYP (3)	MAX (2)	UNIT
	Output Balance Error	ΔV_{OUT} Common Mode / ΔV_{OUT} Differential, ΔV_{OD} = 1 V, f < 1 MHz		60		dB
MISCELLANEOUS PERFORMANCE						
ZT	Open Loop Transimpedance	Differential		107		dBΩ
PSRR	Power Supply Rejection Ratio	DC, ΔV_S = ±1 V		80		dB
I_S	Supply Current (3)	R_L = ∞	17	20.4	24 **27**	mA
	Enable Voltage Threshold		0.5			V
	Disable Voltage Threshold				–0.5	V
	Enable/Disable Time			15		ns
I_{SD}	Disable Shutdown Current			500	600	µA
OUTPUT COMMON MODE CONTROL CIRCUIT						
	Common Mode Small Signal Bandwidth	V_{IN^+} = V_{IN^-} = 0		310		MHz
	Slew Rate	V_{IN^+} = V_{IN^-} = 0		430		V/µs
V_{OSCM}	Input Offset Voltage	Common Mode, V_{ID} = 0, V_{CM} = 0		1.65	±15	mV
	Input Bias Current	(6)		−2.9		µA
	Voltage Range		±1.19	±1.25		V
	CMRR	Measure V_{OD}, V_{ID} = 0 V		80		dB
	Input Resistance			200		kΩ
	Gain	$\Delta V_{O,CM}$ / ΔV_{CM}	0.995	1.0	1.012	V/V

(6) Negative input current implies current flowing out of the device.

6.7 Typical Characteristics $V^+ = +5$ V, $V^- = -5$ V

(T_A = 25°C, $R_F = R_G$ = 357 Ω, R_L = 500 Ω, A_V = 1, for single ended in, differential out, unless specified).

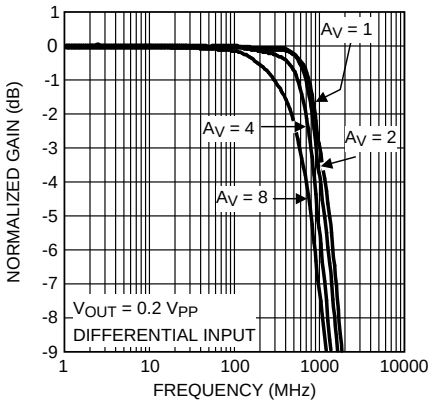


Figure 1. Frequency Response vs Gain

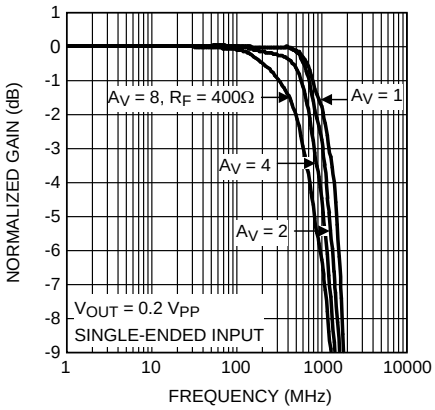


Figure 2. Frequency Response vs Gain

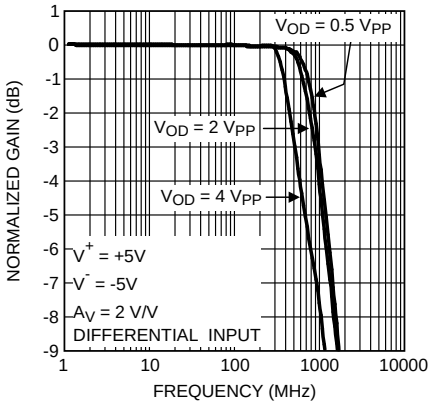


Figure 3. Frequency Response vs V_{OUT}

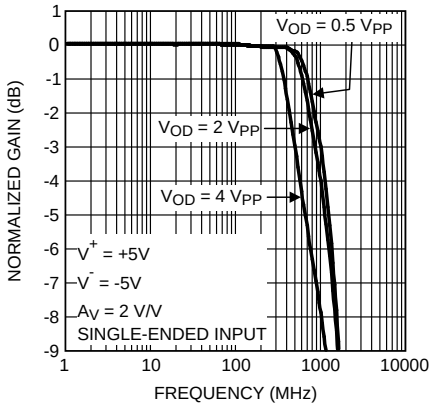


Figure 4. Frequency Response vs V_{OUT}

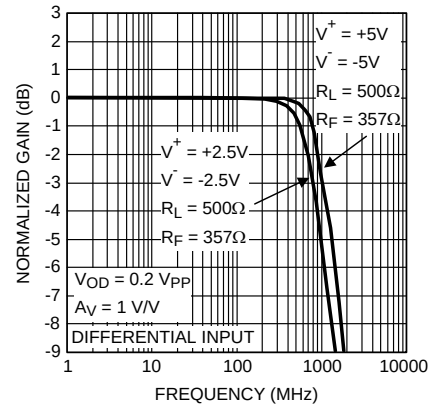


Figure 5. Frequency Response vs Supply Voltage

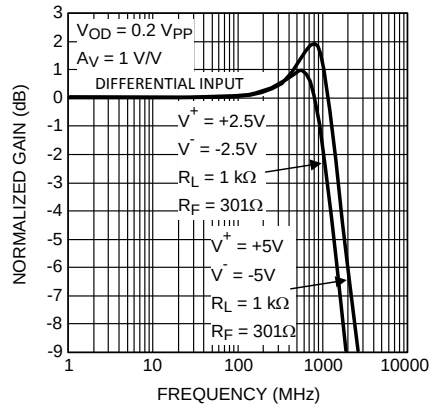


Figure 6. Frequency Response vs Supply Voltage

Typical Characteristics $V^+ = +5$ V, $V^- = -5$ V (continued)

(T_A = 25°C, $R_F = R_G$ = 357 Ω, R_L = 500 Ω, A_V = 1, for single ended in, differential out, unless specified).

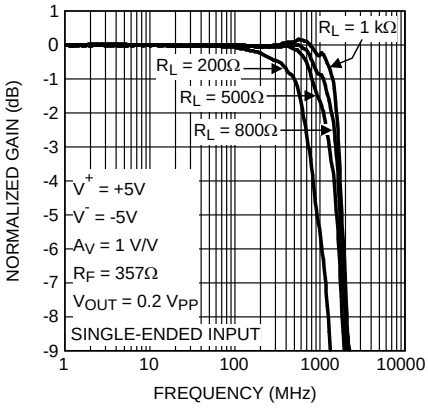


Figure 7. Frequency Response vs Resistive Load

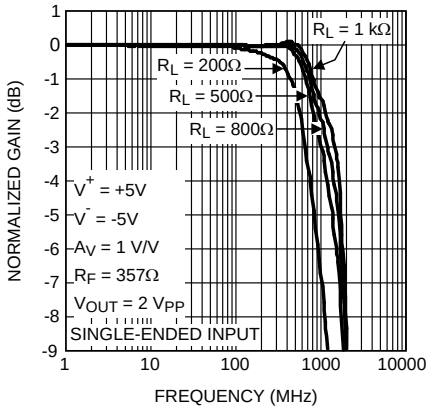


Figure 8. Frequency Response vs Resistive Load

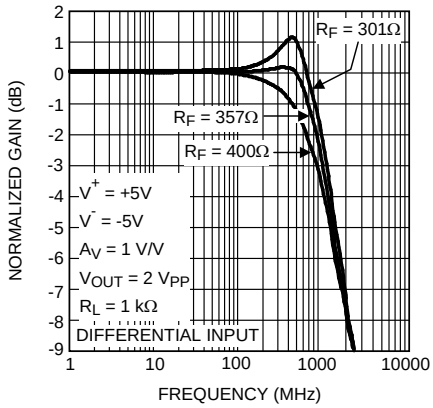


Figure 9. Frequency Response vs R_F

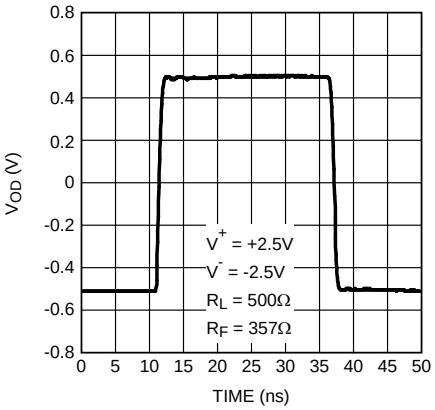


Figure 10. 1 V_{PP} Pulse Response Single Ended Input

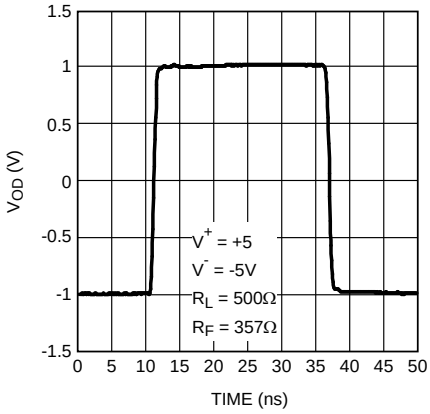


Figure 11. 2 V_{PP} Pulse Response Single Ended Input

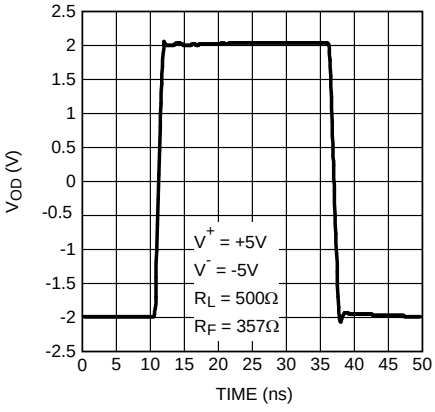


Figure 12. Large Signal Pulse Response

Typical Characteristics V^+ = +5 V, V^- = −5 V (continued)

(T_A = 25°C, R_F = R_G = 357 Ω, R_L = 500 Ω, A_V = 1, for single ended in, differential out, unless specified).

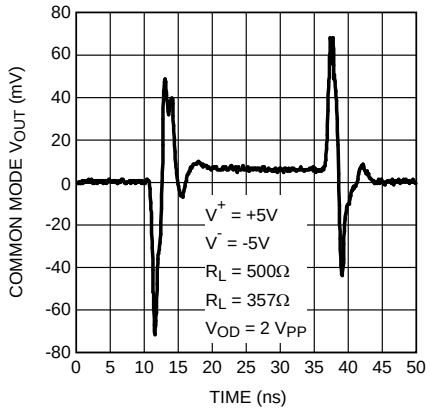


Figure 13. Output Common Mode Pulse Response

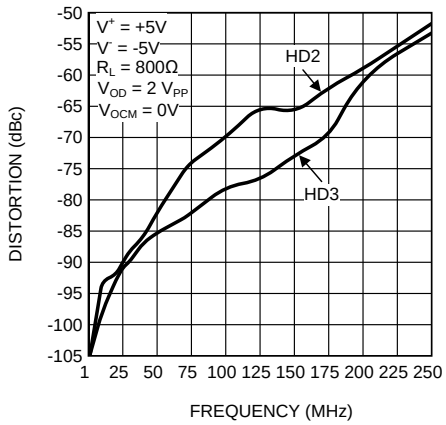


Figure 14. Distortion vs Frequency Single Ended Input

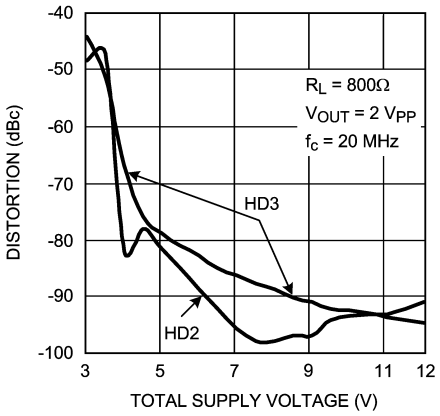


Figure 15. Distortion vs Supply Voltage

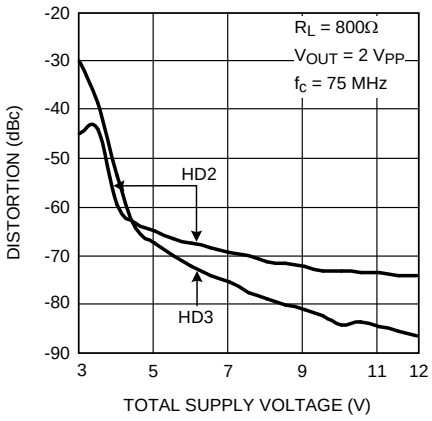


Figure 16. Distortion vs Supply Voltage

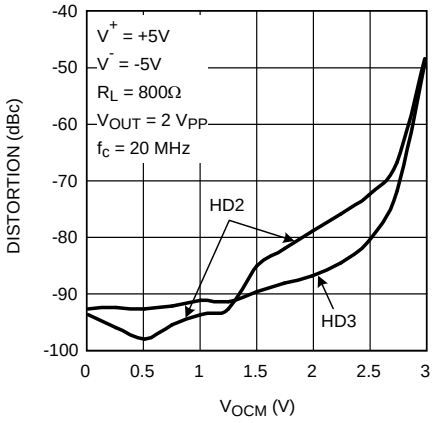


Figure 17. Distortion vs Output Common Mode Voltage

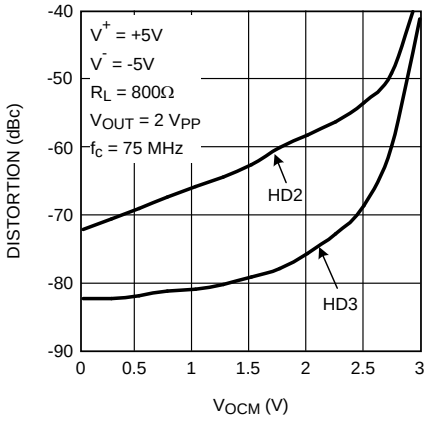


Figure 18. Distortion vs Output Common Mode Voltage

Typical Characteristics $V^+ = +5$ V, $V^- = -5$ V (continued)

(T_A = 25°C, $R_F = R_G$ = 357 Ω, R_L = 500 Ω, A_V = 1, for single ended in, differential out, unless specified).

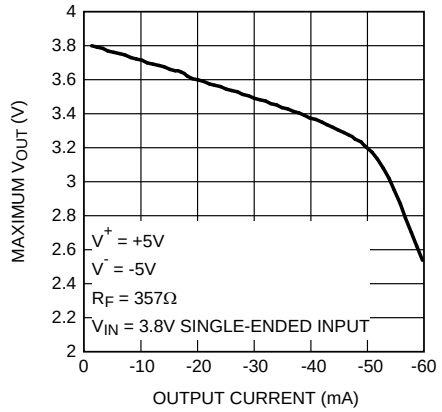


Figure 19. Maximum V_{OUT} vs I_{OUT}

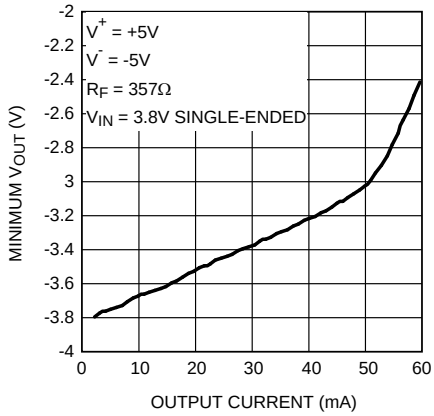


Figure 20. Minimum V_{OUT} vs I_{OUT}

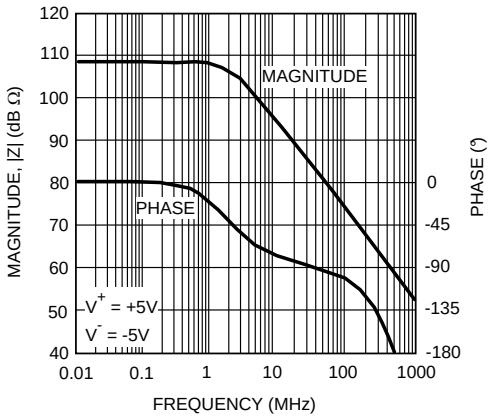


Figure 21. Open Loop Transimpedance

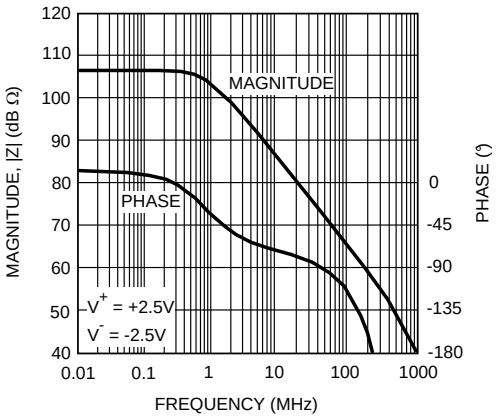


Figure 22. Open Loop Transimpedance

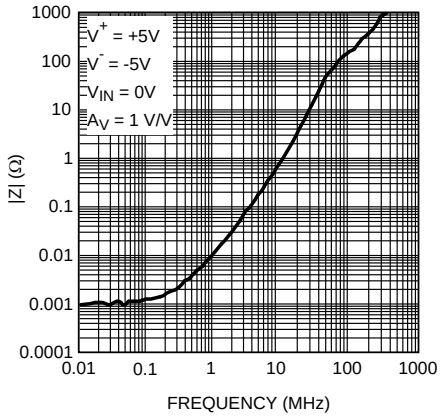


Figure 23. Closed Loop Output Impedance

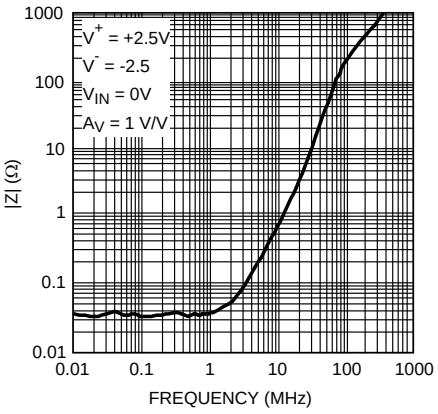


Figure 24. Closed Loop Output Impedance

Typical Characteristics V^+ = +5 V, V^- = −5 V (continued)

(T_A = 25°C, R_F = R_G = 357 Ω, R_L = 500 Ω, A_V = 1, for single ended in, differential out, unless specified).

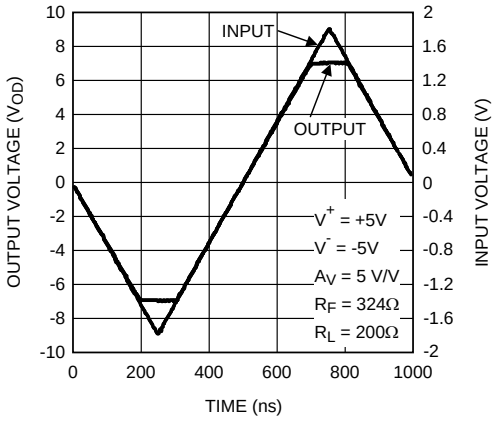


Figure 25. Overdrive Recovery

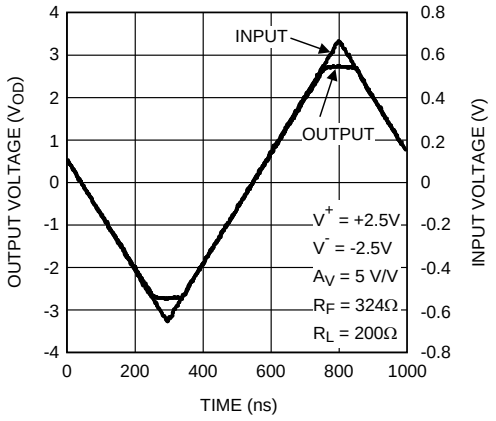


Figure 26. Overdrive Recovery

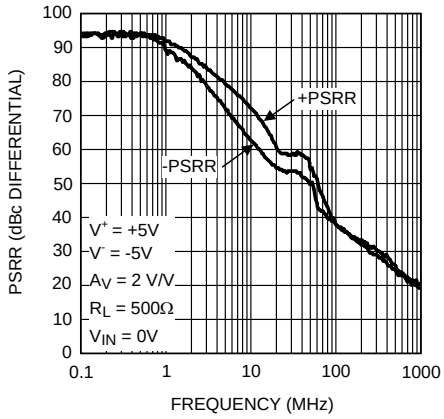


Figure 27. PSRR

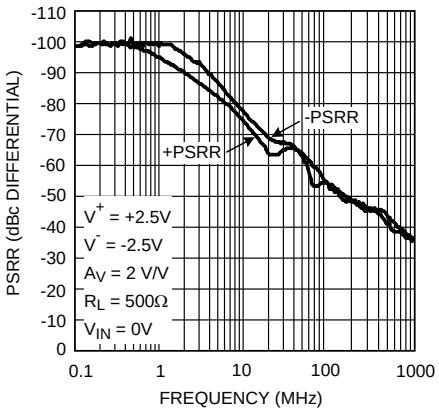


Figure 28. PSRR

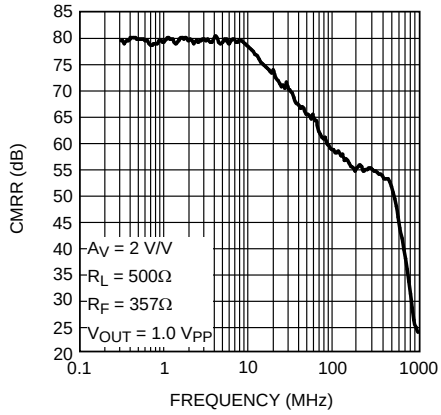


Figure 29. CMRR

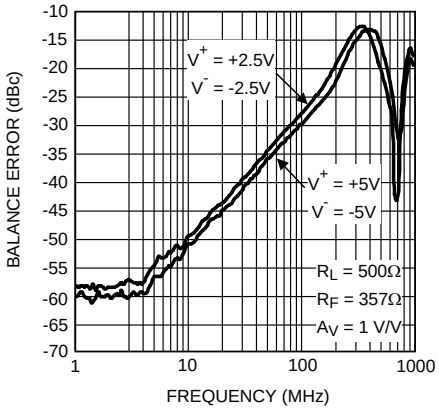


Figure 30. Balance Error

Typical Characteristics V^+ = +5 V, V^- = −5 V (continued)

(T_A = 25°C, R_F = R_G = 357 Ω, R_L = 500 Ω, A_V = 1, for single ended in, differential out, unless specified).

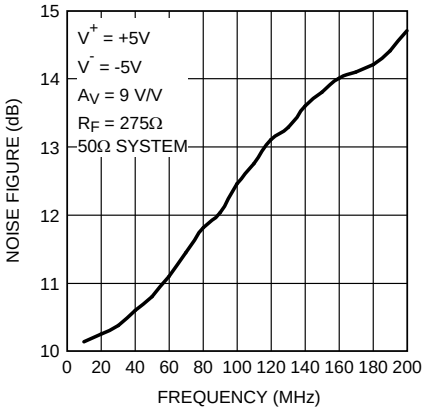


Figure 31. Noise Figure

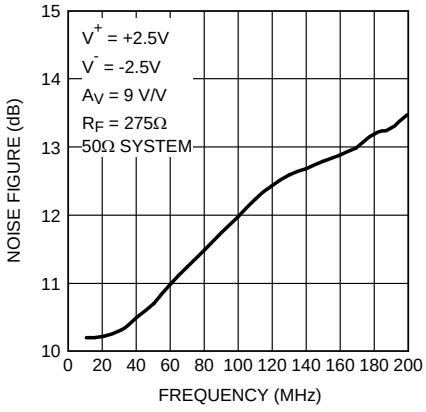


Figure 32. Noise Figure

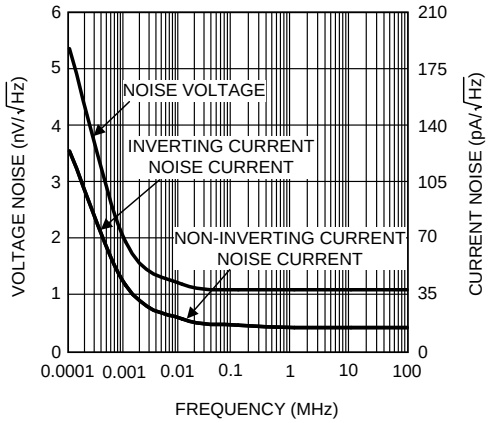


Figure 33. Input Noise vs Frequency

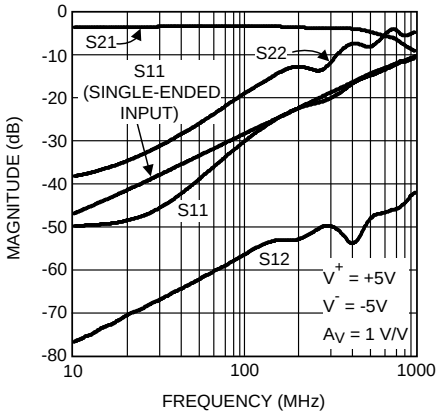


Figure 34. Differential S-Parameter Magnitude vs Frequency

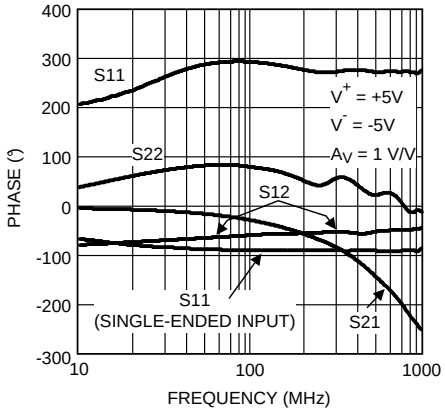


Figure 35. Differential S-Parameter Phase vs Frequency

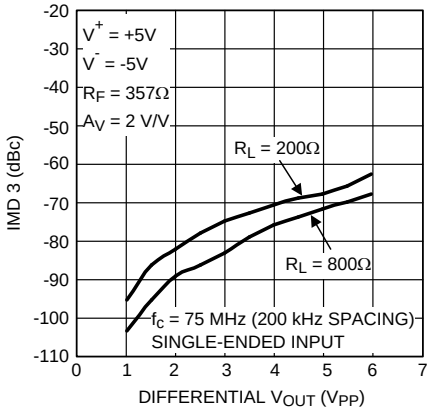


Figure 36. 3rd Order Intermodulation Products vs V_{OUT}

Typical Characteristics $V^+ = +5$ V, $V^- = -5$ V (continued)

(T_A = 25°C, $R_F = R_G$ = 357 Ω, R_L = 500 Ω, A_V = 1, for single ended in, differential out, unless specified).

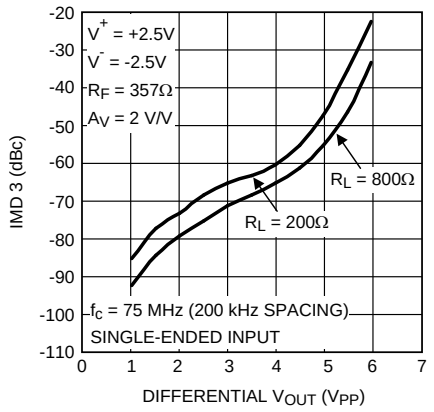


Figure 37. 3rd Order Intermodulation Products vs V_{OUT}

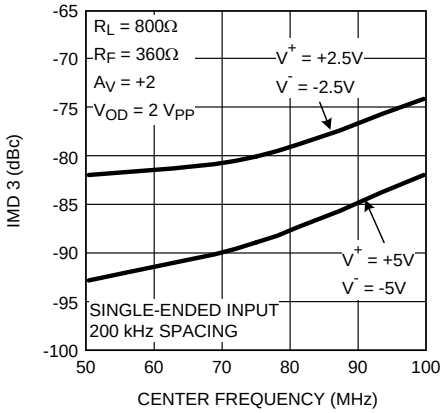


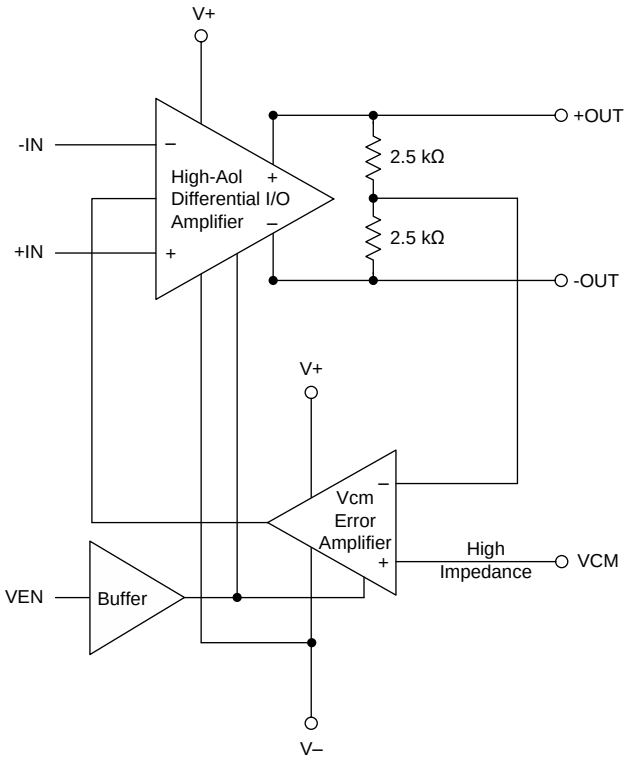
Figure 38. 3rd Order Intermodulation Products vs Center Frequency

7 Detailed Description

7.1 Overview

The LMH6552 is a fully differential current feedback amplifier with integrated output common mode control, designed to provide low distortion amplification to wide bandwidth differential signals. The common mode feedback circuit sets the output common mode voltage independent of the input common mode, as well as forcing the V+ and V− outputs to be equal in magnitude and opposite in phase, even when only one of the inputs is driven as in single to differential conversion.

7.2 Functional Block Diagram



7.3 Feature Description

The proprietary current feedback architecture of the LMH6552 offers gain and bandwidth independence with exceptional gain flatness and noise performance, even at high values of gain, simply with the appropriate choice of RF1 and RF2. Generally, RF1 is set equal to RF2, and RG1 equal to RG2, so that the gain is set by the ratio RF/RG. Matching of these resistors greatly affects CMRR, DC offset error, and output balance. A maximum of 0.1% tolerance resistors are recommended for optimal performance, and the amplifier is internally compensated to operate with optimum gain flatness with RF value of 200 Ω depending on PCB layout, and load resistance. The output common mode voltage is set by the VCM pin with a fixed gain of 1 V/V. Drive this pin by a low impedance reference and bypassed to ground with a 0.1-µF ceramic capacitor. Any unwanted signal coupling into the VCM pin is passed along to the outputs, reducing the performance of the amplifier. The LMH6552 can be configured to operate on a single 10V supply connected to V+ with V- grounded or configured for a split supply operation with V+ = +5 V and V− = −5 V. Operation on a single 10-V supply, depending on gain, is limited by the input common mode range; therefore, AC coupling may be required.

7.4 Device Functional Modes

This wideband FDA requires external resistors for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be either on with the PD pin asserted to a voltage greater than Vs– + 3.0 V, or turned off by asserting PD low. Disabling the amplifier shuts off the quiescent current and stops correct amplifier operation. The signal path is still present for the source signal through the external resistors. The Vocm control pin sets the output average voltage. Left open, Vocm floats to an indeterminate voltage. Driving this high-impedance input with a voltage reference within its valid range sets a target for the internal Vcm error amplifier.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The proprietary current feedback architecture of the LMH6552 offers gain and bandwidth independence with exceptional gain flatness and noise performance, even at high values of gain, simply with the appropriate choice of R_{F1} and R_{F2}. Generally R_{F1} is set equal to R_{F2}, and R_{G1} equal to R_{G2}, so that the gain is set by the ratio R_F/R_G. Matching of these resistors greatly affects CMRR, DC offset error, and output balance. A minimum of 0.1% tolerance resistors are recommended for optimal performance, and the amplifier is internally compensated to operate with optimum gain flatness with values of R_F between 270 Ω and 390 Ω depending on package selection, PCB layout, and load resistance.

The output common mode voltage is set by the V_{CM} pin with a fixed gain of 1 V/V. This pin must be driven by a low impedance reference and must be bypassed to ground with a 0.1 µF ceramic capacitor. Any unwanted signal coupling into the V_{CM} pin is passed along to the outputs, reducing the performance of the amplifier. This pin must not be left floating.

The LMH6552 can be operated on a supply range as either a single 5V supply or as a split +5 V and −5 V. Operation on a single 5-V supply, depending on gain, is limited by the input common mode range; therefore, AC coupling may be required. For example, in a DC coupled input application on a single 5-V supply, with a V_{CM} of 1.5 V, the input common voltage at a gain of 1 is 0.75 V, which is outside the minimum 1.2-V to 3.8-V input common mode range of the amplifier. The minimum V_{CM} for this application must be greater than 2.5 V depending on output signal swing. Alternatively, AC coupling of the inputs in this example results in equal input and output common mode voltages, so a 1.5 V V_{CM} would be achievable. Split supplies allow much less restricted AC and DC coupled operation with optimum distortion performance.

The LMH6552 is equipped with an ENABLE pin to reduce power consumption when not in use. The ENABLE pin, when not driven, floats high (on). When the ENABLE pin is pulled low the amplifier is disabled and the amplifier output stage goes into a high impedance state so the feedback and gain set resistors determine the output impedance of the circuit. For this reason input to output isolation is poor in the disabled state and the part is not recommended in multiplexed applications where outputs are all tied together.

8.2 Typical Applications

8.2.1 Typical Fully Differential Application

In many applications, it is required to drive a differential input ADC from a single ended source. Traditionally, transformers have been used to provide single to differential conversion, but these are inherently bandpass by nature and cannot be used for DC coupled applications. The LMH6552 provides excellent performance as a single-to-differential converter down to DC. Figure 45 illustrates a typical application circuit where an LMH6552 is used to produce a differential signal from a single ended source.

Typical Applications (continued)

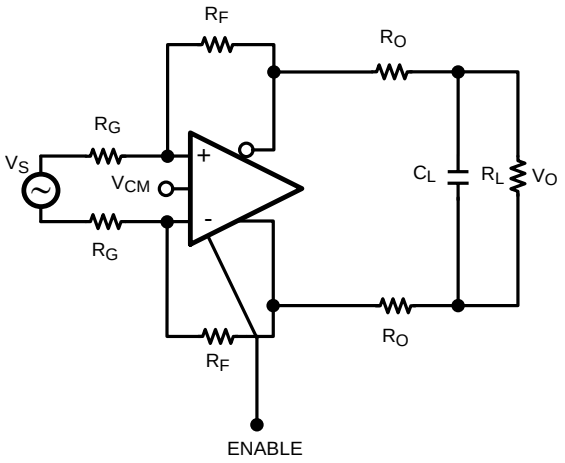


Figure 39. Typical Fully Differential Application Schematic

8.2.1.1 Design Requirements

One typical application for the LMH6552 is to drive an ADC. The following design is a single ended to differential circuit with an input impedance of 50 Ω and an output impedance of 100 Ω. The VCM voltage of the amplifier needs to be set to the same voltage as the ADC reference voltage which is typically 1.2 V. Figure 45 illustrates the design equations required to set the external resistor values. This design also requires a gain of 1 and -74 dBc THD at 70 MHz.

8.2.1.2 Detailed Design Procedure

To match the input impedance of the circuit in Figure 45 to a specified source resistance, RS, requires that RT || RIN = RS. The equations governing RIN and AV for single-to-differential operation are also provided in Figure 45. These equations, along with the source matching condition, must be solved iteratively to achieve the desired gain with the proper input termination. Component values for several common gain configurations in a 50-Ω environment are given in Table 1. Gain Component Values for 50-Ω System WSON Package. Typically RS=50 Ω and RM=RS||RT.

8.2.1.2.1 WSON Package

Due to its size and lower parasitics, the WSON requires the lower optimum value of 275 Ω for R_F. This gives a flat frequency response with minimal peaking. With a lower R_F value the WSON package has a reduction in noise compared to the SOIC with its optimum R_F = 360 Ω.

8.2.1.2.2 Fully Differential Operation

The LMH6552 performs best in a fully differential configuration. The circuit illustrated in Figure 39 is a typical fully differential application circuit as might be used to drive an analog to digital converter (ADC). In this circuit the closed loop gain $A_V = V_{OUT}/ V_{IN} = R_F/R_G$, where the feedback is symmetric. The series output resistors, R_O, are optional and help keep the amplifier stable when presented with a capacitive load. Refer to *Driving Capacitive Loads* for details.

When driven from a differential source, the LMH6552 provides low distortion, excellent balance, and common mode rejection. This is true provided the resistors R_F, R_G and R_O are well matched and strict symmetry is observed in board layout. With an intrinsic device CMRR of 80 dB, using 0.1% resistors gives a worst case CMRR of around 60 dB for most circuits.

The circuit configuration illustrated in Figure 40 was used to measure differential S parameters in a 50-Ω environment at a gain of 1 V/V. Refer to Figure 34 and Figure 35 in the *Typical Characteristics* for measurement results.

Typical Applications (continued)

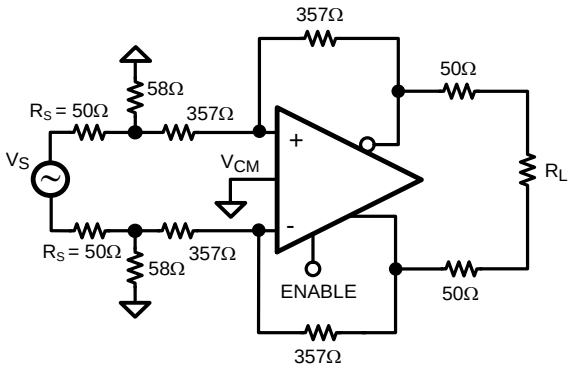


Figure 40. Differential S-Parameter Test Circuit

Table 1. Gain Component Values for 50Ω System WSON Package

Gain	R_F	R_G	R_T	R_M
0 dB	275Ω	255Ω	59Ω	26.7Ω
6 dB	275Ω	127Ω	68.1Ω	28.7Ω
12 dB	275Ω	54.9Ω	107Ω	34Ω

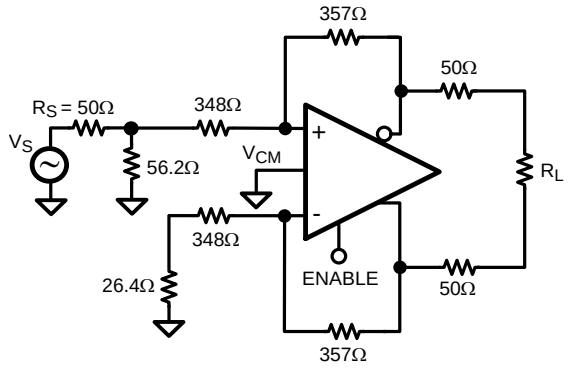


Figure 41. Single Ended Input S-Parameter Test Circuit (50Ω System)

The circuit shown in Figure 41 was used to measure S-parameters for a single-to-differential configuration. Figure 34 and Figure 35 in *Typical Characteristics* are taken using the recommended component values for 0 dB gain.

8.2.1.2.3 Driving Capacitive Loads

As noted previously, capacitive loads must be isolated from the amplifier output with small valued resistors. This is particularly the case when the load has a resistive component that is 500 Ω or higher. A typical ADC has capacitive components of around 10 pF and the resistive component could be 1000 Ω or higher. If driving a transmission line, such as 50Ω coaxial or 100Ω twisted pair, using matching resistors is sufficient to isolate any subsequent capacitance.

8.2.1.2.3.1 Balanced Cable Driver

With up to 15 V_{PP} differential output voltage swing and 80 mA of linear drive current the LMH6552 makes an excellent cable driver as illustrated in Figure 42. The LMH6552 is also suitable for driving differential cables from a single ended source.

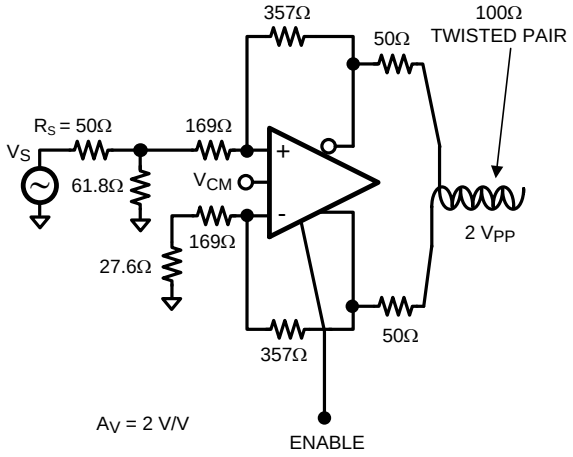


Figure 42. Fully Differential Cable Driver

8.2.1.3 Application Curves

Many application circuits have capacitive loading. As shown in Figure 43 amplifier bandwidth is reduced with increasing capacitive load, so parasitic capacitance must be strictly limited.

In order to ensure stability resistance must be added between the capacitive load and the amplifier output pins. The value of the resistor is dependent on the amount of capacitive load as shown in Figure 44. This resistive value is a suggestion. System testing is required to determine the optimal value. Using a smaller resistor retains more system bandwidth at the expense of overshoot and ringing, and larger values of resistance reduce overshoot but also reduce system bandwidth.

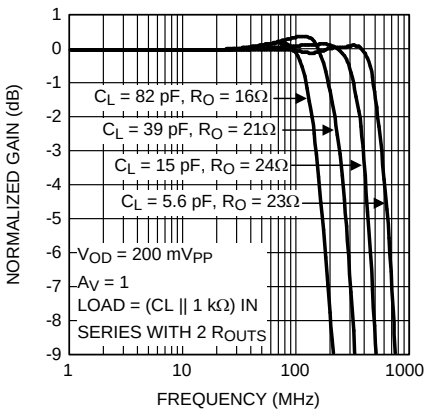


Figure 43. Frequency Response vs Capacitive Load

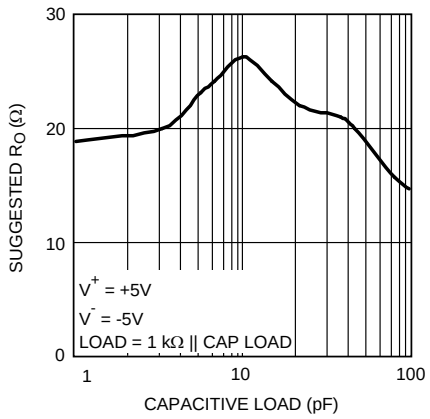
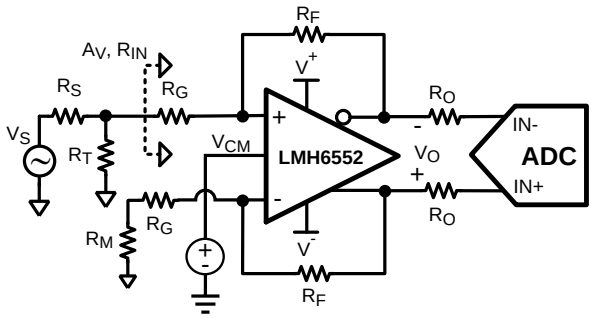


Figure 44. Suggested R_{OUT} vs Capacitive Load

8.2.2 Single-Ended Input to Differential Output Operation

In many applications, it is required to drive a differential input ADC from a single-ended source. Traditionally, transformers have been used to provide single to differential conversion, but these are inherently bandpass by nature and cannot be used for DC coupled applications. The LMH6552 provides excellent performance as a single-to-differential converter down to DC. Figure 45 shows a typical application circuit where an LMH6552 is used to produce a differential signal from a single-ended source.



$$A_V = \left(\frac{2(1-\beta_1)}{\beta_1+\beta_2}\right) \qquad \beta_1 = \left(\frac{R_G}{R_G+R_F}\right)$$

$$R_{IN} = \left(\frac{2R_G + R_M(1-\beta_2)}{1+\beta_2}\right) \qquad \beta_2 = \left(\frac{R_G+R_M}{R_G+R_F+R_M}\right)$$

$$R_S = R_T \parallel R_{IN} \qquad R_M = R_T \parallel R_S$$

Figure 45. Single-Ended Input with Differential Output

When using the LMH6552 in single-to-differential mode, the complementary output is forced to a phase inverted replica of the driven output by the common mode feedback circuit as opposed to being driven by its own complimentary input. Consequently, as the driven input changes, the common mode feedback action results in a varying common mode voltage at the amplifier's inputs, proportional to the driving signal. Due to the non-ideal common mode rejection of the amplifier's input stage, a small common mode signal appears at the outputs which is superimposed on the differential output signal. The ratio of the change in output common mode voltage to output differential voltage is commonly referred to as output balance error. The output balance error response of the LMH6552 over frequency is shown in the *Typical Characteristics*.

To match the input impedance of the circuit in Figure 45 to a specified source resistance, R_S, requires that $R_T \parallel R_{IN} = R_S$. The equations governing R_{IN} and A_V for single-to-differential operation are also provided in Figure 45. These equations, along with the source matching condition, must be solved iteratively to achieve the desired gain with the proper input termination. Component values for several common gain configurations in a 50-Ω environment are given in Table 1. Typically R_S=50Ω and R_M=R_S||R_T.

8.2.3 Single Supply Operation

Single supply operation is possible on supplies from 5 V to 10 V; however, as discussed earlier, AC input coupling is recommended for low supplies such as 5 V due to input common mode limitations. An example of an AC coupled, single supply, single-to-differential circuit is illustrated in Figure 46. Note that when AC coupling, both inputs need to be AC coupled irrespective of single-to-differential or differential-to-differential configuration. For higher supply voltages DC coupling of the inputs may be possible provided that the output common mode DC level is set high enough so that the amplifier's inputs and outputs are within their specified operating ranges.

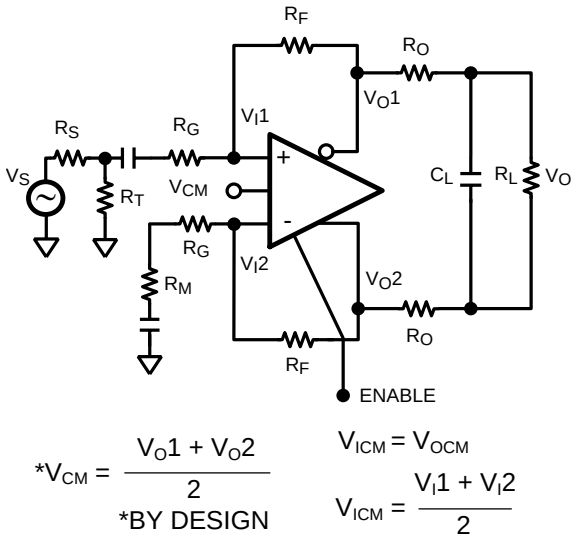


Figure 46. AC Coupled for Single Supply Operation

8.2.4 Split Supply Operation

For optimum performance, split supply operation is recommended using +5 V and −5 V supplies; however, operation is possible on split supplies as low as +2.25 V and −2.25 V and as high as +6 V and −6 V. Provided the total supply voltage does not exceed the 4.5-V to 12-V operating specification, non-symmetric supply operation is also possible and in some cases advantageous. For example, if a 5-V DC coupled operation is required for low power dissipation but the amplifier input common mode range prevents this operation, it is still possible with split supplies of (V^+) and (V^-). Where (V^+) - (V^-) = 5V and V^+ and V^- are selected to center the amplifier input common mode range to suit the application.

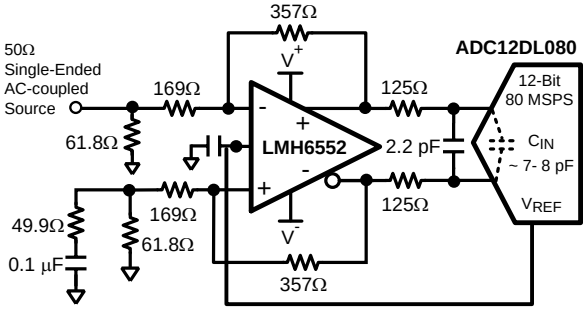
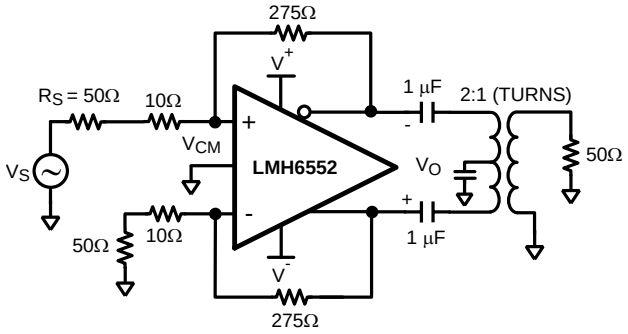


Figure 47. Split Supply

8.2.5 Output Noise Performance and Measurement

Unlike differential amplifiers based on voltage feedback architectures, noise sources internal to the LMH6552 refer to the inputs largely as current sources, hence the low input referred voltage noise and relatively higher input referred current noise. The output noise is therefore more strongly coupled to the value of the feedback resistor and not to the closed loop gain, as would be the case with a voltage feedback differential amplifier. This allows operation of the LMH6552 at much higher gain without incurring a substantial noise performance penalty, simply by choosing a suitable feedback resistor.

Figure 48 shows a circuit configuration used to measure noise figure for the LMH6552 in a 50-Ω system. An R_F value of 275 Ω is chosen for the SOIC package to minimize output noise and simultaneously allows both high gain (9 V/V) and proper 50-Ω input termination. Refer to *Single-Ended Input to Differential Output Operation* for calculation of resistor and gain values. Noise figure values at various frequencies are shown Figure 31 in the *Typical Characteristics*.



A_V = 9 V/V

Figure 48. Noise Figure Circuit Configuration

8.2.6 Driving Analog to Digital Converters

Analog-to-digital converters present challenging load conditions. They typically have high impedance inputs with large and often variable capacitive components. As well, there are usually current spikes associated with switched capacitor or sample and hold circuits. Figure 49 shows a combination circuit of the LMH6552 driving the ADC12DL080. The two 125-Ω resistors serve to isolate the capacitive loading of the ADC from the amplifier and ensure stability. In addition, the resistors, along with a 2.2-pF capacitor across the outputs (in parallel with the ADC input capacitance), form a low pass anti-aliasing filter with a pole frequency of about 60 MHz. For switched capacitor input ADCs, the input capacitance varies based on the clock cycle, as the ADC switches between the sample and hold mode. See your particular ADC's datasheet for details.

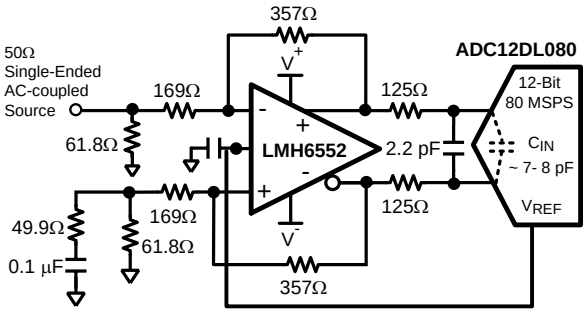


Figure 49. Driving a 12-Bit ADC

Figure 50 illustrates the SFDR and SNR performance vs frequency for the LMH6552 and ADC12DL080 combination circuit with the ADC input signal level at −1 dBFS. The ADC12DL080 is a dual 12-bit ADC with maximum sampling rate of 80 MSPS. The amplifier is configured to provide a gain of 2 V/V in single to differential mode. An external band-pass filter is inserted in series between the input signal source and the amplifier to reduce harmonics and noise from the signal generator. In order to properly match the input impedance seen at the LMH6552 amplifier inputs, R_M is chosen to match Z_S || R_T for proper input balance.

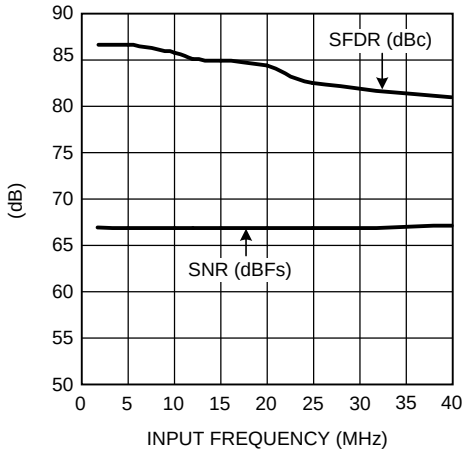


Figure 50. LMH6552/ADC12DL080 SFDR and SNR Performance vs. Frequency

Figure 51 shows a combination circuit of the LMH6552 driving the ADC14DS105. The ADC14DS105 is a dual channel 14-bit ADC with a sampling rate of 105 MSPS. The circuit in Figure 51 has a 2nd order low-pass LC filter formed by the 620 nH inductor along with the 22-pF capacitor across the differential outputs of the LMH6552. The filter has a pole frequency of about 50 MHz. Figure 52 shows the combined SFDR and SNR performance over frequency with a −1 dBFs input signal and a sampling rate of 1000 MSPS.

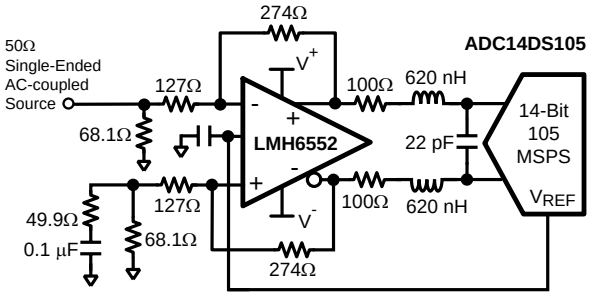


Figure 51. Driving a 14-bit ADC

The amplifier is configured to provide a gain of 2 V/V in a single-to-differential mode. The LMH6552 common mode voltage is set by the ADC14DS105. Circuit testing is the same as described for the LMH6552 and ADC12DL080 combination circuit. The 0.1-µF capacitor, in series with the 49.9-Ω resistor, is inserted to ground across the 68.1Ω-resistor to balance the amplifier inputs.

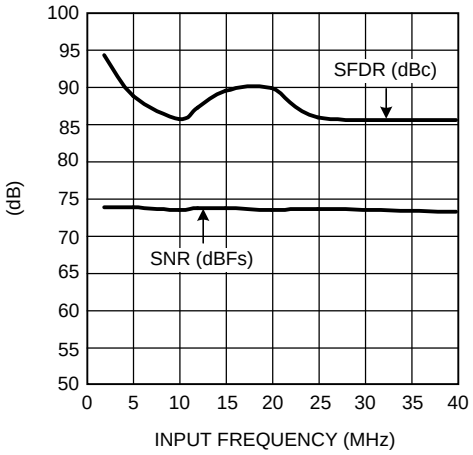


Figure 52. LMH6552/ADC14DS105 SFDR and SNR Performance vs. Frequency

The amplifier and ADC must be located as close as possible. Both devices require that the filter components be in close proximity to them. The amplifier needs to have minimal parasitic loading on the output traces and the ADC is sensitive to high frequency noise that may couple in on its input lines. Some high performance ADCs have an input stage that has a bandwidth of several times its sample rate. The sampling process results in all input signals presented to the input stage mixing down into the first Nyquist zone (DC to Fs/2).

The LMH6552 is capable of driving a variety of Texas Instruments Analog-to-Digital Converters. This is shown in Table 2, which offers a list of possible signal path ADC and amplifier combinations. The use of the LMH6552 to drive an ADC is determined by the application and the desired sampling process (Nyquist operation, sub-sampling or over-sampling). See application note AN-236 for more details on the sampling processes and application note AN-1393 'Using High Speed Differential Amplifiers to Drive ADCs. For more information regarding a particular ADC, refer to the particular ADC datasheet for details.

Table 2. Differential Input ADCs Compatible With LMH6552 Driver

Product Number	Max Sampling Rate (MSPS)	Resolution	Channels
ADC1173	15	8	SINGLE
ADC1175	20	8	SINGLE
ADC08351	42	8	SINGLE
ADC1175-50	50	8	SINGLE
ADC08060	60	8	SINGLE
ADC08L060	60	8	SINGLE
ADC08100	100	8	SINGLE
ADC08200	200	8	SINGLE
ADC08500	500	8	SINGLE
ADC081000	1000	8	SINGLE
ADC08D1000	1000	8	DUAL
ADC10321	20	10	SINGLE
ADC10D020	20	10	DUAL
ADC10030	27	10	SINGLE
ADC10040	40	10	DUAL
ADC10065	65	10	SINGLE
ADC10DL065	65	10	DUAL
ADC10080	80	10	SINGLE
ADC11DL066	66	11	DUAL
ADC11L066	66	11	SINGLE
ADC11C125	125	11	SINGLE

Table 2. Differential Input ADCs Compatible With LMH6552 Driver (continued)

Product Number	Max Sampling Rate (MSPS)	Resolution	Channels
ADC11C170	170	11	SINGLE
ADC12010	10	12	SINGLE
ADC12020	20	12	SINGLE
ADC12040	40	12	SINGLE
ADC12D040	40	12	DUAL
ADC12DL040	40	12	DUAL
ADC12DL065	65	12	DUAL
ADC12DL066	66	12	DUAL
ADC12L063	63	12	SINGLE
ADC12C080	80	12	SINGLE
ADC12DS080	80	12	DUAL
ADC12L080	80	12	SINGLE
ADC12C105	105	12	SINGLE
ADC12DS105	105	12	DUAL
ADC12C170	170	12	SINGLE
ADC14L020	20	14	SINGLE
ADC14L040	40	14	SINGLE
ADC14C080	80	14	SINGLE
ADC14DS080	80	14	DUAL
ADC14C105	105	14	SINGLE
ADC14DS105	105	14	DUAL
ADC14155	155	14	SINGLE

9 Power Supply Recommendations

The LMH6552 can be used with any combination of positive and negative power supplies as long as the combined supply voltage is between 4.5 V and 12 V. The LMH6552 provides best performance when the output voltage is set at the mid supply voltage, and when the total supply voltage is between 9 V and 12 V. When selecting a supply voltage that is less than 9 V, it is important to consider both the input common mode voltage range as well as the output voltage range.

Power supply bypassing as shown in *Power Supply Bypassing* is important and power supply regulation must be within 5% or better using a supply voltage near the edges of the operating range.

9.1 Power Supply Bypassing

The LMH6552 requires supply bypassing capacitors as illustrated in Figure 53 and Figure 54. The 0.01-µF and 0.1-µF capacitors must be leadless SMT ceramic capacitors and must be no more than 3 mm from the supply pins. These capacitors must be star routed with a dedicated ground return plane or trace for best harmonic distortion performance. A small capacitor, ~0.01 µF, placed across the supply rails, and as close to the chip's supply pins as possible, can further improve HD2 performance. Thin traces or small vias reduce the effectiveness of bypass capacitors. Also shown in both figures is a capacitor from the V_{CM} and ENABLE pins to ground. These inputs are high impedance and can provide a coupling path into the amplifier for external noise sources, possibly resulting in loss of dynamic range, degraded CMRR, degraded balance and higher distortion.

Power Supply Bypassing (continued)

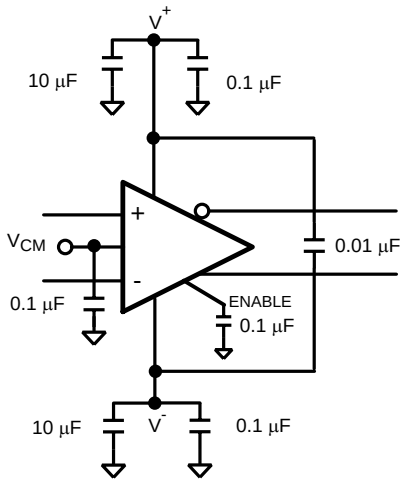


Figure 53. Split Supply Bypassing Capacitors

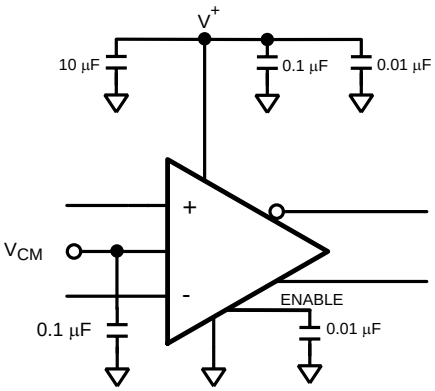


Figure 54. Single Supply Bypassing Capacitors

10 Layout

10.1 Layout Guidelines

The LMH6552 is a very high performance amplifier. In order to get maximum benefit from the differential circuit architecture board layout and component selection is very critical. The circuit board must have a low inductance ground plane and well bypassed broad supply lines. External components must be leadless surface mount types. The feedback network and output matching resistors must be composed of short traces and precision resistors (0.1%). The output matching resistors must be placed within 3 or 4 mm of the amplifier as must the supply bypass capacitors. Refer to *Power Supply Bypassing* for recommendations on bypass circuit layout. Evaluation boards are available free of charge through the product folder on ti.com.

By design, the LMH6552 is relatively insensitive to parasitic capacitance at its inputs. Nonetheless, ground and power plane metal must be removed from beneath the amplifier and from beneath R_F and R_G for best performance at high frequency.

With any differential signal path, symmetry is very important. Even small amounts of asymmetry can contribute to distortion and balance errors.

10.2 Layout Example

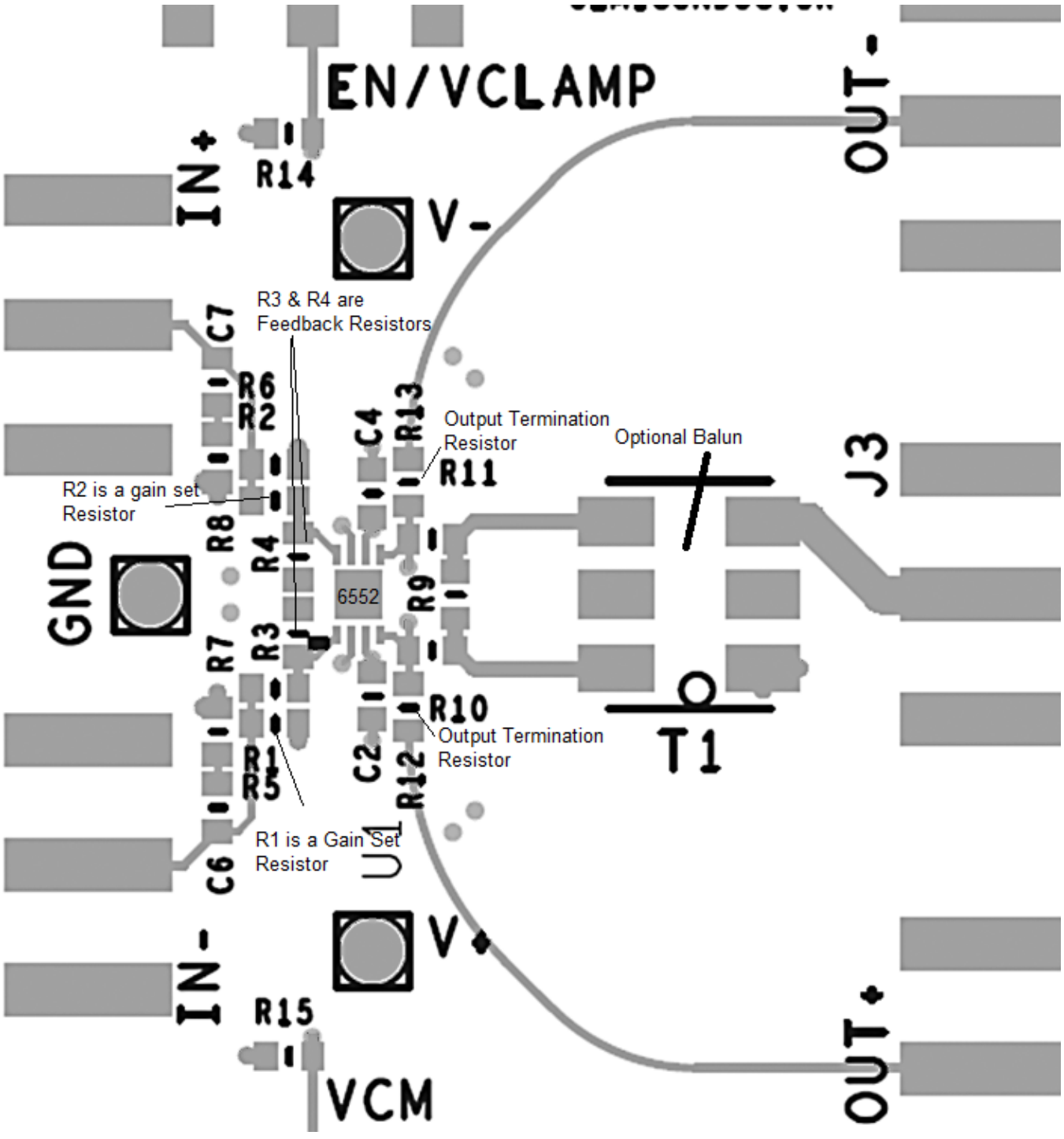


Figure 55. Layout Schematic

10.3 Thermal Considerations

The WSON package is designed for enhanced thermal performance and features an exposed die attach pad (DAP) at the bottom center of the package that creates a direct path to the PCB for maximum power dissipation. The DAP is floating and is not electrically connected to internal circuitry. Compared to the traditional leaded packages where the die attach pad is embedded inside the molding compound, the WSON reduces one layer in the thermal path.

The thermal advantage of the WSON package is fully realized only when the exposed die attach pad is soldered down to a thermal land on the PCB board with thermal vias planted underneath the thermal land. The thermal land can be connected to any power or ground plane within the allowable supply voltage range of the device. Based on thermal analysis of the WSON package, the junction-to-ambient thermal resistance (θ_{JA}) can be improved by a factor of two when the die attach pad of the WSON package is soldered directly onto the PCB with thermal land and thermal vias are 1.27 mm and 0.33 mm respectively. Typical copper via barrel plating is 1 oz, although thicker copper may be used to further improve thermal performance.

For more information on board layout techniques, refer to Application Note 1187 *Leadless Lead Frame Package (LLP)*. This application note also discusses package handling, solder stencil and the assembly process.

10.4 Power Dissipation

The LMH6552 is optimized for maximum speed and performance in the small form factor of the standard SOIC package, and is essentially a dual channel amplifier. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the $T_{JMAX}$of 150°C is never exceeded due to the overall power dissipation.

Follow these steps to determine the maximum power dissipation for the LMH6552:

1. Calculate the quiescent (no-load) power:

   $P_{AMP} = I_{CC}* (V_S)$

   where

   - $V_S = V^+ - V^-$. (Be sure to include any current through the feedback network if V_{OCM} is not mid-rail.) (1)

2. Calculate the RMS power dissipated in each of the output stages:

   P_D (rms) = rms $((V_S - V^+_{OUT}) * I^+_{OUT})$ + rms $((V_S - V^-_{OUT}) * I^-_{OUT})$

   where

   - V_{OUT} and I_{OUT} are the voltage and the current measured at the output pins of the differential amplifier as if they were single ended amplifiers and V_S is the total supply voltage (2)

3. Calculate the total RMS power:

   $P_T = P_{AMP} + P_D$ (3)

The maximum power that the LMH6552 package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150° – T_{AMB})/ \theta_{JA}$

where

- T_{AMB} = Ambient temperature (°C)
- θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W)
- For the SOIC package θ_{JA} is 150°C/W
- For WSON package θ_{JA} is 58°C/W (4)

NOTE

If V_{CM} is not 0V then there is quiescent current flowing in the feedback network. This current must be included in the thermal calculations and added into the quiescent power dissipation of the amplifier.

10.5 ESD Protection

The LMH6552 is protected against electrostatic discharge (ESD) on all pins. The LMH6552 can survive 2000 V Human Body model and 200 V Machine model events. Under normal operation the ESD diodes have no affect on circuit performance. There are occasions, however, when the ESD diodes are evident. If the LMH6552 is driven by a large signal when the device is powered down the ESD diodes conduct. The current that flows through the ESD diodes either exits the chip through the supply pins or flows through the device, hence a chip can be powered up with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Leadless Lead Frame Package (LLP), SNOA401

11.2.1.1 Evaluation Board

See the LMH6552 Product Folder for evaluation board availability and ordering information.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH6552MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 52MA
LMH6552MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 52MA
LMH6552MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 52MA
LMH6552MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 52MA
LMH6552SD/NOPB	Active	Production	WSON (NGS) | 8	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	6552
LMH6552SD/NOPB.A	Active	Production	WSON (NGS) | 8	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	6552

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

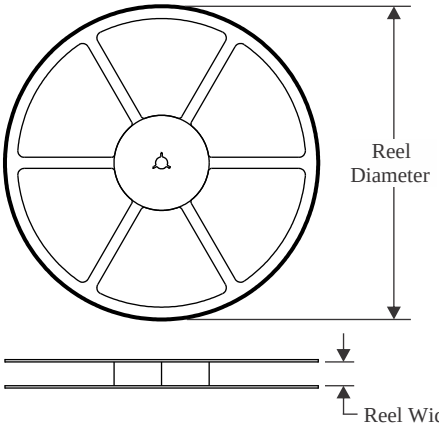
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

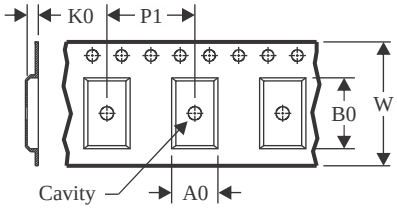
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

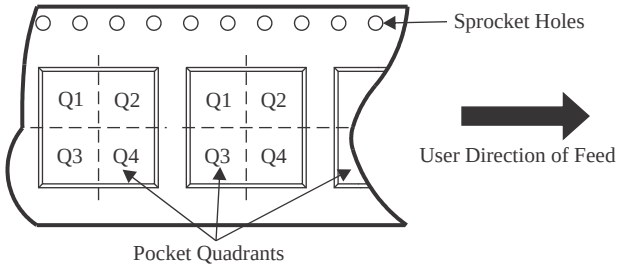


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

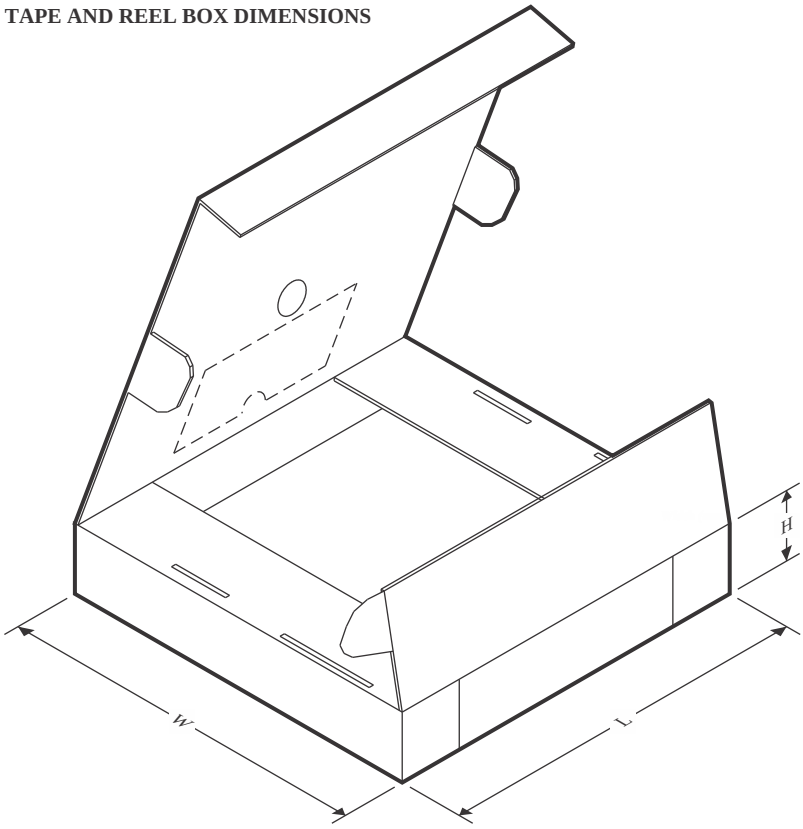
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6552MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6552SD/NOPB	WSON	NGS	8	1000	177.8	12.4	3.3	2.8	1.0	8.0	12.0	Q1

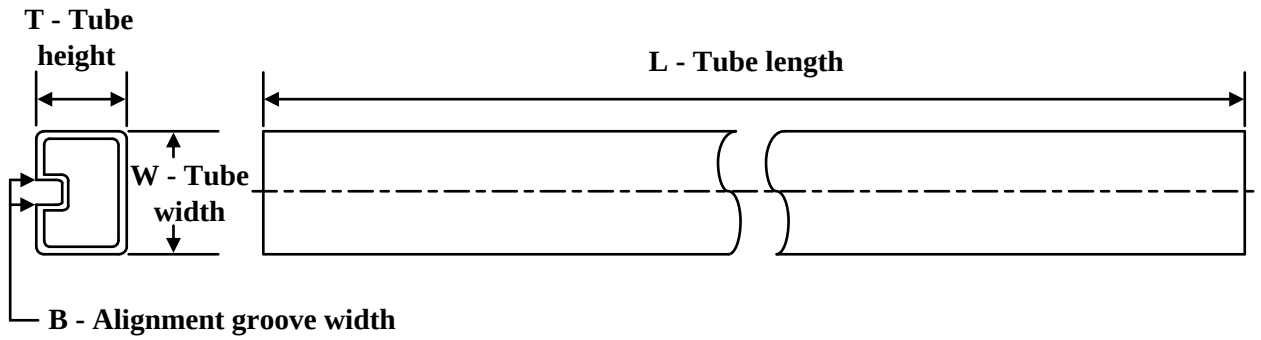
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6552MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6552SD/NOPB	WSON	NGS	8	1000	208.0	191.0	35.0

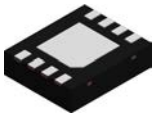
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6552MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMH6552MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05

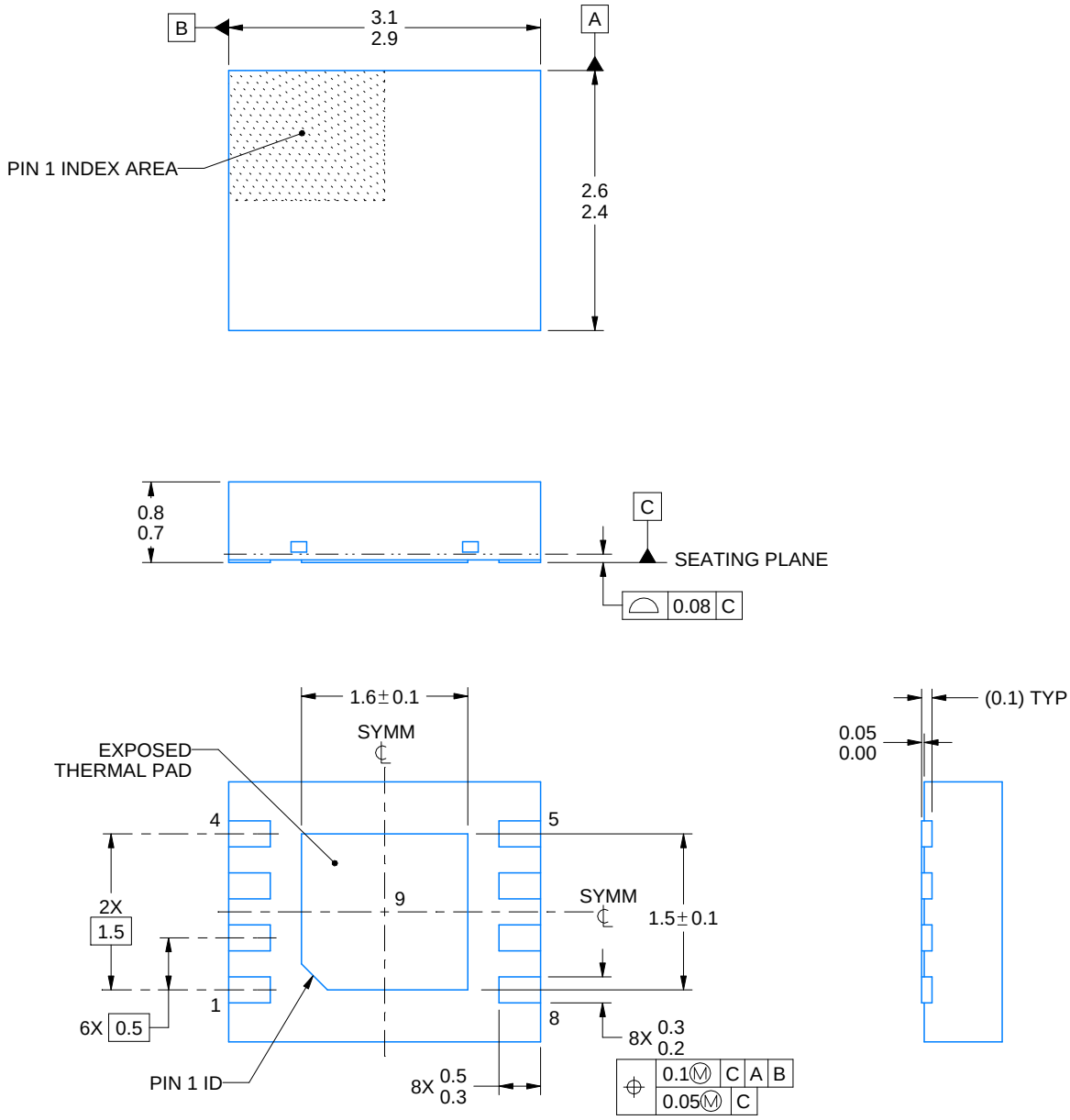
NGS0008C



PACKAGE OUTLINE

WSON - 0.8 mm max height

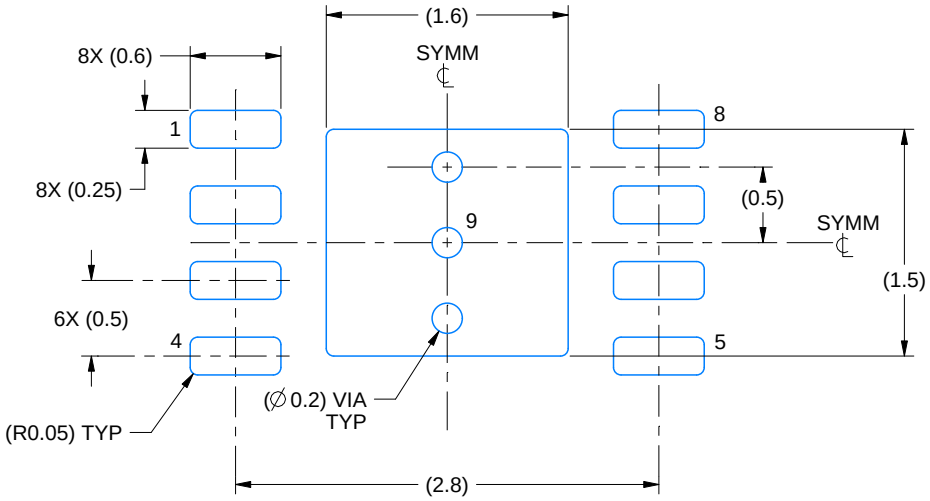
PLASTIC SMALL OUTLINE - NO LEAD



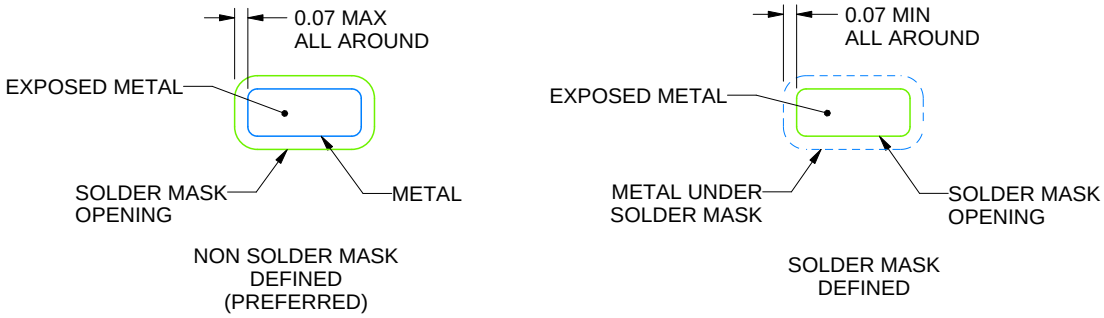
4214924/A 07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

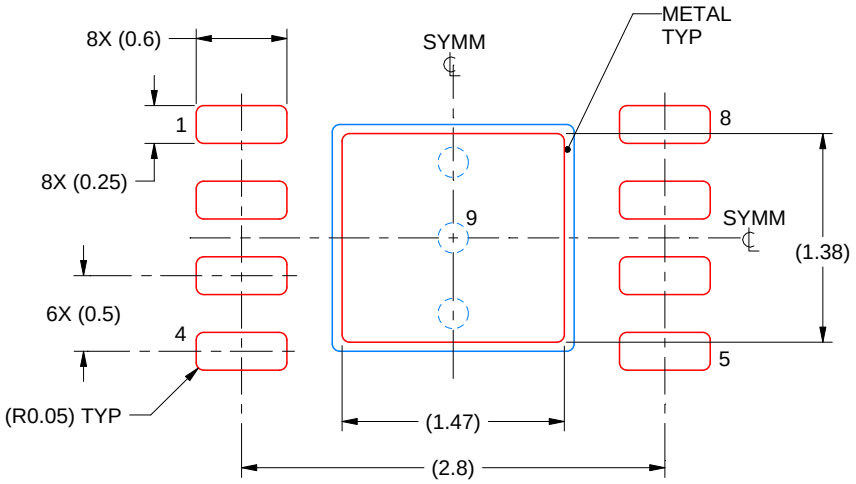


SOLDER MASK DETAILS

4214924/A 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



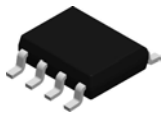
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214924/A 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

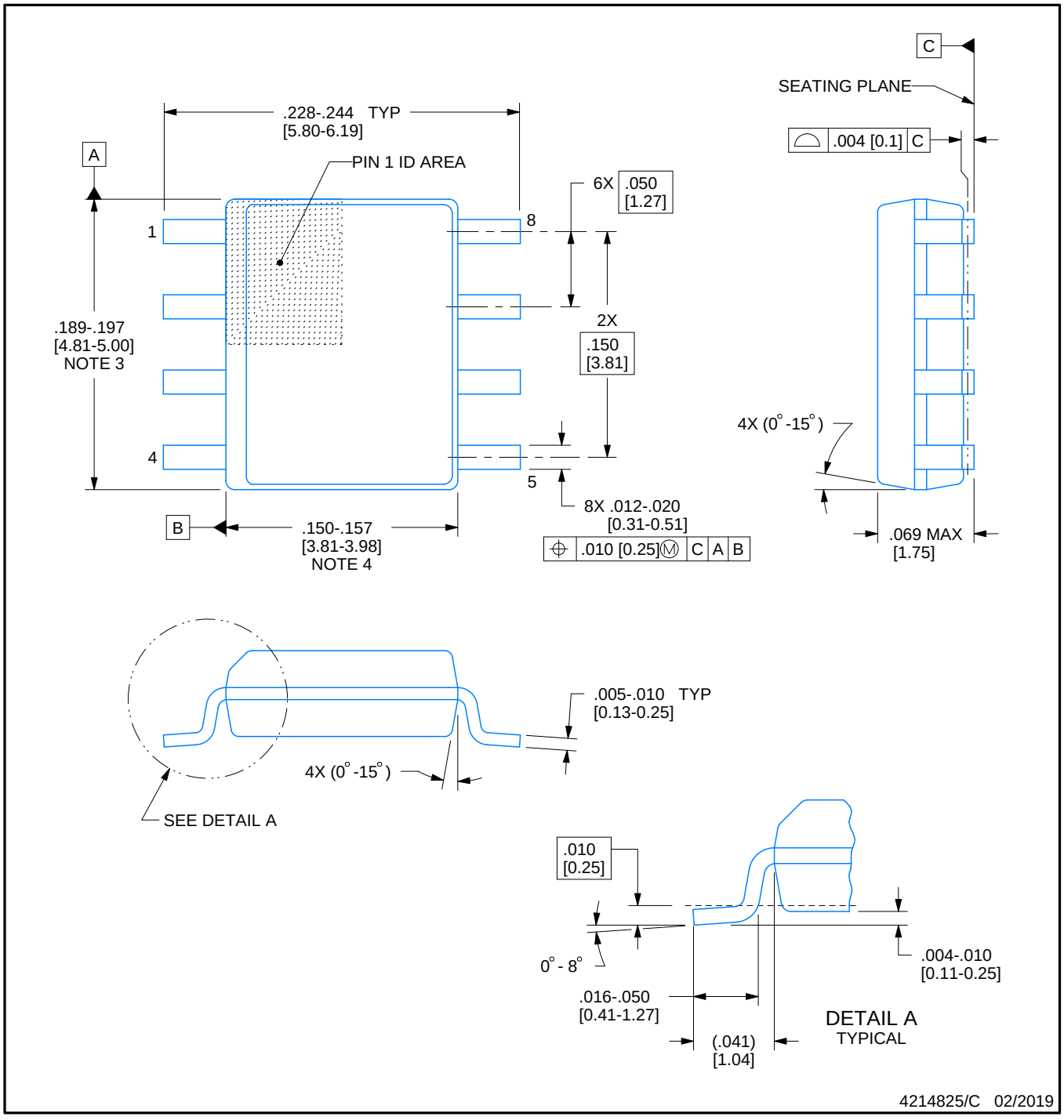


PACKAGE OUTLINE

D0008A

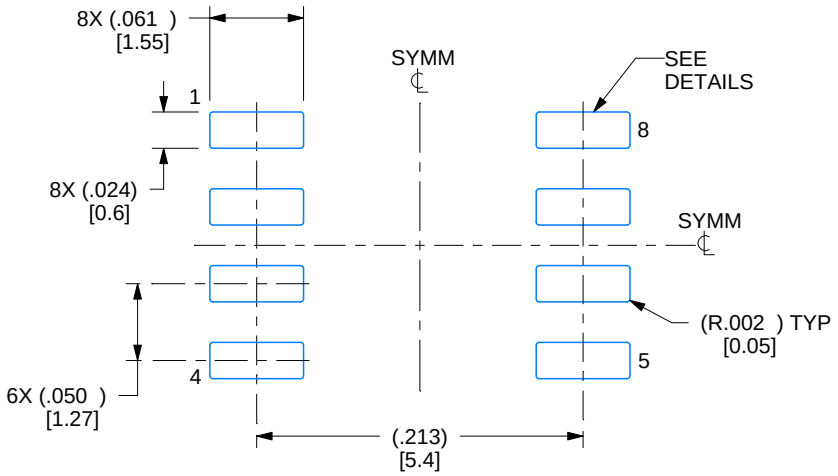
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

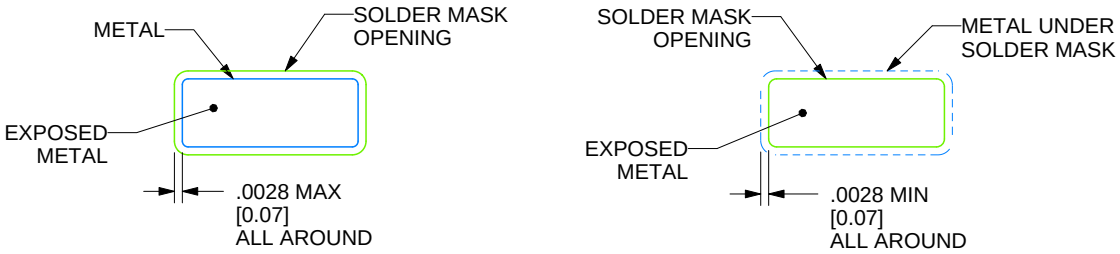


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

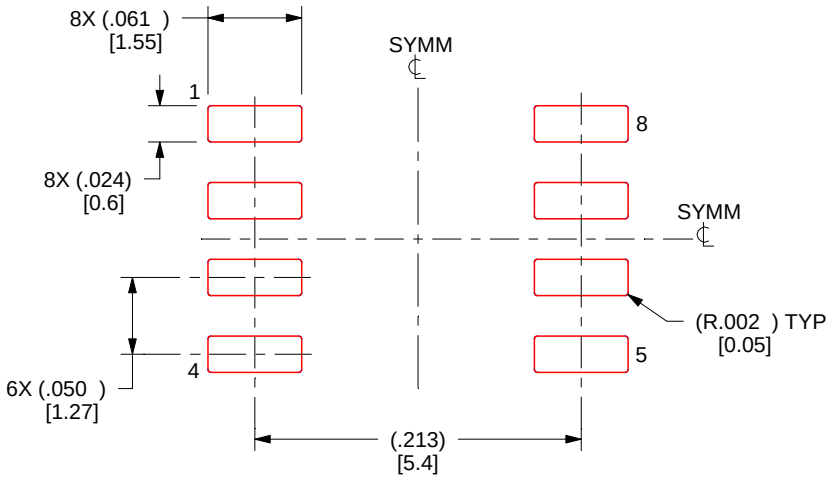
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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