LPV521 毫微功耗、1.8V、RRIO、CMOS 输入运算放大器

1 特性

- V_S = 5V 时的典型值（除非另有说明）：
  - 电源电流 (V_{CM} = 0.3V)：400nA（最大值）
  - 工作电压范围：1.6V 至 5.5V
  - 低 TCV_{OS}：3.5μV/°C（最大值）
  - V_{OS}：1mV（最大值）
  - 输入偏置电流：40fA
  - PSRR：109dB
  - CMRR：102dB
  - 开环增益：132dB
  - 增益带宽积：6.2kHz
  - 压摆率： 2.4V/ms
  - 输入电压噪声 (f = 100Hz)：255nV/ $\sqrt{Hz}$
  - 温度范围：-40°C 至 +125°C

2 应用

- 无线环境传感器
- 电网资产监控
- 电表
- 烟雾和热量探测器
- 气体检测仪
- 便携式电子产品
- 恒温器
- 现场变送器和传感器

3 说明

LPV521 是一款单通道毫微功耗 552nW 放大器，专为超长使用寿命电池应用而设计。1.6V 至 5.5V 工作电压范围和 351nA 典型电源电流使得该器件非常适合 RFID 阅读器和远程传感器毫微功耗应用。该器件具有超出电源轨 0.1V 的输入共模电压、指定 TCV_{OS} 和电压摆幅接近电源轨输出性能。LPV521 具有经过精心设计的 CMOS 输入级，具有 40fA I_{BIAS} 电流（典型值），优于竞争产品。较低的输入电流能够显著降低在兆欧级电阻、高阻抗光电二极管和充电检测应用中引入的 I_{BIAS} 和 I_{OS} 误差。LPV521 是 PowerWise® 系列产品的一员，具有出色的功耗/性能比。

宽输入共模电压范围、指定的 1mV V_{OS} 和 3.5μV/°C TCVOS 支持在高侧和低侧电流检测中实现精确、稳定的测量。

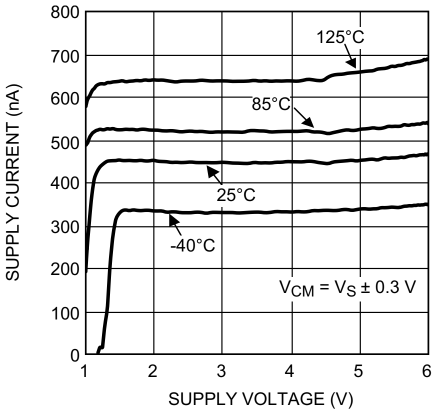
该器件集成了 EMI 保护，可降低对来自手机或其他 RFID 阅读器的意外 RF 信号的敏感度。

LPV521 采用 5 引脚 SC70 和 8 引脚 PDIP 封装。

封装信息

器件型号	封装[1]	封装尺寸[2]
LPV521	DCK（SC70，5）	2mm × 2.1mm
	P（PDIP，8）	9.81mm × 9.43mm

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



毫微功耗电源电流

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4 Pin Configuration and Functions

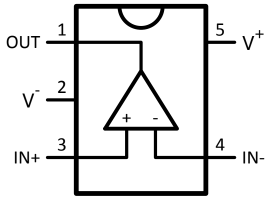
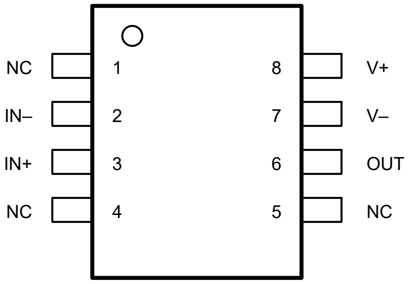


图 4-1. DCK Package, 5-Pin SC70 (Top View)



Not to scale

图 4-2. P Package, 8-Pin PDIP (Top View)

表 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	DCK (SC70)	P (PDIP)		
IN+	3	3	Input	Noninverting input
IN –	4	2	Input	Inverting input
OUT	1	6	Output	Output
NC	—	1, 4, 5	—	Do not connect
V+	5	8	Power	Positive power supply
V –	2	7	Power	Negative power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Any pin relative to V^-		−0.3	6	V
	Input voltage, IN+, IN−, OUT pins		$V^- - 0.3$	$V^+ + 0.3$	V
	Input current, V^+, V^-, OUT pins			40	mA
	Differential input voltage ($V_{IN+} - V_{IN-}$)		−300	300	mV
T_J	Junction temperature(2)		−40	150	°C
	Mounting temperature	Infrared or convection (30s)		260	°C
		Wave soldering lead temperature (4s)		260	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The maximum power dissipation is a function of TJ(MAX), θJA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(MAX) – TA) / θJA. All numbers apply for packages soldered directly onto a printed circuit board (PCB).

5.2 ESD Ratings

			VALUE	UNIT
DCK (SC70) PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM) per JEDEC specification JESD22-C101(2)	±1000	
		Machine model	±200	
P (PDIP) PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002(2)	±1000	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, $V_S = (V+) - (V-)$	1.6		5.5	V
T_A	Temperature(2)	−40		125	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not tested. For tested specifications and test conditions, see *Electrical Characteristics*.

(2) The maximum power dissipation is a function of TJ(MAX), θJA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(MAX) – TA) / θJA. All numbers apply for packages soldered directly onto a PCB.

5.4 Thermal Information

THERMAL METRIC[1]		LPV521		UNIT
		DCK (SC70)	P (PDIP)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	456	102.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	53.9	81.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.9	64.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	47.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.3	64.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

(2) The maximum power dissipation is a function of TJ(MAX), θ JA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(MAX) – TA) / θ JA. All numbers apply for packages soldered directly onto a PCB.

5.5 Electrical Characteristics

at T_A = 25°C, V^+ = 1.8V, 3.3V, and 5V, V^- = 0V, $V_{CM} = V_O = V_S / 2$, and $R_L > 1\ M\Omega$ (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	$V_{CM} = V^- + 0.3V$		–1	0.1	1	mV
			T_A = –40°C to +125°C	–1.23		1.23	
		$V_{CM} = V^+ - 0.3V$		–1	0.1	1	
			T_A = –40°C to +125°C	–1.23		1.23	
TCV_{OS}	Input offset voltage drift[2]				±0.4		μV/°C
		T_A = –40°C to +125°C	V^+ = 1.8V, 3.3V	–3		3	
			V^+ = 5V	–3.5		3.5	
PSRR	Power-supply rejection ratio	$1.6V \leq V^+ \leq 5.5V$, V_{CM} = 0.3V		85	109		dB
			T_A = –40°C to +125°C	76			
INPUT BIAS CURRENT							
I_{BIAS}	Input bias current	V^+ = 1.8V, 3.3V		–1	0.01	1	pA
		V^+ = 5V		–1	0.04	1	
		T_A = –40°C to +125°C		–50		+50	
I_{OS}	Input offset current	V^+ = 1.8V			10		fA
		V^+ = 3.3V			20		
		V^+ = 5V			60		
NOISE							
	Input-referred voltage noise	V^+ = 1.8V			24		μV_{PP}
		V^+ = 3.3V, 5V			22		
e_n	Input-referred voltage noise density	f = 100Hz	V^+ = 1.8V		265		$nV/\sqrt{Hz}$
			V^+ = 3.3V		259		
			V^+ = 5V		255		
i_n	Input-referred current noise	f = 100Hz			100		$fA/\sqrt{Hz}$

5.5 Electrical Characteristics （续）

at T_A = 25°C, V^+ = 1.8V, 3.3V, and 5V, V^- = 0V, $V_{CM} = V_O = V_S / 2$, and $R_L > 1\ M\Omega$ (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE							
CMRR	Common-mode rejection ratio	$V^- \leqslant V_{CM} \leqslant V^+$	V^+ = 1.8V	66	92		dB
			V^+ = 1.8V, T_A = –40°C to +125°C	60			
			V^+ = 3.3V	72	97		
			V^+ = 3.3V, T_A = –40°C to +125°C	70			
			V^+ = 5V	75	102		
			V^+ = 5V, T_A = –40°C to +125°C	74			
		$V^- \leqslant V_{CM} \leqslant V^+ - 1.1V$	V^+ = 1.8V	75	101		
			V^+ = 1.8V, T_A = –40°C to +125°C	74			
			V^+ = 3.3V	78	106		
			V^+ = 3.3V, T_A = –40°C to +125°C	75			
			V^+ = 5V	84	108		
			V^+ = 5V, T_A = –40°C to +125°C	80			
		$V^+ - 0.6V \leqslant V_{CM} \leqslant V^+$	V^+ = 1.8V	75	120		
			V^+ = 1.8V, T_A = –40°C to +125°C	53			
			V^+ = 3.3V	77	121		
			V^+ = 3.3V, T_A = –40°C to +125°C	76			
			V^+ = 5V	77	115		
			V^+ = 5V, T_A = –40°C to +125°C	76			
CMVR	Common-mode voltage range	V^+ = 1.8V, CMRR ⩾ 67dB, V^+ = 3.3V, CMRR ⩾ 72dB, V^+ = 5V, CMRR ⩾ 75dB		$(V^-) - 0.1$		$(V^+) + 0.1$	V
		T_A = –40°C to +125°C, V^+ = 1.8V, CMRR ⩾ 60dB, V^+ = 3.3V, CMRR ⩾ 70dB, V^+ = 5V, CMRR ⩾ 74dB		(V^-)		(V^+)	V
OPEN-LOOP GAIN							
A_{VOL}	Large-signal voltage gain	$V^- + 0.5V \leqslant V_O \leqslant V^+ - 0.5V$, R_L = 100kΩ to $V^+/2$	V^+ = 1.8V	74	125		dB
			V^+ = 1.8V, T_A = –40°C to +125°C	73			
			V^+ = 3.3V	82	120		
			V^+ = 3.3V, T_A = –40°C to +125°C	76			
			V^+ = 5V	84	132		
			V^+ = 5V, T_A = –40°C to +125°C	76			
FREQUENCY RESPONSE							
GBW	Gain bandwidth product	C_L = 20pF, R_L = 100kΩ	V^+ = 1.8V		6.1		kHz
			V^+ = 3.3V, 5V		6.2		
SR	Slew rate	Falling edge, A_V = +1, $V_{IN} = V^+$ to V^-	V^+ = 1.8V		2.9		V/ms
			V^+ = 3.3V		2.9		
			V^+ = 5V	1.1	2.7		
			V^+ = 5V, T_A = –40°C to +125°C	1.2			
		Rising edge, A_V = +1, $V_{IN} = V^-$ to V^+	V^+ = 1.8V		2.3		
			V^+ = 3.3V		2.5		
			V^+ = 5V	1.1	2.4		
			V^+ = 5V, T_A = –40°C to +125°C	1.2			
θ_m	Phase margin	C_L = 20pF, R_L = 100kΩ	V+ = 1.8V		72		deg
			V^+ = 3.3V, 5V		73		
G_m	Gain margin	C_L = 20pF, R_L = 100kΩ	V^+ = 1.8V, 3.3V		19		dB
			V+ = 5V		20		

5.5 Electrical Characteristics（续）

at T_A = 25°C, V^+ = 1.8V, 3.3V, and 5V, V^- = 0V, V_{CM} = V_O = V_S / 2, and R_L > 1 MΩ (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Output voltage	Swing from positive rail, R_L = 100kΩ to V^+/2, V_{IN}(diff) = 100mV	V^+ = 1.8V		2	50	mV
			V^+ = 1.8V, T_A = –40°C to +125°C			50	
			V^+ = 3.3V		3	50	
			V^+ = 3.3V, T_A = –40°C to +125°C			50	
			V^+ = 5V		3	50	
			V^+ = 5V, T_A = –40°C to +125°C			50	
		Swing from negative rail, R_L = 100kΩ to V^+/2, V_{IN}(diff) = –100mV	V^+ = 1.8V		2	50	
			V^+ = 1.8V, T_A = –40°C to +125°C			50	
			V^+ = 3.3V		2	50	
			V^+ = 3.3V, T_A = –40°C to +125°C			50	
			V^+ = 5V		3	50	
			V^+ = 5V, T_A = –40°C to +125°C			50	
I_O	Output current(3)	Sourcing, V_O to V^-, V_{IN}(diff) = 100mV	V^+ = 1.8V	1	3		mA
			V^+ = 1.8V, T_A = –40°C to +125°C	0.5			
			V^+ = 3.3V	5	11		
			V^+ = 3.3V, T_A = –40°C to +125°C	4			
			V^+ = 5V	15	23		
			V^+ = 5V, T_A = –40°C to +125°C	8			
		Sinking, V_O to V^+, V_{IN}(diff) = –100mV	V^+ = 1.8V	1	3		
			V^+ = 1.8V, T_A = –40°C to +125°C	0.5			
			V^+ = 3.3V	5	12		
			V^+ = 3.3V, T_A = –40°C to +125°C	4			
			V^+ = 5V	15	22		
			V^+ = 5V, T_A = –40°C to +125°C	8			

5.5 Electrical Characteristics（续）

at T_A = 25°C, V^+ = 1.8V, 3.3V, and 5V, V^- = 0V, V_{CM} = V_O = V_S / 2, and R_L > 1 MΩ (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_S	Supply current	V_{CM} = V^- + 0.3 V	V^+ = 1.8V		345	400	nA
			V^+ = 1.8V, T_A = –40°C to +125°C			580	nA
			V^+ = 3.3V		346	400	nA
			V^+ = 3.3V, T_A = –40°C to +125°C			600	nA
			V^+ = 5V		351	400	nA
			V^+ = 5V, T_A = –40°C to +125°C			620	nA
		V_{CM} = V^+ – 0.3 V	V^+ = 1.8V		472	600	nA
			V^+ = 1.8V, T_A = –40°C to +125°C			850	nA
			V^+ = 3.3V		471	600	nA
			V^+ = 3.3V, T_A = –40°C to +125°C			860	nA
			V^+ = 5V		475	600	nA
			V^+ = 5V, T_A = –40°C to +125°C			870	nA
NOISE IMMUNITY							
EMIRR	EMI rejection ratio, IN+ and IN– (4)	V^+ = 5V, V_{RF_PEAK} = 100mV$_P$ (–20dB$_P$)	f = 400MHz		121		dB
			f = 900MHz		121		
			f = 1800MHz		124		
			f = 2400MHz		142		

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No min and max specifications of parametric performance are indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

(2) The offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.

(3) The short circuit test is a momentary open-loop test.

(4) The EMI rejection ratio is defined as EMIRR = 20log (V_{RF_PEAK}/ ΔV_{OS}).

5.6 Typical Characteristics

at T_J = 25°C (unless otherwise specified)

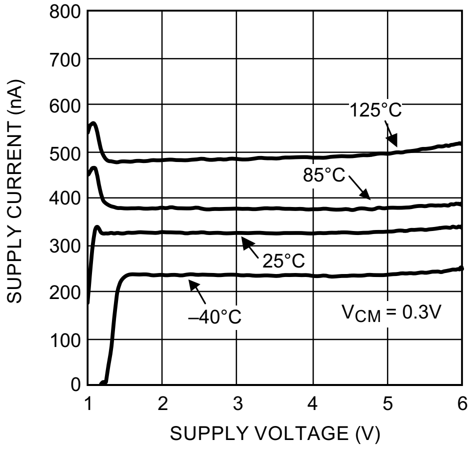


图 5-1. Supply Current vs Supply Voltage

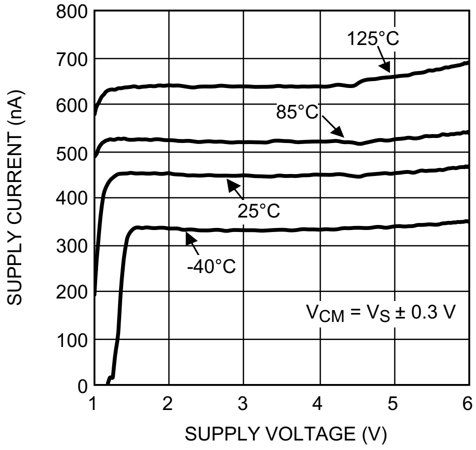


图 5-2. Supply Current vs Supply Voltage

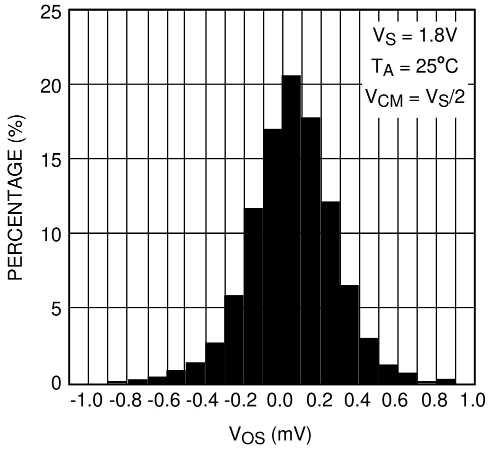


图 5-3. Offset Voltage Distribution

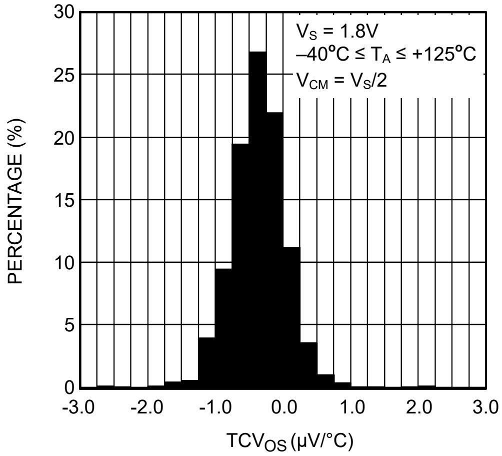


图 5-4. Tcv$_{OS}$ Distribution

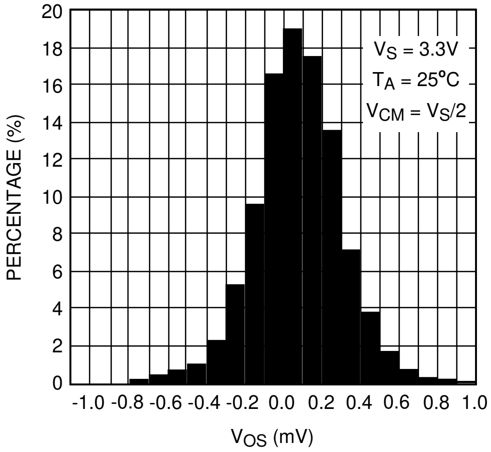


图 5-5. Offset Voltage Distribution

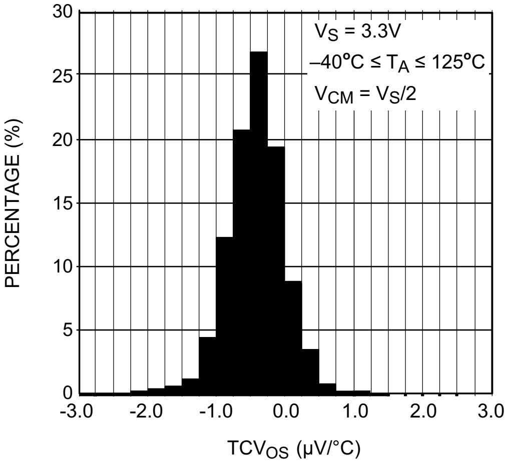


图 5-6. Tcv$_{OS}$ Distribution

5.6 Typical Characteristics (continued)

at T_J = 25°C (unless otherwise specified)

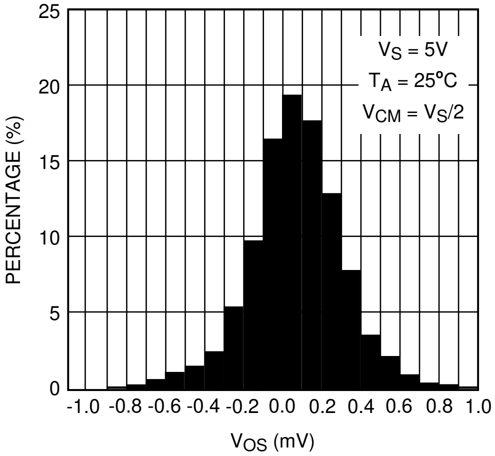


图 5-7. Offset Voltage Distribution

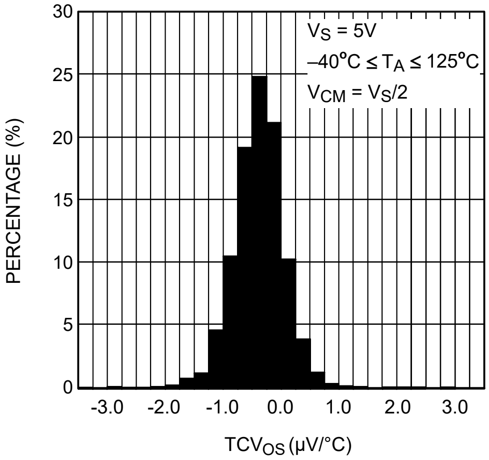


图 5-8. Tcv_{OS} Distribution

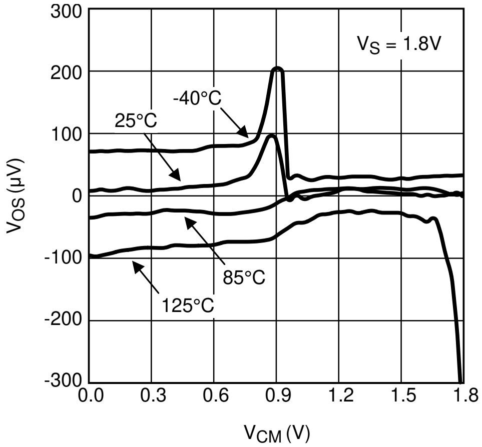


图 5-9. Input Offset Voltage vs Input Common Mode

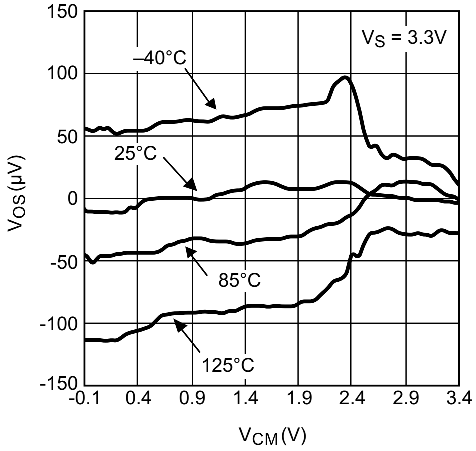


图 5-10. Input Offset Voltage vs Input Common Mode

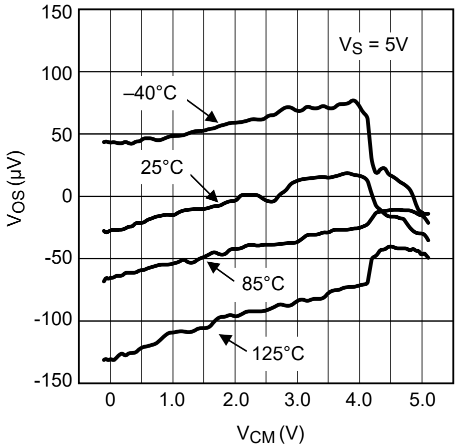


图 5-11. Input Offset Voltage vs Input Common Mode

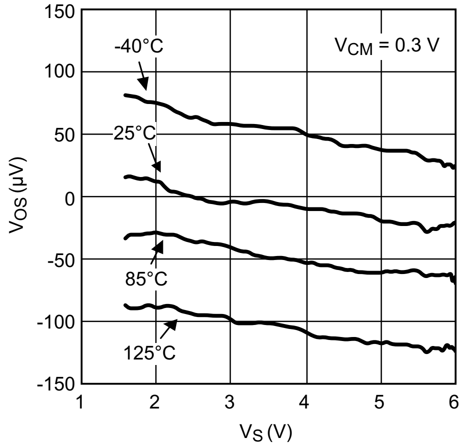


图 5-12. Input Offset Voltage vs Supply Voltage

5.6 Typical Characteristics (continued)

at T_J = 25°C (unless otherwise specified)

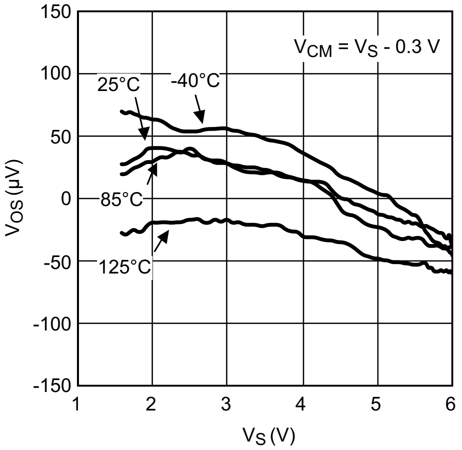


图 5-13. Input Offset Voltage vs Supply Voltage

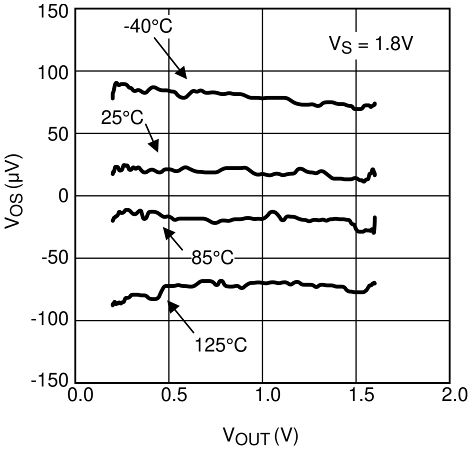


图 5-14. Input Offset Voltage vs Output Voltage

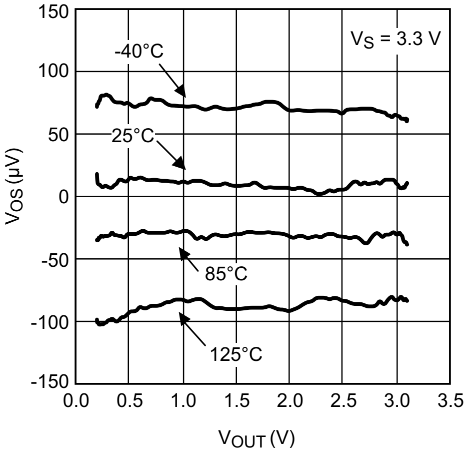


图 5-15. Input Offset Voltage vs Output Voltage

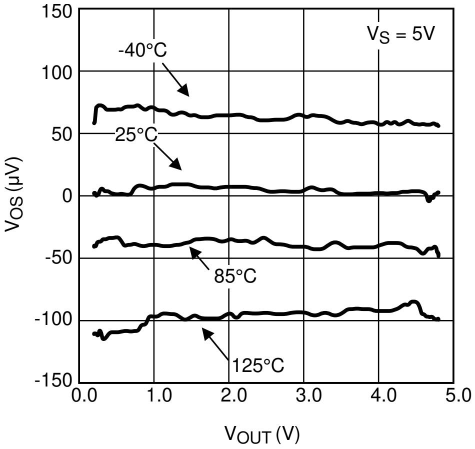


图 5-16. Input Offset Voltage vs Output Voltage

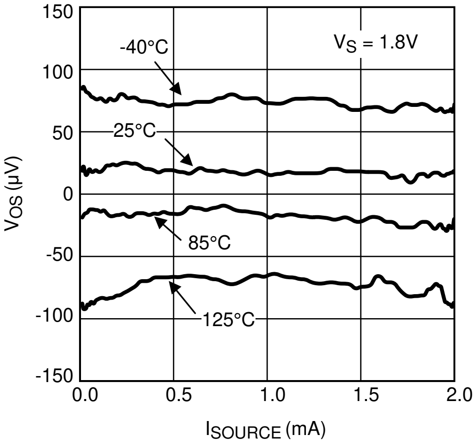


图 5-17. Input Offset Voltage vs Sourcing Current

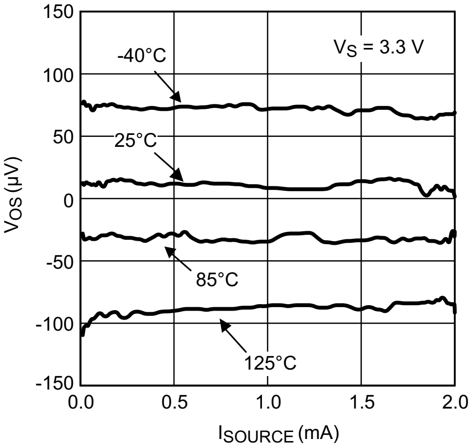


图 5-18. Input Offset Voltage vs Sourcing Current

5.6 Typical Characteristics (continued)

at T_J = 25°C (unless otherwise specified)

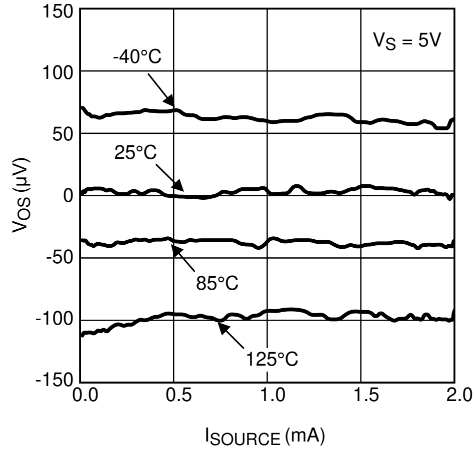


图 5-19. Input Offset Voltage vs Sourcing Current

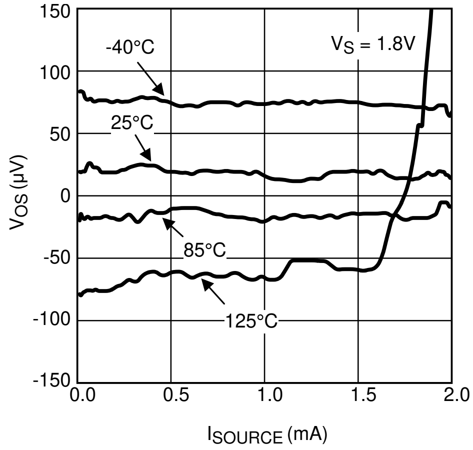


图 5-20. Input Offset Voltage vs Sinking Current

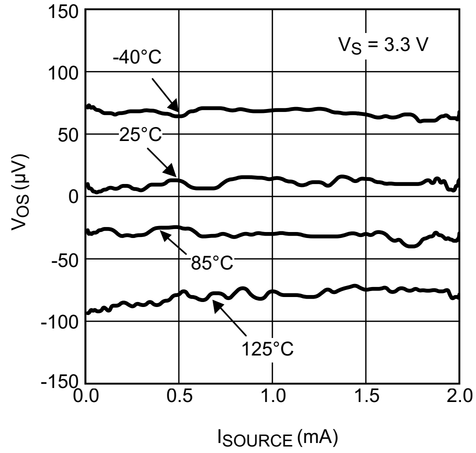


图 5-21. Input Offset Voltage vs Sinking Current

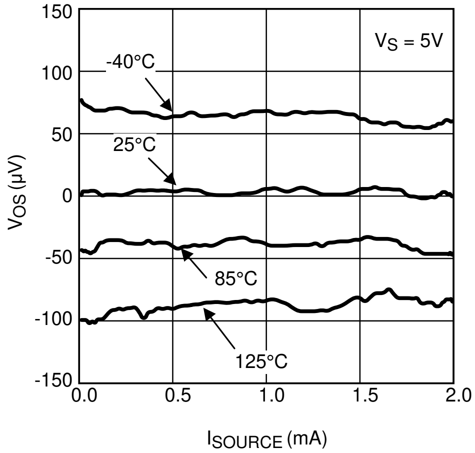


图 5-22. Input Offset Voltage vs Sinking Current

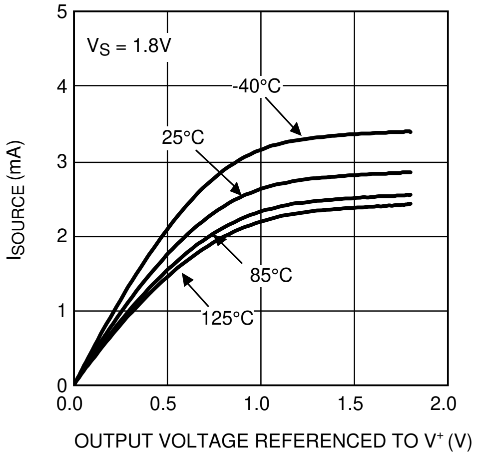


图 5-23. Sourcing Current vs Output Voltage

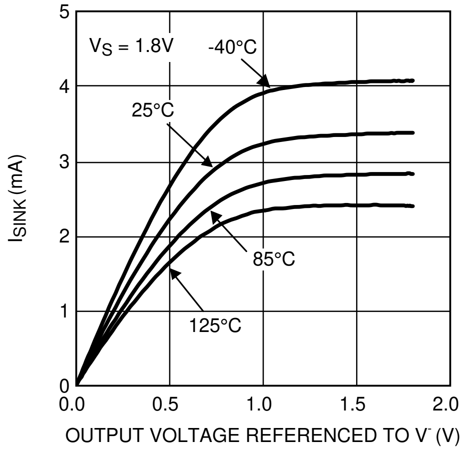


图 5-24. Sinking Current vs Output Voltage

5.6 Typical Characteristics (continued)

at T_J = 25°C (unless otherwise specified)

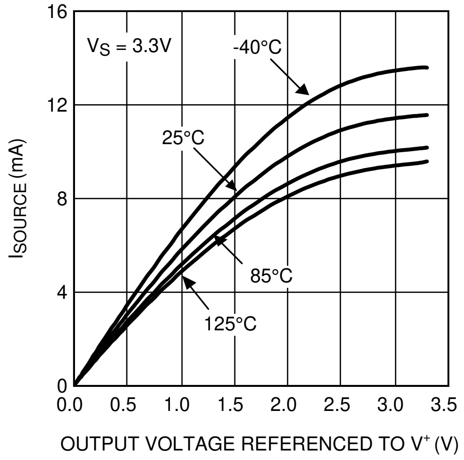


图 5-25. Sourcing Current vs Output Voltage

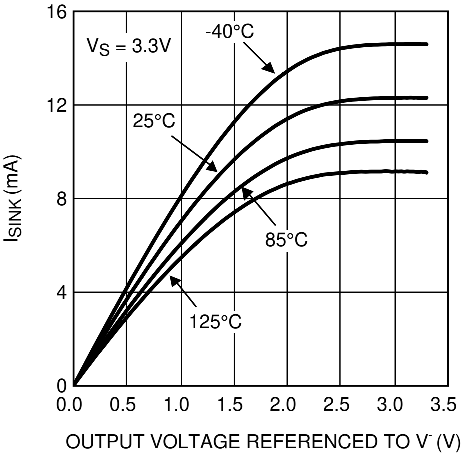


图 5-26. Sinking Current vs Output Voltage

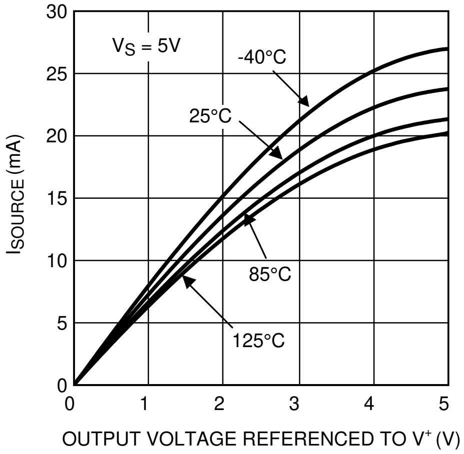


图 5-27. Sourcing Current vs Output Voltage

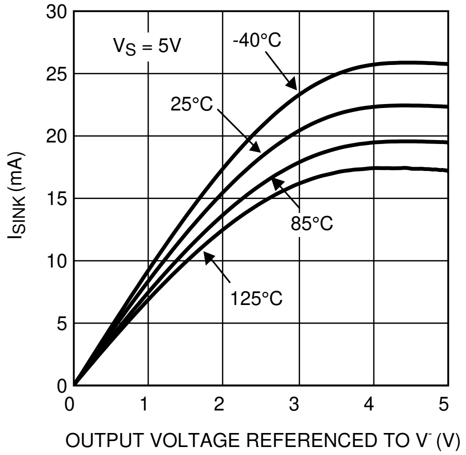


图 5-28. Sinking Current vs Output Voltage

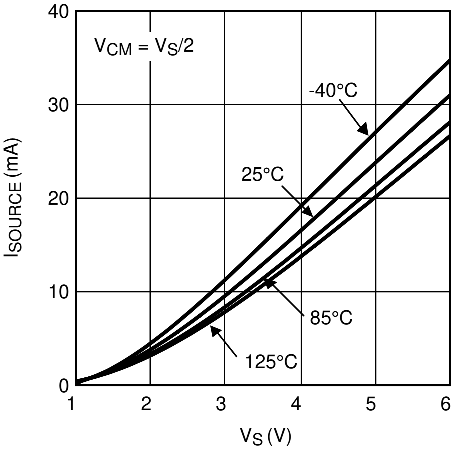


图 5-29. Sourcing Current vs Supply Voltage

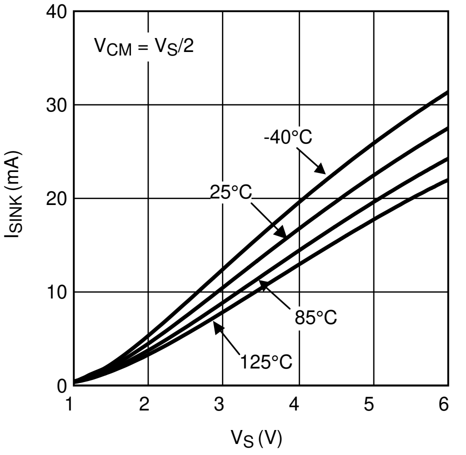


图 5-30. Sinking Current vs Supply Voltage

5.6 Typical Characteristics (continued)

at T_J = 25°C (unless otherwise specified)

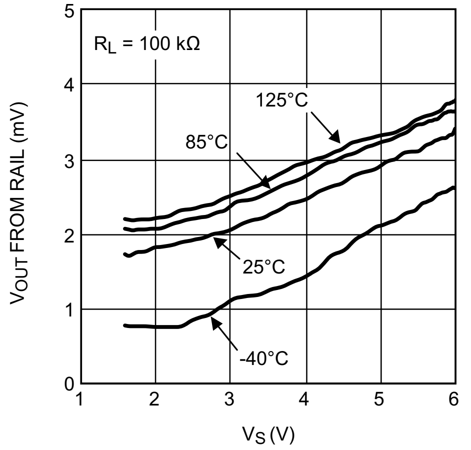


图 5-31. Output Swing High vs Supply Voltage

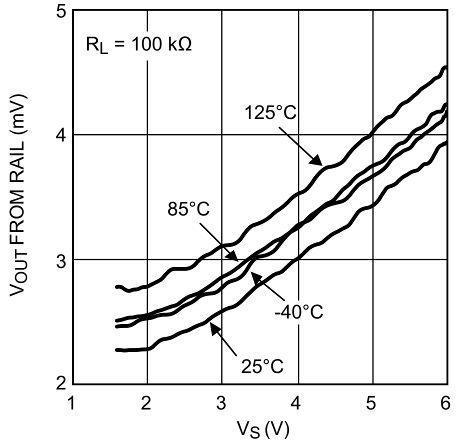


图 5-32. Output Swing Low vs Supply Voltage

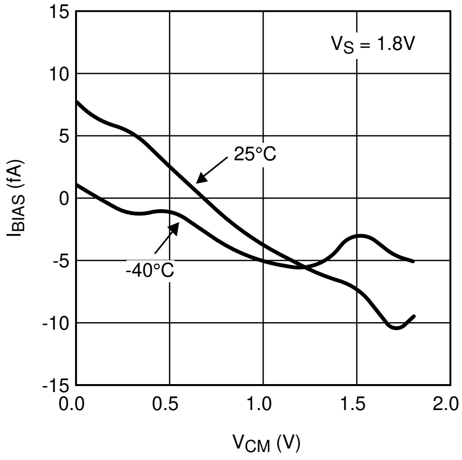


图 5-33. Input Bias Current vs Common Mode Voltage

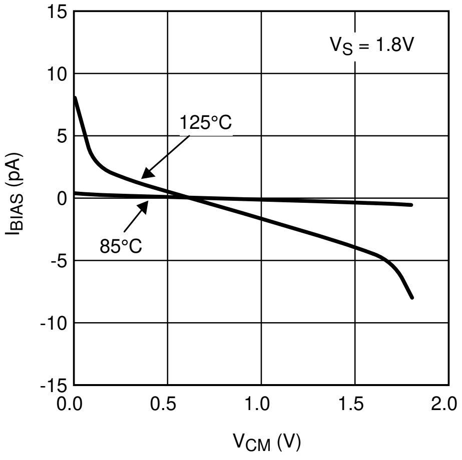


图 5-34. Input Bias Current vs Common Mode Voltage

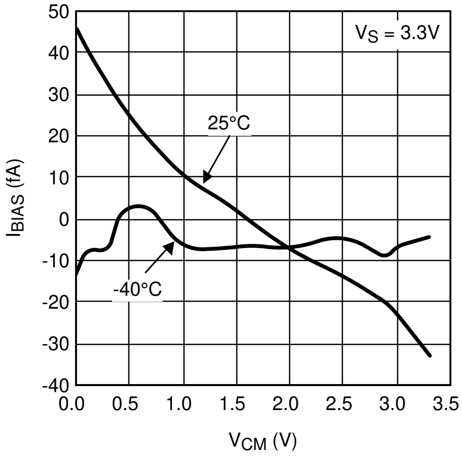


图 5-35. Input Bias Current vs Common Mode Voltage

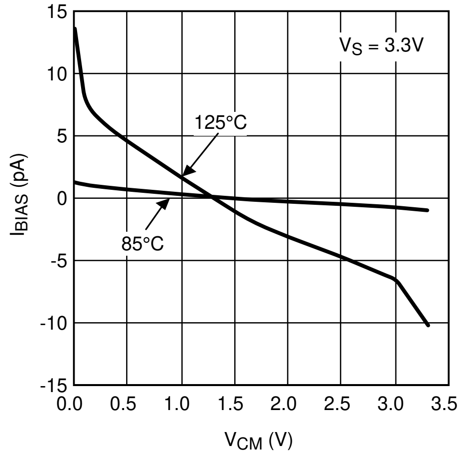


图 5-36. Input Bias Current vs Common Mode Voltage

5.6 Typical Characteristics (continued)

at T_J = 25°C (unless otherwise specified)

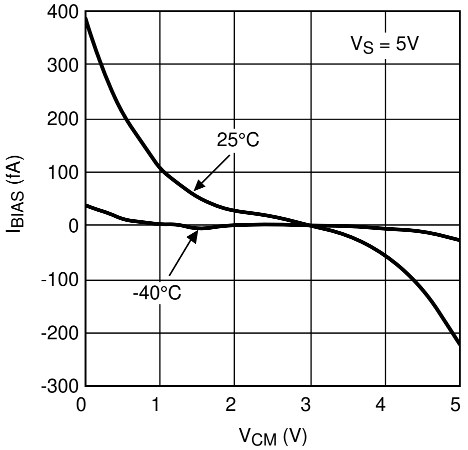


图 5-37. Input Bias Current vs Common Mode Voltage

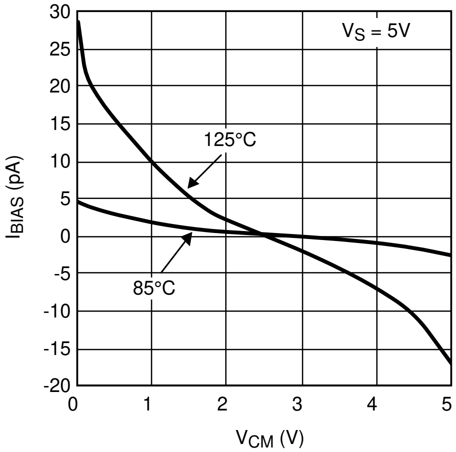


图 5-38. Input Bias Current vs Common Mode Voltage

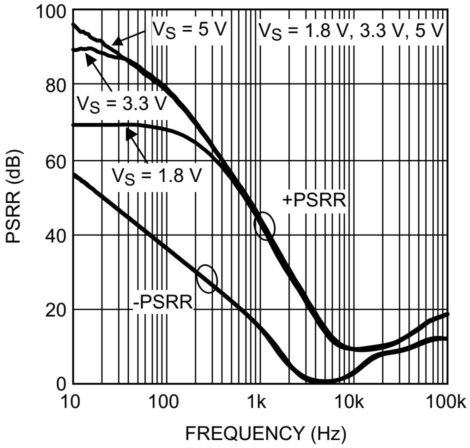


图 5-39. PSRR vs Frequency

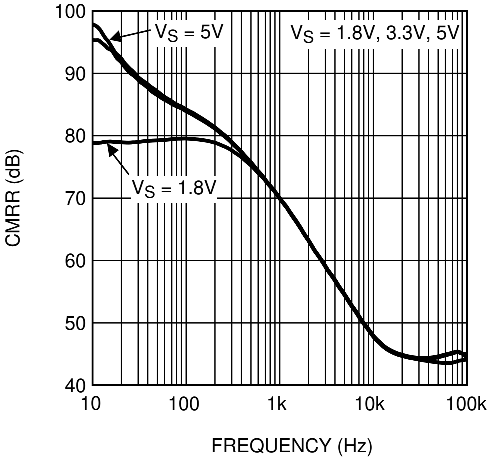


图 5-40. CMRR vs Frequency

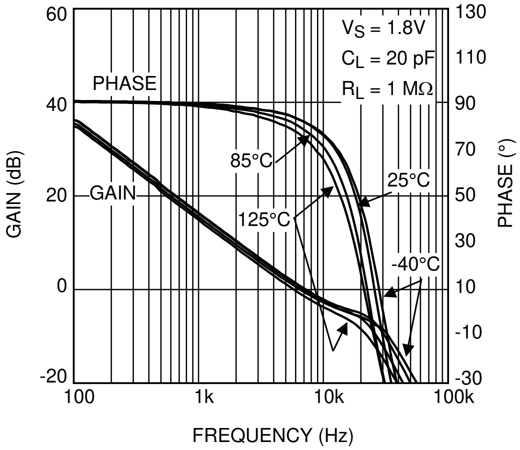


图 5-41. Frequency Response vs Temperature

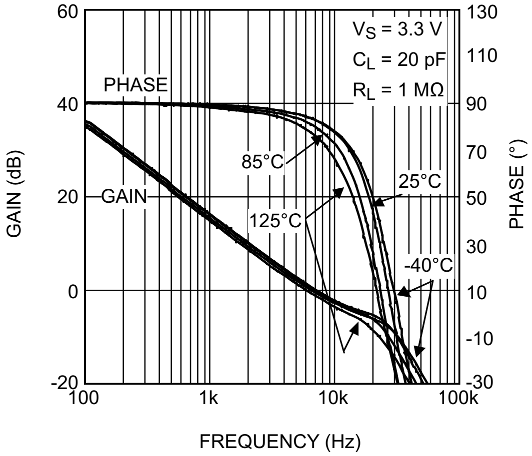


图 5-42. Frequency Response vs Temperature

5.6 Typical Characteristics (continued)

at T_J = 25°C (unless otherwise specified)

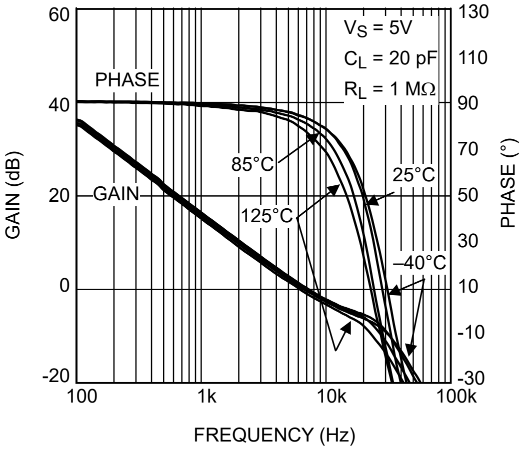


图 5-43. Frequency Response vs Temperature

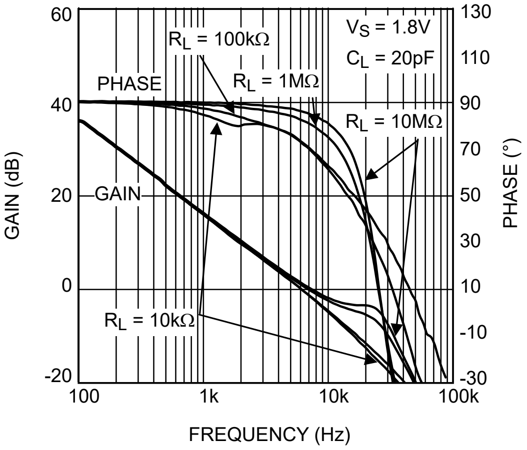


图 5-44. Frequency Response vs R_L

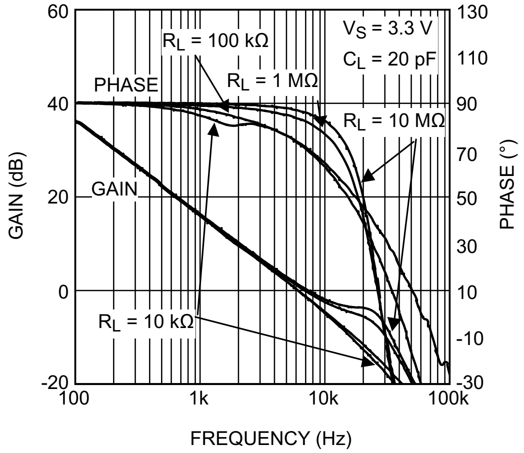


图 5-45. Frequency Response vs R_L

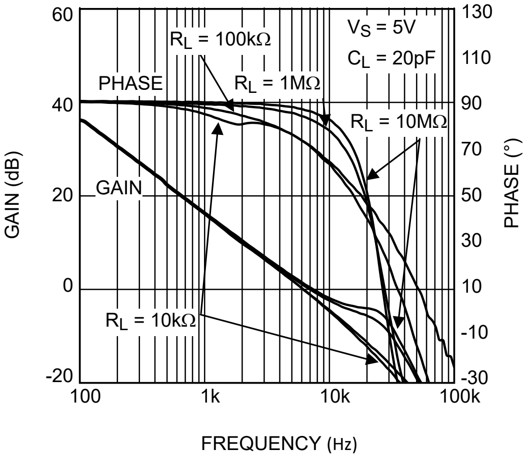


图 5-46. Frequency Response vs R_L

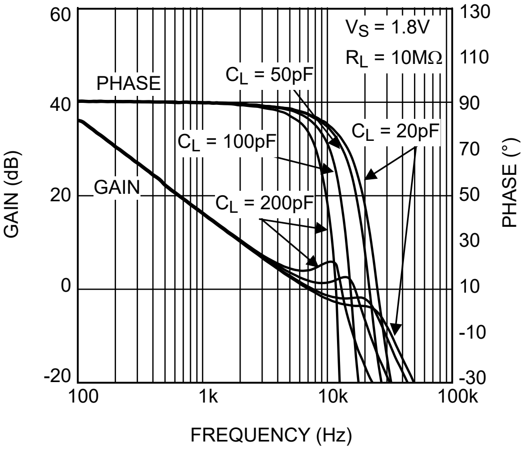


图 5-47. Frequency Response vs C_L

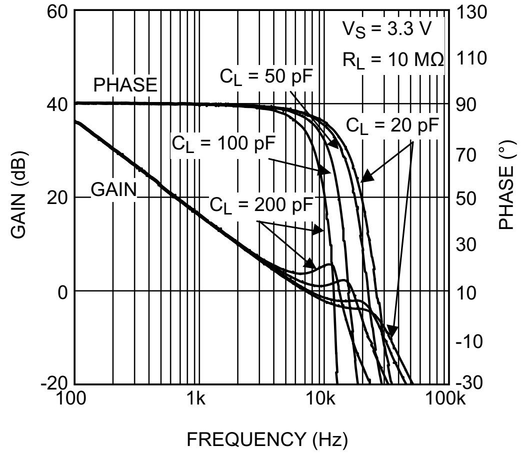


图 5-48. Frequency Response vs C_L

5.6 Typical Characteristics (continued)

at T_J = 25°C (unless otherwise specified)

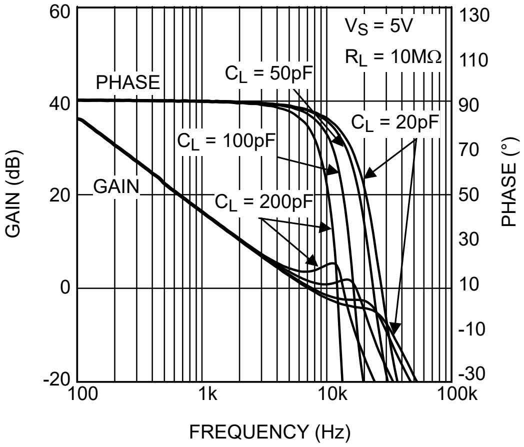


图 5-49. Frequency Response vs C_L

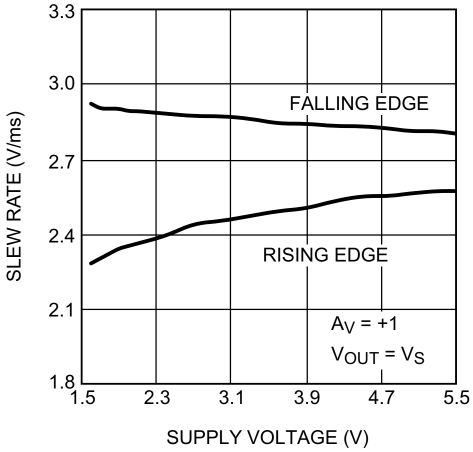


图 5-50. Slew Rate vs Supply Voltage

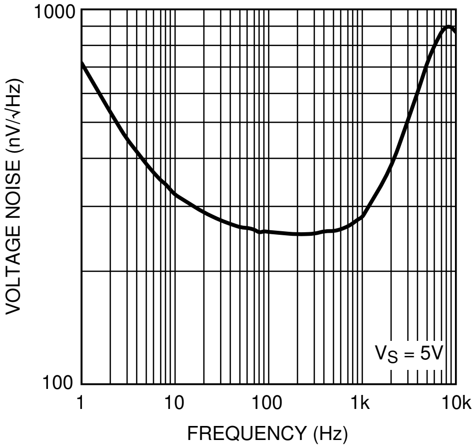


图 5-51. Voltage Noise vs Frequency

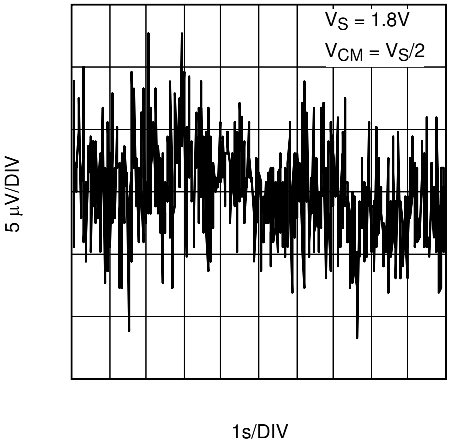


图 5-52. 0.1-Hz to 10-Hz Time Domain Voltage Noise

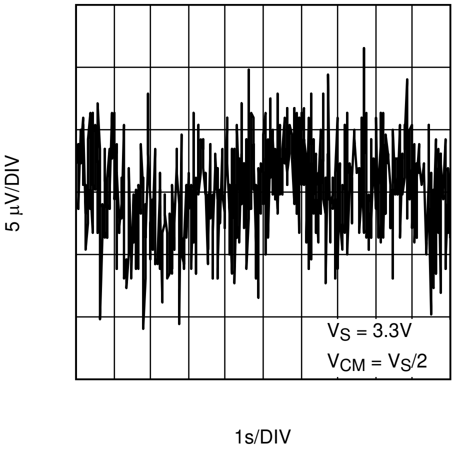


图 5-53. 0.1-Hz to 10-Hz Time Domain Voltage Noise

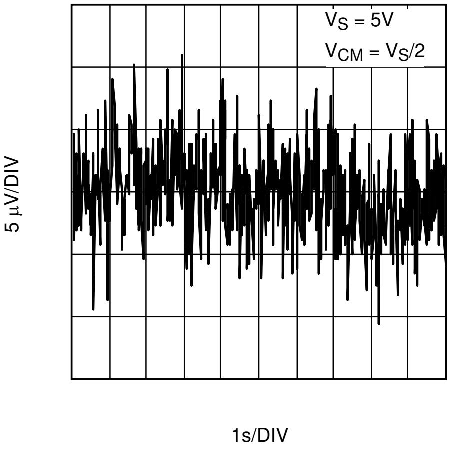


图 5-54. 0.1-Hz to 10-Hz Time Domain Voltage Noise

5.6 Typical Characteristics (continued)

at T_J = 25°C (unless otherwise specified)

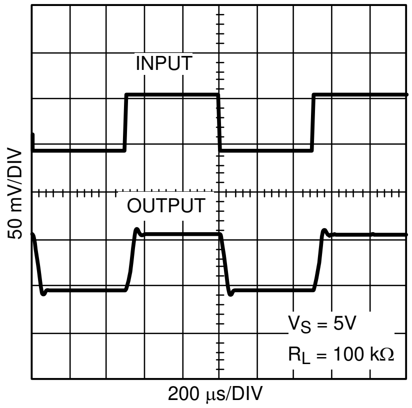


图 5-55. Small-Signal Pulse Response

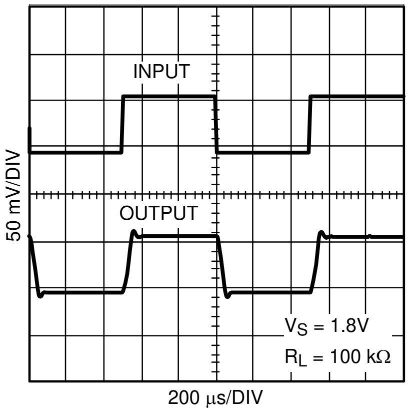


图 5-56. Small-Signal Pulse Response

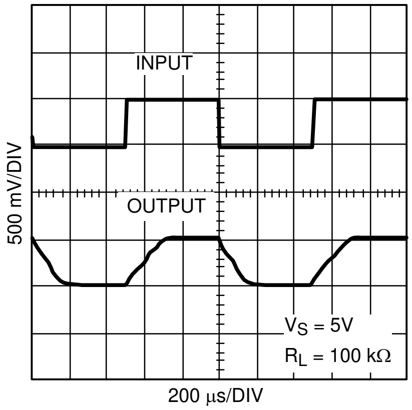


图 5-57. Large-Signal Pulse Response

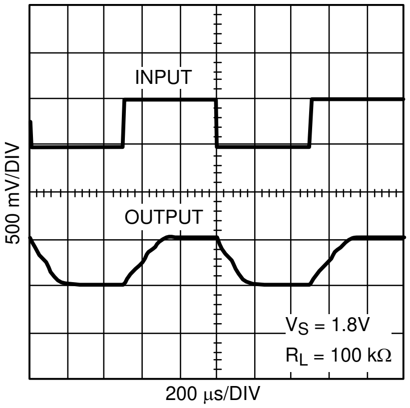


图 5-58. Large-Signal Pulse Response

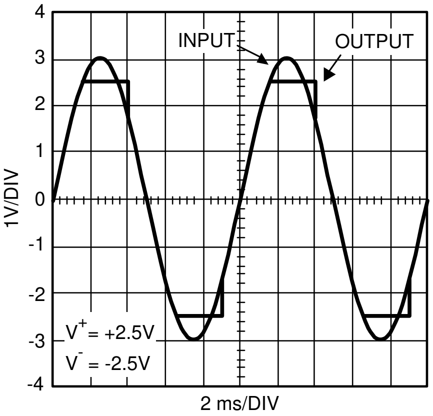


图 5-59. Overload Recovery Waveform

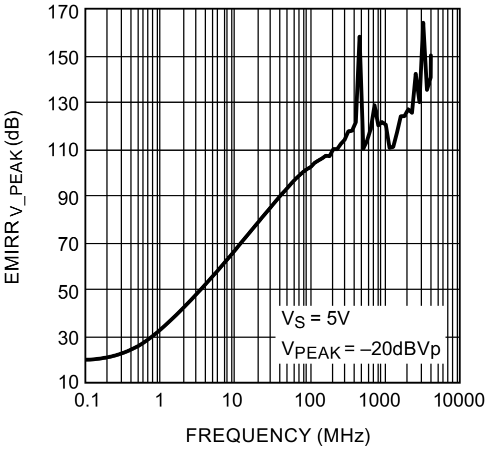


图 5-60. EMIRR vs Frequency

6 Detailed Description

6.1 Overview

The LPV521 is fabricated with Texas Instruments' state-of-the-art VIP50 process. This proprietary process dramatically improves the performance of Texas Instruments' low-power and low-voltage operational amplifiers. The following sections showcase the advantages of the VIP50 process and highlight circuits that enable ultra-low power consumption.

6.2 Functional Block Diagram

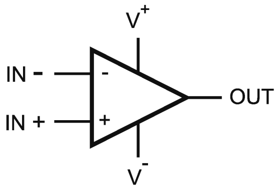


图 6-1. Block Diagram

6.3 Feature Description

The amplifier differential inputs consist of a noninverting input (+IN) and an inverting input (– IN). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by 方程式 1:

$$V_{OUT} = A_{OL} (IN^{+} - IN^{-}) \tag{1}$$

where A_{OL} is the open-loop gain of the amplifier, typically around 132dB (4,000,000 ×, or 0.25μV/V).

6.4 Device Functional Modes

6.4.1 Input Stage

The LPV521 has a rail-to-rail input that provides more flexibility for the system designer. Rail-to-rail input is achieved by using in parallel, one PMOS differential pair and one NMOS differential pair. When the common mode input voltage (V_{CM}) is near V^{+}, the NMOS pair is on and the PMOS pair is off. When V_{CM} is near V^{-}, the NMOS pair is off and the PMOS pair is on. When V_{CM} is between V^{+} and V^{-}, internal logic decides how much current each differential pair get. This special logic maintains stable and low-distortion amplifier operation within the entire common-mode voltage range.

Both input stages have an offset voltage (V_{OS}) characteristic; therefore, the offset voltage of the LPV521 becomes a function of V_{CM}. V_{OS} has a crossover point at 1.0V less than V^{+}. See the *Input Offset Voltage vs Input Common Mode* curves in the *Typical Characteristics*. Take care in situations where the input signal amplitude is comparable to the V_{OS} value or the design requires high accuracy. In these situations, the input signal must avoid the crossover point. In addition, parameters such as PSRR and CMRR that involve the input offset voltage are also affected by changes in V_{CM} across the differential-pair transition region.

6.4.2 Output Stage

The LPV521 output voltage swings 3mV from rails at a 3.3V supply, which provides the maximum possible dynamic range at the output. This feature is particularly important when operating on low supply voltages.

The LPV521 maximum output voltage swing defines the maximum swing possible under a particular output load. The LPV521 output swings 50mV from the rail at a 5V supply with an output load of 100kΩ.

7 Applications and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The LPV521 is specified for operation from 1.6V to 5.5V (±0.8V to ±2.25V). Many of the specifications apply from –40°C to +125°C. The LMV521 features rail-to-rail input and rail-to-rail output swings while consuming only nanowatts of power. Parameters that exhibit significant variance with regard to operating voltage or temperature are presented in 节 5.6.

7.1.1 Driving Capacitive Load

The LPV521 is internally compensated for stable unity gain operation, with a 6.2kHz, typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. The combination of a capacitive load placed at the output of an amplifier along with the amplifier output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response is underdamped, and causes peaking in the transfer. When there is too much peaking, the op amp can start oscillating.

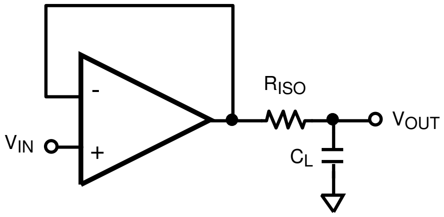


图 7-1. Resistive Isolation of Capacitive Load

To drive heavy capacitive loads, use an isolation resistor, R_{ISO}, as in 图 7-1. By using this isolation resistor, the capacitive load is isolated from the amplifier output. The larger the value of R_{ISO}, the more stable the amplifier. If the value of R_{ISO} is sufficiently large, the feedback loop is stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

表 7-1 shows the recommended minimum R_{ISO} values for a 5V supply. 图 7-2 shows the typical response obtained with the C_L = 50pF and R_{ISO} = 154kΩ. The other values of R_{ISO} in Table 7-1 are chosen to achieve similar dampening at the respective capacitive loads. Notice that for the LPV521 with larger a C_L, a smaller R_{ISO} can be used for stability. However, for a given C_L, a larger R_{ISO} provides a more damped response. For capacitive loads of 20pF and less, no isolation resistor is needed.

表 7-1. Recommended Minimum R_{ISO} Values for a 5V Supply

C_L	R_{ISO}
0pF to 20pF	Not needed
50pF	154kΩ
100pF	118kΩ
500pF	52.3kΩ
1nF	33.2kΩ
5nF	17.4kΩ
10nF	13.3kΩ

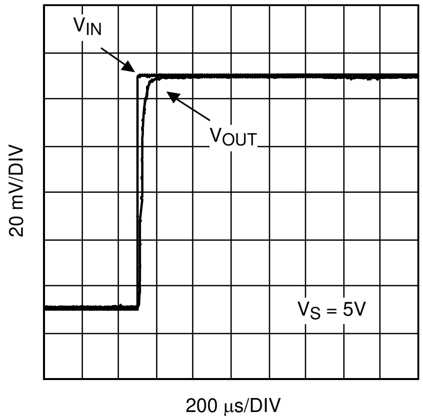


图 7-2. Step Response

7.1.2 EMI Suppression

The near-ubiquity of cellular, Bluetooth®, and Wi-Fi® signals and the rapid rise of sensing systems incorporating wireless radios make electromagnetic interference (EMI) an evermore important design consideration for precision signal paths. Though RF signals lie outside the op-amp band, RF carrier switching can modulate the dc offset of the op amp. Also some common RF modulation schemes can induce down-converted components. The added dc offset and the induced signals are amplified with the signal of interest and thus corrupt the measurement. The LPV521 uses on-chip filters to reject these unwanted RF signals at the inputs and power supply pins, thereby preserving the integrity of the precision signal path.

Twisted pair cabling and the active front-end common-mode rejection provide immunity against low-frequency noise (for example, 60Hz or 50Hz mains) but are ineffective against RF interference. Even a few centimeters of printed circuit board (PCB) trace and wiring for sensors located close to the amplifier can pick up significant 1GHz RF. The integrated EMI filters of the LPV521 reduce or eliminate external shielding and filtering requirements, thus increasing system robustness. A larger EMIRR means more rejection of the RF interference. For more information on EMIRR, see the *AN-1698 A Specification for EMI Hardened Operational Amplifiers* application report.

7.2 Typical Applications

7.2.1 60Hz Twin T-Notch Filter

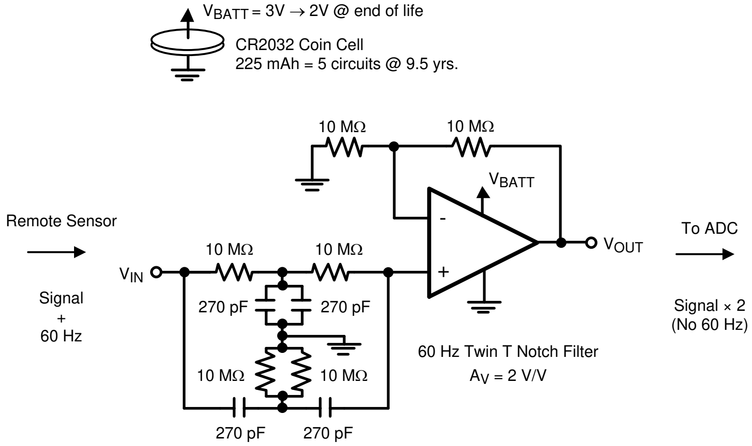


图 7-3. 60Hz Notch Filter

7.2.1.1 Design Requirements

Small signals from transducers in remote and distributed sensing applications commonly suffer strong 60Hz interference from ac power lines. The circuit of 图 7-3 notches out the 60Hz and provides a gain A_V = 2 for the sensor signal represented by a 1kHz sine wave. Similar stages can be cascaded to remove 2nd and 3rd harmonics of 60Hz. Thanks to the nA power consumption of the LPV521, even five such circuits can run for 9.5 years from a small CR2032 lithium cell. These batteries have a nominal voltage of 3V and an end of life voltage of 2V. With an operating voltage from 1.6V to 5.5V, the LPV521 can function over this voltage range.

7.2.1.2 Detailed Design Procedure

The notch frequency is set by $F_0 = 1 / 2\pi RC$. To achieve a 60Hz notch, use R = 10MΩ and C = 270pF. If eliminating 50Hz noise, which is common in European systems, use R = 11.8MΩ and C = 270pF.

The twin T notch filter works by having two separate paths from V_{IN} to the amplifier input. A low-frequency path through resistors R-R and another separate high-frequency path through capacitors C-C. However, at frequencies around the notch frequency, the two paths have opposing phase angles and the two signals tend to cancel at the amplifier input.

To ensure that the target center frequency is achieved, and to maximize the notch depth (Q factor), balance the filter as much as possible. To obtain circuit balance, while overcoming limitations of available standard resistor and capacitor values, use passives in parallel to achieve the 2C and R/2 circuit requirements for the filter components that connect to ground.

To ensure that passive component values stay as expected, clean the board with alcohol, rinse with deionized water, and air dry. Ensure that the board remains in a relatively low humidity environment to minimize moisture that can increase the conductivity of board components. Also large resistors come with considerable parasitic stray capacitance; the effects can be reduced by cutting out the ground plane below components of concern.

Use Large resistors in the feedback network to minimize battery drain. When designing with large resistors, consider the resistor thermal noise, op-amp current noise, as well as op-amp voltage noise in the noise analysis of the circuit. The noise analysis for the circuit in 图 7-3 can be done over a bandwidth of 5kHz, which takes the conservative approach of overestimating the bandwidth (LPV521 typical GBW/A_V is less). The total noise at the output is approximately 800µV_{PP}, which is excellent considering the total consumption of the circuit is only 540nA. The dominant noise terms are op-amp voltage noise (550µV_{PP}), current noise through the feedback network (430µV_{PP}), and current noise through the notch filter network (280µV_{PP}). Thus, the total circuit noise is less than ½ LSB of a 10-bit system with a 2V reference, which is 1mV.

7.2.1.3 Application Curve

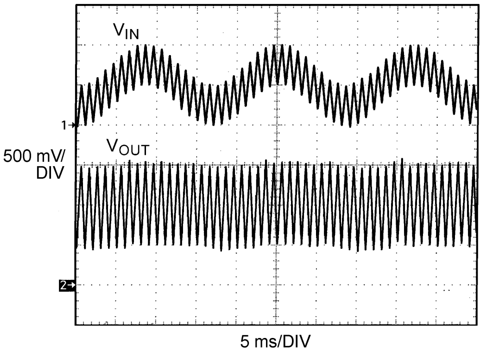


图 7-4. 60Hz Notch Filter Waveform

7.2.2 Portable Gas Detection Sensor

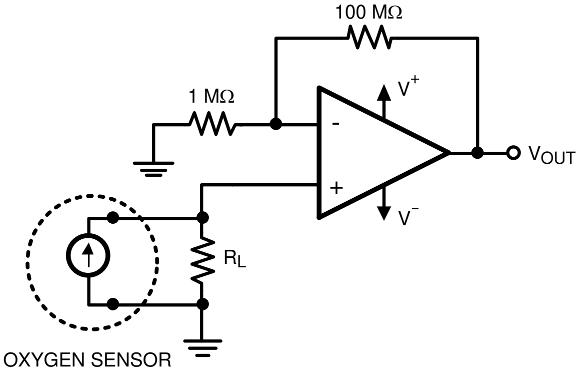


图 7-5. Precision Oxygen Sensor

7.2.2.1 Design Requirements

Gas sensors are used in many different industrial and medical applications. Gas sensors generate a current that is proportional to the percentage of a particular gas sensed in an air sample. This current goes through a load resistor and the resulting voltage drop is measured. The LPV521 is an excellent choice for this application because the device draws only 345nA of current and operates on supply voltages down to 1.6V. Depending on the sensed gas and sensitivity of the sensor, the output current can be in the order of tens of microamperes to a few milliamperes. Gas sensor data sheets often specify a recommended load resistor value or suggest a range of load resistors from which to choose.

Oxygen sensors are used when air quality or oxygen delivered to a patient needs to be monitored. Fresh air contains 20.9% oxygen. Air samples containing less than 18% oxygen are considered dangerous. This application detects oxygen in air. Oxygen sensors are also used in industrial applications where the environment must lack oxygen. An example is when food is vacuum packed. There are two main categories: oxygen sensors that sense oxygen when oxygen is abundantly present (for example, in air or near an oxygen tank), and oxygen sensors that detect traces of oxygen in ppm.

7.2.2.2 Detailed Design Procedure

图 7-5 shows a typical circuit used to amplify the output of an oxygen detector. The oxygen sensor outputs a known current through the load resistor. This value changes with the amount of oxygen present in the air sample. Oxygen sensors usually recommend a particular load resistor value or specify a range of acceptable values for the load resistor. The use of the nanopower LPV521 means minimal power usage by the op amp, and enhanced battery life. With the components shown in 图 7-5, the circuit consumes less than 0.5μA of current, so that even batteries used in compact portable electronics, with low mAh charge ratings, can last beyond the life of the oxygen sensor. The precision specifications of the LPV521, such as the very low offset voltage, low TCV_{OS}, low input bias current, high CMRR, and high PSRR are other factors that make the LPV521 a great choice for this application.

7.2.2.3 Application Curve

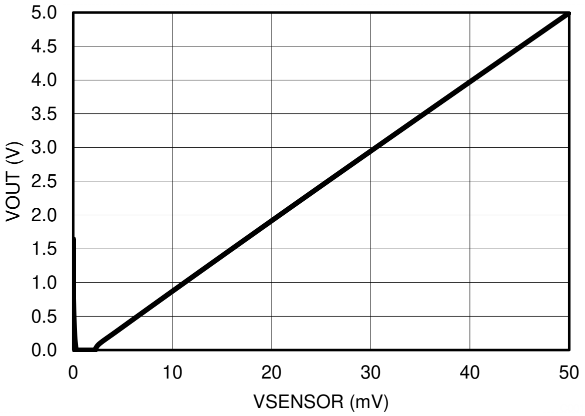
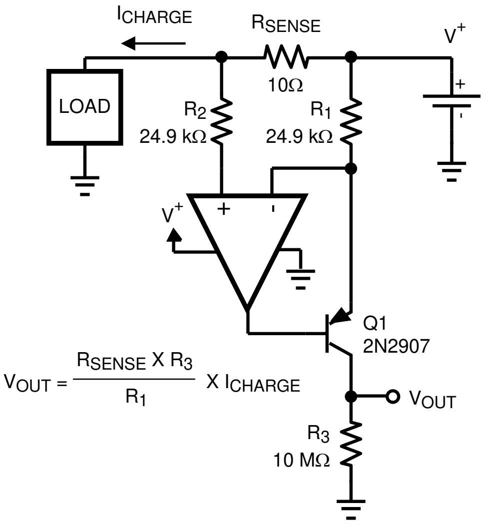


图 7-6. Calculated Oxygen Sensor Circuit Output (Single 5V Supply)

7.2.3 High-Side Battery Current Sensing



$$V_{OUT} = \frac{R_{SENSE} \times R_3}{R_1} \times I_{CHARGE}$$

图 7-7. High-Side Current Sensing

7.2.3.1 Design Requirements

The rail-to-rail common-mode input range and the very low quiescent current make the LPV521 an excellent choice for use in high-side and low-side battery current-sensing applications. The high-side current-sensing circuit in 图 7-7 is commonly used in a battery charger to monitor the charging current to prevent overcharging. A sense resistor R_{SENSE} is connected in series with the battery.

7.2.3.2 Detailed Design Procedure

The theoretical output voltage of the circuit is V_{OUT} = [(R_{SENSE} × R_3) / R_1] × I_{CHARGE}. In reality, however, as a result of the finite current gain of the transistor (β), the current that travels through R_3 is not I_{CHARGE}. Instead, R_3 is α × I_{CHARGE} or β / (β +1) × I_{CHARGE}. A Darlington pair can be used to increase the β and performance of the measuring circuit.

Using the components shown in 图 7-7 results in V_{OUT} ≈ 4000Ω × I_{CHARGE}. This result is needed to amplify a 1mA I_{CHARGE} to near full-scale of an analog-to-digital converter (ADC) with V_{REF} at 4.1V. A resistor, R_2 is used at the noninverting input of the amplifier, with the same value as R_1 to minimize offset voltage.

Selecting values per 图 7-7 limits the current traveling through the R_1 – Q1 – R_3 leg of the circuit to under 1µA, which is on the same order as the LPV521 supply current. Increasing resistors R_1, R_2, and R_3 decreases the measuring circuit supply current and extends battery life.

Decreasing R_{SENSE} minimizes error due to resistor tolerance; however, this decrease also decreases V_{SENSE} = I_{CHARGE} × R_{SENSE}, and in turn, the amplifier offset voltage has a more significant contribution to the total error of the circuit. With the components shown in 图 7-7, the measurement circuit supply current can be kept below 1.5µA and measure 100µA to 1mA.

7.2.3.3 Application Curve

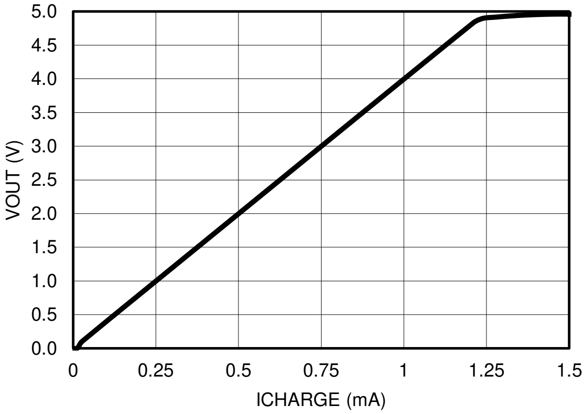


图 7-8. Calculated High-Side Current Sense Circuit Output

7.3 Power Supply Recommendations

The LPV521 is specified for operation from 1.6V to 5.5V (±0.8V to ±2.75V) over a –40°C to +125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *节 5.6* .

小心

Supply voltages greater than 6 V can permanently damage the device.

Low bandwidth nanopower devices do not have good high frequency (> 1kHz) ac PSRR rejection against high-frequency switching supplies and other kHz and greater noise sources; therefore, extra supply filtering is recommended if kHz-range noise is expected on the power-supply lines.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1 µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If not possible, cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. 节 7.4.2 shows how keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

7.4.2 Layout Example

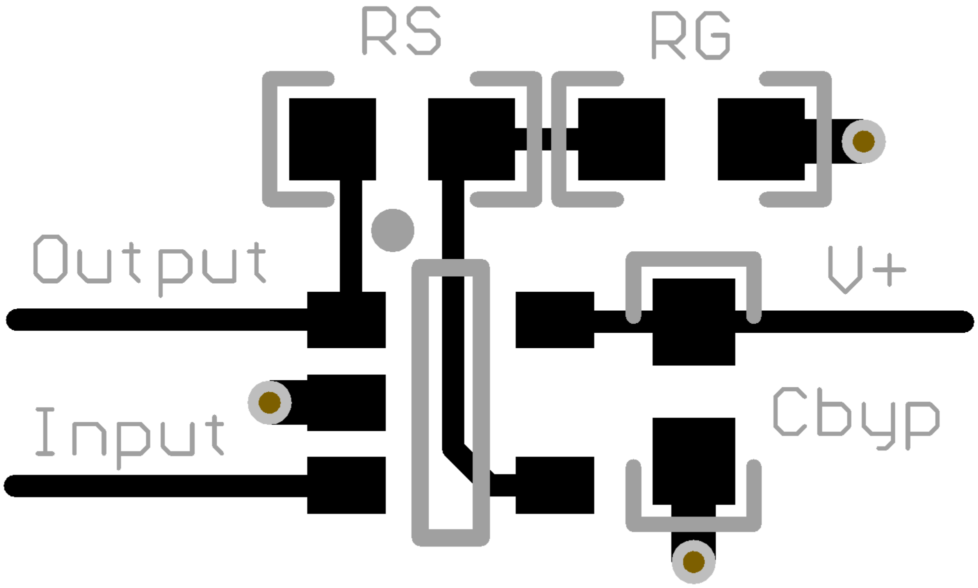


图 7-9. Noninverting Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

- LPV521 PSPICE Model
- TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti
- *Capacitive Load Drive Solution Using an Isolation Resistor* reference design
- DIP Adapter Evaluation Module, http://www.ti.com/tool/dip-adapter-evm
- Evaluation board for 5-pin, north-facing amplifiers in the SC70 package, SNOA487.
- Manual for LMH730268 Evaluation board 551012922-001

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Feedback Plots Define Op Amp AC Performance* application bulletin
- Texas Instruments, *AN-1698 A Specification for EMI Hardened Operational Amplifiers*application report
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report
- Texas Instruments, *Handbook of Operational Amplifier Applications* application report

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.5 Trademarks

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Bluetooth® is a registered trademark of Bluetooth SIG, Inc..
Wi-Fi® is a registered trademark of The Wi-Fi Alliance.
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8.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (December 2014) to Revision E (July 2024) Page

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- 向文档中添加了 P（PDIP，8）封装和相关内容 1
- 更新了*应用* 1
- 更新了*封装信息* 表 1
- Added missing thermal information for DCK (SC70) package 4
- Moved all *Electrical Characteristics* tables into one table 4
- Updated *Electrical Characteristics* note 1 4
- Added missing CMRR test condition for V+ = 5V 4
- Updated common mode voltage range to fix the incorrect conditions 4
- Updated Figure 5-4 and Figure 5-6, *TcvOS Distribution*, to fix test condition typos 8
- Changed A_{OL} typical value from "100 dB (100,000 ×, or 10 µV/V)" to "132dB (4000,000 ×, or 0.25 µV/V)" in *Feature Description* 18

Changes from Revision C (February 2013) to Revision D (December 2014) Page

- 添加了*引脚配置和功能* 部分、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPV521MG/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	AHA	Samples
LPV521MGE/NOPB	ACTIVE	SC70	DCK	5	250	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	AHA	Samples
LPV521MGX/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	AHA	Samples
LPV521P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	LPV521	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

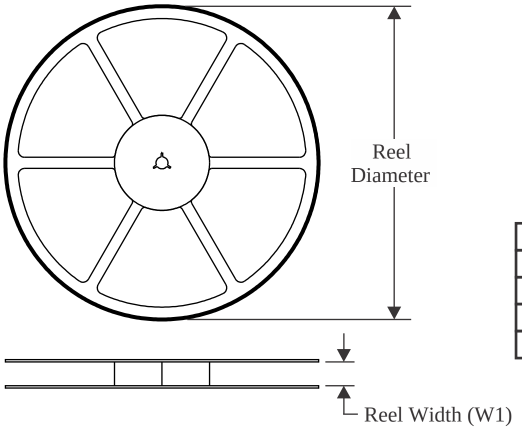
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

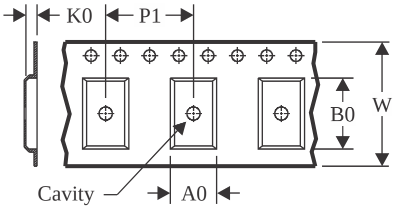
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

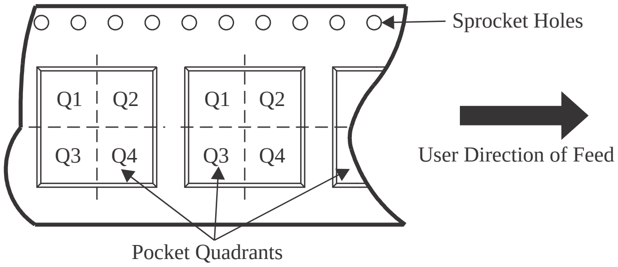


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

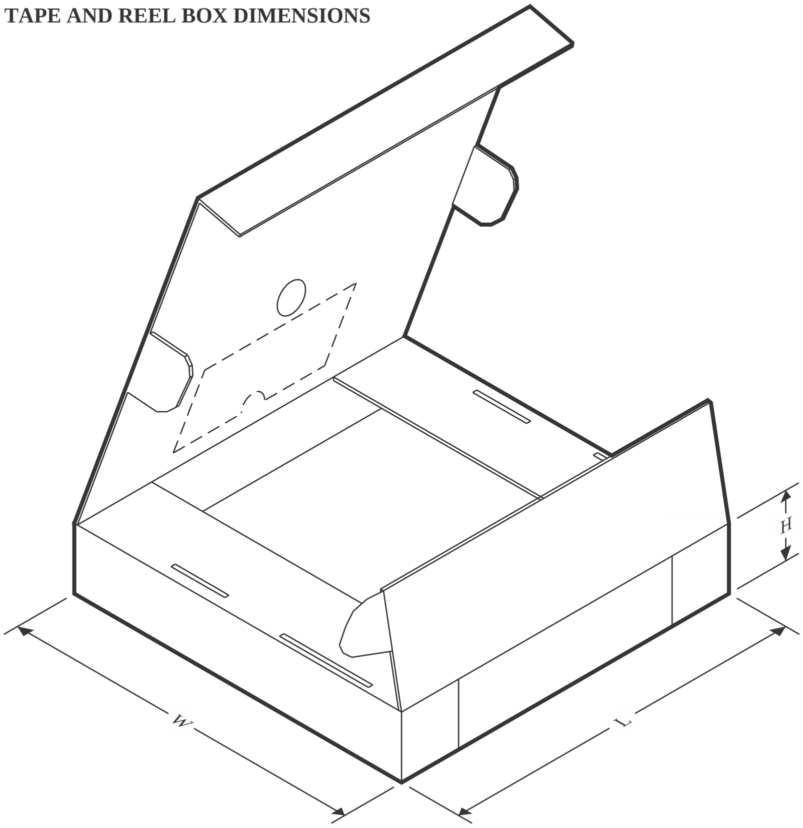
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV521MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV521MGE/NOPB	SC70	DCK	5	250	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV521MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

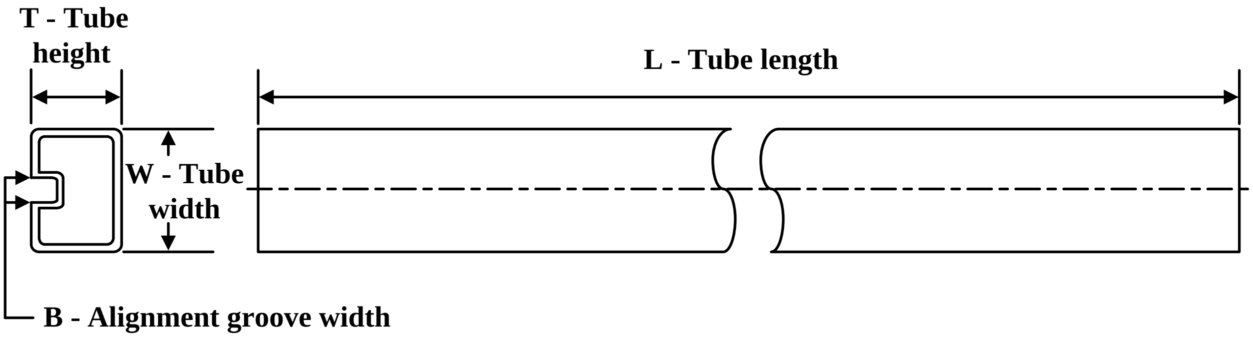
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV521MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LPV521MGE/NOPB	SC70	DCK	5	250	208.0	191.0	35.0
LPV521MGX/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0

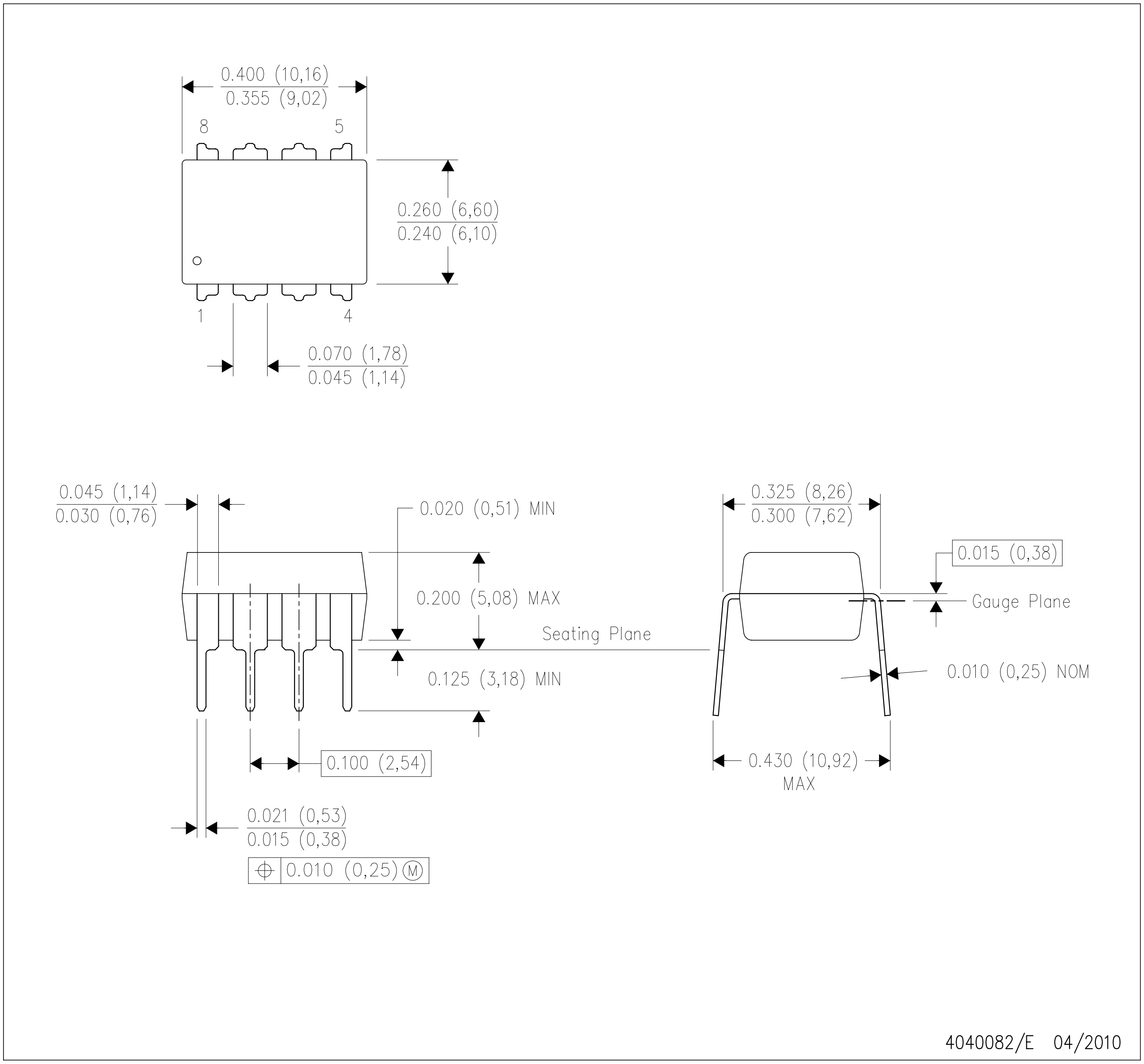
TUBE



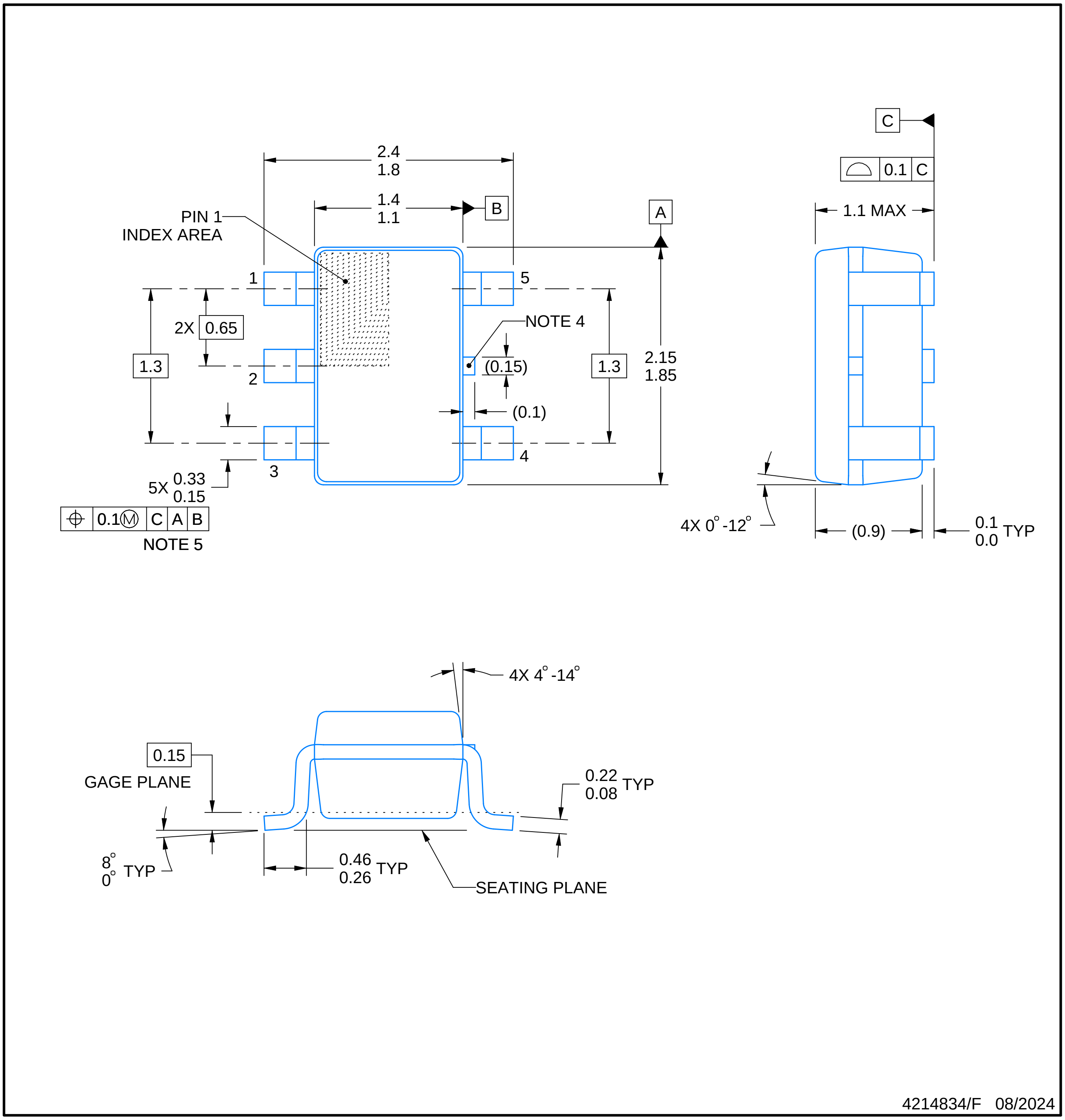
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LPV521P	P	PDIP	8	50	506	13.97	11230	4.32

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.



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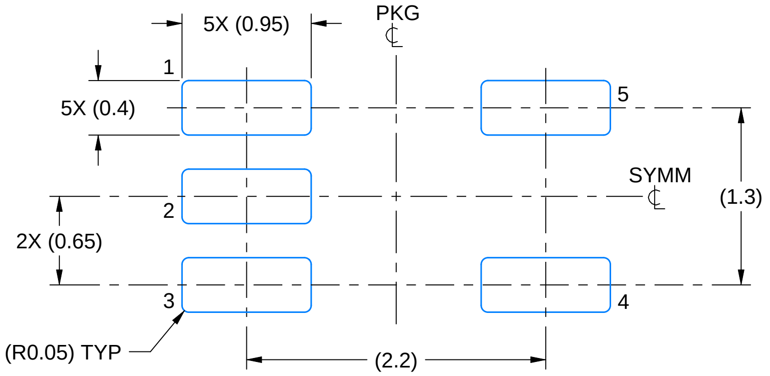
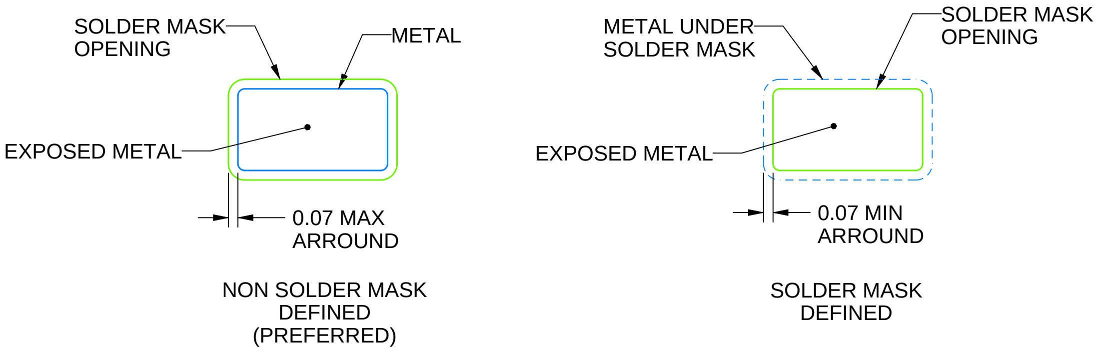
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



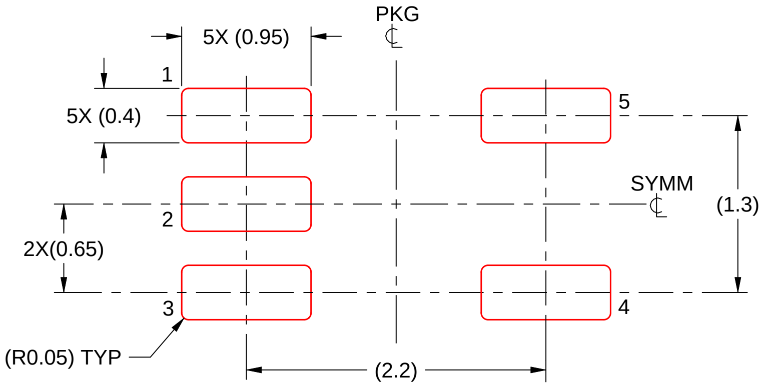
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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