具有中断输出和配置寄存器的 PCA9534 远程 8 位 I2C 和 SMBus 低功耗 I/O 扩展器

1 特性

- 1μA 低待机电流消耗（最大值）
- I^2C 至并行端口扩展器
- 开漏电路低电平有效中断输出
- 工作电源电压范围为 2.3V 至 5.5V
- 可耐受 5V 电压的 I/O 端口
- 400kHz 快速 I^2C 总线
- 三个硬件地址引脚允许在 I^2C/SMBus 上使用多达八个器件
- 与 PCA9534A 结合使用时，允许在 I^2C/SMBus 上使用多达 16 个器件 请参阅，节 5 了解 I^2C 扩展器产品
- 输入/输出配置寄存器
- 极性反转寄存器
- 内部上电复位
- 加电时所有通道均被配置为输入
- 加电时无干扰
- SCL/SDA 输入端上的噪声滤波器
- 具有最大高电流驱动能力的锁存输出，适用于直接驱动 LED
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 200V 机器放电模型 (A115-A)
  - 1000V 带电器件模型 (C101)

2 说明

这个用于两线双向总线 (I2C) 的 8 位 I/O 扩展器设计用于在 2.3V 至 5.5V VCC 之间运行。通过 I^2C 接口 [串行时钟 (SCL)，串行数据 (SDA)]，它为大多数微控制器系列产品提供通用远程 I/O 扩展。

PCA9534 包含一个 8 位配置（输入或输出可选）、输入端口、输出端口和极性反转（高电平有效或低电平有效）寄存器。在加电时，I/O 被配置为输入。但是，系统主控制器可以通过写入 I/O 配置位将 I/O 启用为输入或输出。每个输入或输出的数据均保存在相应的输入或输出寄存器中。输入端口寄存器的极性可借助极性反转寄存器进行转换。所有寄存器都可由系统主控器读取。

发生超时或其他不当操作时，系统主控器可通过使用上电复位功能，将寄存器置于其默认状况并初始化 I2C/SMBus 状态机来复位 PCA9534。

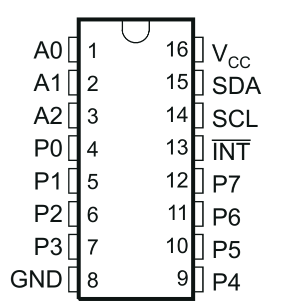
PCA9534 开漏中断 (INT) 输出在任意输入状态与其对应的输入端口寄存器状态不同时被激活，并用于向系统主控器指明输入状态已改变。

器件信息(1)

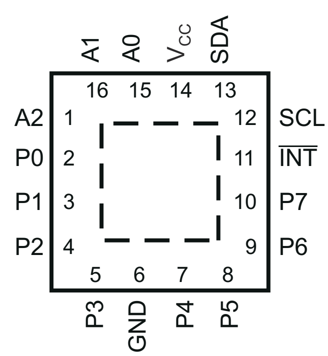
器件型号	封装	封装尺寸（标称值）
PCA9534	SSOP (16)	6.20mm x 5.30mm
	VQFN (16)	4.00mm x 4.00mm
	四方扁平无引线 (QFN) (16)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

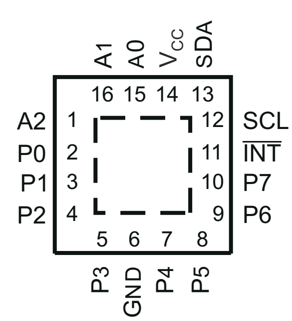
DB, DGV, DW, OR PW PACKAGE
(TOP VIEW)



RGV PACKAGE
(TOP VIEW)



RGT PACKAGE
(TOP VIEW)



English Data Sheet: SCPS124

Table of Contents

3 Revision History

Changes from Revision G (May 2014) to Revision H (March 2021) — **Page**

- Moved the "Storage temperature range" to the *Absolute Maximum Ratings* 6
- Moved the "Package thermal impedance" to the *Thermal Resistance Characteristic* 6
- Changed the V_{IH} High-level input voltage (SDL, SDA) Max value From: 5.5 V To: V_{CC} in the *Recommended Operating Conditions* 6
- Changed the V_{IH} High-level input voltage (A0, A1, A2, P7 – P0) MIN value From: 2 V To: V_{CC} in the *Recommended Operating Conditions* 6
- Changed the V_{IL} Low-level input voltage (A0, A1, A2, P7 – P0) MAX value From: 0.8 V To: 0.3 x V_{CC} in the *Recommended Operating Conditions* 6
- Added the *Thermal Resistance Characteristics* 6
- Changed the V_{PORR} row in the *Electrical Characteristics* 7
- Added the V_{PORF} row in the *Electrical Characteristics* 7
- Changed the I_{CC} Standby mode values in the *Electrical Characteristics* 7
- Changed the ΔI_{CC} Additional current in standby mode (5.5 V) mAX value From: 1 mA To: 4 mA in the *Electrical Characteristics* 7
- Changed the C_i SCL Max value From: 5 pF To: 8 pF in the *Electrical Characteristics* 7
- Changed the C_{io} SDA Max value From:6.5 pF To: 9.5 pF in the *Electrical Characteristics* 7
- Changed the t_{pv} Output data valid MAX values From: 200 ns To 350 ns in the *Swirtching Characteristics* 8
- Changed the *Typical Characteristics* graphs 9
- Changed the *Power Supply Recommendations* 25

Changes from Revision F (June 2010) to Revision G (June 2014) — **Page**

- Added Interrupt Errata section 17

4 Description (Continued)

$\overline{INT}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the PCA9534 can remain a simple slave device.

The device's outputs (latched) have high-current drive capability for directly driving LEDs. It has low current consumption.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I^2C address and allow up to eight devices to share the same I^2C bus or SMBus.

The PCA9534 is pin-to-pin and I^2C address compatible with the PCF8574. However, software changes are required due to the enhancements in the PCA9534 over the PCF8574.

The PCA9534 is a low-power version of the PCA9554. The only difference between the PCA9534 and PCA9554 is that the PCA9534 eliminates an internal I/O pullup resistor, which dramatically reduces power consumption in the standby mode when the I/Os are held low.

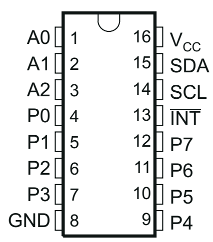
The PCA9534A and PCA9534 are identical, except for their fixed I^2C address. This allows for up to 16 of these devices (8 of each) on the same I^2C bus.

5 Device Comparison Table

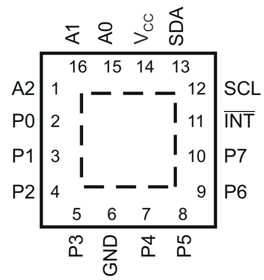
DEVICE	MAX FREQUENCY	I2C ADDRESS	NO. OF GPIOs	INTERRUPT OUTPUT	RESET INPUT	CONFIGURATION REGISTERS	5-V TOLERANT	PUSH-PULL I/O TYPE	OPEN-DRAIN I/O TYPE	COMMENT
V_{CC} = 1.65 to 5.5 V										
TCA6408	400	0100 00x	8	Yes	Yes	Yes	Yes	Yes	No	Power on reset, t_f (fall time) > 100 ms and t_r (ramp time) < 10 ms
TCA6408	400	0100 00x	8	Yes	Yes	Yes	Yes	Yes	No	Unrestricted power on reset ramp/fall time. Both t_f (fall time) and TRT (ramp time) can be between 0.1 ms and 2000 ms
TCA6416	400	0100 00x	16	Yes	Yes	Yes	Yes	Yes	No	Power on reset, t_f (fall time) > 100 ms and TRT (ramp time) < 10 ms
TCA6416A	400	0100 00x	16	Yes	Yes	Yes	Yes	Yes	No	Unrestricted power on reset ramp/fall time. Both t_f (fall time) and TRT (ramp time) can be between 0.1 ms and 2000ms
TCA6424	400	0100 00x	24	Yes	Yes	Yes	Yes	Yes	No	Power on reset, t_f (fall time) > 100 ms and TRT (ramp time) < 10 ms
TCA9535	400	0100 xxx	16	Yes	No	Yes	Yes	Yes	No	
TCA9539	400	1110 1xx	16	Yes	Yes	Yes	Yes	Yes	No	
TCA9555	400	0100 xxx	16	Yes	No	Yes	Yes	Yes	No	
V_{CC} = 2.3 to 5.5 V										
PCA6107	400	0011 xxx	8	Yes	Yes	Yes	Yes	Yes P1—P7 bits	Yes P0 bit	One open drain output; eight push pull outputs
PCA9534	400	0100 xxx	8	Yes	No	Yes	Yes	Yes	No	PCA9534 has a different slave address as the PCA9534A, allowing up to 16 devices '9534 type devices on the same I2C bus
PCA9534A	400	0111 xxx	8	Yes	No	Yes	Yes	Yes	No	PCA9534A has a different slave address as the PCA9534, allowing up to 16 devices '9534 type devices on the same I2C bus
PCA9535	400	0100 xxx	16	Yes	No	Yes	Yes	Yes	No	
PCA9536	400	1000 001	4	No	No	Yes	Yes	Yes	No	
PCA9538	400	1110 0xx	8	Yes	Yes	Yes	Yes	Yes	No	
PCA9539	400	1110 1xx	16	Yes	Yes	Yes	Yes	Yes	No	
PCA9554	400	0100 xxx	8	Yes	No	Yes	Yes	Yes	No	
PCA9554A	400	0111 xxx	8	Yes	No	Yes	Yes	Yes	No	
PCA9555	400	0100 xxx	16	Yes	No	Yes	Yes	Yes	No	
PCA9557	400	0011 xxx	8	No	Yes	Yes	Yes	Yes	Yes	
V_{CC} = 2.5 to 6.0 V										
PCF8574	400	0100 xxx	8	Yes	No	No	Yes	Yes	No	PCA8574 has a different slave address as the PCA8574A, allowing up to 16 devices '9534 type devices on the same I2C bus
PCF8574A	400	0111 xxx	8	Yes	No	No	Yes	Yes	No	PCA8574A has a different slave address as the PCA8574, allowing up to 16 devices '9534 type devices on the same I2C bus
V_{CC} = 2.5 to 5.5 V										
PCF8575	400	0100 xxx	16	Yes	No	No	Yes	Yes	No	
PCF8575C	400	0100 xxx	16	Yes	No	No	Yes	No	Yes	

6 Pin Configuration and Functions

DB, DGV, DW, OR PW PACKAGE
(TOP VIEW)



RGV PACKAGE
(TOP VIEW)



RGT PACKAGE
(TOP VIEW)

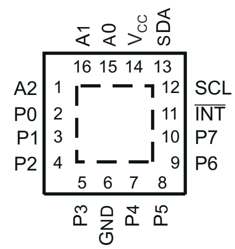


表 6-1. Pin Functions

PIN			DESCRIPTION
NAME	SOIC (DW), SSOP (DB), TSSOP (PW), AND TVSOP (DGV)	QFN (RGT AND RGV)	
A0	1	15	Address input. Connect directly to V_{CC} or ground.
A1	2	16	Address input. Connect directly to V_{CC} or ground.
A2	3	1	Address input. Connect directly to V_{CC} or ground.
P0	4	2	P-port input/output. Push-pull design structure.
P1	5	3	P-port input/output. Push-pull design structure.
P2	6	4	P-port input/output. Push-pull design structure.
P3	7	5	P-port input/output. Push-pull design structure.
GND	8	6	Ground
P4	9	7	P-port input/output. Push-pull design structure.
P5	10	8	P-port input/output. Push-pull design structure.
P6	11	9	P-port input/output. Push-pull design structure.
P7	12	10	P-port input/output. Push-pull design structure.
$\overline{INT}$	13	11	Interrupt output. Connect to V_{CC} through a pullup resistor.
SCL	14	12	Serial clock bus. Connect to V_{CC} through a pullup resistor.
SDA	15	13	Serial data bus. Connect to V_{CC} through a pullup resistor.
V_{CC}	16	14	Supply voltage

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6	V
V_I	Input voltage range[(2)]		–0.5	6	V
V_O	Output voltage range[(2)]		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
	Continuous current through V_{CC}			160	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}	V_{CC}	V
		A0, A1, A2, P7 – P0	0.7 × V_{CC}	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	0.3 × V_{CC}	V
		A0, A1, A2, P7 – P0	–0.5	0.3 × V_{CC}	
I_{OH}	High-level output current	P7 – P0		–10	mA
I_{OL}	Low-level output current	P7 – P0		25	mA
T_A	Operating free-air temperature		–40	85	°C

7.4 Thermal Resistance Characteristics

THERMAL METRIC[(1)]		PCA9535						UNIT
		DB (SSOP)	DBQ (SSOP)	DVG (TVSOP)	DW (SOIC)	PW (TSSOP)	RGV (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.9	61	86	108.8	48.4	43.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	2.3 V to 5.5 V	–1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising	$V_I = V_{CC}$ or GND, I_O = 0			1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling	$V_I = V_{CC}$ or GND, I_O = 0		0.75	1		V
V_{OH}	P-port high-level output voltage[2]	I_{OH} = –8 mA	2.3 V	1.8			V
			3 V	2.6			
			4.5 V	4.1			
			4.75 V	4.1			
		I_{OH} = –10 mA	2.3 V	1.7			
			3 V	2.5			
			4.5 V	4			
			4.75 V	4			
I_{OL}	SDA	V_{OL} = 0.4 V	2.3 V to 5.5 V	3	8		mA
	P port[3]	V_{OL} = 0.5 V	2.3 V	8	10		
			3 V	8	14		
			4.5 V	8	17		
			4.75 V	8	35		
		V_{OL} = 0.7 V	2.3 V	10	13		
			3 V	10	19		
			4.5 V	10	24		
			4.75 V	10	45		
	$\overline{INT}$	V_{OL} = 0.4 V	2.3 V to 5.5 V	3	10		
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	μA
	A0, A1, A2					±1	
I_{IH}	P port	$V_I = V_{CC}$	2.3 V to 5.5 V			1	μA
I_{IL}	P port	V_I = GND	2.3 V to 5.5 V			–1	μA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{scl} = 400 kHz	5.5 V		104	175	μA
			3.6 V		50	90	
			2.7 V		20	65	
		$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{scl} = 100 kHz	5.5 V		60	150	
			3.6 V		15	40	
			2.7 V		8	20	
	Standby mode	V_I = GND, I_O = 0, I/O = inputs, f_{scl} = 0 kHz	5.5 V		1.5	8.7	
			3.6 V		0.9	4	
			2.7 V		0.6	3	
ΔI_{CC}	Additional current in standby mode	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			1.5	mA
		All LED I/Os at V_I = 4.3 V, f_{scl} = 0 kHz	5.5 V			4	
C_i	SCL	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		4	8	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.3 V to 5.5 V		5.5	9.5	pF
	P port				8	9.5	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.
(2) The total current sourced by all I/Os must be limited to 85 mA.
(3) Each I/O must be externally limited to a maximum of 25 mA, and the P port (P7 – P0) must be limited to a maximum current of 200 mA.

7.6 I^2C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see 图 8-1)

			STANDARD MODE I^2C BUS		FAST MODE I^2C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I^2C clock frequency		0	100	0	400	kHz
t_{sch}	I^2C clock high time		4		0.6		μs
t_{scl}	I^2C clock low time		4.7		1.3		μs
t_{sp}	I^2C spike time			50		50	ns
t_{sds}	I^2C serial-data setup time		250		100		ns
t_{sdh}	I^2C serial-data hold time		0		0		ns
t_{icr}	I^2C input rise time			1000	$20 + 0.1C_b$ (1)	300	ns
t_{icf}	I^2C input fall time			300	$20 + 0.1C_b$ (1)	300	ns
t_{ocf}	I^2C output fall time	10-pF to 400-pF bus		300	$20 + 0.1C_b$ (1)	300	ns
t_{buf}	I^2C bus free time between stop and start		4.7		1.3		μs
t_{sts}	I^2C Start or repeated Start condition setup		4.7		0.6		μs
t_{sth}	I^2C Start or repeated Start condition hold		4		0.6		μs
t_{sps}	I^2C Stop condition setup		4		0.6		μs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid	300		50		ns
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.3	3.45	0.1	0.9	μs
C_b	I^2C bus capacitive load			400		400	ns

(1) C_b = total capacitive of one bus in pF

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see 图 8-2 and 图 8-3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	STANDARD MODE I^2C BUS		FAST MODE I^2C BUS		UNIT
				MIN	MAX	MIN	MAX	
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4		4	μs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4		4	μs
t_{pv}	Output data valid	SCL	P7 – P0		350		350	ns
t_{ps}	Input data setup time	P port	SCL	100		100		ns
t_{ph}	Input data hold time	P port	SCL	1		1		μs

7.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

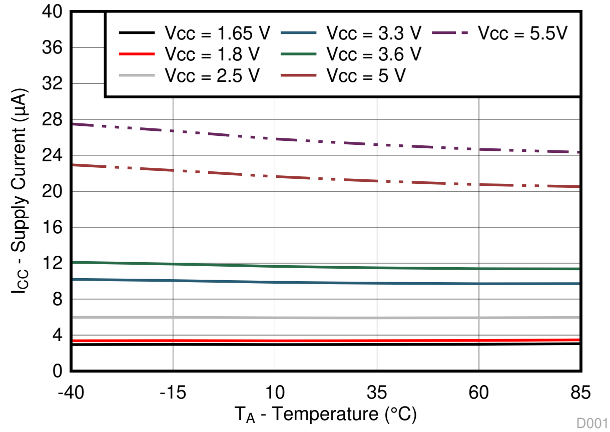


图 7-1. Supply Current vs Temperature for Different Supply Voltage (V_{CC})

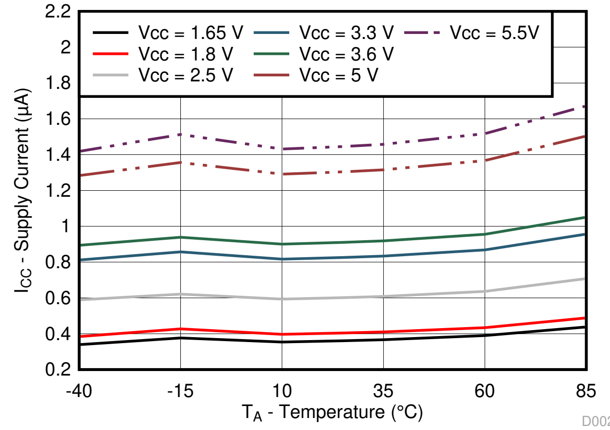


图 7-2. Standby Supply Current vs Temperature for Different Supply Voltage (V_{CC})

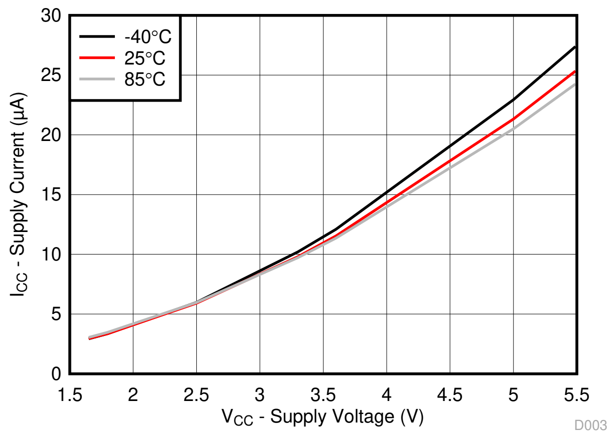


图 7-3. Supply Current vs Supply Voltage for Different Temperature (T_A)

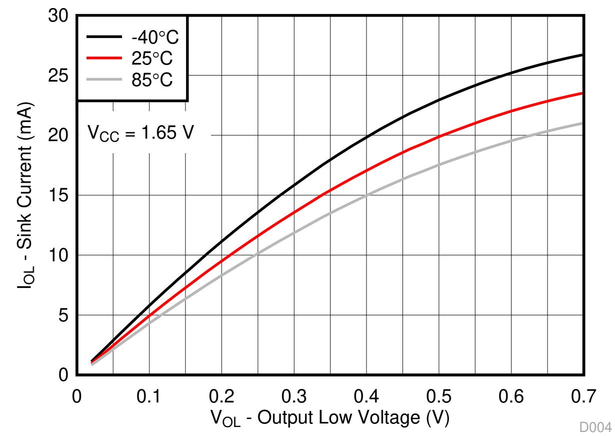


图 7-4. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

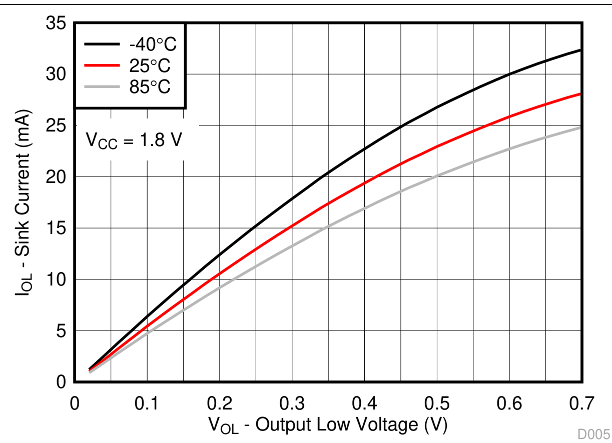


图 7-5. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

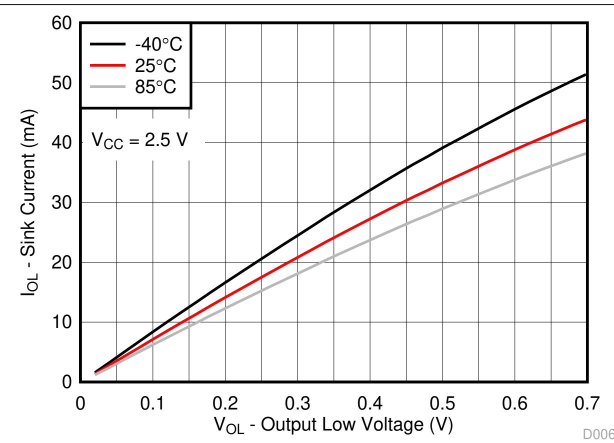


图 7-6. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 2.5 V

7.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

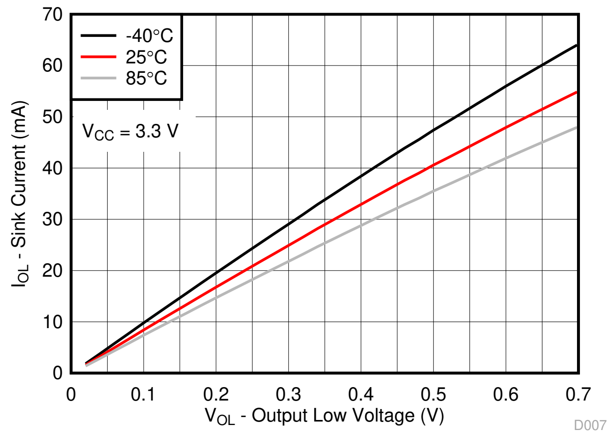


图 7-7. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

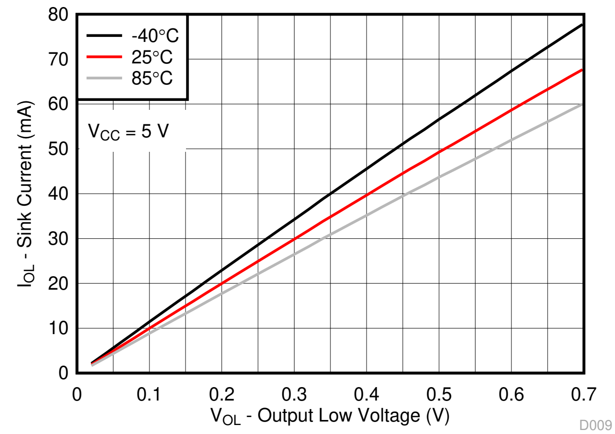


图 7-8. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5 V

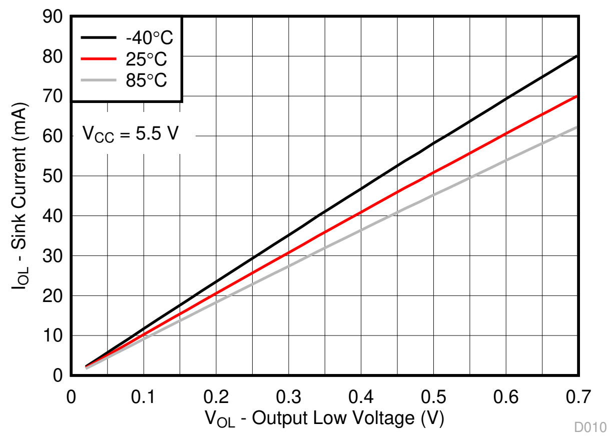


图 7-9. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5.5 V

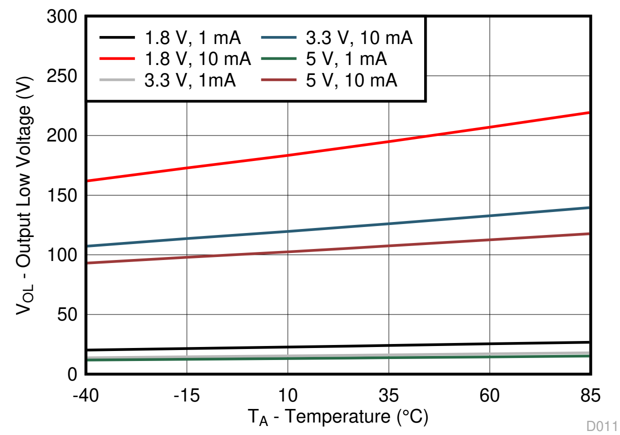


图 7-10. II/O Low Voltage vs Temperature for Different V_{CC} and I_{OL}

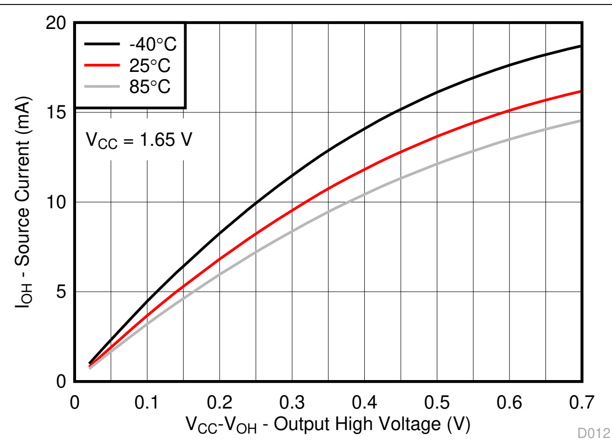


图 7-11. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

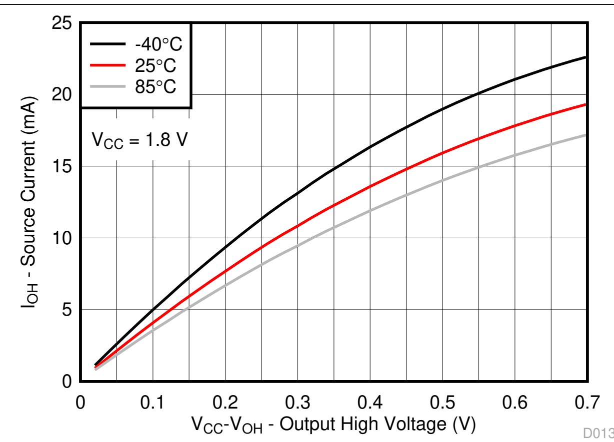


图 7-12. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

7.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

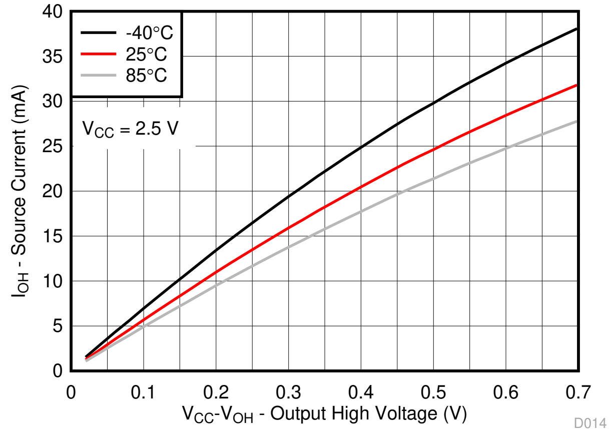


图 7-13. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 2.5 V

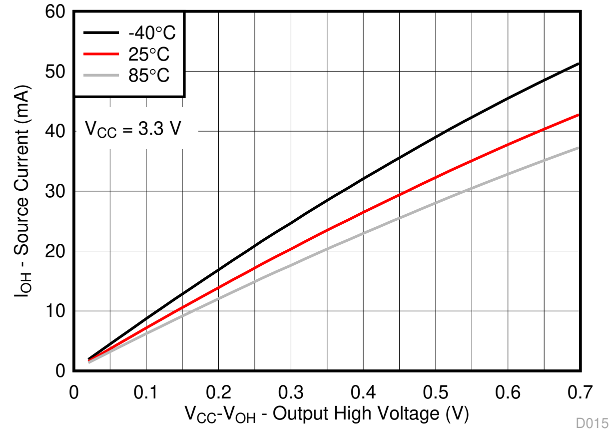


图 7-14. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

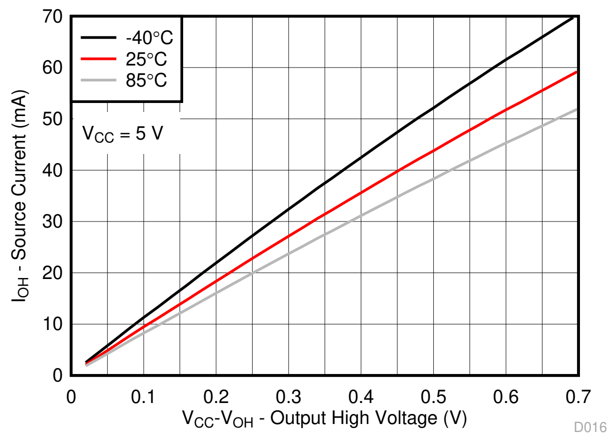


图 7-15. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 5 V

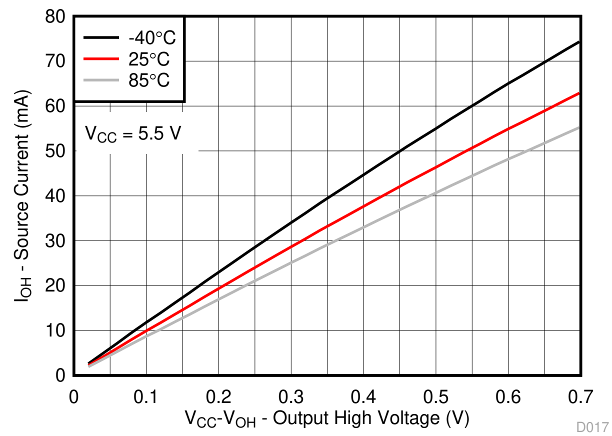


图 7-16. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 5.5 V

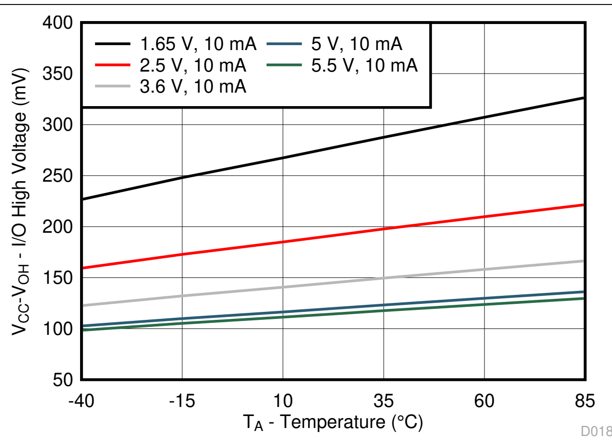


图 7-17. V_{CC} – V_{OH} Voltage vs Temperature for Different V_{CC}

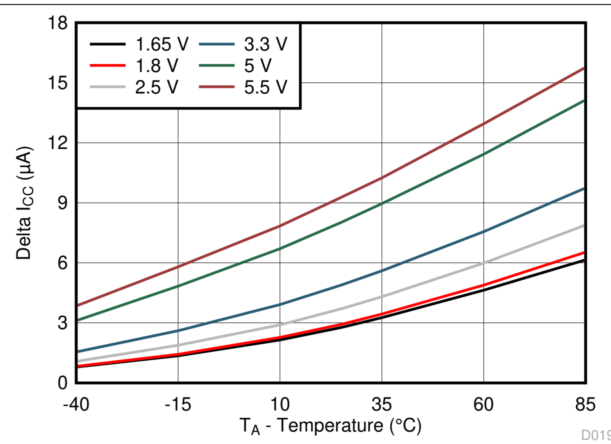
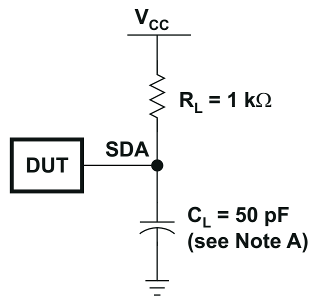
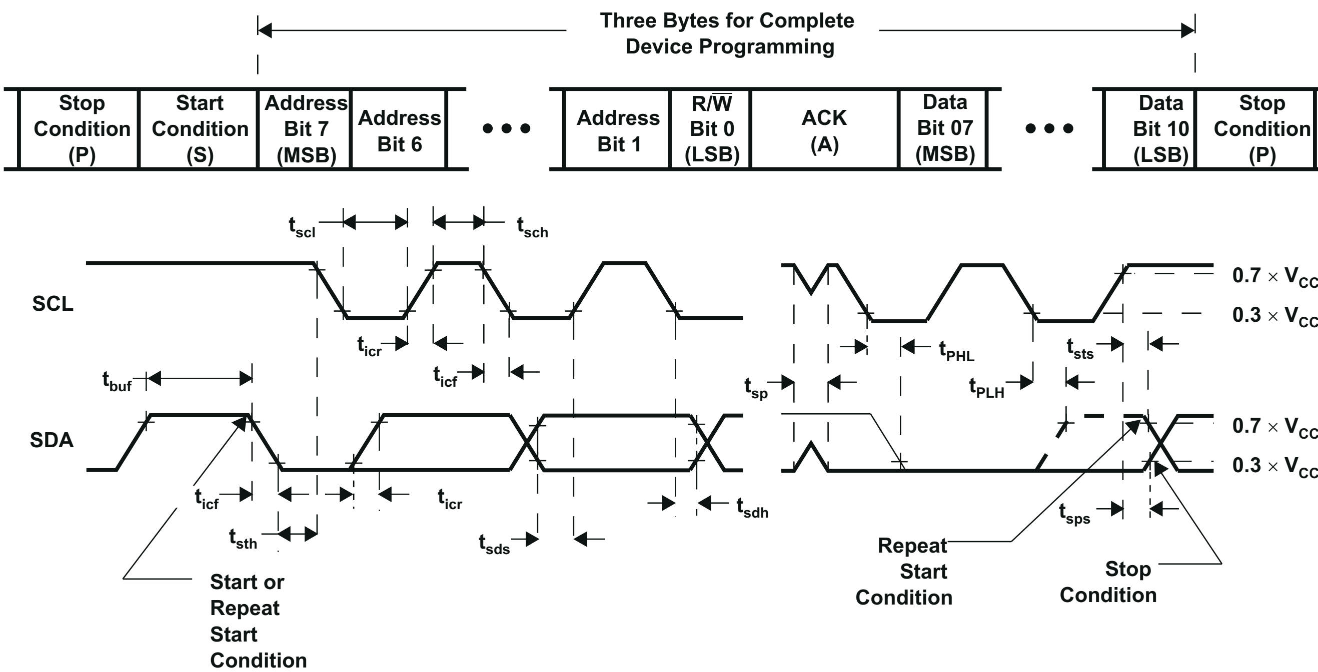


图 7-18. Δ I_{CC} vs Temperature for Different V_{CC} ($V_I = V_{CC}$ – 0.6 V)

8 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

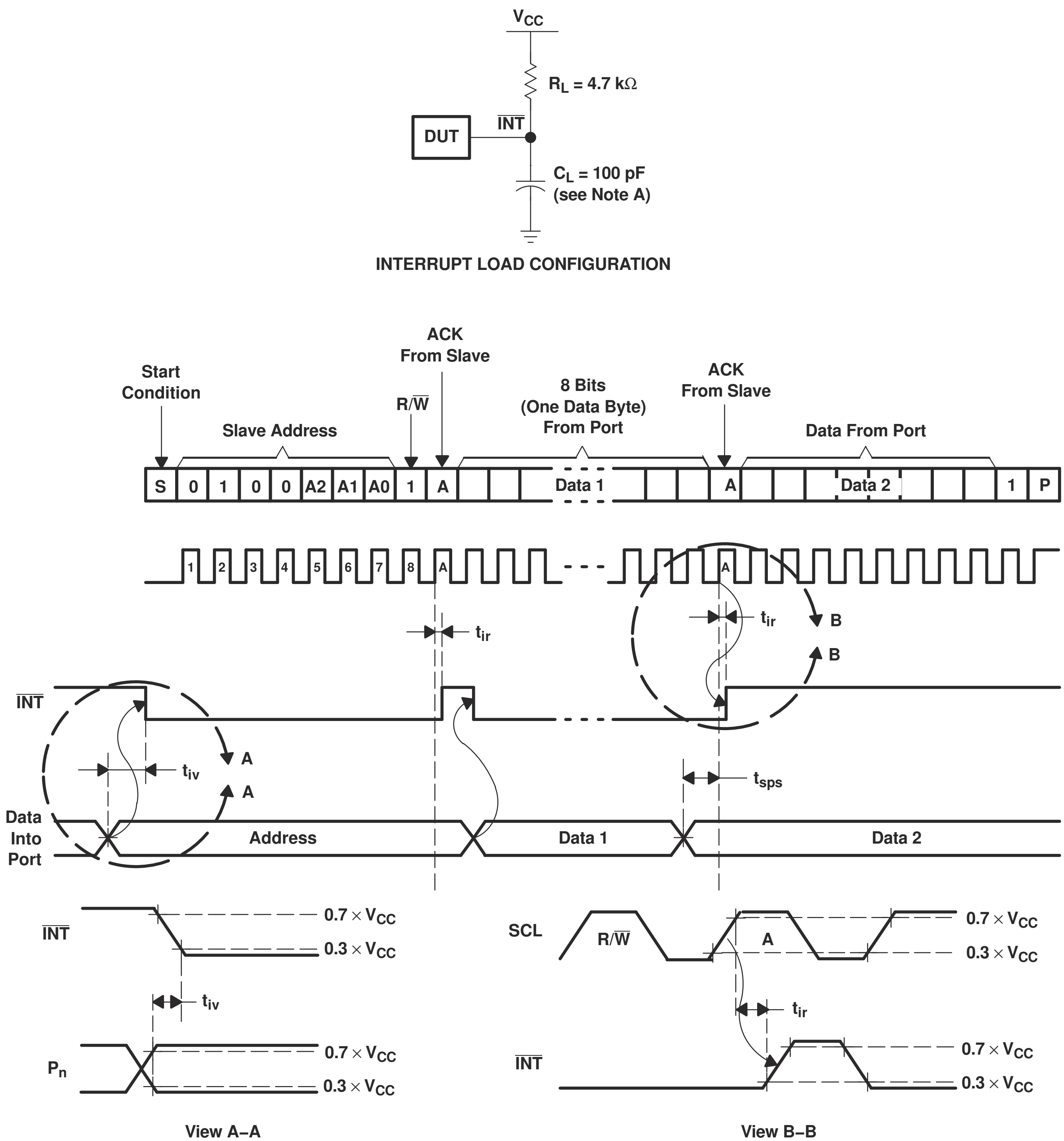
BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

图 8-1. I^2C Interface Load Circuit And Voltage Waveforms

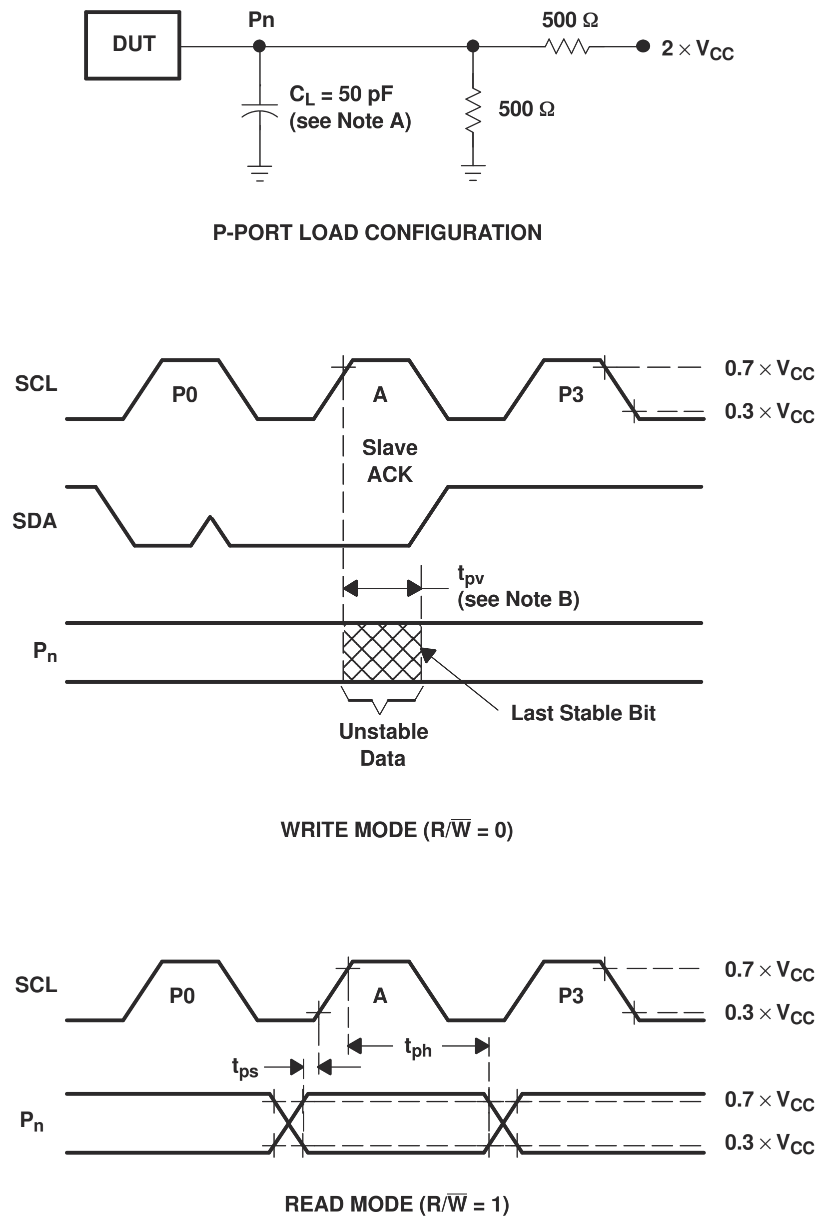


A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ⩽ 10 MHz, Z_O = 50 Ω, t_r/t_f ⩽ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

图 8-2. Interrupt Load Circuit And Voltage Waveforms

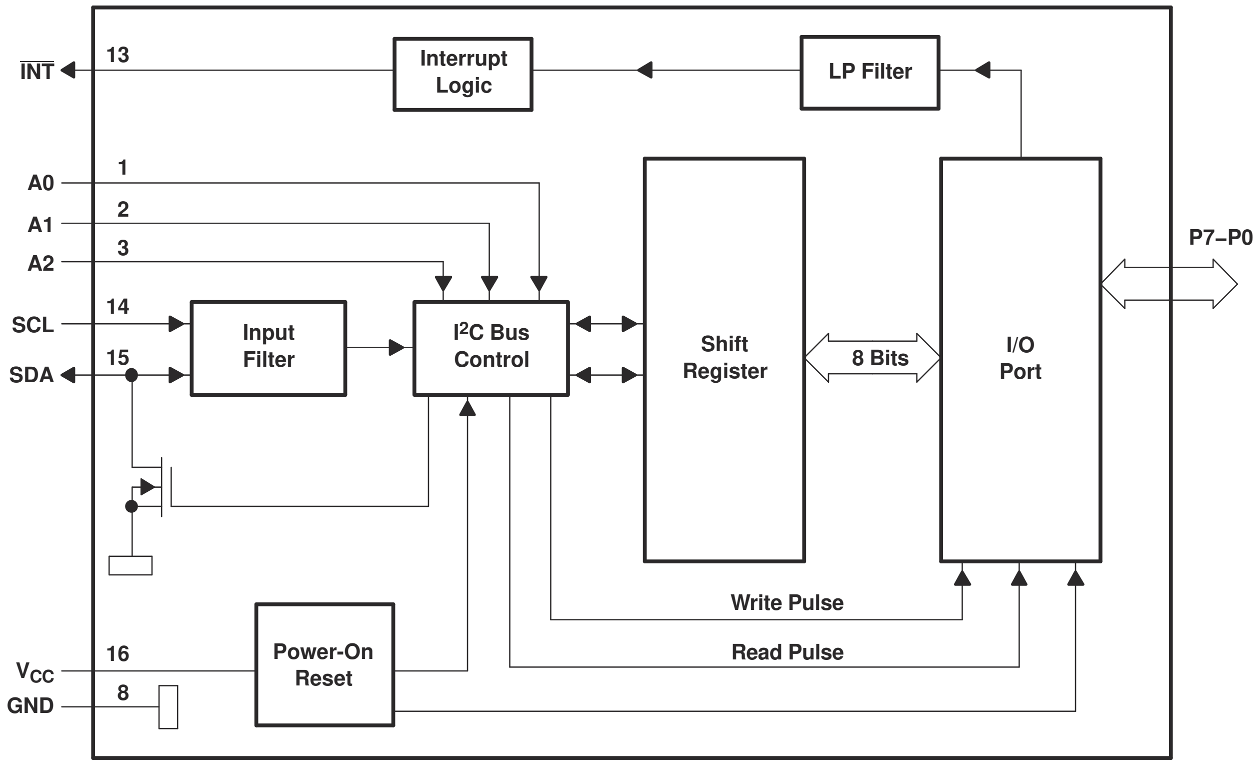


A. C_L includes probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

图 8-3. P-Port Load Circuit And Voltage Waveforms

9 Detailed Description

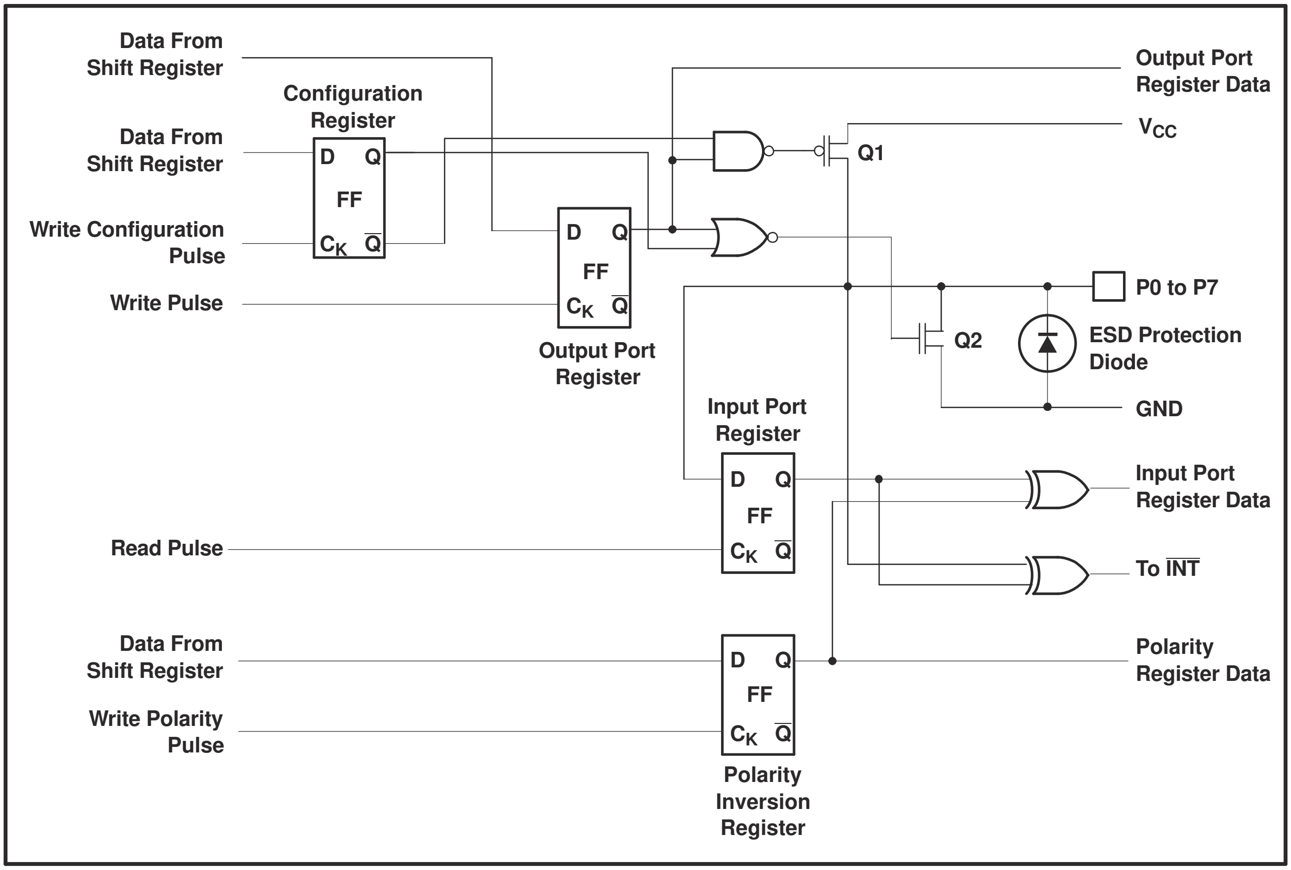
9.1 Functional Block Diagram



A. Pin numbers shown are for DB, DGV, DW, or PW package.

B. All I/Os are set to inputs at reset.

图 9-1. Logic Diagram (Positive Logic)



A. At power-on reset, all registers return to default values.

图 9-2. Simplified Schematic of P0 to P7

9.2 Device Functional Modes

9.2.1 Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9534 in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the PCA9534 registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

9.2.2 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in 图 9-2) are off, creating a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

9.2.3 Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. Writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. Because each 8-pin port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1 or vice versa.

The $\overline{\text{INT}}$ output has an open-drain structure and requires pullup resistor to V_{CC}.

9.2.3.1 Interrupt Errata

9.2.3.1.1 Description

The INT will be improperly de-asserted if the following two conditions occur:

1. The last I²C command byte (register pointer) written to the device was 00h.

> **Note**
>
> This generally means the last operation with the device was a Read of the input register. However, the command byte may have been written with 00h without ever going on to read the input register. After reading from the device, if no other command byte written, it will remain 00h.

2. Any other slave device on the I2C bus acknowledges an address byte with the R/W bit set high

9.2.3.1.2 System Impact

Can cause improper interrupt handling as the Master will see the interrupt as being cleared.

9.2.3.1.3 System Workaround

Minor software change: User must change command byte to something besides 00h after a Read operation to the PCA9534 device or before reading from another slave device.

> **Note**
>
> Software change will be compatible with other versions (competition and TI redesigns) of this device.

9.3 Programming

9.3.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see 图 9-3). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/ $\overline{\text{W}}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/ output during the high of the ACK-related clock pulse. The address inputs (A0 – A2) of the slave device must not be changed between the Start and Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see 图 9-4).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see 图 9-3).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see 图 9-5). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver will signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

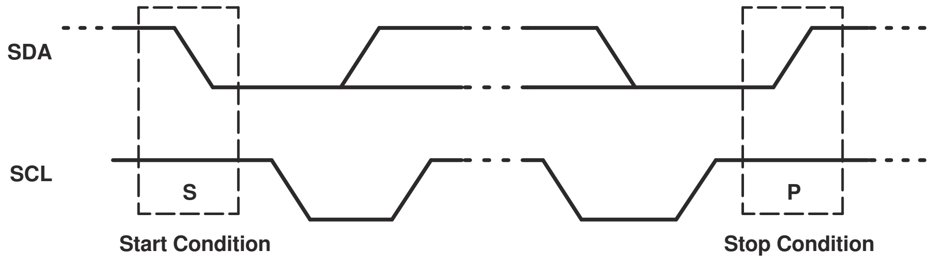


图 9-3. Definition Of Start And Stop Conditions

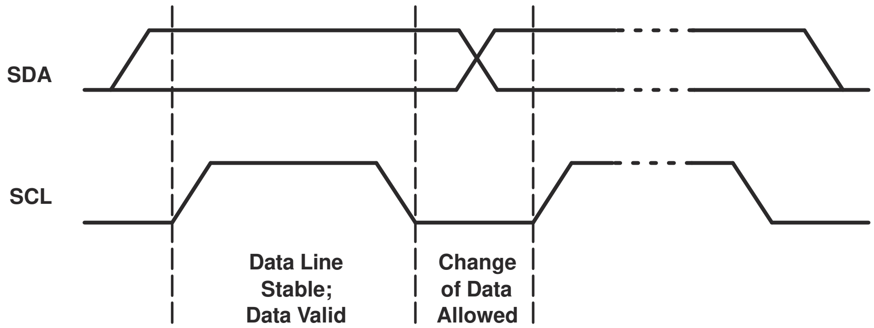


图 9-4. Bit Transfer

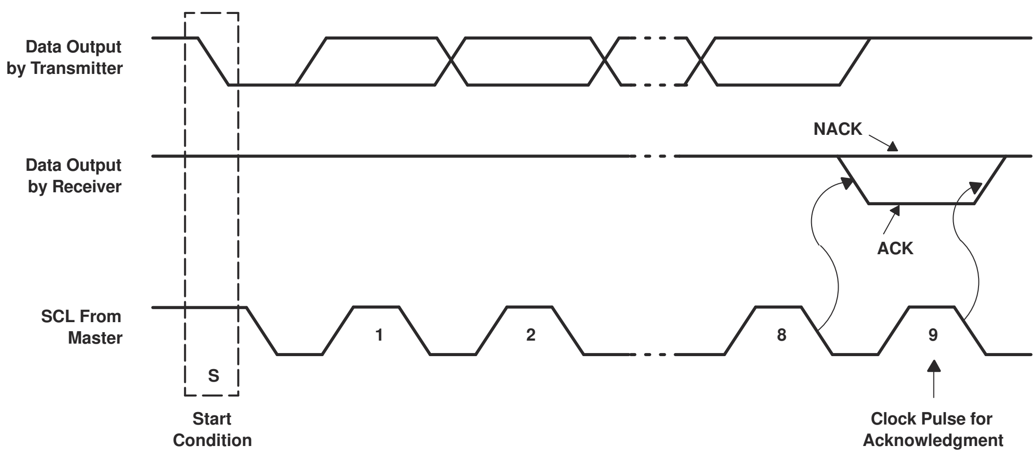


图 9-5. Acknowledgment On I²C Bus

9.3.2 Register Map

表 9-1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	L	H	L	L	A2	A1	A0	R/ $\overline{W}$
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

9.3.2.1 Device Address

图 9-6 shows the address byte of the PCA9534.

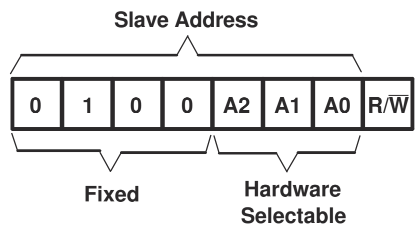


图 9-6. Pca9534 Address

表 9-2. Address Reference

INPUTS			I²C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

9.3.2.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte, which is stored in the control register in the PCA9534. Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that will be affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

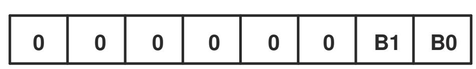


图 9-7. Control Register Bits

表 9-3. Command Byte

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0x00	Input Port	Read byte	xxxx xxxx
0	1	0x01	Output Port	Read/write byte	1111 1111
1	0	0x02	Polarity Inversion	Read/write byte	0000 0000
1	1	0x03	Configuration	Read/write byte	1111 1111

9.3.2.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I²C device know that the Input Port register will be accessed next.

表 9-4. Register 0 (Input Port Register)

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

表 9-5. Register 1 (Output Port Register)

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained.

表 9-6. Register 2 (Polarity Inversion Register)

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

表 9-7. Register 3 (Configuration Register)

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

9.3.2.4 Bus Transactions

Data is exchanged between the master and PCA9534 through write and read commands.

9.3.2.4.1 Writes

Data is transmitted to the PCA9534 by sending the device address and setting the least significant bit (LSB) to a logic 0 (see 图 9-6 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte (see 图 9-8 and 图 9-9). There is no limitation on the number of data bytes sent in one write transmission.

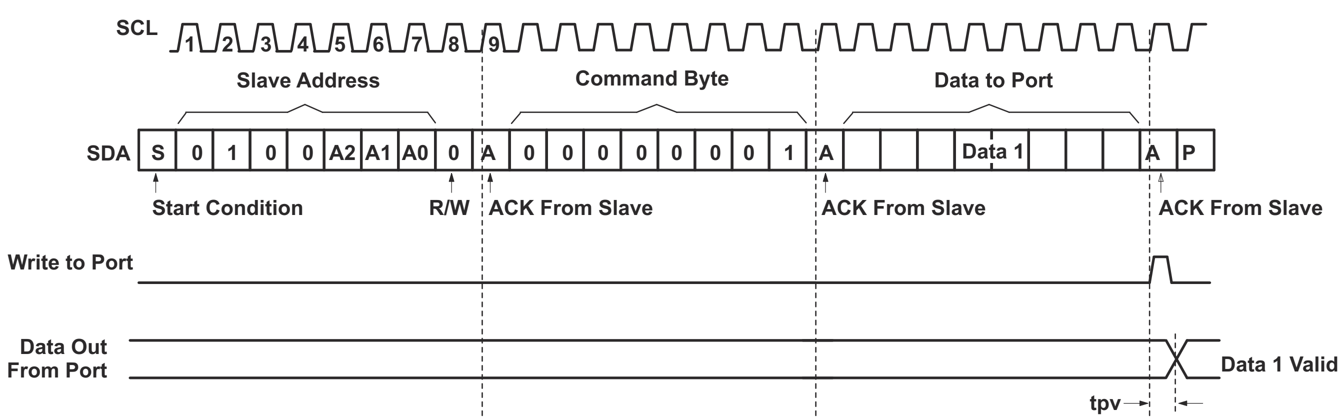


图 9-8. Write To Output Port Register

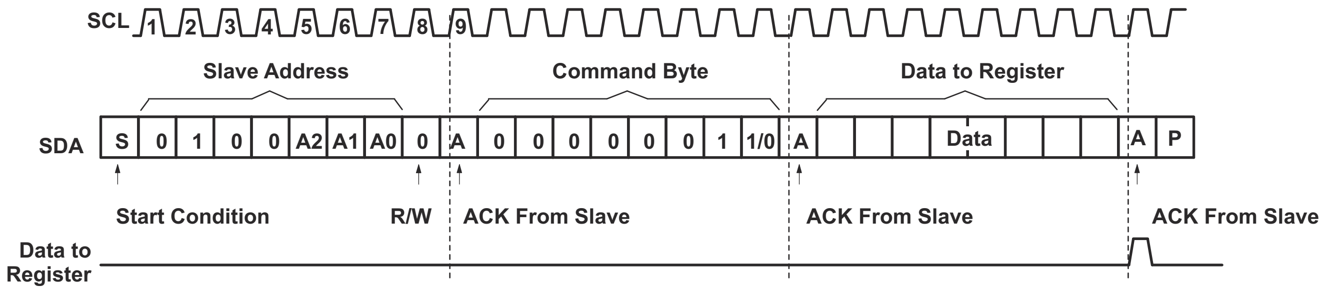


图 9-9. Write To Configuration Or Polarity Inversion Registers

9.3.2.4.2 Reads

The bus master first must send the PCA9534 address with the LSB set to a logic 0 (see 图 9-6 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9534 (see 图 9-10 and 图 9-11). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

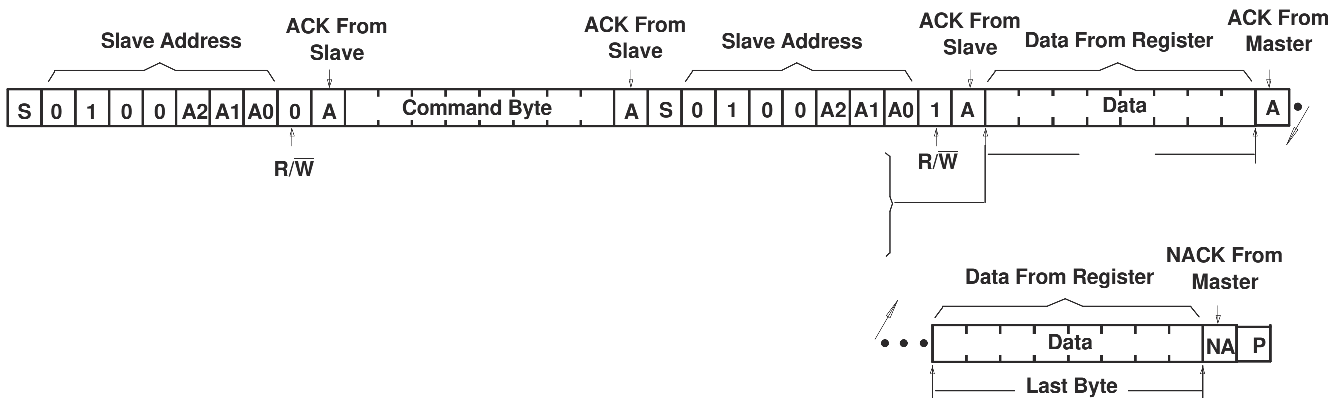
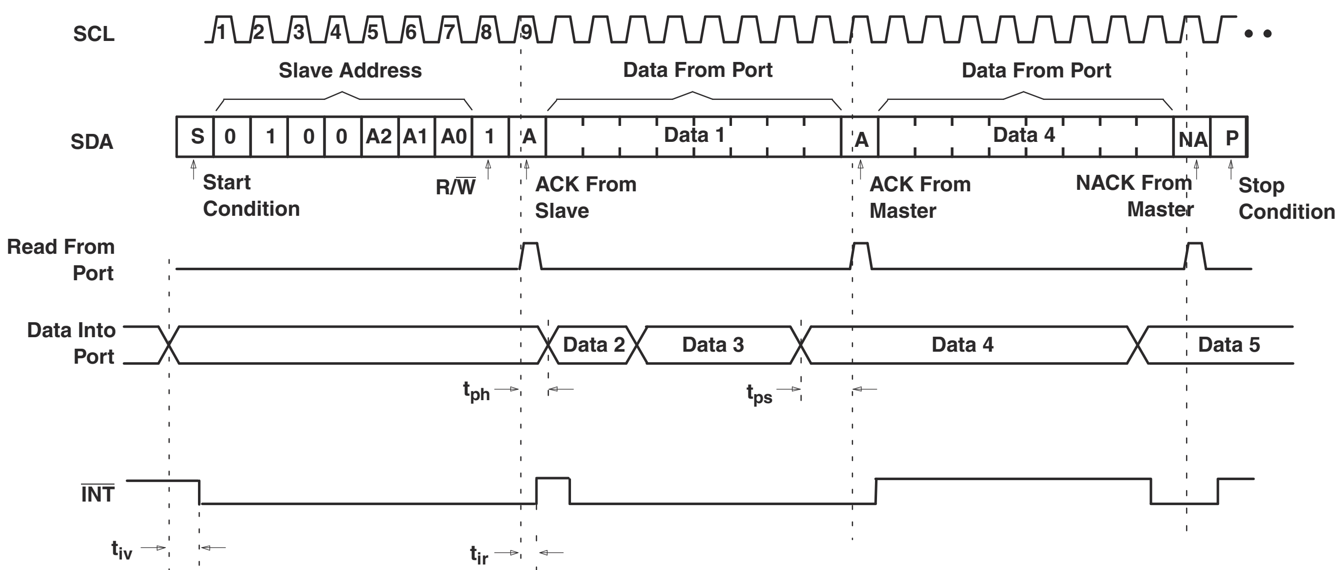


图 9-10. Read From Register



A. This figure assumes that the command byte has previously been programmed with 00h.
B. Transfer of data can be stopped at any moment by a Stop condition.
C. This figure eliminates the command byte transfer, a restart and slave address call between the initial slave address call and the actual data transfer from the P Port. See 图 9-10 for these details.

图 9-11. Read Input Port Register

10 Application Information Disclaimer

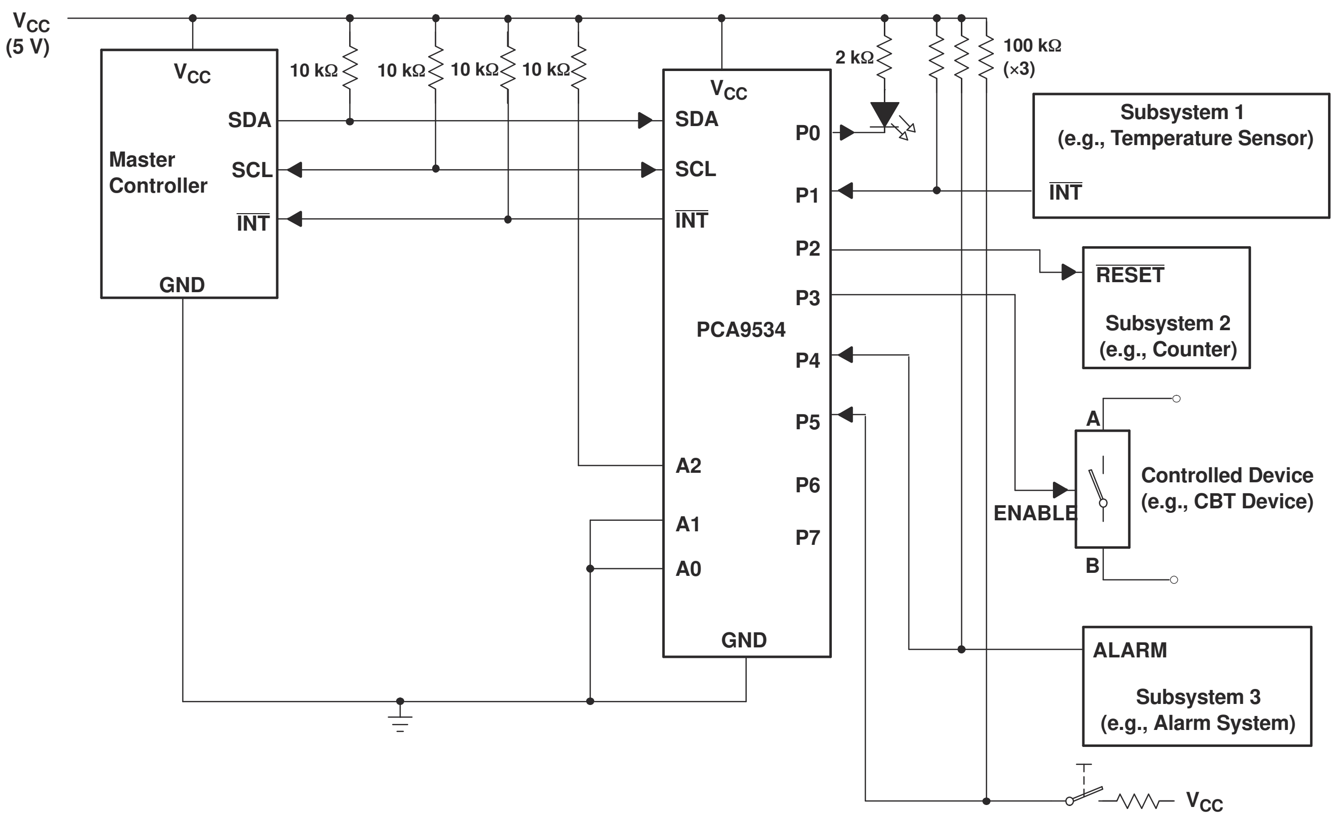
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI' s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Typical Application

图 10-1 shows an application in which the PCA9534 can be used.



A. Device address is configured as 0100100 for this example.
B. P0, P2, and P3 are configured as outputs.
C. P1, P4, and P5 are configured as inputs.
D. P6 and P7 are not used and must be configured as outputs.

图 10-1. Typical Application

10.1.1.1 Design Requirements

10.1.1.1.1 Minimizing I_{CC} When The I/O Controls Leds

When the I/Os are used to control LEDs, they are normally connected to V_{CC} through a resistor, as shown in 图 10-1. Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The supply current, I_{CC}, increases as V_{IN} becomes lower than V_{CC} and is specified as ΔI_{CC} in *Electrical Characteristics*.

For battery-powered applications, it is essential that the voltage of the I/O pins is greater than or equal to V_{CC} when the LED is off to minimize current consumption. 图 10-2 shows a high-value resistor in parallel with the LED. 图 10-3 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevents additional supply-current consumption when the LED is off.

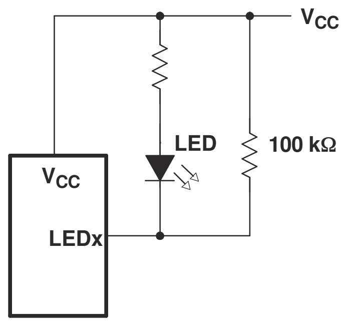


图 10-2. High-Value Resistor In Parallel With The Led

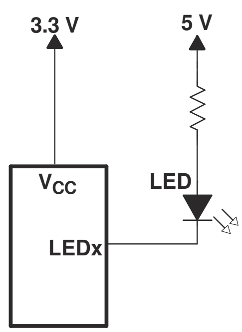


图 10-3. Device Supplied By A Lower Voltage

11 Power Supply Recommendations

11.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCA9534 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in 图 11-1 and 图 11-2.

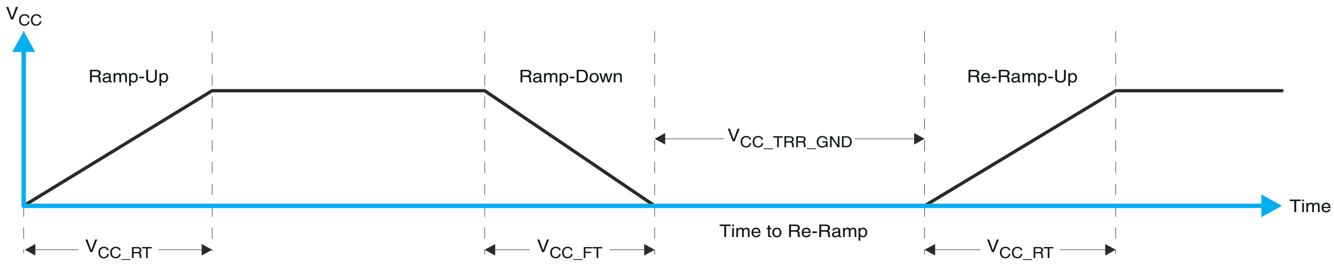


图 11-1. V_{CC} Is Lowered Below 0.2 V Or 0 V And Then Ramped Up To V_{CC}

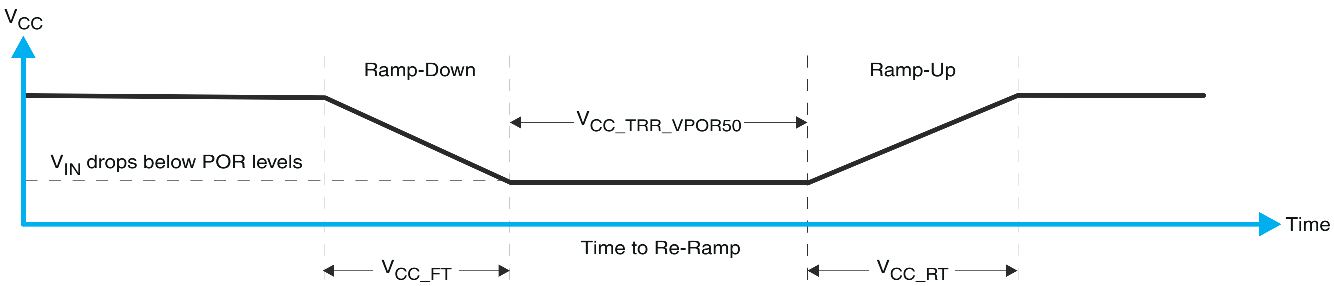


图 11-2. V_{CC} Is Lowered Below The Por Threshold, Then Ramped Back Up To V_{CC}

表 11-1 specifies the performance of the power-on reset feature for PCA9534 for both types of power-on reset.

表 11-1. Recommended Supply Sequencing And Ramp Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See 图 11-1	1		100	ms
V_{CC_RT}	Rise rate	See 图 11-1	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See 图 11-1	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	See 图 11-2	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 μs	See 图 11-3			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See 图 11-3				μs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}		1.033		1.428	V

(1) T_A = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and the device impedance are factors that affect power-on reset performance. 图 11-3 and 表 11-1 provide more information on how to measure these specifications.

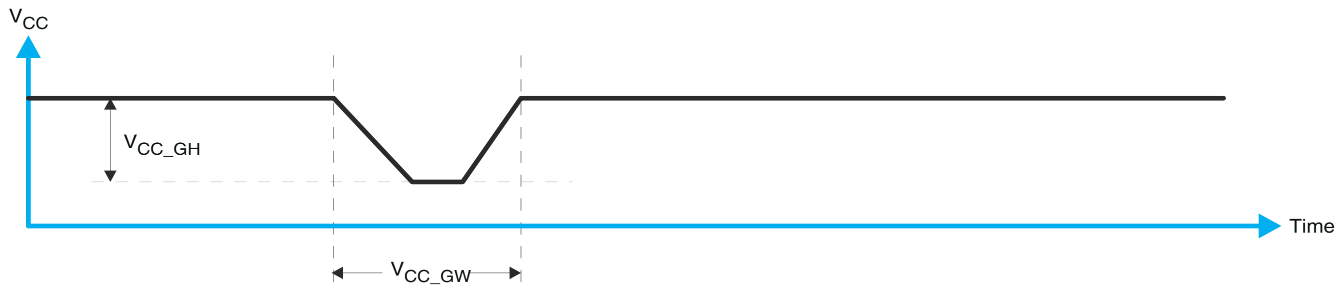


图 11-3. Glitch Width And Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. 图 11-4 and 表 11-1 provide more details on this specification.

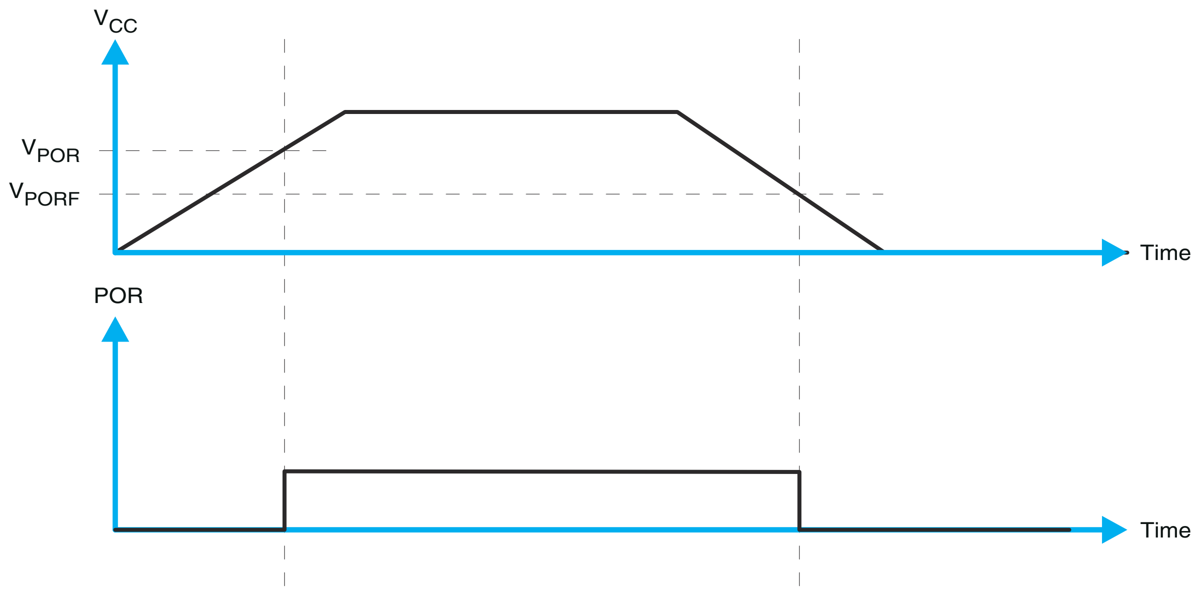


图 11-4. V_{POR}

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9534DB	ACTIVE	SSOP	DB	16	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534	Samples
PCA9534DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534	Samples
PCA9534DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534	Samples
PCA9534DW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 85	PCA9534	
PCA9534DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9534	Samples
PCA9534PW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	PD534	
PCA9534PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD534	Samples
PCA9534RGVR	ACTIVE	VQFN	RGV	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD534	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

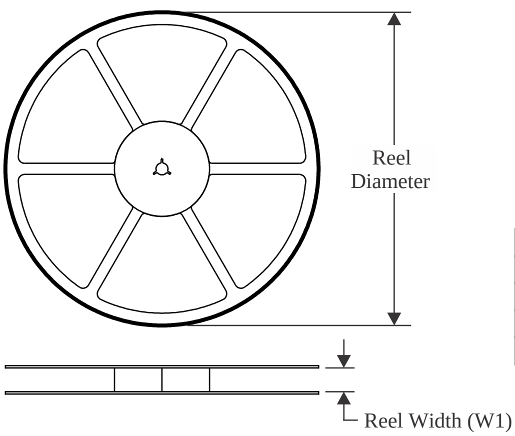
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

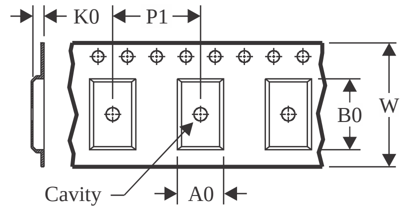
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

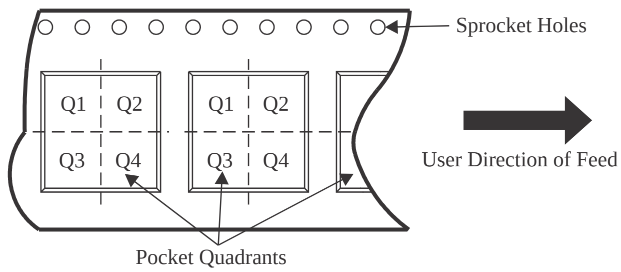


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

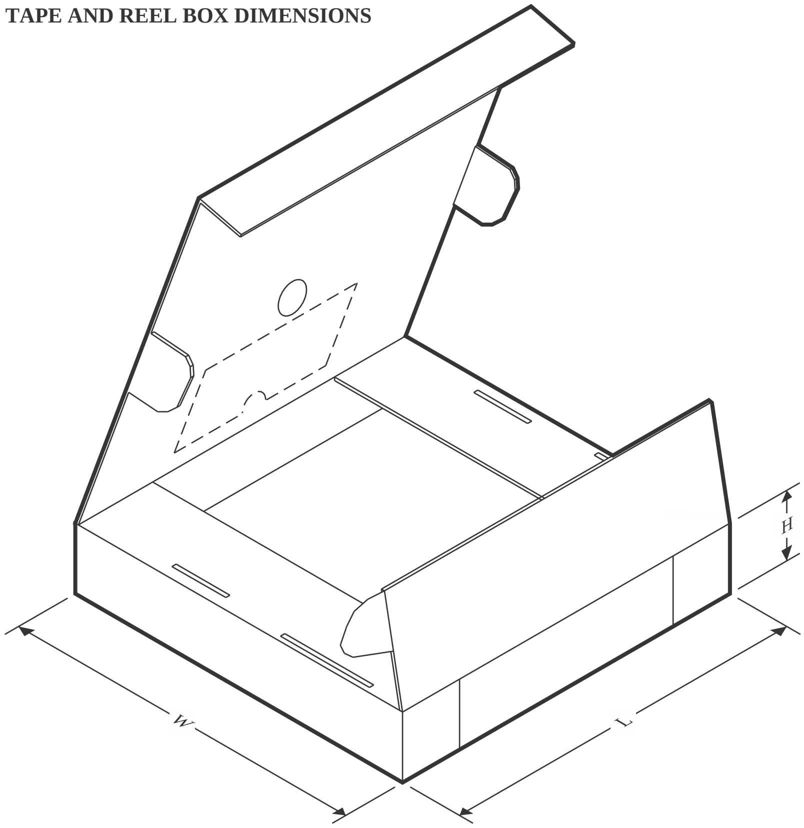
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9534DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
PCA9534DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
PCA9534DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PCA9534PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9534PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9534RGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

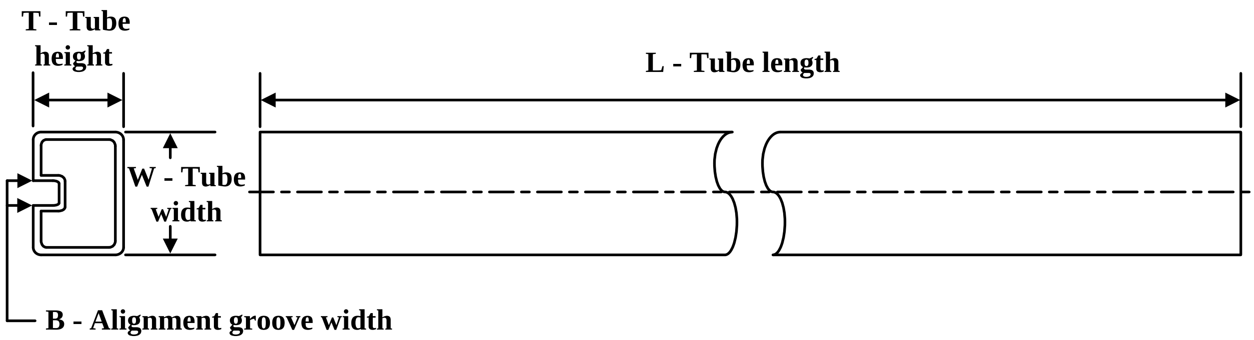
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9534DBR	SSOP	DB	16	2000	356.0	356.0	35.0
PCA9534DGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
PCA9534DWR	SOIC	DW	16	2000	350.0	350.0	43.0
PCA9534PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
PCA9534PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
PCA9534RGVR	VQFN	RGV	16	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

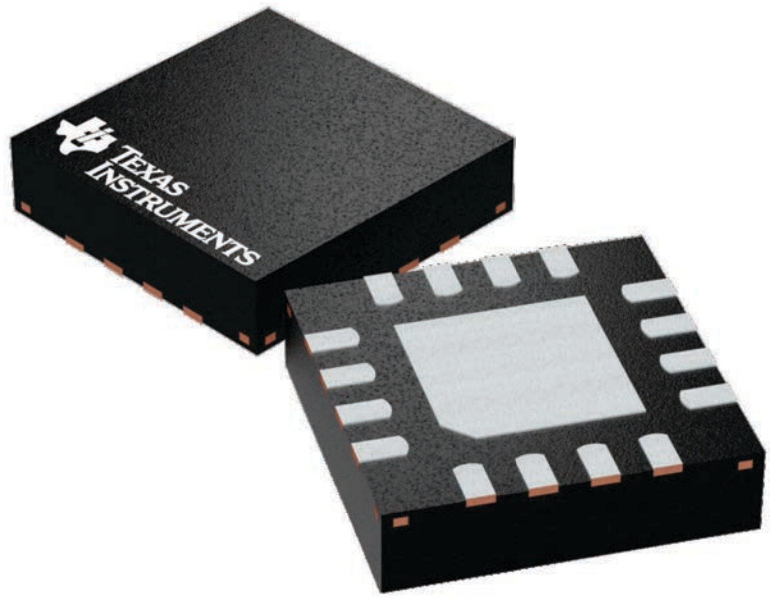
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCA9534DB	DB	SSOP	16	80	530	10.5	4000	4.1

RGV 16

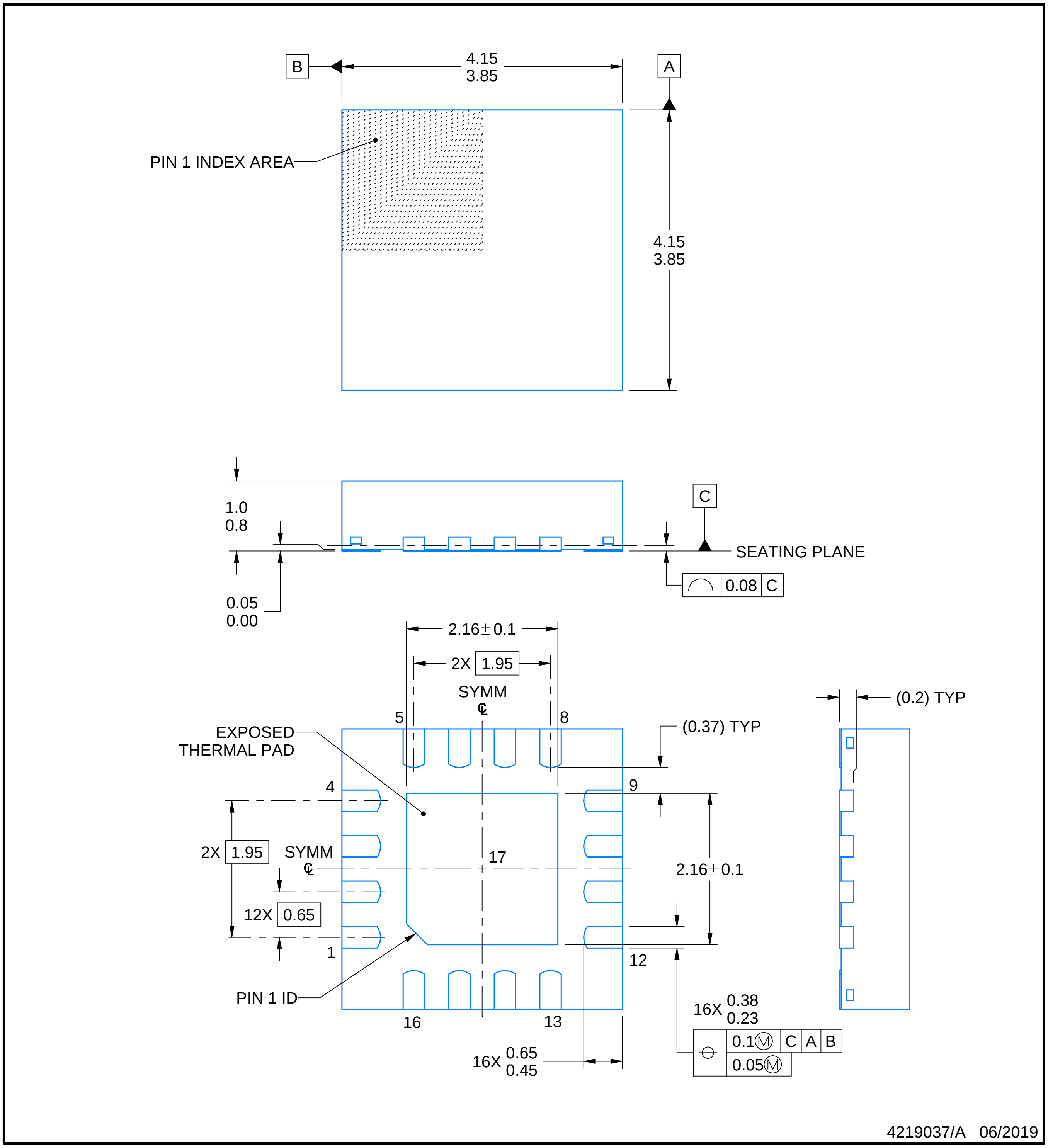
VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

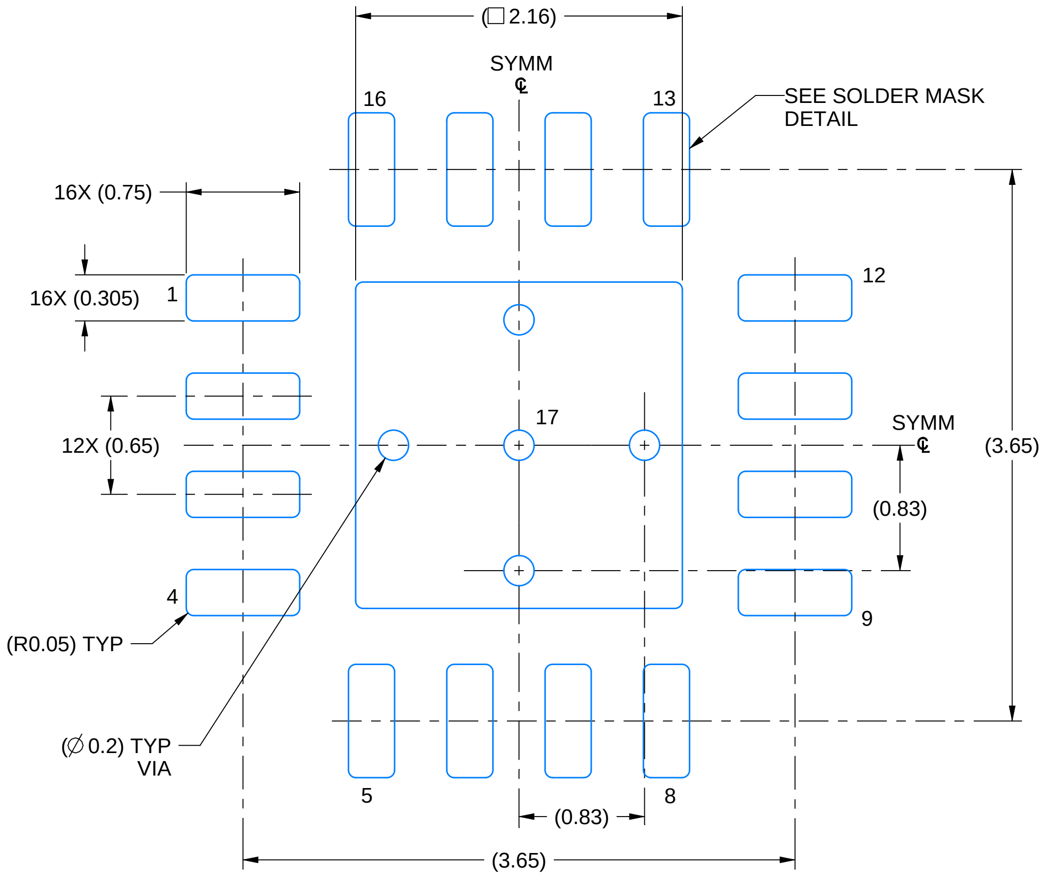


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

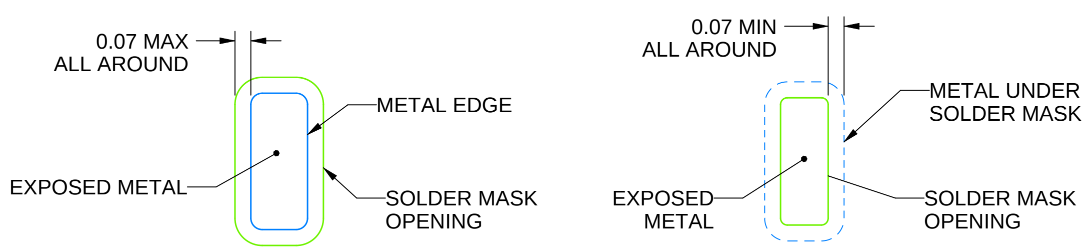


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK
DEFINED
(PREFERRED)

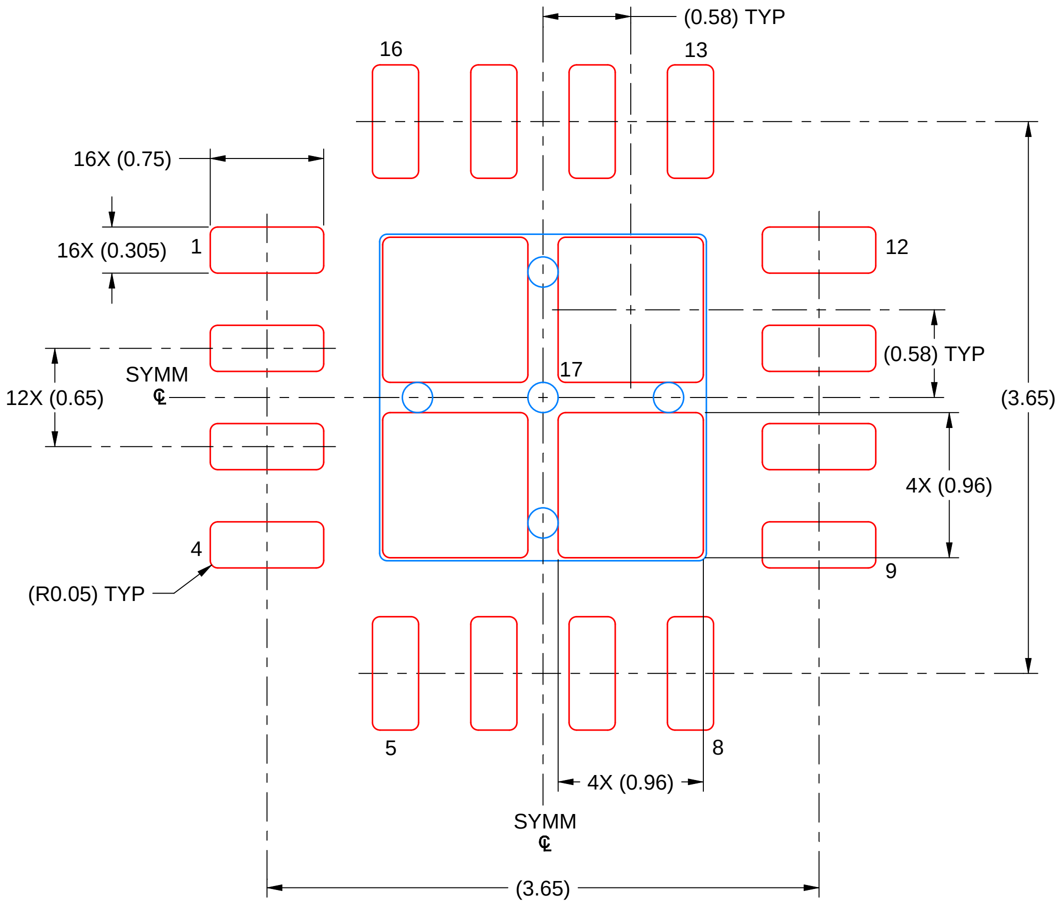
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219037/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



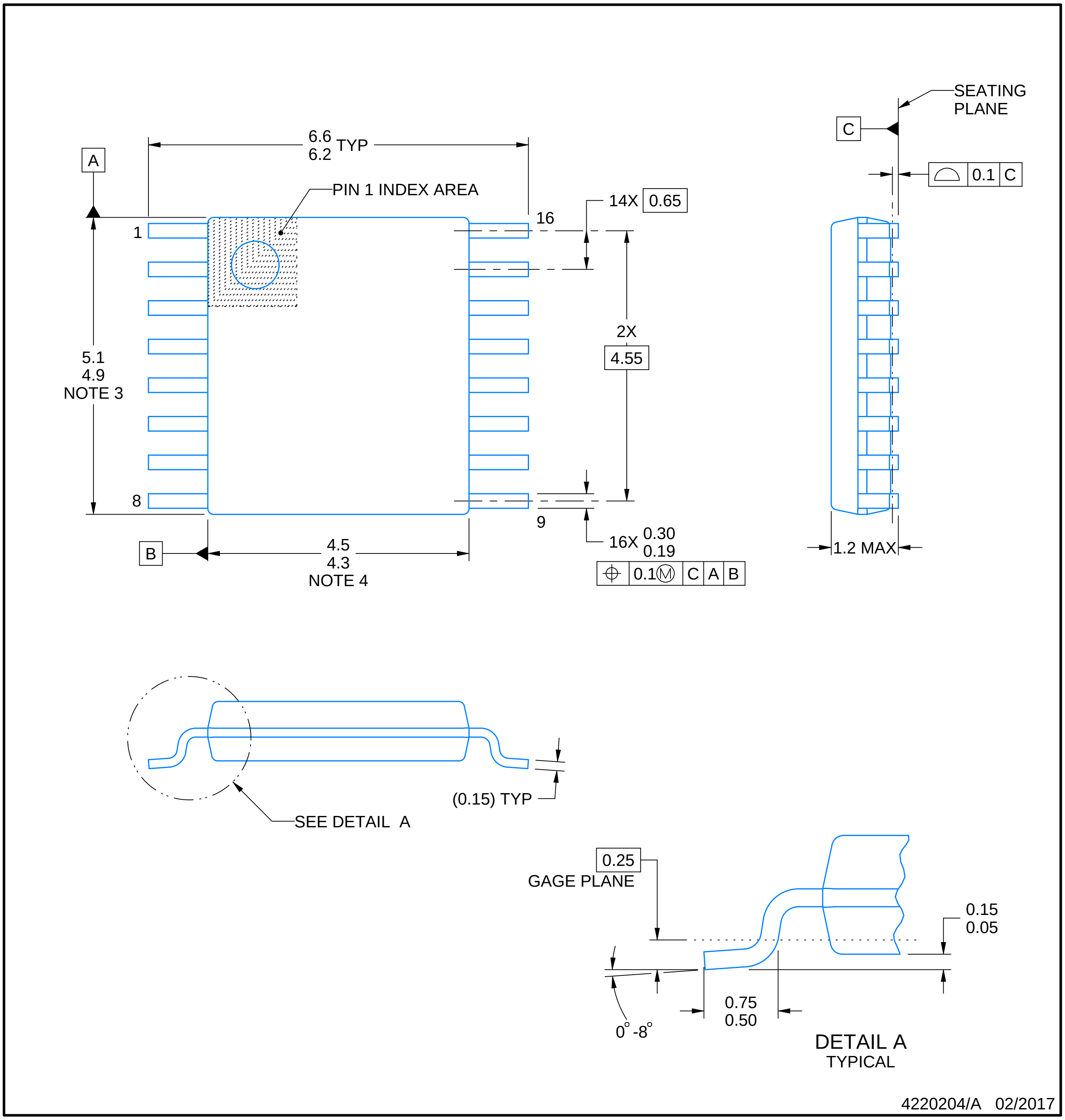
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219037/A 06/2019

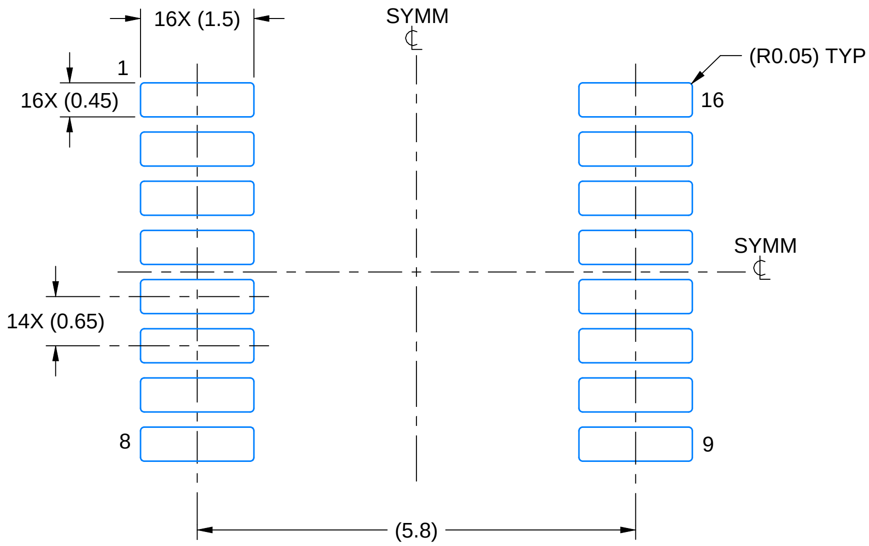
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

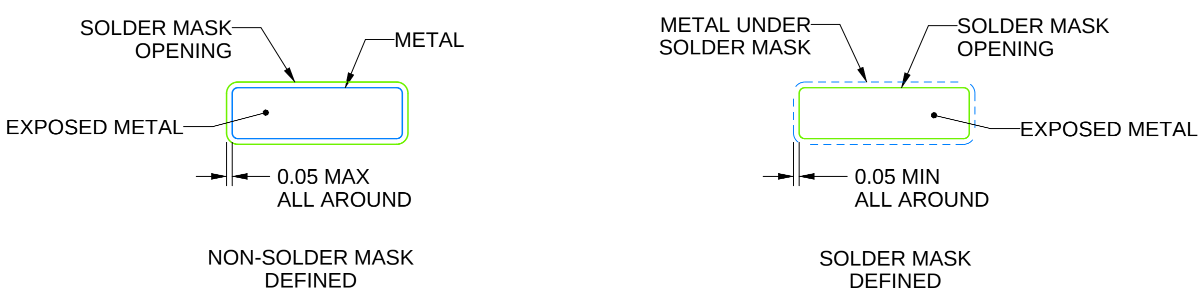


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

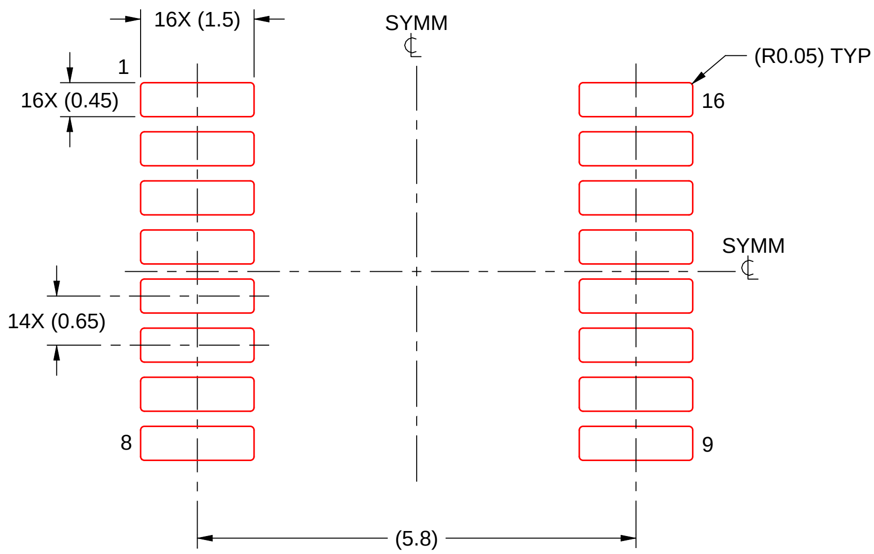


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

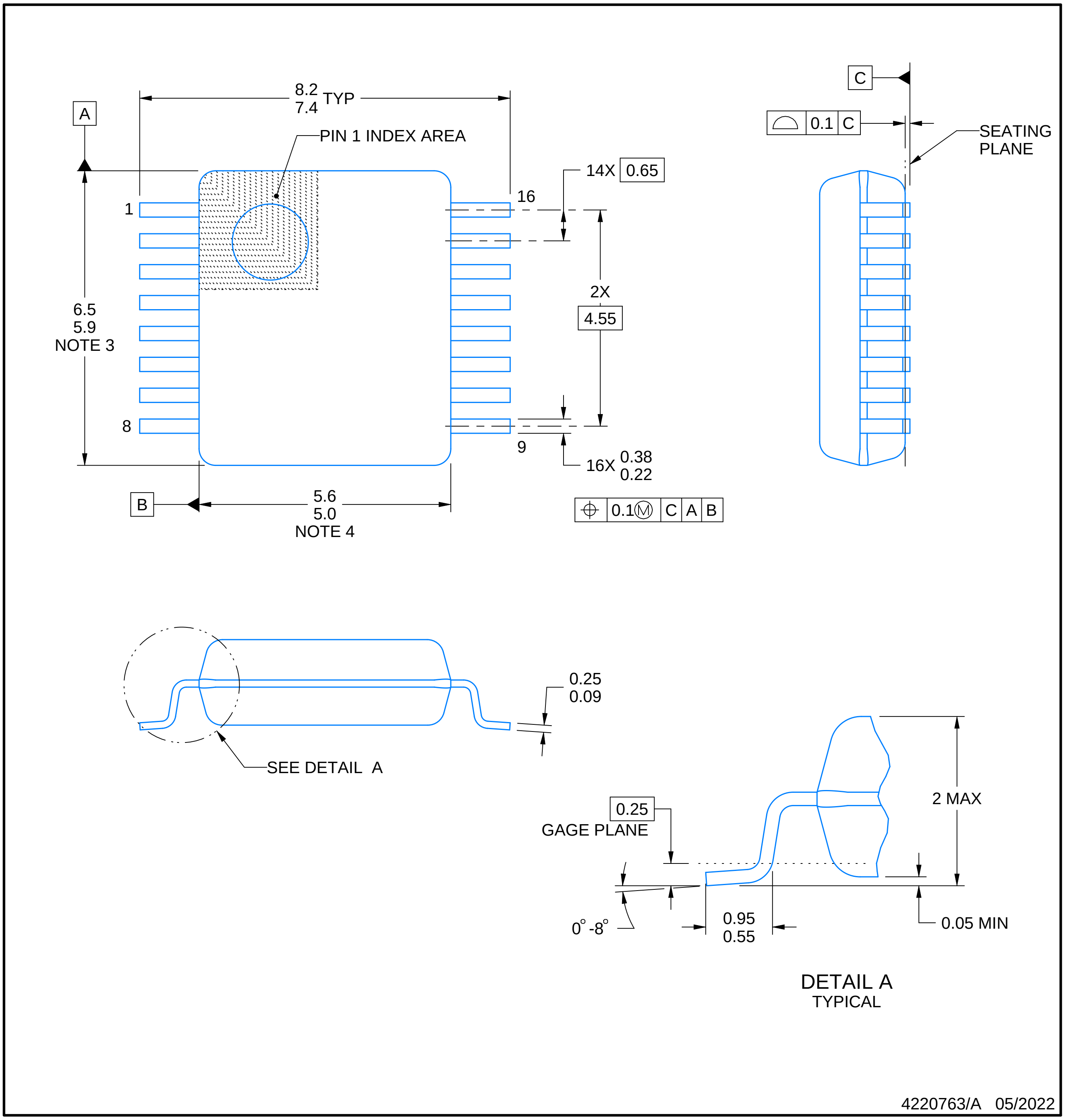


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

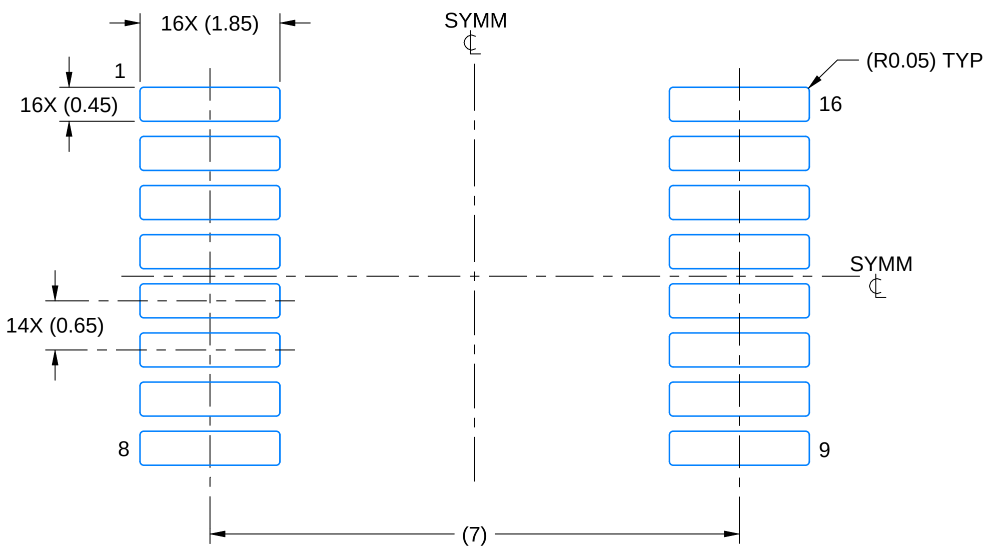
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

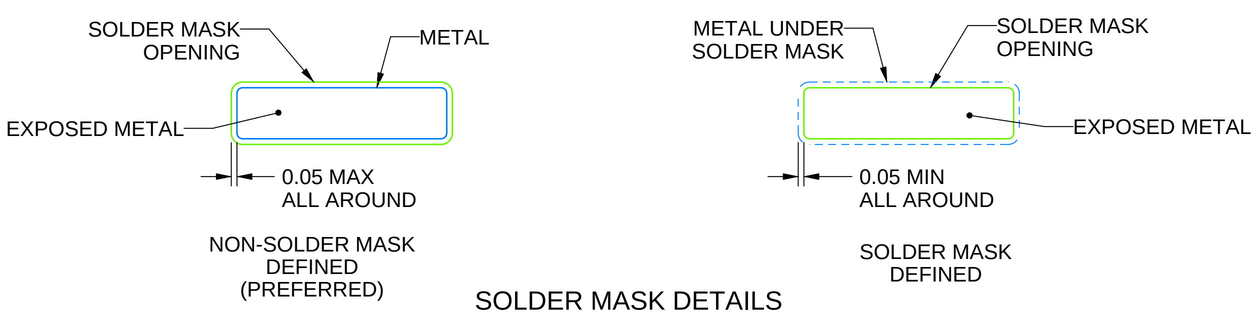


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

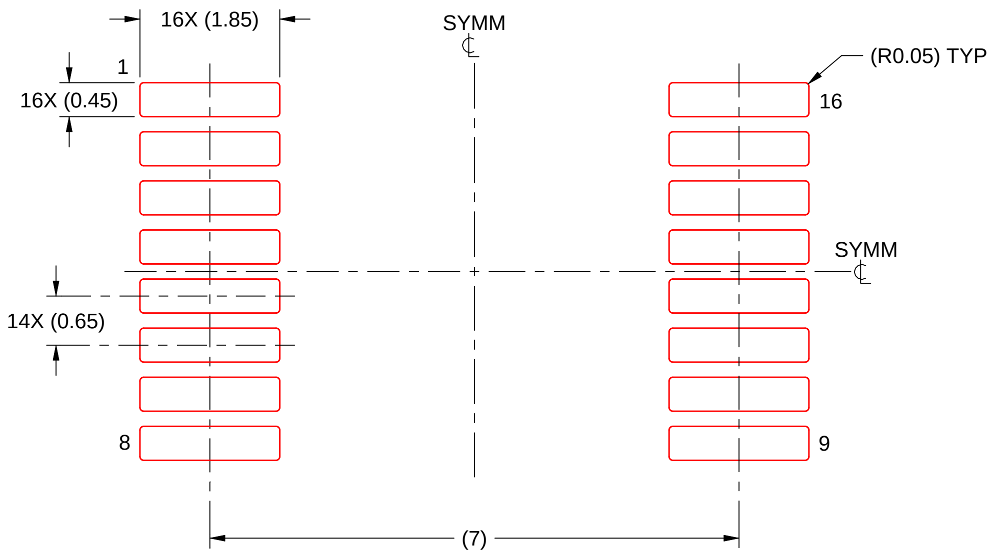


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



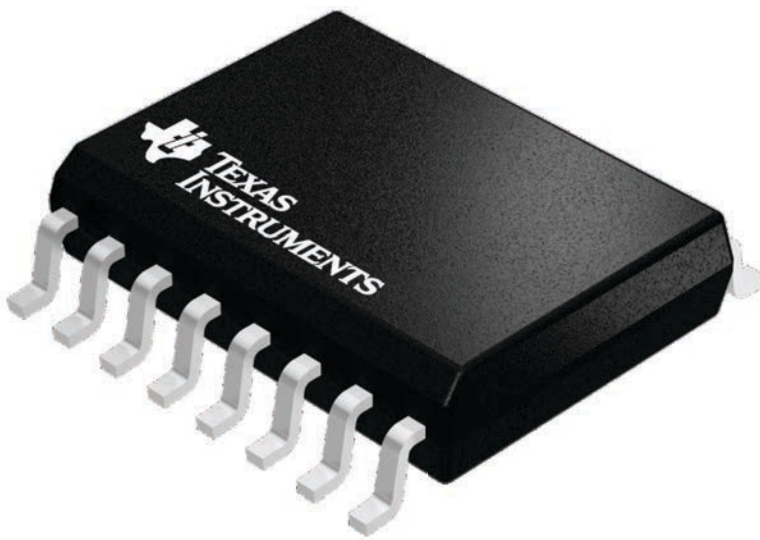
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

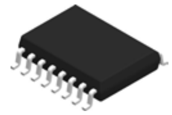
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

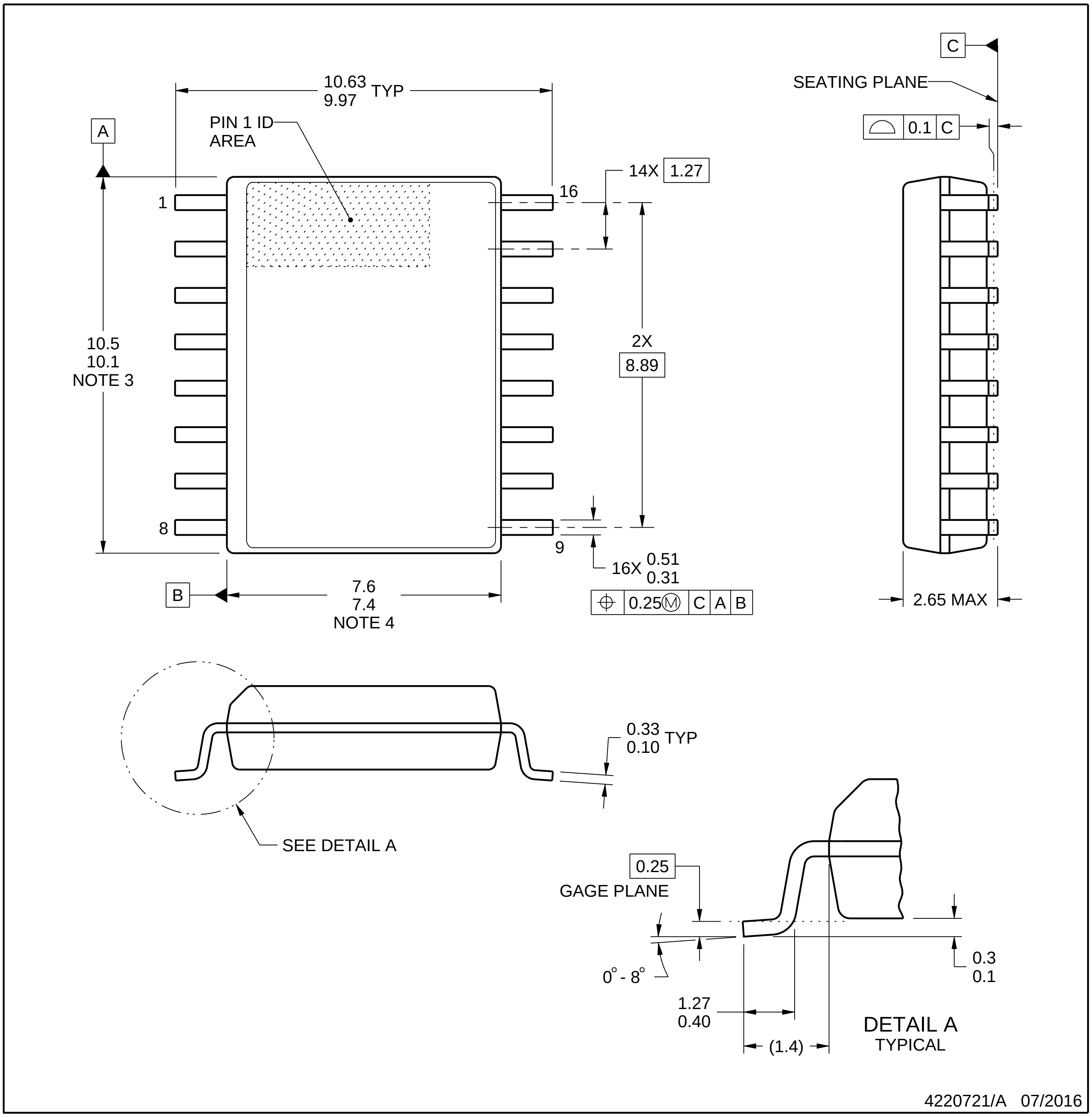


PACKAGE OUTLINE

DW0016A

SOIC - 2.65 mm max height

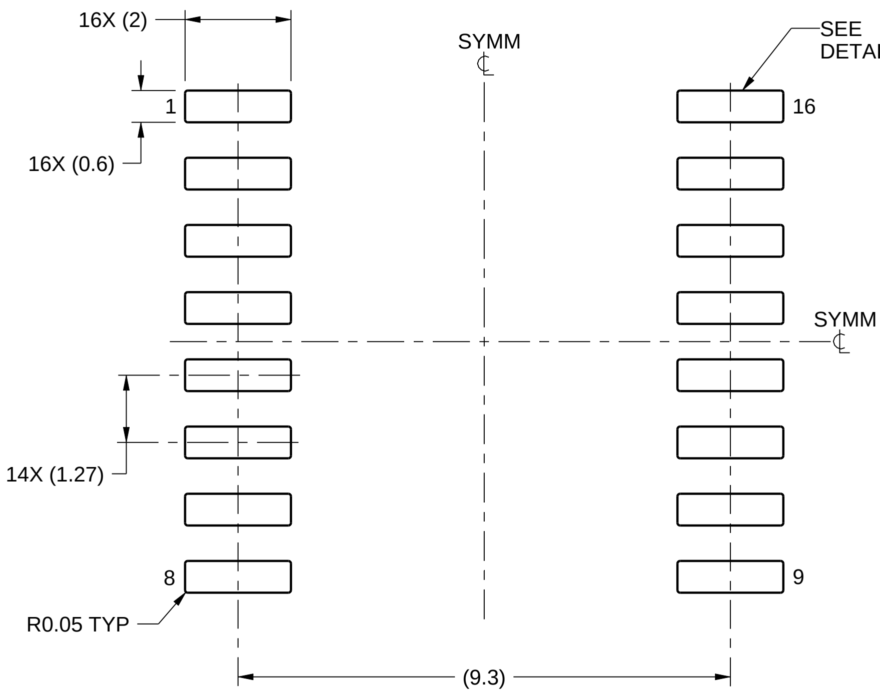
SOIC



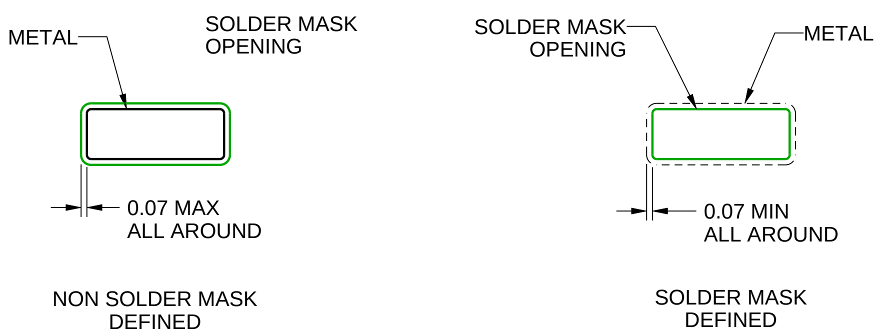
4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

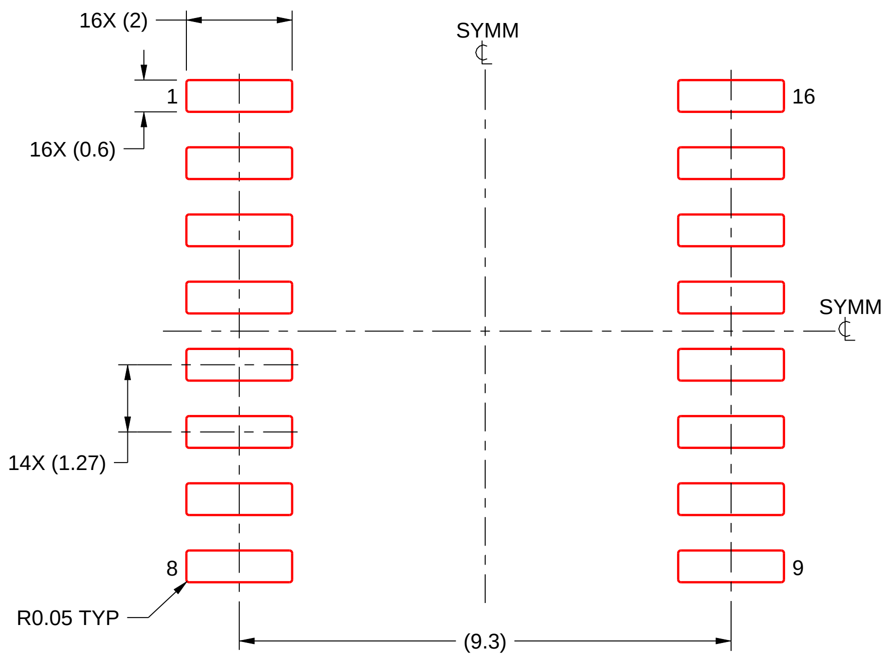


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265