TEXAS INSTRUMENTS

PCM5100A, PCM5101A, PCM5102A
PCM5100A-Q1, PCM5101A-Q1, PCM5102A-Q1
ZHCSA60C – MAY 2012 – REVISED MAY 2015

# PCM510xA具有 PLL 和 32 位、384kHz PCM 接口的 2.1 $V_{RMS}$、112/106/100dB 音频立体声 DAC

## 1 特性

- 超低带外噪声
- 具有 BCK 基准的高性能集成音频锁相环 (PLL)，可在内部生成 SCK
- 直接线路电平 2.1 $V_{RMS}$ 输出
- 无需隔直电容
- 线路电平输出支持低至 1kΩ 的负载
- 智能静音系统：软斜升或斜降搭配模拟静音，实现 120dB 静音信噪比 (SNR)
- 接收 16、24 和 32 位音频数据
- PCM 数据样式：$I^2S$，左对齐
- 当 LRCK 和 BCK 被置为无效时，自动进入省电模式
- 1.8V 或3.3V 故障安全低压 CMOS (LVCMOS) 数字输入
- 采用硬件引脚的简易配置
- 单电源供电：14
  - 3.3V 模拟电源、1.8V 或3.3V 数字电源
- 符合 AEC-Q100 标准

## 2 应用

- A/V 接收器、DVD、BD 播放器
- 汽车信息娱乐系统和远程信息处理
- HDTV 接收器
- 汽车售后加装放大器

## 3 说明

PCM510xA 器件属于单片 CMOS 集成电路系列，由立体声数模转换器 (DAC) 和采用薄型小外形尺寸 (TSSOP) 封装的附加支持电路组成。PCM510xA 器件使用 TI 最新一代高级分段 DAC 架构产品，可实现出色的动态性能并提升针对时钟抖动的耐受度。

凭借 DirectPath™电荷泵技术，PCM510xA 器件提供 2.1 $V_{RMS}$ 中央接地输出（设计人员无需在输出上连接隔直电容）以及传统意义上与单电源线路驱动器相关的外部静音电路。

集成线路驱动器的每个引脚支持低至 1kΩ 的负载，从而在性能上超过其他所有基于电荷泵的线路驱动器。

器件上集成的 PLL 免除了对于系统时钟（通常称为主时钟）的需要，从而实现一个 3 线制 $I^2C$ 连接并减少了系统电磁干扰 (EMI)。

智能时钟误差与 PowerSense 欠压保护采用双层系统，能够消除喀嗒和噼啪声。

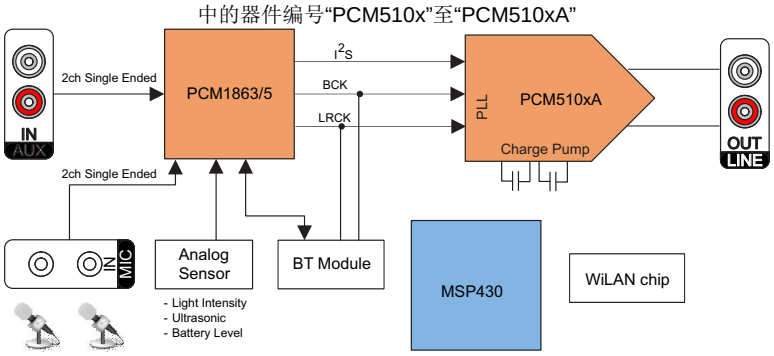
相比许多传统的开关电容 DAC 架构，PCM510xA 系列能够将带外噪声控制在 20dB 的较低水平，从而减少下游放大器/ADC 中的 EMI 和混叠（在 100kHz（OBN 典型值）到 3MHz 之间测得）。

表 1. 器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| PCM5102A | TSSOP (20) | 5.50mm x 4.40mm |
| PCM5101A | | |
| PCM5100A | | |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

## 4 简化系统图

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# 目录



## 5 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision B (January 2015) to Revision C** — **Page**

- 已更改 *简化系统图* ... 1
- Changed typical performance table to reflect part differences accurately ... 4
- Changed "Storage temperatures, $T_{stg}$" to "Operating junction temperature range at –40°C to 130°C" ... 6
- Changed "Storage temperature (Q1 devices) –40°C to 125°C" to "Storage temperatures, $T_{stg}$ –65°C to 150°C" ... 6
- Changed the stereo line output load resistance MIN value in the *Recommended Operating Conditions* from "2 kΩ" to "1 kΩ" ... 6
- Changed the operating junction temperature range in the *Recommended Operating Conditions* from "MIN = –25°C MAX = 85°C" to "MIN = –40°C MAX = 130°C" ... 6
- Added "Q1 Automotive grade devices..." and "Consumer grade (non-Q1) devices..." to the condition statement in the *Electrical Characteristics* ... 7
- Added "Q1 Automotive grade devices..." and "Consumer grade (non-Q1) devices..." to the condition statement in the *Typical Characteristics* graphs section. ... 12
- 已更改 "MCK" to "SCK" at the PLL Clock in the *Functional Block Diagram* ... 14
- Added label "Mute Circuit" and ground symbols to pins DEMP and FMT in Figure 33 ... 26

**Changes from Revision A (September 2012) to Revision B** — **Page**

- 已添加 *ESD 额定值表，详细 说明*部分，*应用和实施*部分，*电源相关建议*部分，*器件和文档支持*部分以及*机械、封装和可订购信息* ... 1
- 已添加 1.8V DVDD 电源项 ... 1
- 已更改 *特性*列表。 ... 1
- Changed "Operating temperature range " to "Operating junction temperature range" ... 6
- Deleted redundant PLL specification in the *Recommended Operating Conditions* ... 6
- 已删除 "Intelligent clock error..." and "...for pop-free performance." ... 14
- Clarified clock generation explanation ... 24


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- Clarified external SCK discussion. ..... 25
- Deleted "The PCM510xA disables the internal PLL when an external SCK is supplied." ..... 25

**Changes from Original (May 2012) to Revision A** **Page**

- 已更改 前两页的编排 ..... 1
- Changed "VOUT = –1 dB" to "THD+N at –1 dBFS" in in the *Dymamic Performance* section of the *Electrical Characteristics* ..... 8
- Changed reference to correct footnote..... 10
- Changed $t_{SCKH}$ and $t_{SCKL}$ values to 9ns..... 11
- Removed 48kHz sample rate with PLL-generated clock..... 25

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# 6 Device Comparison

**Differences Between PCM510xA Devices**

| PART NUMBER | DYNAMIC RANGE | SNR | THD |
|---|---|---|---|
| PCM5102A | 112dB | 112dB | –93 dB |
| PCM5101A | 106 dB | 106 dB | –92 dB |
| PCM5100A | 100 dB | 100 dB | –90 dB |

**Typical Performance (3.3 V Power Supply)**

| PARAMETER | PCM5102 / PCM5101 / PCM5100 |
|---|---|
| SNR | 112 / 106 / 100 dB |
| Dynamic range | 112 /106 / 100 dB |
| THD+N at –1 dBFS | –93/ –92 / –90 dB |
| Full-scale single-ended output | 2.1 $V_{RMS}$ (GND center) |
| Normal 8× oversampling digital filter latency | $20t_S$ |
| Low latency 8× oversampling digital filter latency | $3.5t_S$ |
| Sampling frequency | 8 kHz to 384 kHz |
| System clock multiples ($f_{SCK}$): 64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, 3072 | Up to 50 MHz |


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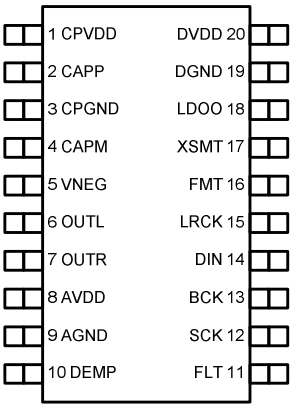
# 7 Pin Configuration and Functions

**PW 20-Pin Package**
**(Top View)**




**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AGND | 9 | — | Analog ground |
| AVDD | 8 | P | Analog power supply, 3.3 V |
| BCK | 13 | I | Audio data bit clock input(1) |
| CAPM | 4 | O | Charge pump flying capacitor terminal for negative rail |
| CAPP | 2 | O | Charge pump flying capacitor terminal for positive rail |
| CPGND | 3 | — | Charge pump ground |
| CPVDD | 1 | P | Charge pump power supply, 3.3 V |
| DEMP | 10 | I | De-emphasis control for 44.1-kHz sampling rate(1): Off (Low) / On (High) |
| DGND | 19 | — | Digital ground |
| DIN | 14 | I | Audio data input(1) |
| DVDD | 20 | P | Digital power supply, 1.8 V or 3.3 V |
| FLT | 11 | I | Filter select : Normal latency (Low) / Low latency (High) |
| FMT | 16 | I | Audio format selection : $I^2S$ (Low) / Left-justified (High) |
| LDOO | 18 | P | Internal logic supply rail terminal for decoupling, or external 1.8 V supply terminal |
| LRCK | 15 | I | Audio data word clock input(1) |
| OUTL | 6 | O | Analog output from DAC left channel |
| OUTR | 7 | O | Analog output from DAC right channel |
| SCK | 12 | I | System clock input(1) |
| VNEG | 5 | O | Negative charge pump rail terminal for decoupling, –3.3 V |
| XSMT | 17 | I | Soft mute control(1): Soft mute (Low) / soft un-mute (High) |

(1) Failsafe LVCMOS Schmitt trigger input

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# 8 Specifications

## 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | AVDD, CPVDD, DVDD | –0.3 | 3.9 | V |
| | LDO with DVDD at 1.8 V | –0.3 | 2.25 | |
| Digital input voltage | DVDD at 1.8 V | –0.3 | 2.25 | |
| | DVDD at 3.3 V | –0.3 | 3.9 | |
| Analog input voltage | | –0.3 | 3.9 | |
| Operating junction temperature range | | –40 | 130 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

## 8.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 8.3 Recommended Operating Conditions

| | | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| AVDD | Analog power supply voltage range | Referenced to AGND[1] | VCOM mode | 3 | 3.3 | 3.46 | V |
| | | | VREF mode | 3.2 | 3.3 | 3.46 | |
| DVDD | Digital power supply voltage range | Referenced to DGND[1] | 1.8 V DVDD | 1.65 | 1.8 | 1.95 | V |
| | | | 3.3 V DVDD | 3.1 | 3.3 | 3.46 | |
| CPVDD | Charge pump supply voltage range | Referenced to CPGND[1] | | 3.1 | 3.3 | 3.46 | V |
| MCLK | Master clock frequency | | | | | 50 | MHz |
| LOL, LOR | Stereo line output load resistance | | | 1 | 10 | | kΩ |
| $C_{LOUT}$ | Digital output load capacitance | | | | 10 | | pF |
| $T_J$ | Operating junction temperature range | | | –40 | | 130 | °C |

(1) All grounds on board are tied together; they must not differ in voltage by more than 0.2 V max, for any combination of ground signals.

## 8.4 Thermal Information

| THERMAL METRIC[1] | | PW | UNIT |
|---|---|---|---|
| | | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 91.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 25.3 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 42 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 41.5 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.


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## 8.5 Electrical Characteristics

Q1 Automotive grade devices are specified for $T_A$ = –40°C to 125°C. Consumer grade (non-Q1) devices are specified at $T_A$ = 25°C. All devices in the family are characterized with AVDD = CPVDD = DVD = 3.3 V, $f_S$ = 48 kHz, system clock = 512 $f_S$ and 24-bit data unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Resolution | | 16 | 24 | 32 | Bits |
| **Data Format (PCM Mode)** | | | | | | |
| | Audio data bit length | | 16 | 24 | 32 | Bits |
| $f_S$ (1) | Sampling frequency | | 8 | | 384 | kHz |
| $f_{SCK}$ | System clock frequency | Clock multiples: 64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, or 3072 | | | 50 | MHz |
| **Digital Input/Output for non-Q1 Consumer Grade Devices** | | | | | | |
| | Logic family: 3.3 V LVCMOS compatible | | | | | |
| $V_{IH}$ | Input logic level | | 0.7×$DV_{DD}$ | | | V |
| $V_{IL}$ | | | | | 0.3×$DV_{DD}$ | |
| $I_{IH}$ | Input logic current | $V_{IN}$ = $V_{DD}$ | | | 10 | µA |
| $I_{IL}$ | | $V_{IN}$ = 0 V | | | –10 | |
| $V_{OH}$ | Output logic level | $I_{OH}$ = –4 mA | 0.8×$DV_{DD}$ | | | V |
| $V_{OL}$ | | $I_{OL}$ = 4 mA | | | 0.22×$DV_{DD}$ | |
| | Logic family 1.8 V LVCMOS compatible | | | | | |
| $V_{IH}$ | Input logic level | | 0.7×$DV_{DD}$ | | | V |
| $V_{IL}$ | | | | | 0.3×$DV_{DD}$ | |
| $I_{IH}$ | Input logic current | $V_{IN}$ = $V_{DD}$ | | | 10 | µA |
| $I_{IL}$ | | $V_{IN}$ = 0 V | | | –10 | |
| $V_{OH}$ | Output logic level | $I_{OH}$ = –2 mA | 0.8×$DV_{DD}$ | | | V |
| $V_{OL}$ | | $I_{OL}$ = 2 mA | | | 0.22×$DV_{DD}$ | |
| **Digital Input/Output for Q1 Automotive Grade Devices** | | | | | | |
| | Logic family: 3.3 V LVCMOS compatible | | | | | |
| $V_{IH}$ | Input logic level | | 0.7×$DV_{DD}$ | | | V |
| $V_{IL}$ | | | | | 0.3×$DV_{DD}$ | |
| $I_{IH}$ | Input logic current | $V_{IN}$ = $V_{DD}$ | | | 10 | µA |
| $I_{IL}$ | | $V_{IN}$ = 0 V | | | –10 | |
| $V_{OH}$ | Output logic level | $I_{OH}$ = –4 mA | 0.8×$DV_{DD}$ | | | V |
| $V_{OL}$ | | $I_{OL}$ = 4 mA | | | 0.22×$DV_{DD}$ | |
| | Logic family 1.8 V LVCMOS compatible | | | | | |
| $V_{IH}$ | Input logic level | | 0.7×$DV_{DD}$ | | | V |
| $V_{IL}$ | | | | | 0.3×$DV_{DD}$ | |
| $I_{IH}$ | Input logic current | $V_{IN}$ = $V_{DD}$ | | | 10 | µA |
| $I_{IL}$ | | $V_{IN}$ = 0 V | | | –10 | |
| $V_{OH}$ | Output logic level | $I_{OH}$ = –2 mA | 0.8×$DV_{DD}$ | | | V |
| $V_{OL}$ | | $I_{OL}$ = 2 mA | | | 0.3×$DV_{DD}$ | |

(1) One sample time is defined as the reciprocal of the sampling frequency. $1t_S = 1/f_S$

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## Electrical Characteristics (continued)

Q1 Automotive grade devices are specified for $T_A$ = –40°C to 125°C. Consumer grade (non-Q1) devices are specified at $T_A$ = 25°C. All devices in the family are characterized with AVDD = CPVDD = DVD = 3.3 V, $f_S$ = 48 kHz, system clock = 512 $f_S$ and 24-bit data unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Dynamic Performance (PCM Mode)(2)(3)** | | | | | | | |
| | THD+N at –1 dBFS(3) | $f_S$ = 48 kHz | PCM5102A | | –93 | –83 | dB |
| | | | PCM5101A | | –92 | –82 | |
| | | | PCM5100A | | –90 | –80 | |
| | | $f_S$ = 96 kHz and 192 kHz | PCM5102A | | –93 | | |
| | | | PCM5101A | | –92 | | |
| | | | PCM5100A | | –90 | | |
| | Dynamic range(3) | EIAJ, A-weighted, $f_S$ = 48 kHz | PCM5102A | 106 | 112 | | |
| | | | PCM5101A | 100 | 106 | | |
| | | | PCM5100A | 95 | 100 | | |
| | | EIAJ, A-weighted, $f_S$ = 96 kHz and 192 kHz | PCM5102A | | 112 | | |
| | | | PCM5101A | | 106 | | |
| | | | PCM5100A | | 100 | | |
| | Signal-to-noise ratio(3) | EIAJ, A-weighted, $f_S$ = 48 kHz | PCM5102A | | 112 | | |
| | | | PCM5101A | | 106 | | |
| | | | PCM5100A | | 100 | | |
| | | EIAJ, A-weighted, $f_S$ = 96 kHz and 192 kHz | PCM5102A | | 112 | | |
| | | | PCM5101A | | 106 | | |
| | | | PCM5100A | | 100 | | |
| | Signal to noise ratio with analog mute(3)(4) | EIAJ, A-weighted, $f_S$ = 48 kHz | | 113 | 123 | | |
| | | EIAJ, A-weighted, $f_S$ = 96 kHz and 192 kHz | | | 123 | | |
| | Channel separation | $f_S$ = 48 kHz | PCM5102A | 100 | 109 | | |
| | | | PCM5101A | 95 | 103 | | |
| | | | PCM5100A | 90 | 97 | | |
| | | $f_S$ = 96 kHz | PCM5102A | | 109 | | |
| | | | PCM5101A | | 103 | | |
| | | | PCM5100A | | 97 | | |
| | | $f_S$ = 192 kHz | PCM5102A | | 109 | | |
| | | | PCM5101A | | 103 | | |
| | | | PCM5100A | | 97 | | |

(2) Filter condition: THD+N: 20-Hz HPF, 20-kHz AES17 LPF; Dynamic range: 20-Hz HPF, 20-kHz AES17 LPF; A-weighted signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF; A-weighted channel separation: 20-Hz HPF, 20-kHz AES17 LPF. Analog performance specifications are measured using the System Two Cascade™ audio measurement system by Audio Precision™ in the RMS mode.
(3) Output load is 10 kΩ, with 470-Ω output resistor and a 2.2-nF shunt capacitor (see recommended output filter).
(4) Assert XSMT or both L-ch and R-ch PCM data are Bipolar Zero.


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## Electrical Characteristics (continued)

Q1 Automotive grade devices are specified for $T_A$ = –40°C to 125°C. Consumer grade (non-Q1) devices are specified at $T_A$ = 25°C. All devices in the family are characterized with AVDD = CPVDD = DVD = 3.3 V, $f_S$ = 48 kHz, system clock = 512 $f_S$ and 24-bit data unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Analog Output** | | | | | | |
| | Output voltage | | | 2.1 | | $V_{RMS}$ |
| | Gain error | | –6 | ±2 | 6 | % of FSR |
| | Gain error on Q1 Automotive Grade Devices | | –7 | ±2 | 7 | % of FSR |
| | Gain mismatch, channel-to-channel | | –6 | ±2 | 6 | % of FSR |
| | Gain mismatch, channel-to-channel on Q1 Devices | | –6 | ±2 | 6 | % of FSR |
| | PCM5100/1 bipolar zero error | At bipolar zero | –5 | ±1 | 5 | mV |
| | PCM5102 Bipolar zero error | At bipolar zero | –2 | ±1 | 2 | mV |
| | Load impedance | | 1 | | | kΩ |
| **Filter Characteristics–1: Normal** | | | | | | |
| | Pass band | | | | $0.45f_S$ | |
| | Stop band | | $0.55f_S$ | | | |
| | Stop band attenuation | | –60 | | | dB |
| | Pass-band ripple | | | | ±0.02 | dB |
| | Delay time | | | $20t_S$ | | s |
| **Filter Characteristics–2: Low Latency** | | | | | | |
| | Pass band | | | | $0.47f_S$ | |
| | Stop band | | $0.55f_S$ | | | |
| | Stop band attenuation | | –52 | | | dB |
| | Pass-band ripple | | | | ±0.0001 | dB |
| | Delay time | | | $3.5t_S$ | | s |
| **Power Supply Requirements** | | | | | | |
| $DV_{DD}$ | Digital supply voltage | Target $DV_{DD}$ = 1.8 V | 1.65 | 1.8 | 1.95 | VDC |
| $DV_{DD}$ | Digital supply voltage | Target $DV_{DD}$ = 3.3 V | 3 | 3.3 | 3.6 | VDC |
| $AV_{DD}$ | Analog supply voltage | | 3 | 3.3 | 3.6 | VDC |
| $CPV_{DD}$ | Charge-pump supply voltage | | 3 | 3.3 | 3.6 | VDC |
| $I_{DD}$ | $DV_{DD}$ supply current at 1.8 V(5) | $f_S$ = 48 kHz | | 7 | | mA |
| | | $f_S$ = 96 kHz | | 8 | | mA |
| | | $f_S$ = 192 kHz | | 9 | | mA |
| $I_{DD}$ | $DV_{DD}$ supply current at 1.8 V(6) | $f_S$ = 48 kHz | | 7 | | mA |
| | | $f_S$ = 96 kHz | | 8 | | mA |
| | | $f_S$ = 192 kHz | | 9 | | mA |
| $I_{DD}$ | $DV_{DD}$ supply current at 1.8 V(7) | Standby | | 0.3 | | mA |
| $I_{DD}$ | $DV_{DD}$ supply current at 3.3 V(5) | $f_S$ = 48 kHz | | 7 | 12 | mA |
| | | $f_S$ = 96 kHz | | 8 | | mA |
| | | $f_S$ = 192 kHz | | 9 | | mA |
| $I_{DD}$ | $DV_{DD}$ supply current at 3.3 V(6) | $f_S$ = 48 kHz | | 8 | 13 | mA |
| | | $f_S$ = 96 kHz | | 9 | | mA |
| | | $f_S$ = 192 kHz | | 10 | | mA |
| $I_{DD}$ | $DV_{DD}$ supply current at 3.3 V(7) | Standby | | 0.5 | 0.8 | mA |
| $I_{DD}$ | $AV_{DD}$ / $CPV_{DD}$ supply current(5) | $f_S$ = 48 kHz | | 11 | 16 | mA |
| | | $f_S$ = 96 kHz | | 11 | | mA |
| | | $f_S$ = 192 kHz | | 11 | | mA |

(5) Input is Bipolar Zero data.
(6) Input is 1 kHz –1 dBFS data.
(7) Power Down Mode

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## Electrical Characteristics (continued)

Q1 Automotive grade devices are specified for $T_A$ = –40°C to 125°C. Consumer grade (non-Q1) devices are specified at $T_A$ = 25°C. All devices in the family are characterized with AVDD = CPVDD = DVD = 3.3 V, $f_S$ = 48 kHz, system clock = 512 $f_S$ and 24-bit data unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{DD}$ | $AV_{DD}$ / $CPV_{DD}$ supply current(6) | $f_S$ = 48 kHz | | 22 | 32 | mA |
| | | $f_S$ = 96 kHz | | 22 | | |
| | | $f_S$ = 192 kHz | | 22 | | |
| $I_{DD}$ | $AV_{DD}$ / $CPV_{DD}$ supply current(7) | $f_S$ = n/a | | 0.2 | 0.4 | mA |
| | Power dissipation, $DV_{DD}$ = 1.8 V(5) | $f_S$ = 48 kHz | | 49 | 185 | mW |
| | | $f_S$ = 96 kHz | | 51 | | |
| | | $f_S$ = 192 kHz | | 53 | | |
| | Power dissipation, $DV_{DD}$ = 1.8 V(6) | $f_S$ = 48 kHz | | 85 | 187 | mW |
| | | $f_S$ = 96 kHz | | 87 | | |
| | | $f_S$ = 192 kHz | | 89 | | |
| | Power dissipation, $DV_{DD}$ = 1.8 V(7) | $f_S$ = n/a (Power Down Mode) | | 1 | | mW |
| | Power dissipation, $DV_{DD}$ = 3.3 V(5) | $f_S$ = 48 kHz | | 60 | 92.4 | mW |
| | | $f_S$ = 96 kHz | | 63 | | |
| | | $f_S$ = 192 kHz | | 66 | | |
| | Power dissipation, $DV_{DD}$ = 3.3 V(6) | $f_S$ = 48 kHz | | 99 | 148.5 | mW |
| | | $f_S$ = 96 kHz | | 102 | | |
| | | $f_S$ = 192 kHz | | 106 | | |
| | Power dissipation, $DV_{DD}$ = 3.3 V(7) | $f_S$ = n/a (Power Down Mode) | | 2 | 4 | mW |


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## 8.6 Timing Requirements

Figure 1 shows the timing requirements for the system clock input. For optimal performance, use a clock source with low phase jitter and noise.

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{SCY}$ | System clock pulse cycle time | | 20 | | 1000 | ns |
| $t_{SCKH}$ | System clock pulse width, High | DVDD = 1.8 V | 8 | | | ns |
| | | DVDD = 3.3 V | 9 | | | |
| $t_{SCKL}$ | System clock pulse width, Low | DVDD = 1.8 V | 8 | | | ns |
| | | DVDD = 3.3 V | 9 | | | |

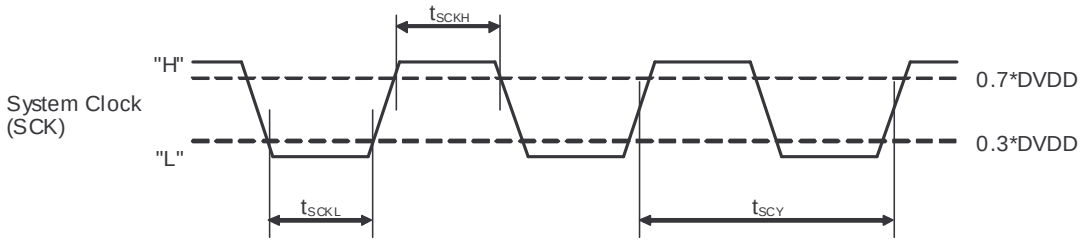


**Figure 1. Timing Requirements for SCK Input**

## 8.7 Timing Requirements, XSMT

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_r$ | Rise time | | | 20 | ns |
| $t_f$ | Fall time | | | 20 | ns |

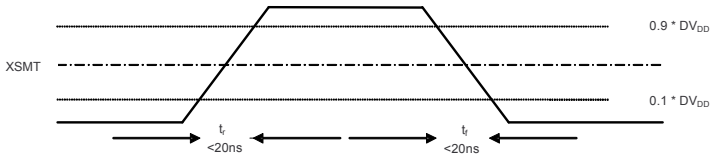


**图 2. XSMT Timing for Soft Mute and Soft Un-Mute**

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## 8.8 Typical Characteristics

Q1 Automotive grade devices are specified for $T_A$ = –40°C to 125°C. Consumer grade (non-Q1) devices are specified at $T_A$ = 25°C, $AV_{DD}$ = $CPV_{DD}$ = $DV_{DD}$ = 3.3 V, $f_S$ = 48 kHz, system clock = 512 $f_S$ and 24-bit data unless otherwise noted.

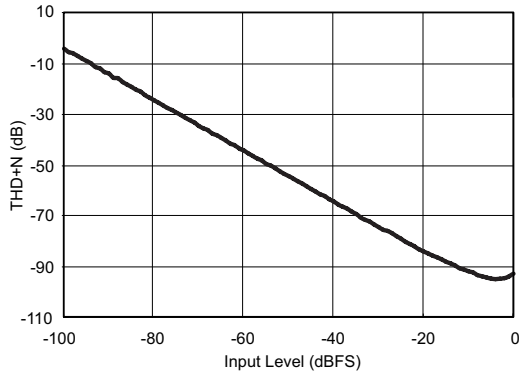


**Figure 3. PCM5101 THD+N versus Input Level**

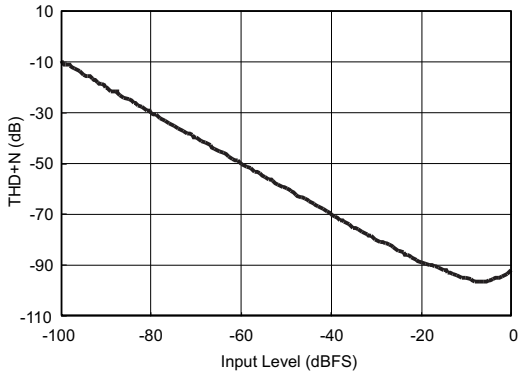


**Figure 4. PCM5102 THD+N versus Input Level**

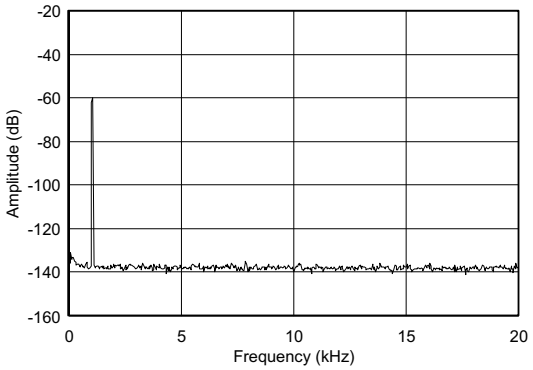


**Figure 5. PCM5101 FFT Plot using a 1-kHz tone (–60dBFS) from DC to 20 kHz**

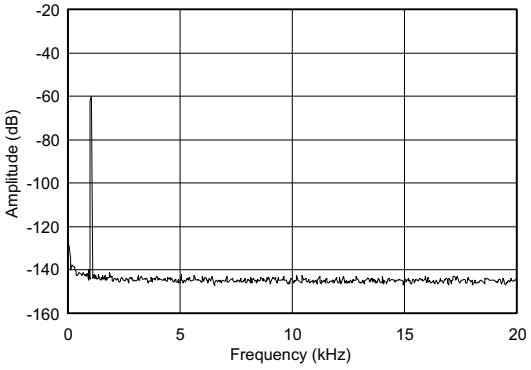


**Figure 6. PCM5102 FFT Plot using a 1-kHz tone (–60dBFS) from DC to 20 kHz**

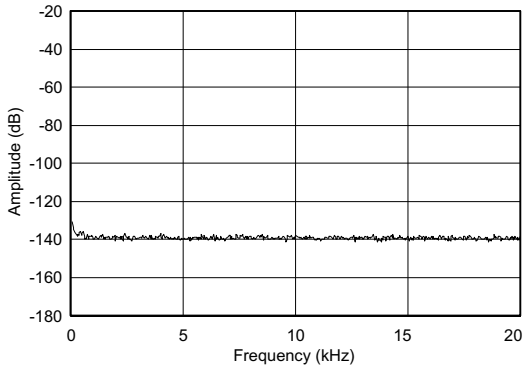


**Figure 7. PCM5101 FFT Plot At Bipolar Zero Data (BPZ)**

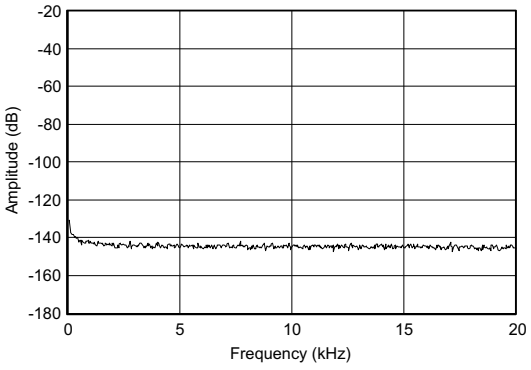


**Figure 8. PCM5102 FFT Plot at BPZ**


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## Typical Characteristics (continued)

Q1 Automotive grade devices are specified for $T_A$ = –40°C to 125°C. Consumer grade (non-Q1) devices are specified at $T_A$ = 25°C, $AV_{DD}$ = $CPV_{DD}$ = $DV_{DD}$ = 3.3 V, $f_S$ = 48 kHz, system clock = 512 $f_S$ and 24-bit data unless otherwise noted.

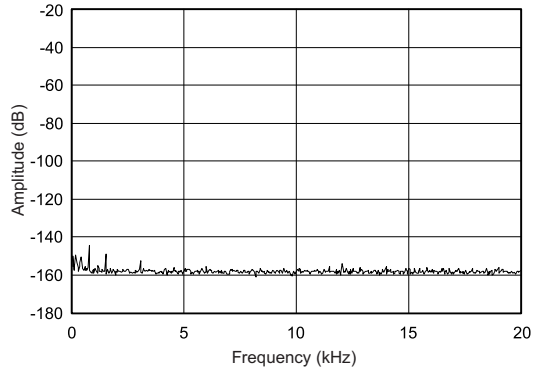



**Figure 9. PCM5101 FFT Plot at BPZ With Analog Mute (AMUTE)**

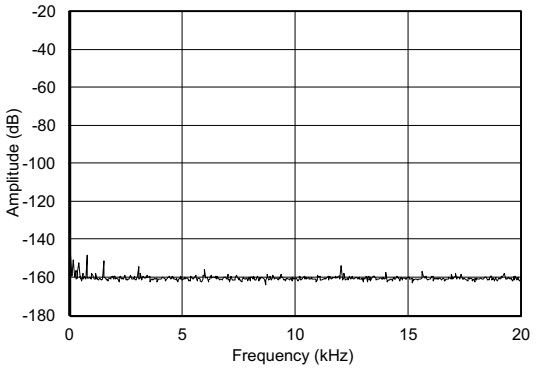



**Figure 10. PCM5102 FFT Plot at BPZ With Analog Mute (AMUTE)**

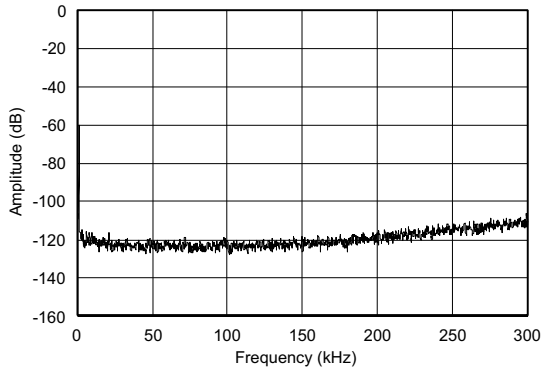



**Figure 11. PCM5101 FFT Plot using a 1-kHz tone (–60dBFS) from DC to 300 kHz**

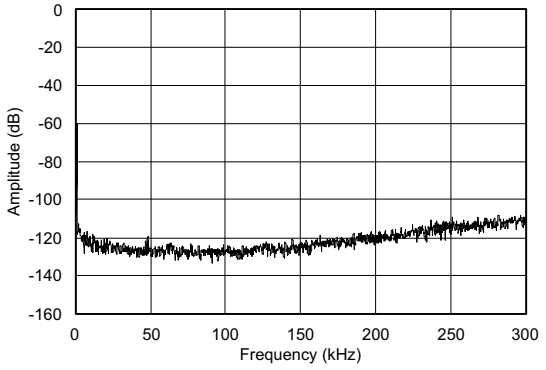



**Figure 12. PCM5102 FFT Plot using a 1-kHz tone (–60dBFS) from DC to 300 kHz**

# 9 Detailed Description

## 9.1 Overview

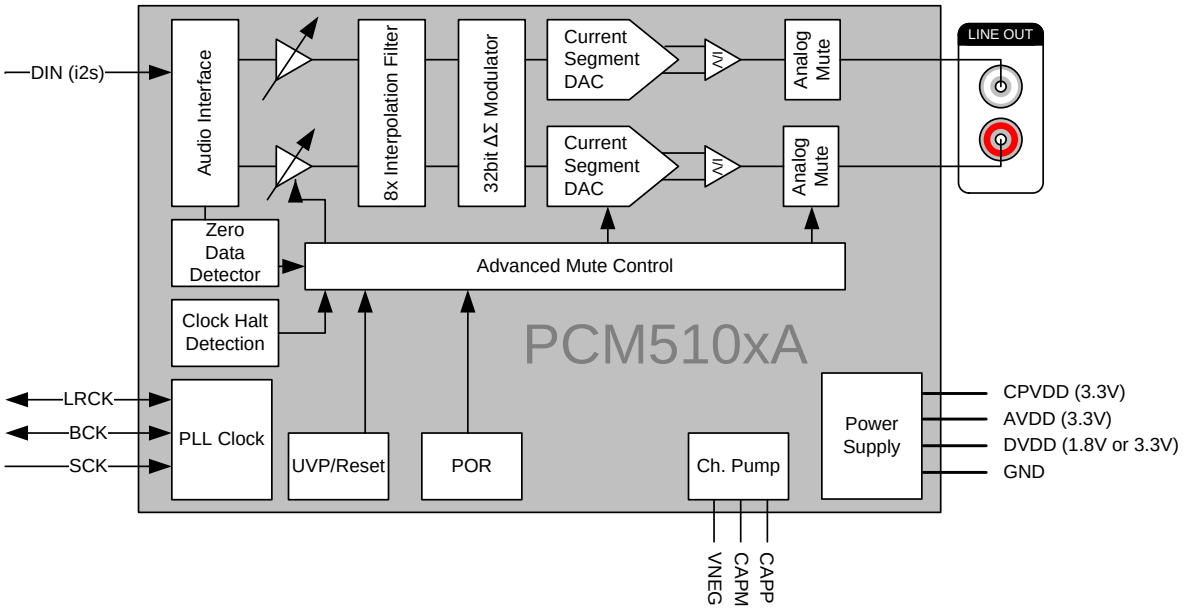
The integrated PLL on the device provided adds the flexibility to remove the system clock (commonly known as master clock), allowing a 3-wire $I^2S$ connection and reducing system EMI.

Powersense undervoltage protection utilizes a two-level mute system. Upon clock error or system power failure, the device digitally attenuates the data (or last known good data) and then mutes the analog circuit.

Compared with existing DAC technology, the PCM510xA devices offer up to 20 dB lower out-of-band noise, reducing EMI and aliasing in downstream amplifiers/ADCs. (from traditional 100-kHz OBN measurements to 3 MHz).

The PCM510xA devices accept industry-standard audio data formats with 16- to 32-bit data. Sample rates up to 384 kHz are supported.

## 9.2 Functional Block Diagram




## 9.3 Feature Description

### 9.3.1 Terminology

Sampling frequency is symbolized by $f_S$. Full scale is symbolized by FS. Sample time as a unit is symbolized by $t_S$.

### 9.3.2 Audio Data Interface

#### *9.3.2.1 Audio Serial Interface*

The audio interface port is a 3-wire serial port with the signals LRCK, BCK, and DIN. BCK is the serial audio bit clock, used to clock the serial data present on DIN into the serial shift register of the audio interface. Serial data is clocked into the PCM510xA on the rising edge of BCK. LRCK is the serial audio left/right word clock. LRCK polarity for left/right is given by the format selected.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## Feature Description (continued)

**Table 2. PCM510xA Audio Data Formats, Bit Depths and Clock Rates**

| CONTROL MODE | FORMAT | DATA BITS | MAX LRCK FREQUENCY [$f_S$] | SCK RATE [x $f_S$] | BCK RATE [x $f_S$] |
|---|---|---|---|---|---|
| Hardware Control | $I^2S$/LJ | 32, 24, 20, 16 | Up to 192 kHz | 128 – 3072 (≤50MHz) | 64, 48, 32 |
| | | | 384 kHz | 64, 128 | 64, 48, 32 |

The PCM510xA requires the synchronization of LRCK and system clock, but does not need a specific phase relation between LRCK and system clock.

If the relationship between LRCK and system clock changes more than ±5 SCK, internal operation (using an onchip oscillator) is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and system clock is completed.

If the relationship between LRCK and BCK are invalid more than 4 LRCK periods, internal operation (using an onchip oscillator) is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and BCK is completed.

### *9.3.2.2 PCM Audio Data Formats*

The PCM510xA supports industry-standard audio data formats, including standard $I^2S$ and left-justified. Data formats are selected using the FMT (pin 16), Low for $I^2S$, and High for Left-justified. All formats require binary twos-complement, MSB-first audio data; up to 32-bit audio data is accepted.

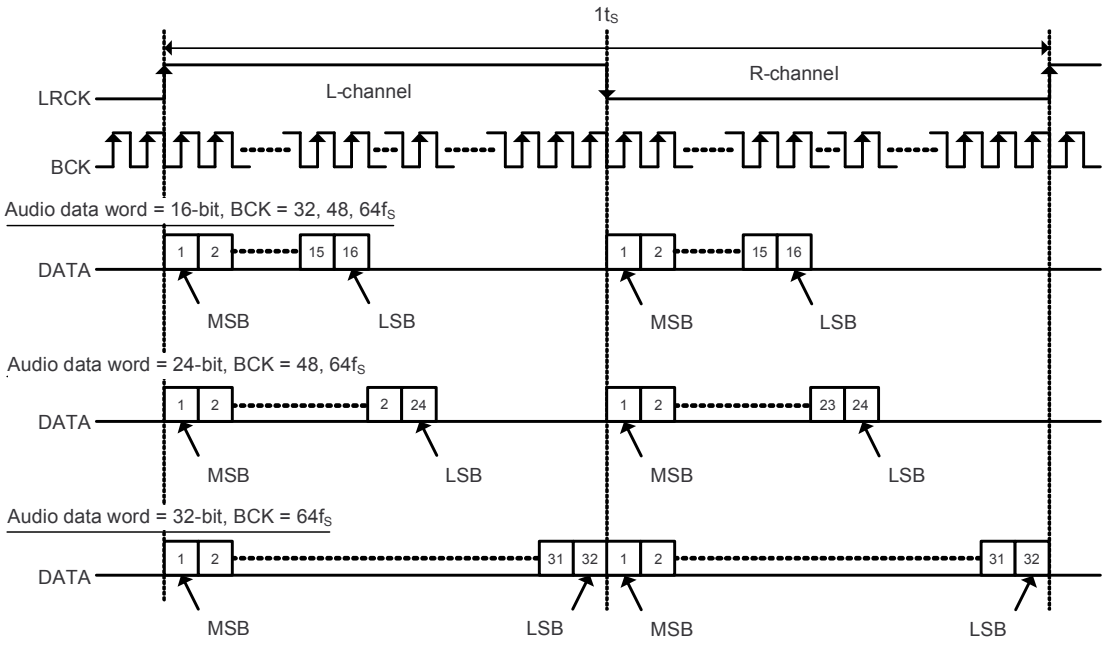
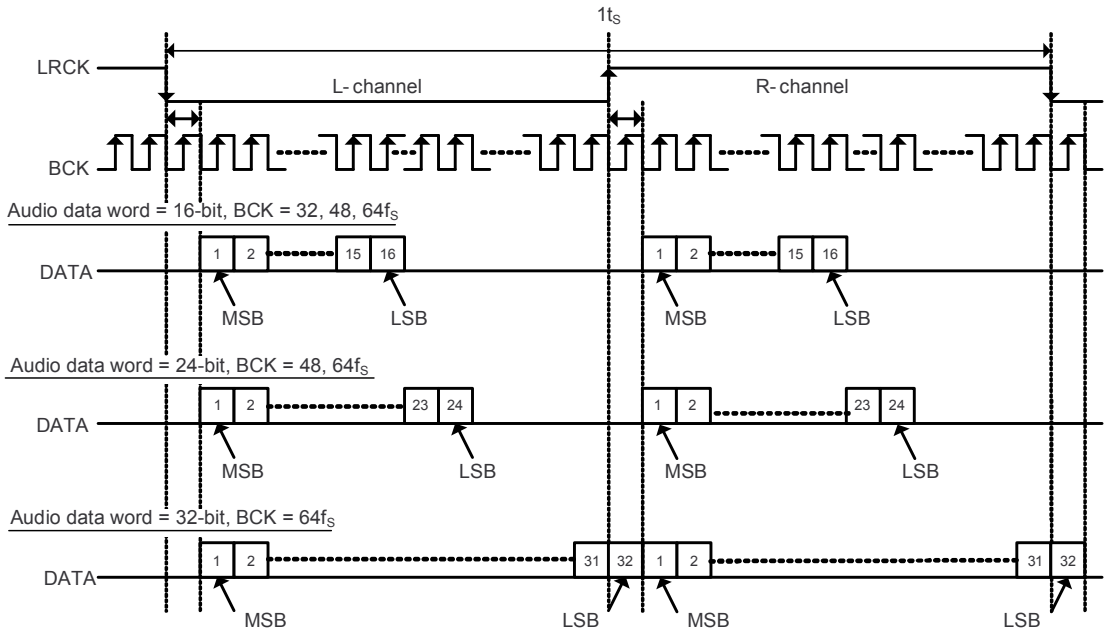



**Figure 13. Left Justified Audio Data Format**




I²S Data Format; L-channel = LOW, R-channel = HIGH

**Figure 14. I²S Audio Data Format**

#### *9.3.2.3 Zero Data Detect*

The PCM510xA has a zero-data detect function. When the device detects continuous zero data, it enters a full analog mute condition. The PCM510xA counts zero data over 1024 LRCKs (21ms @ 48kHz) before setting analog mute.

In Hardware mode, the device uses default values. By default, Both L-ch and R-ch have to be zero data for zero data detection to begin the muting process etc.

### 9.3.3 XSMT Pin (Soft Mute / Soft Un-Mute)

An external digital host controls the PCM510xA soft mute function by driving the XSMT pin with a specific minimum rise time ($t_r$) and fall time ($t_f$) for soft mute and soft un-mute. The PCM510xA requires $t_r$ and $t_f$ times of less than 20ns. In the majority of applications, this is no problem, however, traces with high capacitance may have issues.

When the XSMT pin is shifted from high to low (3.3 V to 0 V), a soft digital attenuation ramp begins. –1-dB attenuation is then applied every sample time from 0 dBFS to –∞. The soft attenuation ramp takes 104 samples.

When the XSMT pin is shifted from low to high (0 V to 3.3 V), a soft digital “un-mute” is started. 1-dB gain steps are applied every sample time from –∞ to 0 dBFS. The un-mute takes 104 samples.

In systems where XSMT is not required, it can be directly connected to AVDD.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### 9.3.4 Audio Processing

#### *9.3.4.1 Interpolation Filter*

The PCM510xA provides two types of interpolation filter. Users can select which filter to use by using the FLT pin (pin 11).

**Table 3. Digital Interpolation Filter Options**

| FLT Pin | Description |
|---|---|
| 0 | FIR normal x8/x4/x2/x1 interpolation filters |
| 1 | IIR low-latency x8/x4/x2/x1 interpolation filters |

The normal x8 / x4 / x2 / x1(bypass) interpolation filter is programmed for sample rates from 8 kHz to 384 kHz.

**Table 4. Normal x8 Interpolation Filter**

| Parameter | Condition | Value (Typ) | Value (Max) | Units |
|---|---|---|---|---|
| Filter gain pass band | 0 ……. $0.45f_S$ | | ±0.02 | dB |
| Filter gain stop band | $0.55f_S$ ….. $7.455f_S$ | –60 | | dB |
| Filter group delay | | $22t_S$ | | s |

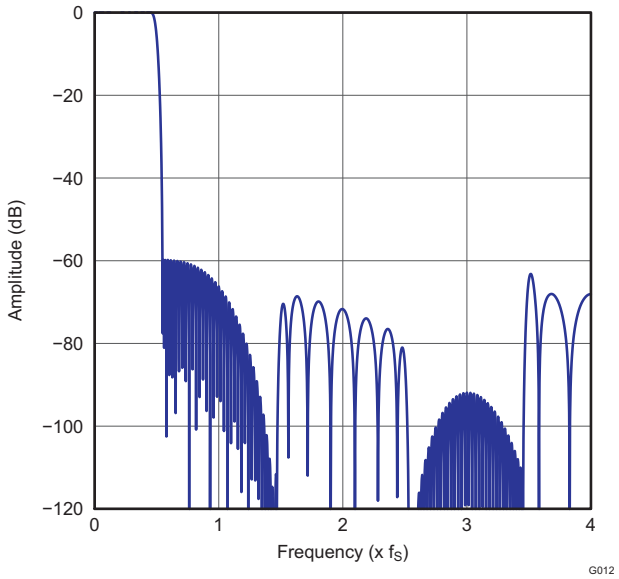


**Figure 15. Normal x8 Interpolation Filter Frequency Response**

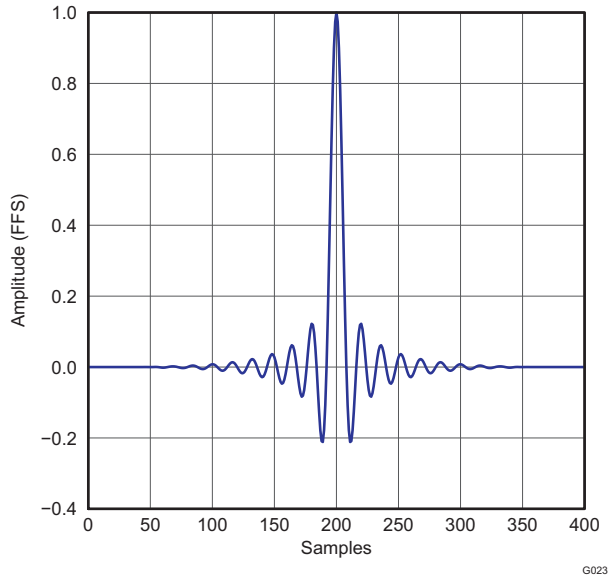


**Figure 16. Normal x8 Interpolation Filter Impulse Response**

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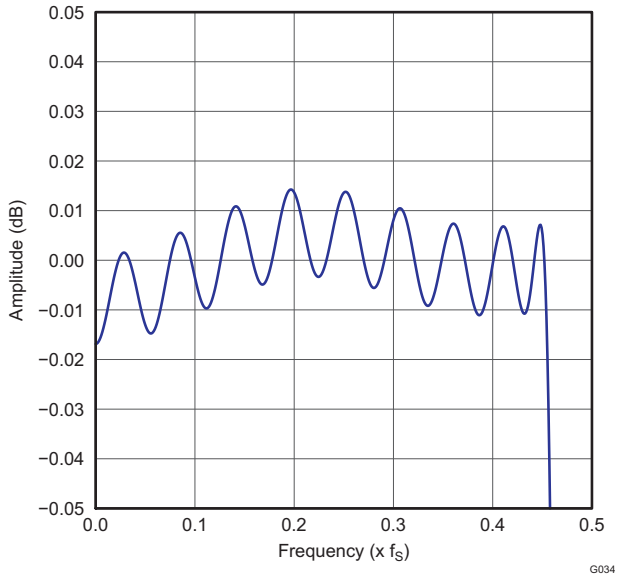


**Figure 17. Normal x8 Interpolation Filter Passband Ripple**


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The normal x4 / x2 / x1 (bypass) interpolation filter is programmed for sample rates from 8 kHz to 384 kHz.

**Table 5. Normal x4 Interpolation Filter**

| Parameter | Condition | Value (Typ) | Value (Max) | Units |
|---|---|---|---|---|
| Filter gain pass band | 0 ……. $0.45f_S$ | | ±0.02 | dB |
| Filter gain stop band | $0.55f_S$ ….. $7.455f_S$ | –60 | | dB |
| Filter group delay | | $22t_S$ | | s |

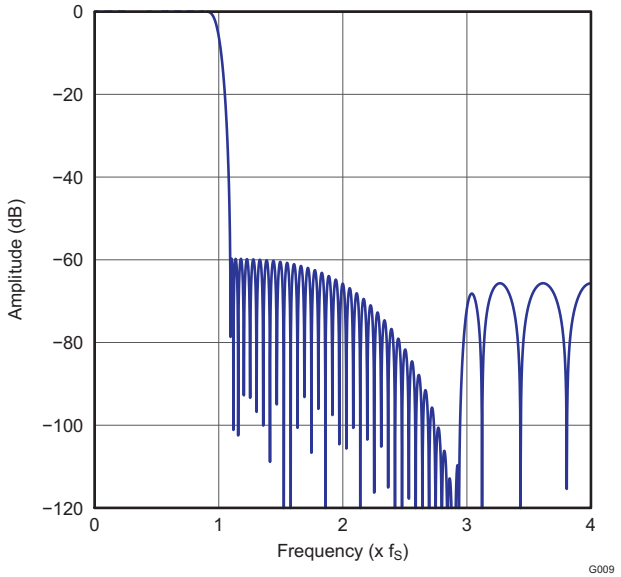


**Figure 18. Normal x4 Interpolation Filter Frequency Response**

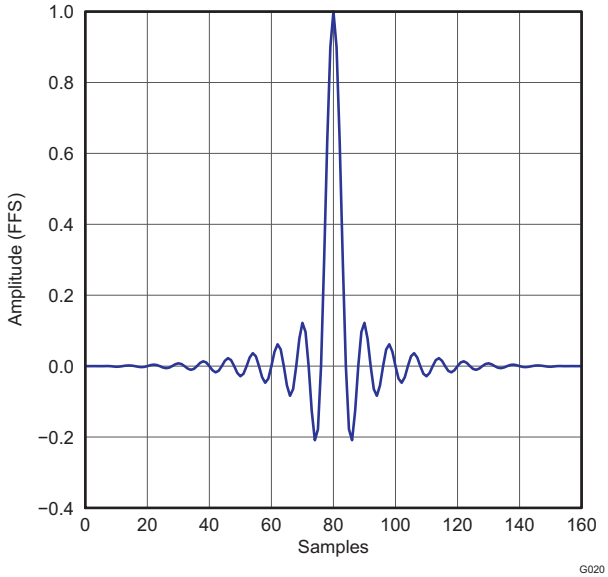


**Figure 19. Normal x4 Interpolation Filter Impulse Response**

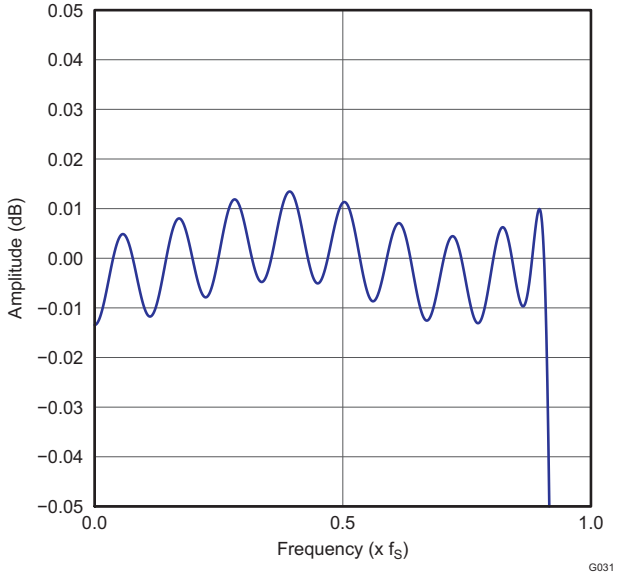


**Figure 20. Normal x4 Interpolation Filter Passband Ripple**

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**Table 6. Normal x2 Interpolation Filter**

| Parameter | Condition | Value (Typ) | Value (Max) | Units |
|---|---|---|---|---|
| Filter gain pass band | 0 ……. $0.45f_S$ | | ±0.02 | dB |
| Filter gain stop band | $0.55f_S$ ….. $7.455f_S$ | –60 | | dB |
| Filter group delay | | $22t_S$ | | s |

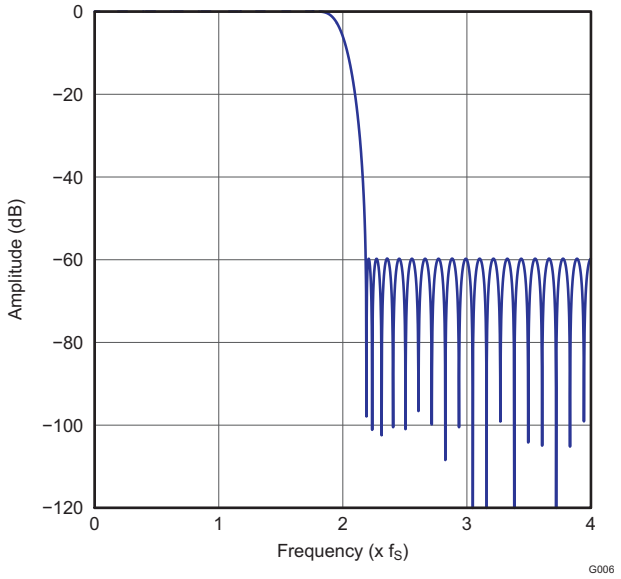


**Figure 21. Normal x2 Interpolation Filter Frequency Response**

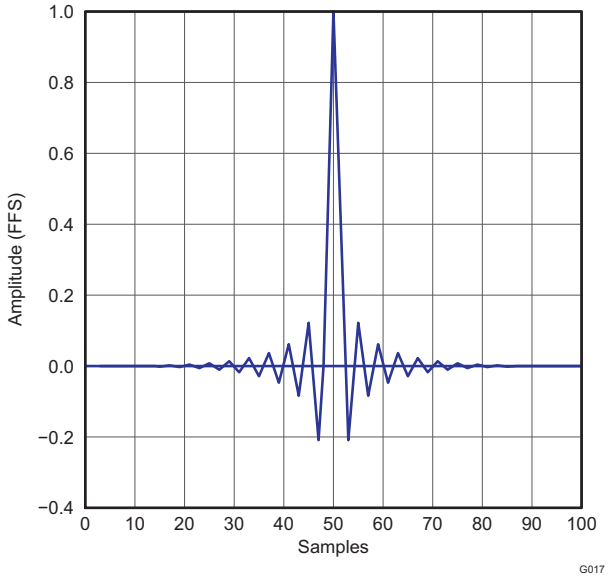


**Figure 22. Normal x2 Interpolation Filter Impulse Response**

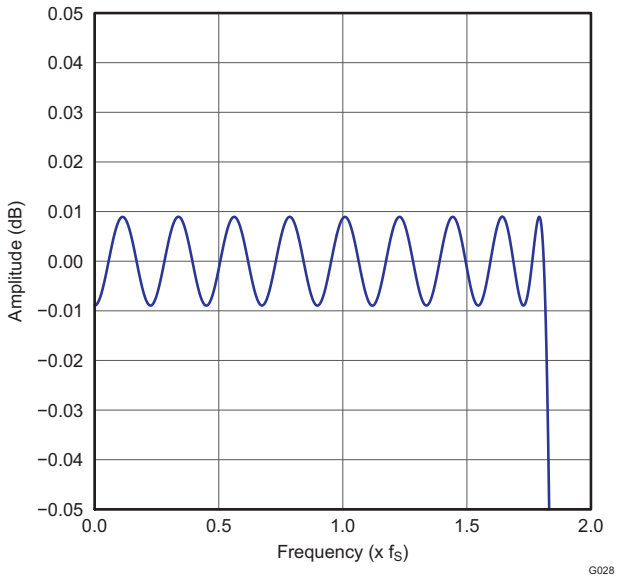


**Figure 23. Normal x2 Interpolation Filter Passband Ripple**


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The low-latency x8 / x4 / x2 / x1 (bypass) interpolation filter is programmed for sample rates from 8 kHz to 384 kHz.

**Table 7. Low Latency x8 Interpolation Filter**

| Parameter | Condition | Value (Typ) | Units |
|---|---|---|---|
| Filter gain pass band | 0 ……. $0.45f_S$ | ±0.0001 | dB |
| Filter gain stop band | $0.55f_S$ ….. $7.455f_S$ | –52 | dB |
| Filter group delay | | $3.5t_S$ | s |

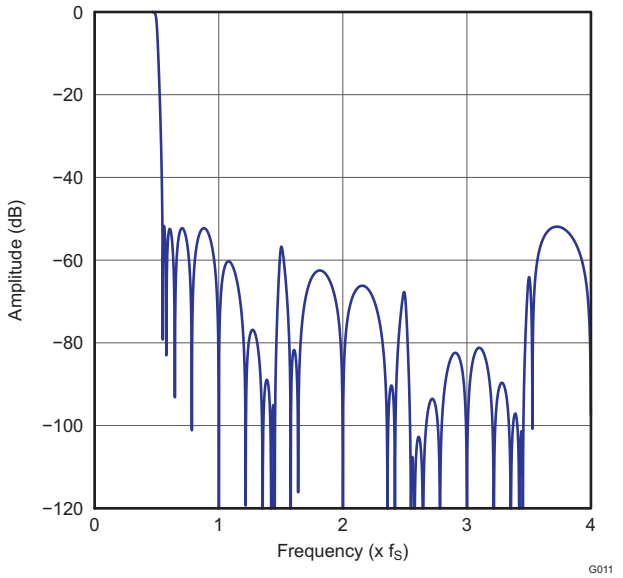


**Figure 24. Low Latency x8 Interpolation Filter Frequency Response**

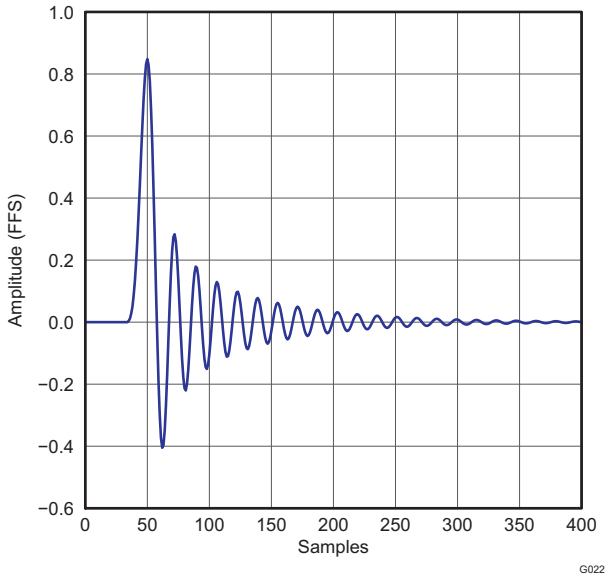


**Figure 25. Low Latency x8 Interpolation Filter Impulse Response**

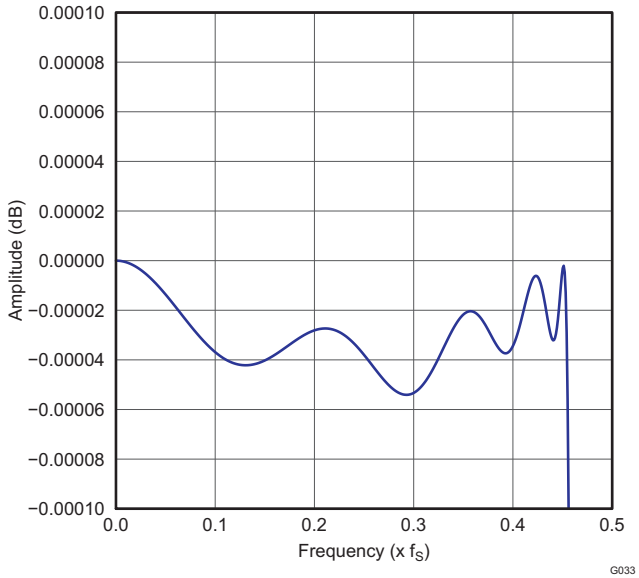


**Figure 26. Low Latency x8 Interpolation Filter Passband Ripple**

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**Table 8. Low Latency x4 Interpolation Filter**

| Parameter | Condition | Value (Typ) | Units |
|---|---|---|---|
| Filter gain pass band | 0 ……. $0.45f_S$ | ±0.0001 | dB |
| Filter gain stop band | $0.55f_S$ ….. $3.455f_S$ | –52 | dB |
| Filter group delay | | $3.5t_S$ | s |

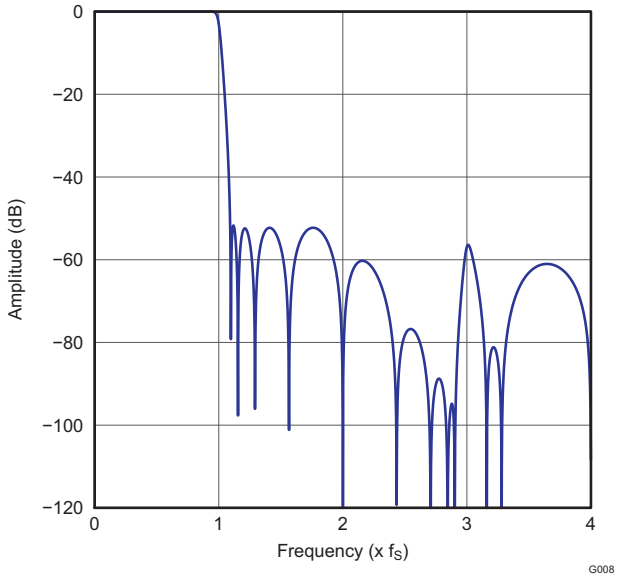


**Figure 27. Low Latency x4 Interpolation Filter Frequency Response**

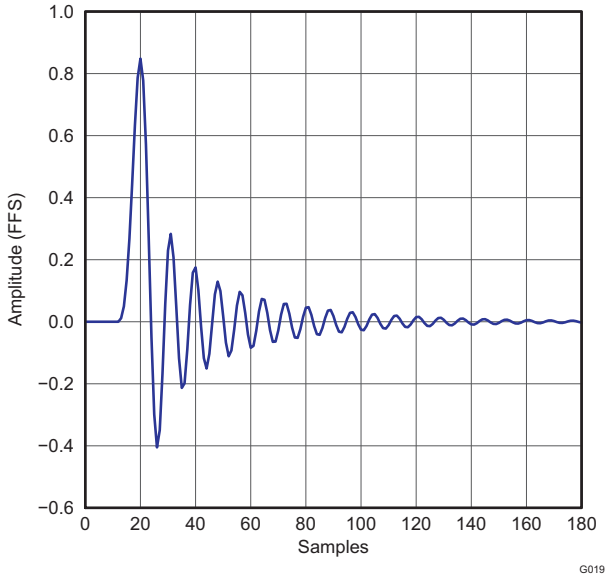


**Figure 28. Low Latency x4 Interpolation Filter Impulse Response**

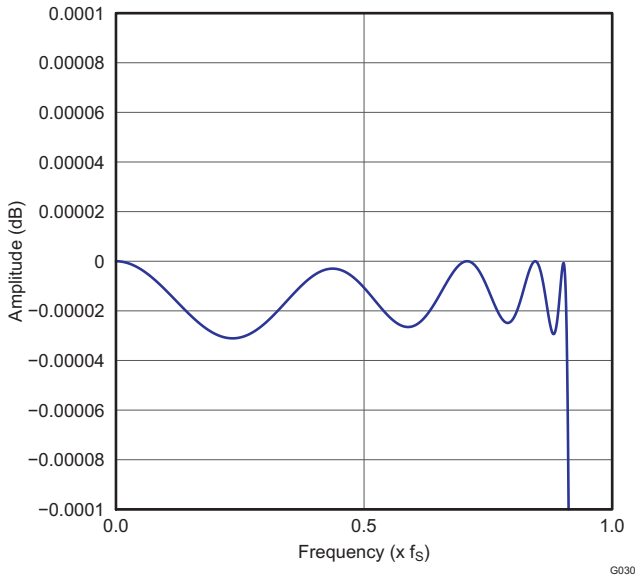


**Figure 29. Low Latency x4 Interpolation Filter Passband Ripple**


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**Table 9. Low Latency x2 Interpolation Filter**

| Parameter | Condition | Value (Typ) | Units |
|---|---|---|---|
| Filter gain pass band | 0 ……. $0.45f_S$ | ±0.0001 | dB |
| Filter gain stop band | $0.55f_S$ ….. $1.455f_S$ | –52 | dB |
| Filter group delay | | $3.5t_S$ | s |

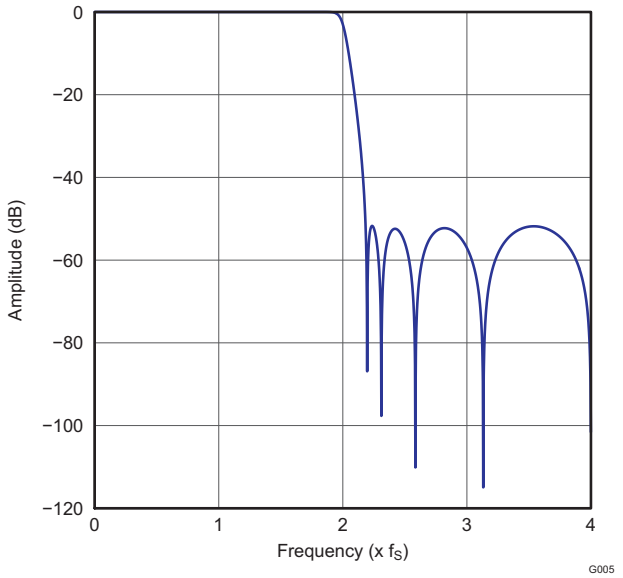


**Figure 30. Low Latency x2 Interpolation Filter Frequency Response**

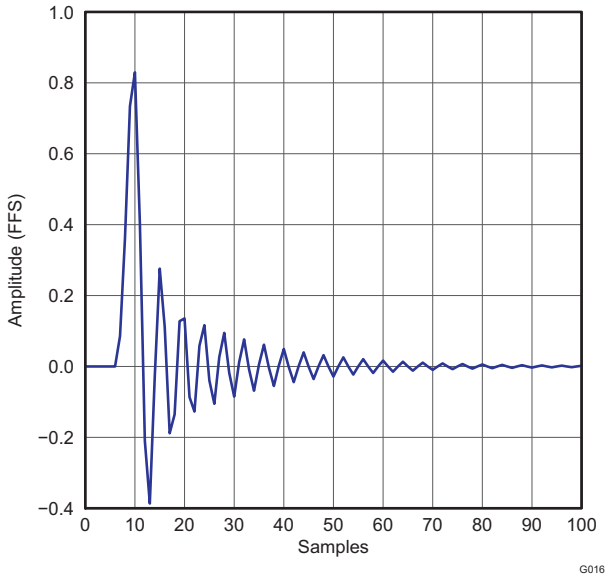


**Figure 31. Low Latency x2 Interpolation Filter Impulse Response**

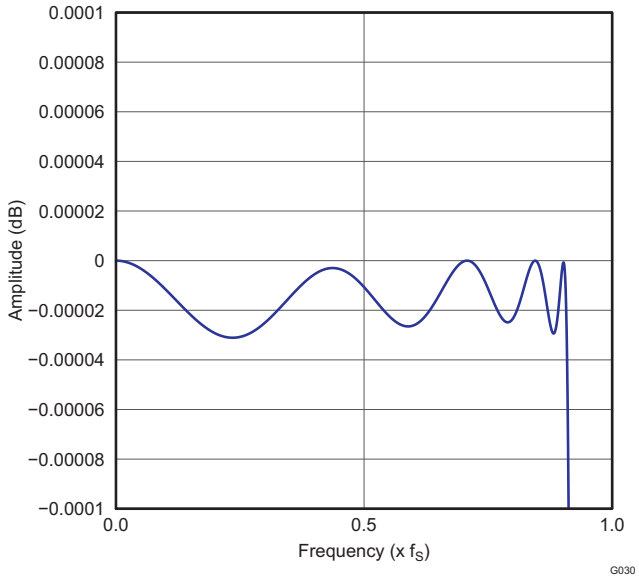


**Figure 32. Low Latency x2 Interpolation Filter Passband Ripple**

### 9.3.5 Reset and System Clock Functions

#### *9.3.5.1 Clocking Overview*

The PCM510xA devices have flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the serial audio interface in one form or another.

The data flows at the sample rate ($f_S$). Once the data is brought into the serial audio interface, it gets processed, interpolated and modulated all the way to 128 × $f_S$ before arriving at the current segments for the final digital to analog conversion.

The serial audio interface typically has 4 connections SCK (system master clock), BCK (bit clock), LRCK (left right word clock) and DIN (data). The device has an internal PLL that is used to take either SCK or BCK and create the higher rate clocks required by the interpolating processor and the DAC clock. This allows the device to operate with or without an external SCK.

#### *9.3.5.2 Clock Slave Mode With Master/System Clock (SCK) Input (4 Wire $I^2S$)*

The PCM510xA requires a system clock to operate the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input and supports up to 50 MHz. The PCM510xA system-clock detection circuit automatically senses the system-clock frequency. Common audio sampling frequencies in the bands of 8 kHz, 16 kHz, (32 kHz - 44.1 kHz - 48 kHz), (88.2kHz - 96kHz), (176.4 kHz - 192 kHz), and 384 kHz with ±4% tolerance are supported. Values in the parentheses are grouped when detected, e.g. 88.2kHZ and 96kHz are detected as "double rate," 32kHz, 44.1kHz and 48kHz will be detected as "single rate".

The sampling frequency detector sets the clock for the digital filter, Delta Sigma Modulator (DSM) and the Negative Charge Pump (NCP) automatically. Table 10 shows examples of system clock frequencies for common audio sampling rates.

SCK rates that are not common to standard audio clocks, between 1 MHz and 50 MHz, are only supported in software mode, available only in the PCM512x, PCM514x, and PCM5242 devices, by configuring various PLL and clock-divider registers. This programmability allows the device to become a clock master and drive the host serial port with LRCK and BCK, from a non-audio related clock (for example, using 12 MHz to generate 44.1 kHz [LRCK] and 2.8224 MHz [BCK]).

**Table 10. System Master Clock Inputs for Audio Related Clocks**

| Sampling Frequency | System Clock Frequency ($f_{SCK}$) (MHz) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 64 $f_S$ | 128 $f_S$ | 192 $f_S$ | 256 $f_S$ | 384 $f_S$ | 512 $f_S$ | 768 $f_S$ | 1024 $f_S$ | 1152 $f_S$ | 1536 $f_S$ | 2048 $f_S$ | 3072 $f_S$ |
| 8 kHz | –(1) | 1.024(2) | 1.536(2) | 2.048 | 3.072 | 4.096 | 6.144 | 8.192 | 9.216 | 12.288 | 16.384 | 24.576 |
| 16 kHz | –(1) | 2.048(2) | 3.072(2) | 4.096 | 6.144 | 8.192 | 12.288 | 16.384 | 18.432 | 24.576 | 36.864 | 49.152 |
| 32 kHz | –(1) | 4.096(2) | 6.144(2) | 8.192 | 12.288 | 16.384 | 24.576 | 32.768 | 36.864 | 49.152 | –(1) | –(1) |
| 44.1 kHz | –(1) | 5.6488(2) | 8.4672(2) | 11.2896 | 16.9344 | 22.5792 | 33.8688 | 45.1584 | –(1) | –(1) | –(1) | –(1) |
| 48 kHz | –(1) | 6.144(2) | 9.216(2) | 12.288 | 18.432 | 24.576 | 36.864 | 49.152 | –(1) | –(1) | –(1) | –(1) |
| 88.2 kHz | –(1) | 11.2896(2) | 16.9344 | 22.5792 | 33.8688 | 45.1584 | –(1) | –(1) | –(1) | –(1) | –(1) | –(1) |
| 96 kHz | –(1) | 12.288(2) | 18.432 | 24.576 | 36.864 | 49.152 | –(1) | –(1) | –(1) | –(1) | –(1) | –(1) |
| 176.4 kHz | –(1) | 22.579 | 33.8688 | 45.1584 | –(1) | –(1) | –(1) | –(1) | –(1) | –(1) | –(1) | –(1) |
| 192 kHz | –(1) | 24.576 | 36.864 | 49.152 | –(1) | –(1) | –(1) | –(1) | –(1) | –(1) | –(1) | –(1) |
| 384 kHz | 24.576 | 49.152 | –(1) | –(1) | –(1) | –(1) | –(1) | –(1) | –(1) | –(1) | –(1) | –(1) |

(1) This system clock rate is not supported for the given sampling frequency.
(2) This system clock rate is supported by PLL mode.


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#### 9.3.5.3 Clock Slave Mode with BCK PLL to Generate Internal Clocks (3-Wire PCM)

The system clock PLL mode allows designers to use a simple 3-wire $I^2S$ audio source. The 3-wire source reduces the need for a high frequency SCK, making PCB layout easier, and reduces high frequency electromagnetic interference.

The internal PLL is disabled as soon as an external SCK is supplied.

The device starts up expecting an external SCK input, but if BCK and LRCK start correctly while SCK remains at ground level for 16 successive LRCK periods, then the internal PLL starts, automatically generating an internal SCK from the BCK reference. Specific BCK rates are required to generate an appropriate master clock. Table 11 describes the minimum and maximum BCK per LRCK for the integrated PLL to automatically generate an internal SCK.

**Table 11. BCK Rates (MHz) by LRCK Sample Rate for PCM510xA PLL Operation**

| | BCK ($f_S$) | |
|---|---|---|
| Sample f (kHz) | 32 | 64 |
| 8 | – | – |
| 16 | – | 1.024 |
| 32 | 1.024 | 2.048 |
| 44.1 | 1.4112 | 2.8224 |
| 48 | 1.536 | 3.072 |
| 96 | 3.072 | 6.144 |
| 192 | 6.144 | 12.288 |
| 384 | 12.288 | 24.576 |

## 9.4 Device Functional Modes

### 9.4.1 External SCK and PLL Activation

As discussed in *Clock Slave Mode with BCK PLL to Generate Internal Clocks (3-Wire PCM)*, the internal PLL of a PCM510xA device supplies a SCK if an external SCK is not present at powerup.

#### 9.4.1.1 Interpolation Filter Modes

Interpolation-filter options are controlled by the FLT pin. See Table 3.

#### 9.4.1.2 44.1kHz De-emphasis

De-emphasis control for 44.1-kHz $f_S$ is controlled by the DEMP pin. See *Pin Configuration and Functions*.

#### 9.4.1.3 Audio Format

Audio format is selected by the FMT pin. See *Pin Configuration and Functions*.

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# 10 Applications and Implementation

**注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

### 10.1.1 Typical Applications

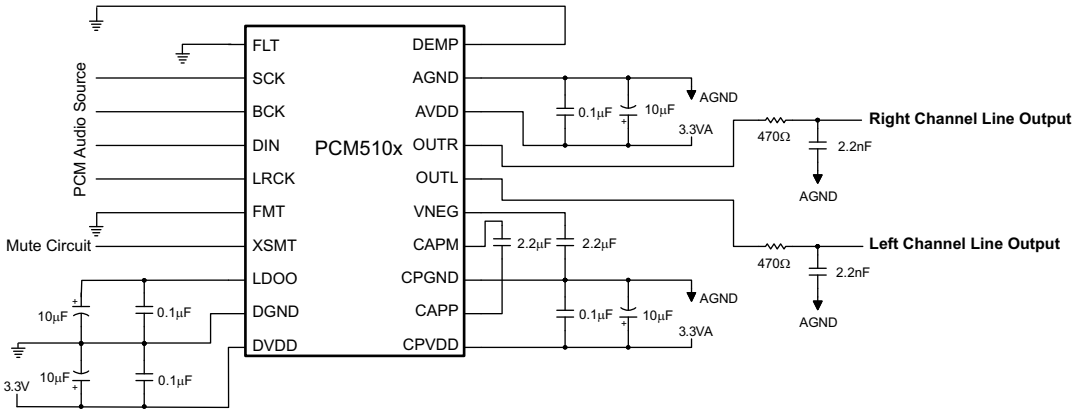


**Figure 33. Simplified Schematic, Hardware-Controlled Subsystem**

#### *10.1.1.1 Example Design Requirements*

- Device control method: hardware control
  - Normal filter latency
  - $I^2S$ digital audio interface
  - Power rail monitoring from the system 12-V rail to mute early on system power loss
- Single-ended 2.1-$V_{RMS}$ analog outputs
- 3-wire $I^2S$ interface (BCK PLL)
- Single 3.3-V supply

#### *10.1.1.2 Detailed Design Procedure*

- Device control method: See *Pin Configuration and Functions* and *Audio Processing*.
  - Normal filter latency: FLT pin tied low
  - Audio format selection: FMT pin tied low
- Clock and PLL setup (See *Reset and System Clock Functions*). Ensure incoming BCK meets minimum requirements.
- XSMT pin setup for 12-V monitoring (See *External Power Sense Undervoltage Protection Mode*).
- Single-supply 3.3-V operation (See *Setting Digital Power Supplies and I/O Voltage Rails*)


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## Application Information (接下页)

### *10.1.1.3 Application Curve*

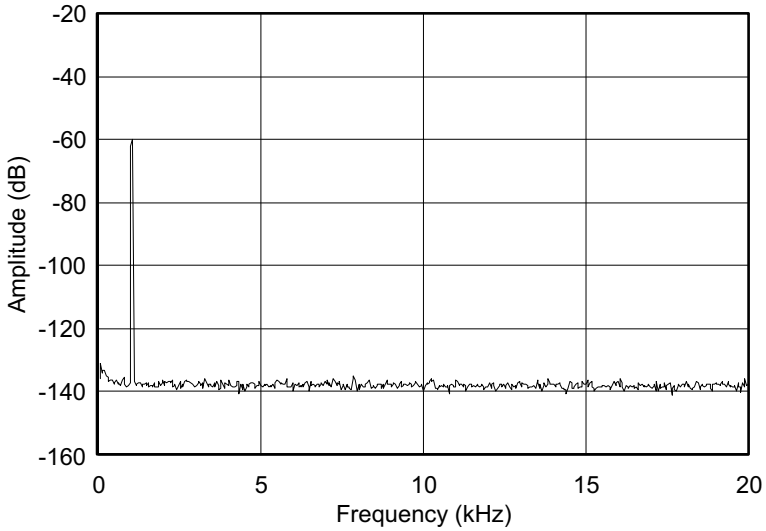


**Figure 34. PCM5101A FFT Plot, DC to 20 kHz with a 1 kHz, –60dBFS Input**

# 11 Power Supply Recommendations

## 11.1 Power Supply Distribution and Requirements

The PCM510xA devices are powered through the following pins:

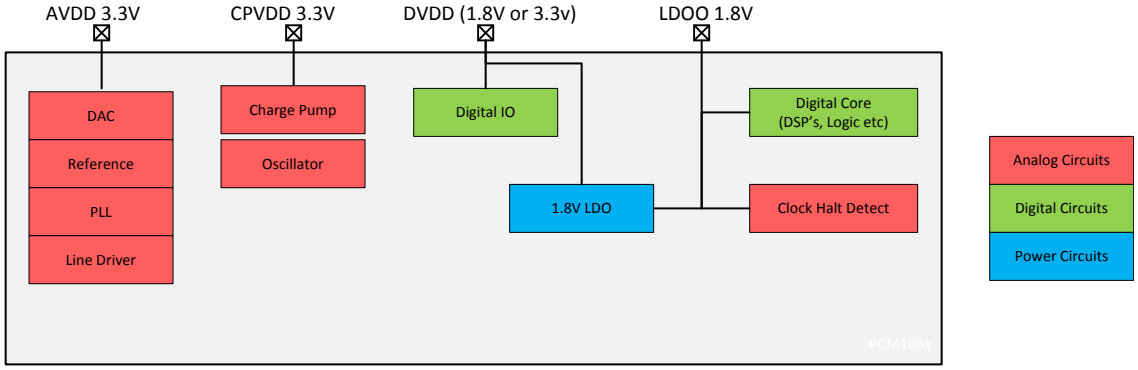


**图 35. Power Distribution Tree within PCM510xA**

**表 12. Power Supply Pin Descriptions**

| NAME | USAGE / DESCRIPTION |
|---|---|
| AVDD | Analog voltage supply; must be 3.3 V. This powers all analog circuitry that the DAC runs on. |
| DVDD | Digital voltage supply. This is used as the I/O voltage control and the input to the onchip LDO. |
| CPVDD | Charge Pump Voltage Supply - must be 3.3 V |
| LDOO | Output from the onchip LDO. Should be used with a 0.1-µF decoupling cap. Can be driven (used as power input) with a 1.8-V supply to bypass the onchip LDO for lower power consumption. |
| AGND | Analog ground |
| DGND | Digital ground |

## 11.2 Recommended Powerdown Sequence

Under certain conditions, the PCM510xA devices can exhibit some pop on power down. Pops are caused by a device not having enough time to detect power loss and start the muting process.

The PCM510xA devices have two auto-mute functions to mute the device upon power loss (intentional or unintentional).

**XSMT = 0**

When the XSMT pin is pulled low, the incoming PCM data is attenuated to 0, closely followed by a hard analog mute. This process takes 150 sample times ($t_s$) + 0.2 ms.

Because this mute time is mainly dominated by the sampling frequency, systems sampling at 192 kHz will mute much faster than a 48-kHz system.

**Clock Error Detect**

When clock error is detected on the incoming data clock, the PCM510xA devices switch to an internal oscillator, and continue to the drive the output, while attenuating the data from the last known value. Once this process is complete, the PCM510xA outputs are hard muted to ground.

### 11.2.1 Planned Shutdown

These auto-muting processes can be manipulated by system designs to mute before power loss in the following ways:

1. Assert XSMT low 150 $t_S$ + 0.2 ms before power is removed.


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## Recommended Powerdown Sequence (continued)

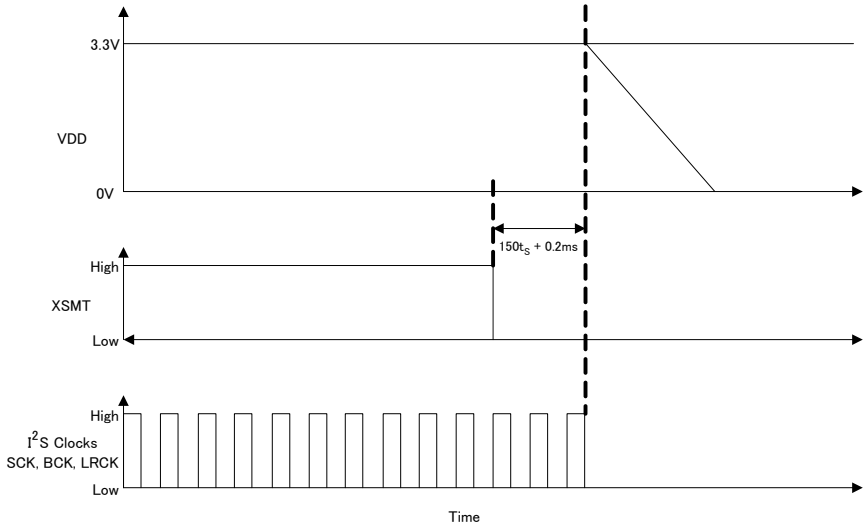


**Figure 36. Assert XSMT**

2. Stop $I^2S$ clocks (SCK, BCK, LRCK) 3 ms before powerdown as shown in Figure 37.

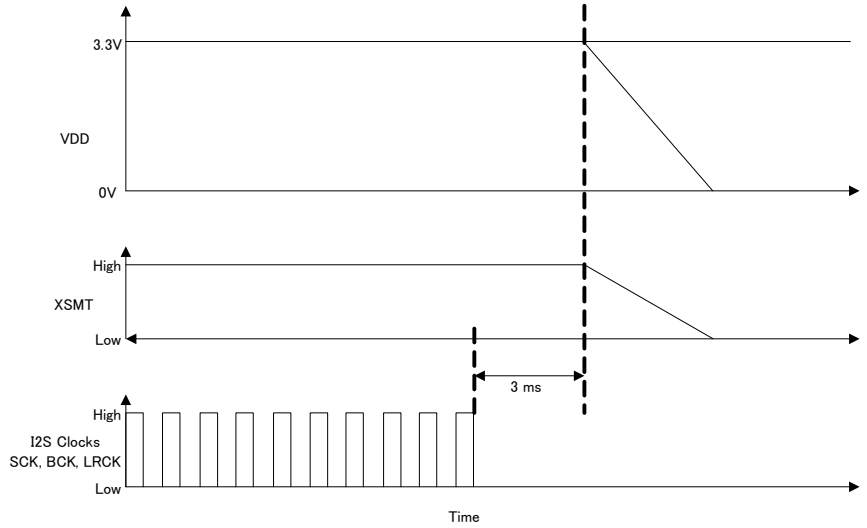


**Figure 37. Stop $I^2C$ Clocks**

### 11.2.2 Unplanned Shutdown

Many systems use a low-noise regulator to provide an AVDD 3.3-V supply for the DAC. The XSMT Pin can take advantage of such a feature to measure the pre-regulated output from the system SMPS to mute the output before the entire SMPS discharges. Figure 38 shows how to configure such a system to use the XSMT pin. The XSMT pin can also be used in parallel with a GPIO pin from the system microcontroller/DSP or power supply.

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## Recommended Powerdown Sequence (continued)

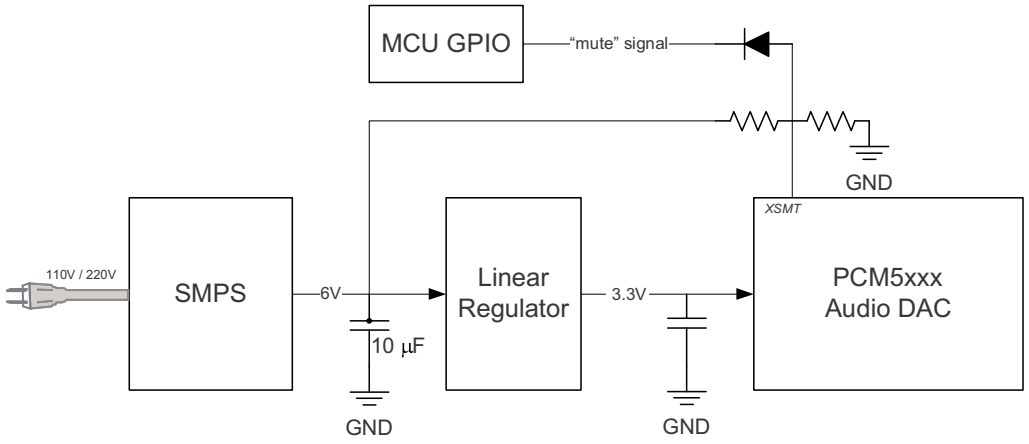


**Figure 38. Using the XSMT Pin**

## 11.3 External Power Sense Undervoltage Protection Mode

**NOTE**

External Power Sense Undervoltage Protection Mode is supported only when DVDD = 3.3 V.

The XSMT pin can also be used to monitor a system voltage, such as the 24-VDC LCD TV backlight, or 12-VDC system supply using a voltage divider created with two resistors. (See Figure 39 )

- If the XSMT pin makes a transition from “1” to “0” over 6 ms or more, the device switches into external under-voltage protection mode. This mode uses two trigger levels:
  - When the XSMT pin level reaches 2 V, soft mute process begins.
  - When the XSMT pin level reaches 1.2 V, analog mute engages, regardless of digital audio level, and analog shutdown begins. (DAC and related circuitry powers down).

If XSMT is moved from "1" to "0" in 20 ns or less, then the device will interpret it as a digital controlled request to mute. It will perform a soft mute, then move to standby.

A timing diagram to show this is shown in Figure 40.

**NOTE**

The XSMT input pin voltage range is from –0.3 V to DVDD+0.3 V. The ratio of external resistors must produce a voltage within this input range. Any increase in power supply (such as power supply positive noise or ripple) can pull the XSMT pin higher than DVDD+0.3 V.

For example, if the PCM510xA is monitoring a 12-V input, and dividing the voltage by 4, then the voltage at XSMT during ideal power supply conditions is 3.3 V. A voltage spike higher than 14.4 V causes a voltage greater than 3.6 V (DVDD+0.3) on the XSMT pin, potentially damaging the device.

Providing the divider is set appropriately, any DC voltage can be monitored.


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## External Power Sense Undervoltage Protection Mode (continued)

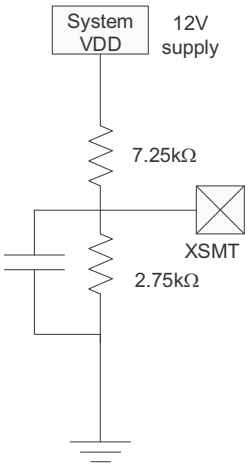


**Figure 39. XSMT in External UVP Mode**

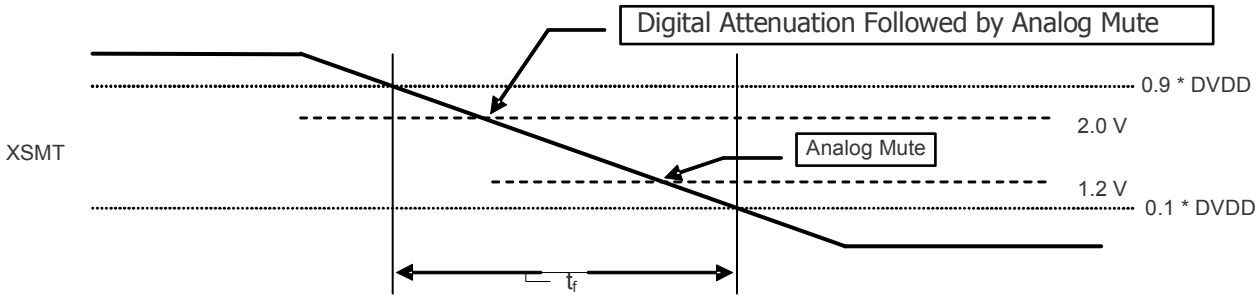


**Figure 40. XSMT Timing for Undervoltage Protection**

The trigger voltage values for the soft mute and hard mute are shown in Table 13. The range of values will vary from device to device, but typical thresholds are shown. XSMT should be set up to nominally be 3.3 V along with DVDD, but derived from a higher system power supply rail.

**Table 13. Distribution of Voltage Thresholds**

| | MIN | TYP | MAX |
|---|---|---|---|
| Soft Mute Threshold Voltage | 2.0 V | 2.2 V | 0.9×DVDD |
| Hard Mute Threshold Voltage | 0.1×DVDD | 0.9 V | 1.2 V |

## 11.4 Power-On Reset Function

### Power-On Reset, DVDD 3.3-V Supply

The PCM510xA includes a power-on reset function shown in Figure 41. With $V_{DD}$ > 2.8 V, the power-on reset function is enabled. After the initialization period, the PCM510xA is set to its default reset state. Analog output will begin ramping after valid data has been passing through the device for the given group delay given by the digital interpolation filter selected.

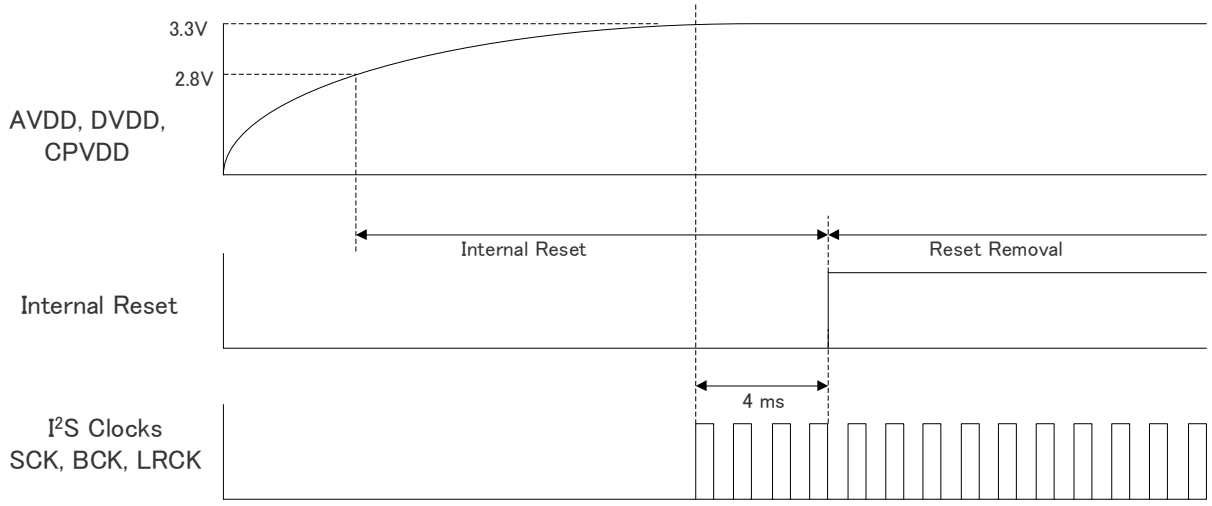


**Figure 41. Power-On Reset Timing, DVDD = 3.3 V**

### Power-On Reset, DVDD 1.8-V Supply

The PCM510xA includes a power-on reset function shown in Figure 42 operating at DVDD = 1.8 V. With AVDD greater than approximately 2.8 V, CPVDD greater than approximately 2.8 V, and DVDD greater than approximately 1.5 V, the power-on reset function is enabled. After the initialization period, the PCM510xA is set to its default reset state.

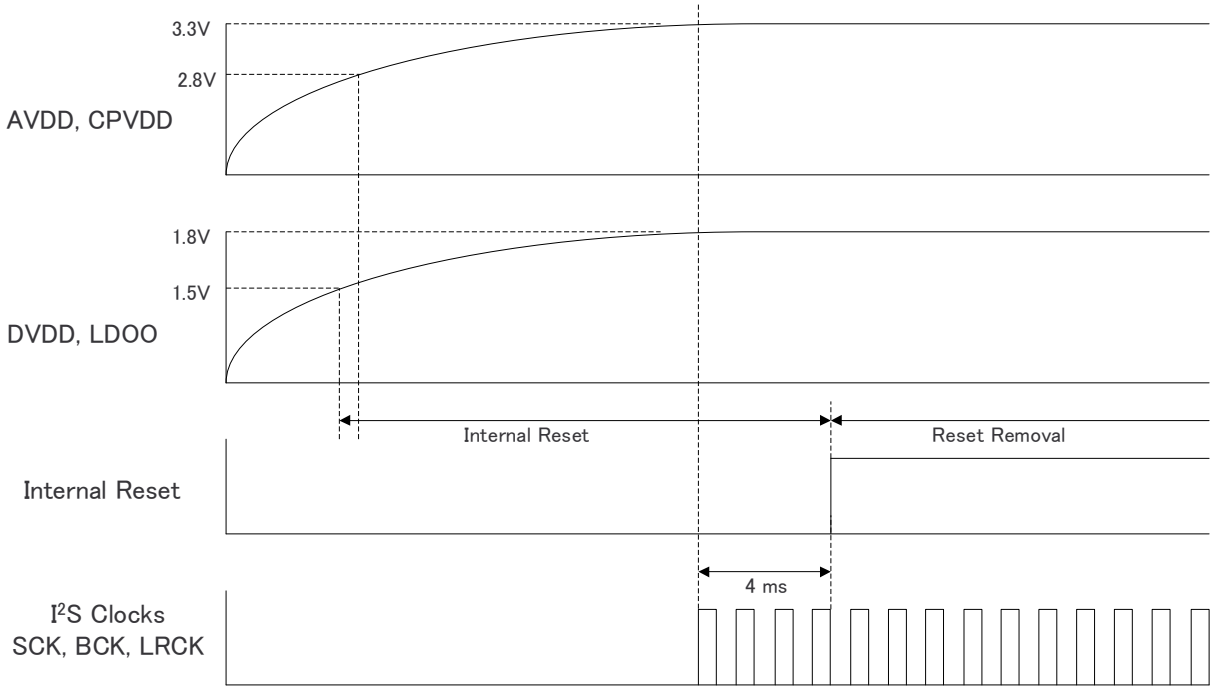


**Figure 42. Power-On Reset Timing, DVDD = 1.8 V**


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## 11.5 PCM510xA Power Modes

### 11.5.1 Setting Digital Power Supplies and I/O Voltage Rails

The internal digital core of the PCM510xA devices run from a 1.8-V supply. This can be generated by the internal LDO, or by an external 1.8-V supply.

DVDD is used to set the I/O voltage, and to be used as the input to the onchip LDO that creates the 1.8 V required by the digital core.

For systems that require 3.3 V I/O support, but lower power consumption, DVDD should be connected to 3.3 V and LDOO can be connected to an external 1.8-V source. Doing so will disable the onchip LDO.

When setting I/O voltage to be 1.8 V, both DVDD and LDOO must be provided with an external 1.8-V supply.

### 11.5.2 Power Save Modes

The PCM510xA devices offer two power-save modes: standby and power-down.

When a clock error (SCK, BCK, and LRCK) or clock halt is detected, the PCM510xA device automatically enters standby mode. The DAC and line driver are also powered down.

When BCK and LRCK remain at a low level for more than 1 second, the PCM510xA device automatically enters powerdown mode. Power-down mode disables the negative charge pump and bias/reference circuit, in addition to those disabled in standby mode.

When expected audio clocks (SCK, BCK, LRCK) are applied to the PCM510xA device, or if BCK and LRCK start correctly while SCK remains at ground level for 16 successive LRCK periods, the device starts its powerup sequence automatically.

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# 12 Layout

## 12.1 Layout Guidelines

- The PCM510xA family of devices are simple to layout. Most engineers use a shared common ground for an entire device. GND can be consider AGND and DGND connected.
- Good system partitioning should keep digital clock and interface traces away from the analog outputs for highest analog performance. This reduces any high speed clock return currents influencing the analog outputs.
- Power supply and charge pump decoupling capacitors should be placed as close as possible to the device.
- The top layer should be used for routing signals, whilst the bottom layer can be used for GND.

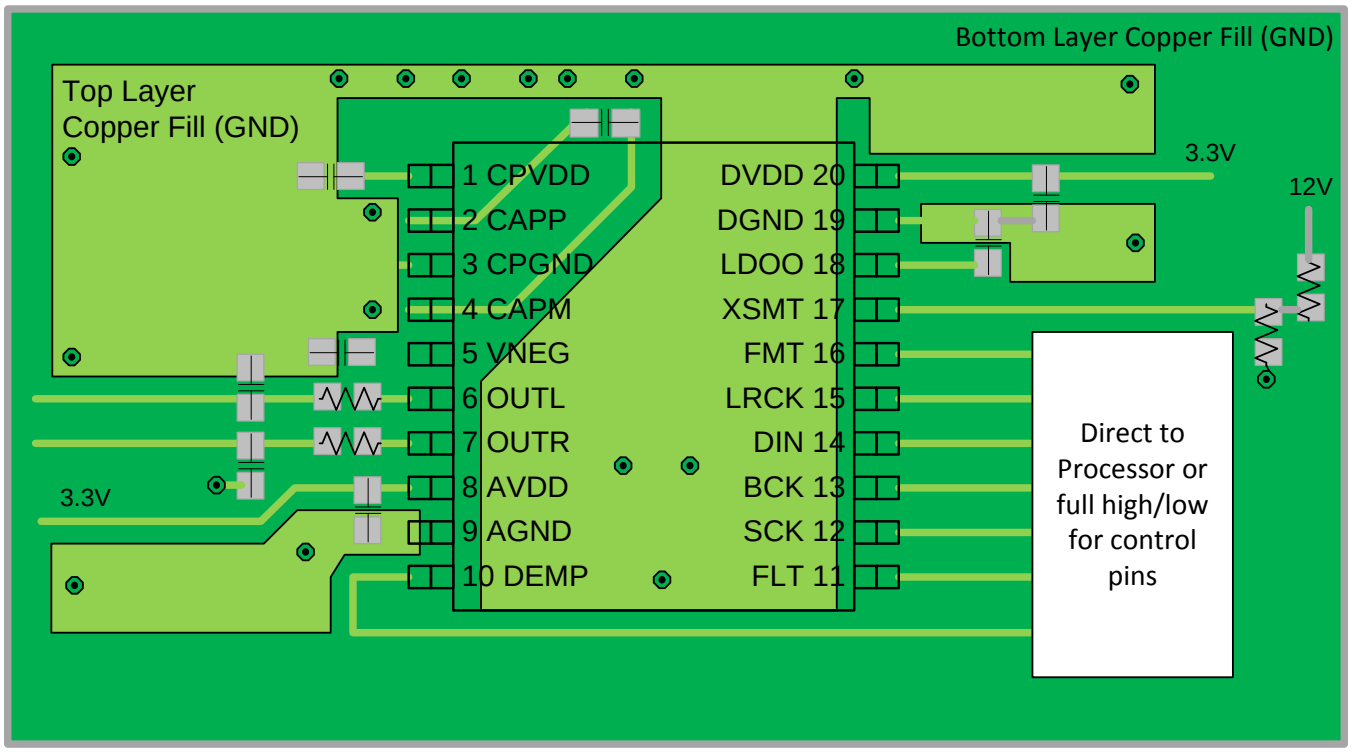


**图 43. PCM510x Layout Example**


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# 13 器件和文档支持

## 13.1 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持和社区资源、工具和软件，以及样片或购买的快速访问。

表 **14.** 相关链接

| 部件 | 产品文件夹 | 样片与购买 | 技术文档 | 工具与软件 | 支持与社区 |
|---|---|---|---|---|---|
| PCM5100A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| PCM5101A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| PCM5102A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| PCM5100A-Q1 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| PCM5101A-Q1 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| PCM5102A-Q1 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |

## 13.2 社区资源

E2E™ 音频转换器论坛 TI

E2E 社区

## 13.3 商标

DirectPath is a trademark of Texas Instruments, Inc.
System Two Cascade, Audio Precision are trademarks of Audio Precision.

## 13.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

# 14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## 14.1 机械数据

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCM5100APW | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -25 to 85 | PCM5100A | Samples |
| PCM5100APWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -25 to 85 | PCM5100A | Samples |
| PCM5100AQPWRQ1 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | P5100AQ1 | Samples |
| PCM5101APW | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -25 to 85 | PCM5101A | Samples |
| PCM5101APWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -25 to 85 | PCM5101A | Samples |
| PCM5101AQPWRQ1 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | P5101AQ1 | Samples |
| PCM5102APW | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -25 to 85 | PCM5102A | Samples |
| PCM5102APWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -25 to 85 | PCM5102A | Samples |
| PCM5102AQPWRQ1 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | P5102AQ1 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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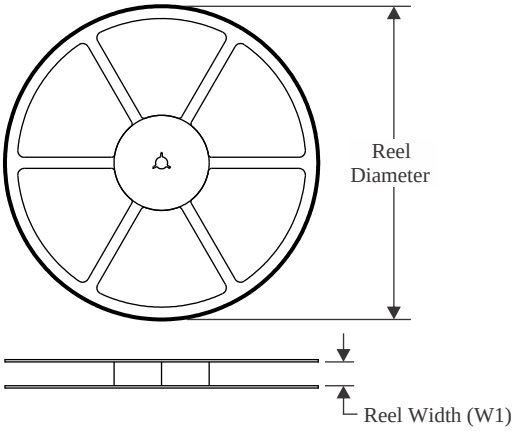
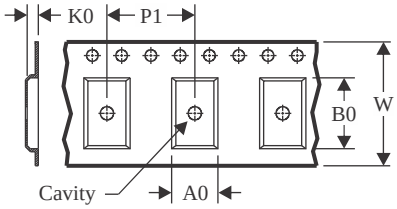
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

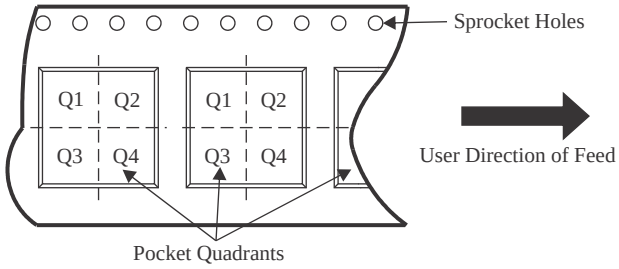



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

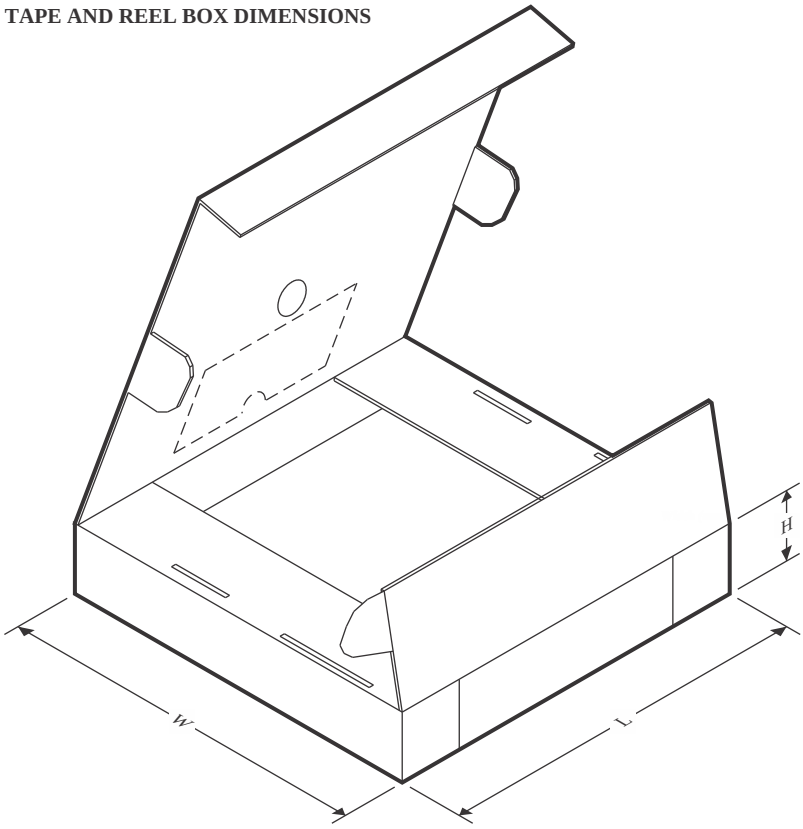
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PCM5100APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| PCM5100AQPWRQ1 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| PCM5101APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| PCM5101AQPWRQ1 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| PCM5102APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| PCM5102AQPWRQ1 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

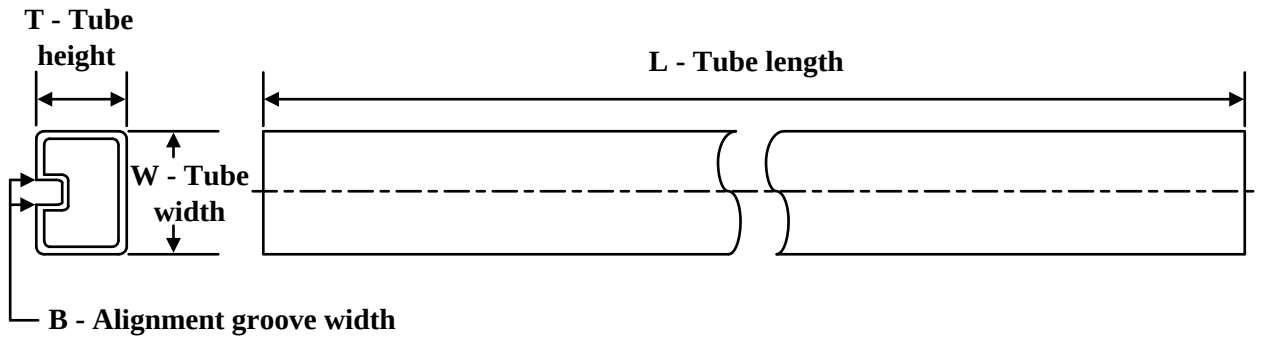
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| PCM5100APWR | TSSOP | PW | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| PCM5100AQPWRQ1 | TSSOP | PW | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| PCM5101APWR | TSSOP | PW | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| PCM5101AQPWRQ1 | TSSOP | PW | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| PCM5102APWR | TSSOP | PW | 20 | 2000 | 350.0 | 350.0 | 43.0 |
| PCM5102AQPWRQ1 | TSSOP | PW | 20 | 2000 | 350.0 | 350.0 | 43.0 |

## TUBE




*All dimensions are nominal

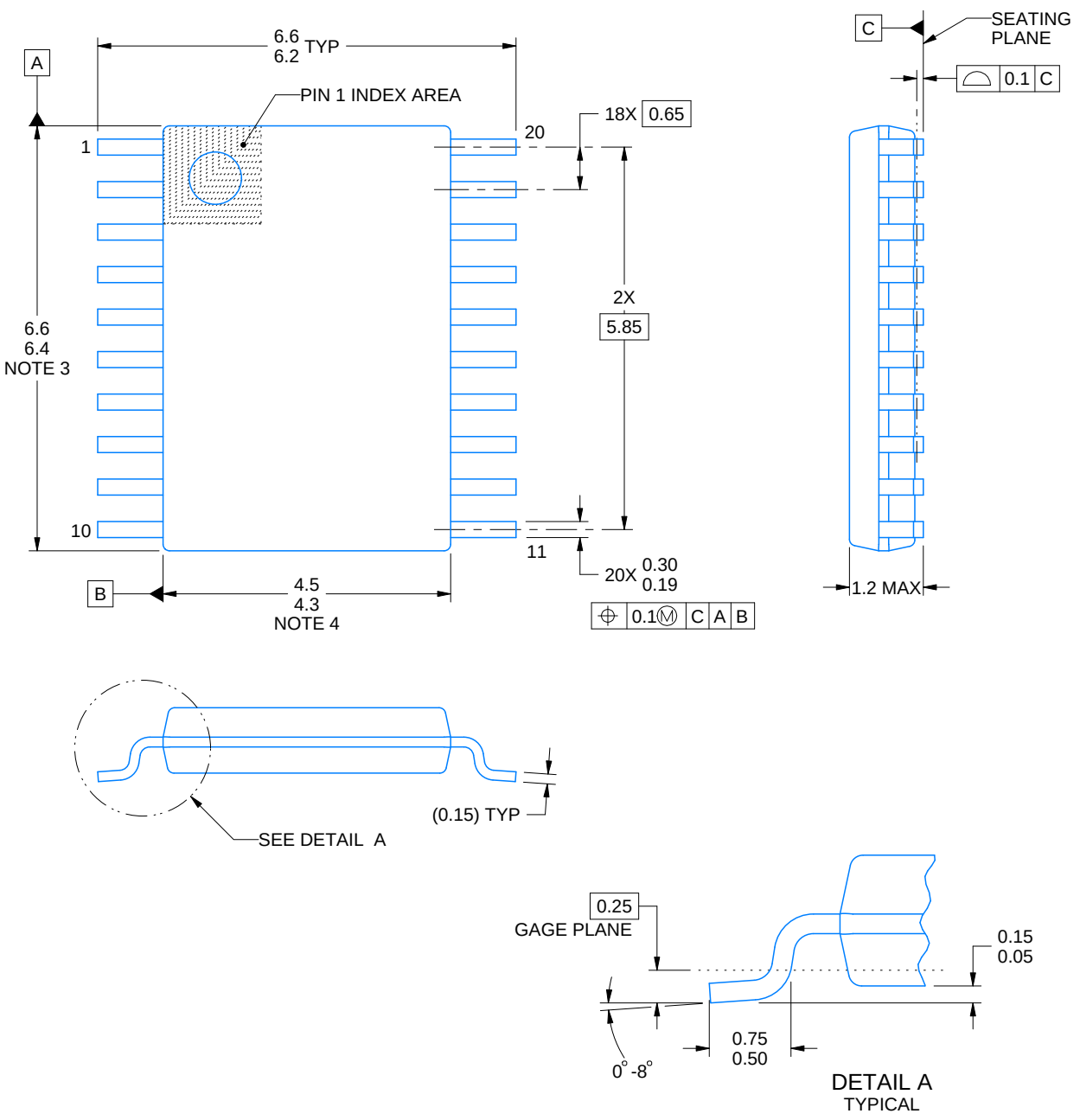
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| PCM5100APW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| PCM5101APW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| PCM5102APW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |

# PACKAGE OUTLINE

## PW0020A

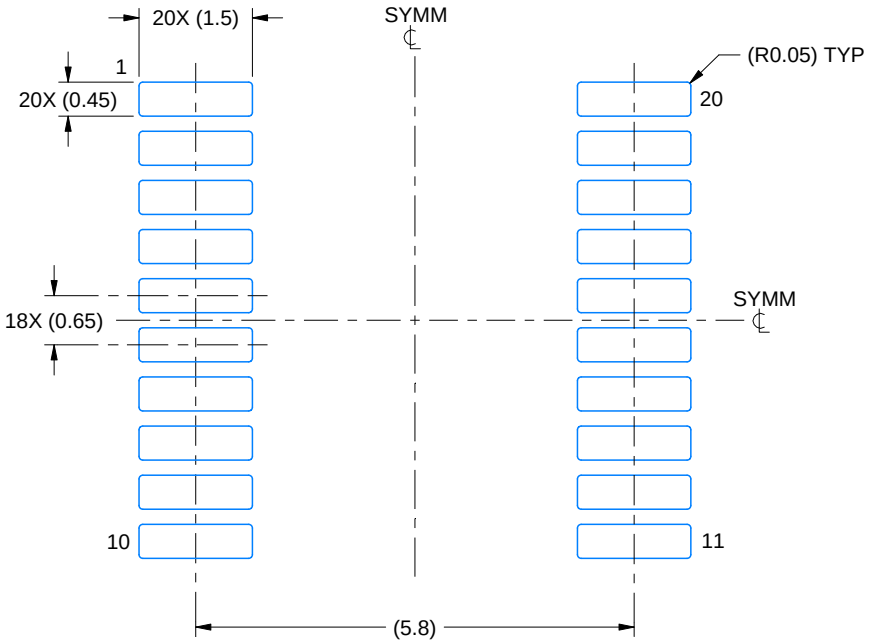
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



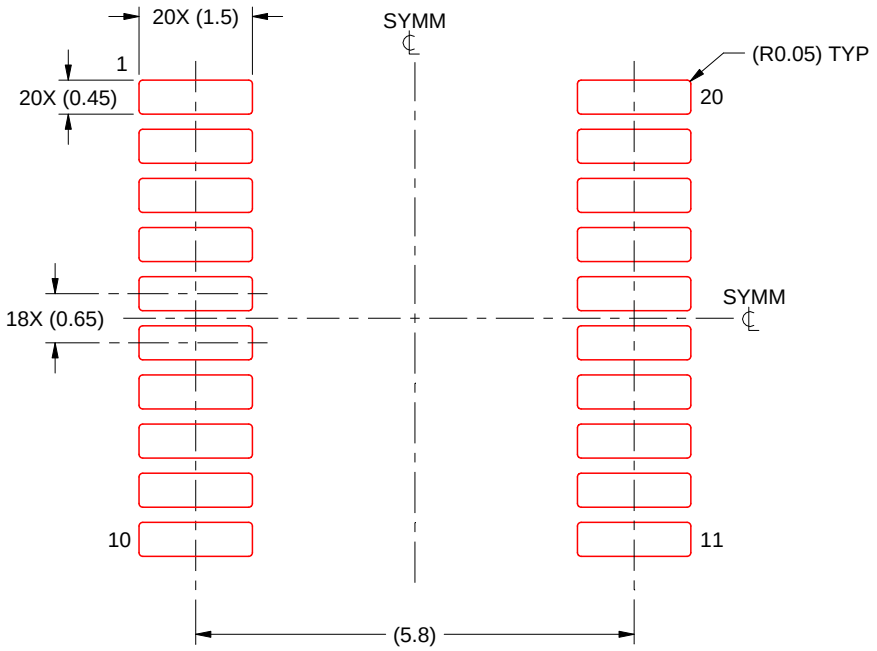

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



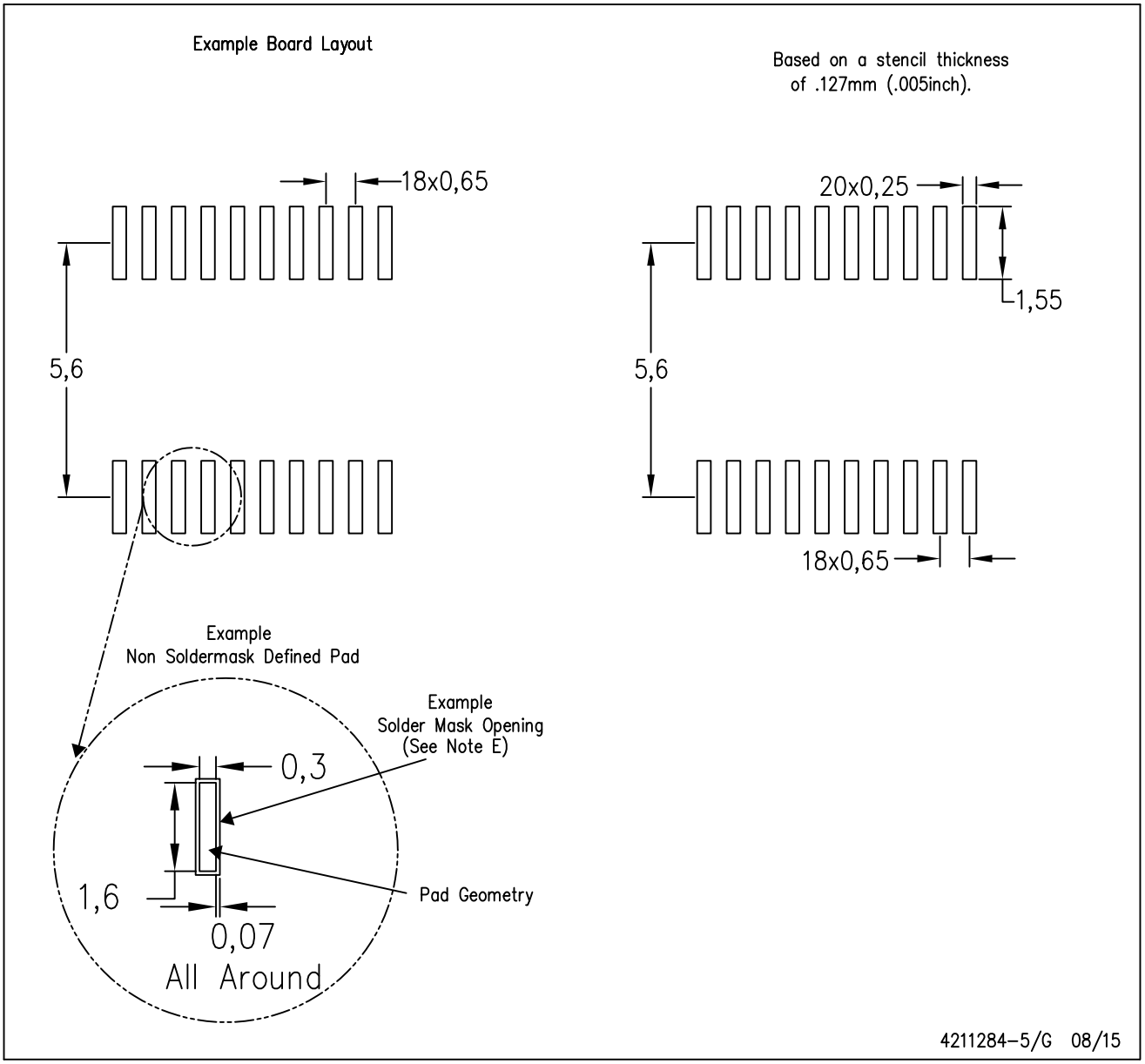

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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