

SNx5ALS180 差分驱动器和接收器对

1 特性

- 符合或超出 TIA/EIA-422-B、TIA/EIA-485-A 的要求¹ 和 ITU 建议 V.11
- 高速高级低功耗肖特基电路
- 专为串行和并行应用中的 25Mbaud 运行而设计
- 低器件间延迟：6ns (最大值)
- 低电源电流要求：30 mA (最大值)
- 具有双 V_{CC} 和双 GND 的独立驱动器和接收器 I/O 引脚
- 宽正负输入/输出总线电压范围
- 驱动器输出容量：±60mA
- 热关断保护
- 驱动器正负电流限制
- 接收器输入阻抗：12kΩ 最小值
- 接收器输入灵敏度：±200mV (最大值)
- 接收器输入迟滞：60 mV (典型值)
- 由一个 5V 单电源供电运行
- 无干扰上电和断电保护

2 说明

SN65ALS180 和 SN75ALS180 差分驱动器和接收器对是专为多点总线传输线路上的双向数据通信而设计的集成电路。这些器件专为平衡传输线路而设计，符合 TIA/EIA-422-B、TIA/EIA-485-A 和 ITU 建议 V.11。

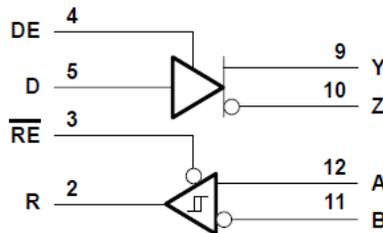
SN65ALS180 和 SN75ALS180 整合了一个三态差分线路驱动器和一个差分输入线路接收器，两者均采用 5V 单电源供电。驱动器和接收器分别具有高电平有效和低电平有效使能端，它们可以在外部连接在一起以用作方向控制。驱动器差分输出端和接收器差分输入端连接到单独的终端以实现更大的灵活性，这些端口用于在禁用驱动器或 V_{CC} = 0 时为总线提供最小负载。

这些端口具有正负宽共模电压范围，使得该器件非常适用于合用线应用。

封装信息

| 器件型号 | 封装 ⁽¹⁾ | 封装尺寸 (标称值) |
|------------|-------------------|-----------------|
| SNx5ALS176 | D (SOIC) | 8.65mm x 3.91mm |
| | N (PDIP) | 19.3mm x 6.35mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图 (正逻辑)

¹ 这些器件符合或超出 TIA/EIA-485-A 的要求，但发生器争用测试 (第 3.4.2 段) 和发生器电流限制 (第 3.4.3 段) 除外。对于 SN75ALS180，所施加的测试电压范围为 -6V 至 8V；对于 SN65ALS180，所施加的测试电压范围为 -4V 至 8V。



Table of Contents

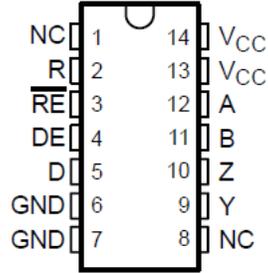
| | | | |
|--|-----------|--|-----------|
| 1 特性 | 1 | 7 Detailed Description | 13 |
| 2 说明 | 1 | 7.1 Functional Block Diagram..... | 13 |
| 3 Revision History | 2 | 7.2 Device Functional Modes..... | 14 |
| 4 Pin Configuration and Functions | 3 | 8 Application and Implementation | 15 |
| 5 Specifications | 4 | 8.1 Application Information..... | 15 |
| 5.1 Absolute Maximum Ratings..... | 4 | 8.2 Typical Application..... | 15 |
| 5.2 Recommended Operating Conditions..... | 4 | 9 Device and Documentation Support | 16 |
| 5.3 Thermal Information..... | 4 | 9.1 Documentation Support..... | 16 |
| 5.4 Electrical Characteristics - Driver..... | 5 | 9.2 接收文档更新通知..... | 16 |
| 5.5 Switching Characteristics - Driver..... | 5 | 9.3 支持资源..... | 16 |
| 5.6 Symbol Equivalents..... | 6 | 9.4 Trademarks..... | 16 |
| 5.7 Electrical Characteristics - Receivers..... | 7 | 9.5 静电放电警告..... | 16 |
| 5.8 Switching Characteristics - Receivers..... | 7 | 9.6 术语表..... | 16 |
| 5.9 Typical Characteristics..... | 8 | 10 Mechanical, Packaging, and Orderable Information | 16 |
| 6 Parameter Measurement Information | 10 | | |

3 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision G (April 2003) to Revision H (January 2023) | Page |
|--|-------------|
| • 将文档更改为了最新 TI 格式..... | 1 |
| • Deleted the Package thermal impedance from the <i>Absolute Maximum Ratings</i> | 4 |
| • Added the <i>Thermal Information</i> table..... | 4 |
| • Changed the <i>Typical Characteristics</i> graphs..... | 8 |

4 Pin Configuration and Functions



NC - No internal connection

**图 4-1. SN65ALS180 D Package
 SN75ALS180 D or N Package
 (Top View)**

表 4-1. Pin Functions

| NO | Name | Type | Description |
|--------|-----------------|--------|--|
| 1 | NC | - | No Internal connection |
| 2 | R | O | Receive data output |
| 3 | RE | I | Receiver enable, active low |
| 4 | DE | I | Driver enable, active high |
| 5 | D | I | Driver data input |
| 6, 7 | GND | GND | Device ground |
| 8 | NC | - | No Internal connection |
| 9 | Y | O | Digital bus output, Y (Complementary to Z) |
| 10 | Z | O | Digital bus output, Z (Complementary to Y) |
| 11 | A | I | Bus input, A (complementary to B) |
| 12 | B | I | Bus input, B (complementary to A) |
| 13, 14 | V _{CC} | SUPPLY | 4.75V to 5.25V supply |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|--|-----|-----|------|
| V _{CC} | Supply voltage ⁽²⁾ | | 7 | V |
| | Voltage range at any bus terminal | -10 | 15 | V |
| V _I | Enable input voltage | | 5.5 | V |
| T _J | Operating virtual junction temperature | | 150 | °C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 260 | °C |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

5.2 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|-----------------------------------|---|---------------|-----|-----------|------|
| V _{CC} | Supply voltage | 4.75 | 5 | 5.25 | V |
| V _I or V _{IC} | Voltage at any bus terminal (separately or common mode) | | | 12 - 7 | V |
| V _{IH} | High-level input voltage | D, DE, and RE | | 2 | V |
| V _{IL} | Low-level input voltage | D, DE, and RE | | 0.8 | V |
| V _{ID} | Differential input voltage ⁽¹⁾ | | | ±12 | V |
| I _{OH} | High-level output current | Driver | | - 60 | mA |
| | | Receiver | | - 400 | μA |
| I _{OL} | Low-level output current | Driver | | 60 | mA |
| | | Receiver | | 8 | |
| T _A | Operating free-air temperature | SN65ALS180 | | - 40 | °C |
| | | SN75ALS180 | | 0 | |

- (1) Differential-input/output bus voltage is measured at the noninverting terminal, A/Y, with respect to the inverting terminal, B/Z.

5.3 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | N (PDIP) | D (SOIC) (SN65 Devices) | D (SOIC) (SN75 Devices) | UNIT |
|-------------------------------|--|----------|----------------------------|----------------------------|------|
| | | 14-Pins | 14-Pins | 14-Pins | |
| R _{θJA} | Junction-to-ambient thermal resistance | 53.4 | 93.2 | 83.7 | °C/W |
| R _{θJC(top)} | Junction-to-case thermal resistance | 40 | 47.5 | 39.8 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 33.3 | 49.4 | 39.7 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 1 | 11.2 | 7.2 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 33 | 48.9 | 39.7 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP ⁽²⁾ | MAX | UNIT |
|-------------------|---|----------------------------------|--------------------------------|---|--------------------|---------|------|
| V _{IK} | Input clamp voltage | I _I = -18 mA | | | | -1.5 | V |
| V _O | Output voltage | I _O = 0 | | 0 | | 6 | V |
| V _{OD1} | Differential output voltage | I _O = 0 | | 1.5 | | 6 | V |
| V _{OD2} | Differential output voltage | R _L = 100 Ω | See Figure 6-1 | 1/2V _{OD1} or 2 ⁽³⁾ | | | V |
| | | R _L = 54 Ω | See Figure 6-1 | 1.5 | 2.5 | 5 | |
| V _{OD3} | Differential output voltage | V _{test} = -7 V to 12 V | See Figure 6-2 | 1.5 | | 5 | V |
| Δ V _{OD} | Change in magnitude of differential output voltage ⁽⁴⁾ | R _L = 54 Ω or 100 Ω | See Figure 6-1 | | | ±0.2 | V |
| V _{OC} | Common-mode output voltage | R _L = 54 Ω or 100 Ω | See Figure 6-1 | | | 3 -1 | V |
| Δ V _{OC} | Change in magnitude of common-mode output voltage ⁽⁴⁾ | R _L = 54 Ω or 100 Ω | See Figure 6-1 | | | ±0.2 | V |
| I _O | Output current | Output disabled ⁽⁶⁾ | | V _O = 12 V | | 1 | mA |
| | | | | V _O = -7 V | | -0.8 | |
| I _{IH} | High-level input current | V _I = 2.4 V | | | | 20 | μA |
| I _{IL} | Low-level input current | V _I = 0.4 V | | | | -400 | μA |
| I _{OS} | Short-circuit output current ⁽⁵⁾ | V _O = -6 V | SN75ALS180 | | | -250 | mA |
| | | V _O = -4 V | SN65ALS180 | | | -250 | |
| | | V _O = 0 | All | | | -150 | |
| | | V _O = V _{CC} | All | | | 250 | |
| | | V _O = 8 V | All | | | 250 | |
| I _{CC} | Supply current | No load | | Driver outputs enabled, Receiver disabled | 25 | 30 | mA |
| | | | | Outputs disabled | 19 | 26 | |

- (1) The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
- (2) All typical values are at V_{CC} = 5 V, T_A = 25°C.
- (3) The minimum V_{OD2} with 100-Ω load is either 1/2 V_{OD2} or 2 V, whichever is greater.
- (4) Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
- (5) Duration of the short circuit should not exceed one second for this test.
- (6) This applies for both power on and off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

5.5 Switching Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------------|---|------------------------|--------------------------------|--------------------------------|-----|--------------------|-----|------|
| t _{d(OD)} | Differential output delay time | R _L = 54 Ω | C _L = 50 pF, | See Figure 6-3 | 3 | 8 | 13 | ns |
| | Pulse skew (t _{d(ODH)} - t _{d(ODL)}) | R _L = 54 Ω | C _L = 50 pF, | See Figure 6-3 | | 1 | 6 | ns |
| t _{t(OD)} | Differential output transition time | R _L = 54 Ω | C _L = 50 pF, | See Figure 6-3 | 3 | 8 | 13 | ns |
| t _{PZH} | Output enable time to high level | R _L = 110 Ω | See Figure 6-4 | | | 23 | 50 | ns |
| t _{PZL} | Output enable time to low level | R _L = 110 Ω | See Figure 6-5 | | | 19 | 24 | ns |
| t _{PHZ} | Output disable time from high level | R _L = 110 Ω | See Figure 6-4 | | | 8 | 13 | ns |

5.5 Switching Characteristics - Driver (continued)

over recommended ranges of supply voltage and operating free-air temperature

| PARAMETER | | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------|------------------------------------|--------------------|-----------|-----|--------------------|-----|------|
| t_{PLZ} | Output disable time from low level | $R_L = 110 \Omega$ | See 图 6-5 | | 8 | 13 | ns |

(1) All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

5.6 Symbol Equivalents

| DATA-SHEET PARAMETER | TIA/EIA-422-B | TIA/EIA-485-A |
|-------------------------|-------------------------|---|
| V_O | V_{oa}, V_{ob} | V_{oa}, V_{ob} |
| $ V_{OD1} $ | V_o | V_o |
| $ V_{OD2} $ | $V_t(R_L = 100 \Omega)$ | $V_t(R_L = 54 \Omega)$ |
| $ V_{OD3} $ | | V_t (test termination measurement 2) |
| V_{test} | | V_{tst} |
| $\Delta V_{OD} $ | $ V_t - V_t $ | $ V_t - V_t $ |
| V_{OC} | $ V_{os} $ | $ V_{os} $ |
| $\Delta V_{OC} $ | $ V_{os} - V_{os} $ | $ V_{os} - V_{os} $ |
| I_{OS} | $ I_{sa} , I_{sb} $ | |
| I_O | $ I_{xa} , I_{xb} $ | I_{ia}, I_{ib} |

5.7 Electrical Characteristics - Receivers

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|---|----------------------------------|---|-----------|----------------------|--------------------|-----|------|
| V _{IT+} | Positive-going input threshold voltage | V _O = 2.7 V, | I _O = - 0.4 mA | | | 0.2 | V | |
| V _{IT-} | Negative-going input threshold voltage | V _O = 0.5 V, | I _O = 8 mA | | - 0.2 ⁽²⁾ | | V | |
| V _{hys} | Hysteresis voltage (V _{IT+} - V _{IT-}) | | | | 60 | | mV | |
| V _{IK} | Enable-input clamp voltage | I _I = - 18 mA | | | | - 1.5 | V | |
| V _{OH} | High-level output voltage | V _{ID} = 200 mV, | I _{OH} = - 400 μA, | See 图 6-6 | 2.7 | | V | |
| V _{OL} | Low-level output voltage | V _{ID} = - 200 mV, | I _{OL} = 8 mA, | See 图 6-6 | | 0.45 | V | |
| I _{OZ} | High-impedance-state output current | V _O = 0.4 V to 2.4 V | | | | ±20 | μA | |
| I _I | Line input current | Other input = 0 V ⁽³⁾ | V _I = 12 V V _I = - 7 V | | | 1 - 0.8 | mA | |
| I _{IH} | High-level enable-input current | V _{IH} = 2.7 V | | | | 20 | mA | |
| I _{IL} | Low-level enable-input current | V _{IL} = 0.4 V | | | | - 100 | mA | |
| r _i | Input resistance | | | | 12 | | kΩ | |
| I _{OS} | Short-circuit output current | V _{ID} = 200 mV, | V _O = 0 | | - 15 | - 85 | mA | |
| I _{CC} | Supply current | No load | Receiver outputs enabled, Driver inputs disabled | | | 19 30 | mA | |
| | | | Outputs disabled | | | 19 26 | | |

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

(3) This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

5.8 Switching Characteristics - Receivers

over recommended ranges of supply voltage and operating free-air temperature

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|---|--|-------------------------|--|-----|--------------------|-----|------|
| t _{PLH} | Propagation delay time, low- to high-level output | V _{ID} = - 1.5 V to 1.5 V, See 图 6-7 | C _L = 15 pF, | | 9 | 14 | 19 | ns |
| t _{PHL} | Propagation delay time, high- to low-level output | V _{ID} = - 1.5 V to 1.5 V, See 图 6-7 | C _L = 15 pF, | | 9 | 14 | 19 | ns |
| | Skew (t _{PHL} - t _{PLH}) | V _{ID} = - 1.5 V to 1.5 V, See 图 6-7 | C _L = 15 pF, | | | 2 | 6 | ns |
| t _{PZH} | Output enable time to high level | C _L = 15 pF, | See 图 6-8 | | | 7 | 14 | ns |
| t _{PZL} | Output enable time to low level | C _L = 15 pF, | See 图 6-8 | | | 7 | 14 | ns |
| t _{PHZ} | Output disable time from high level | C _L = 15 pF, | See 图 6-8 | | | 20 | 35 | ns |
| t _{PLZ} | Output disable time from low level | C _L = 15 pF, | See 图 6-8 | | | 8 | 17 | ns |

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

5.9 Typical Characteristics

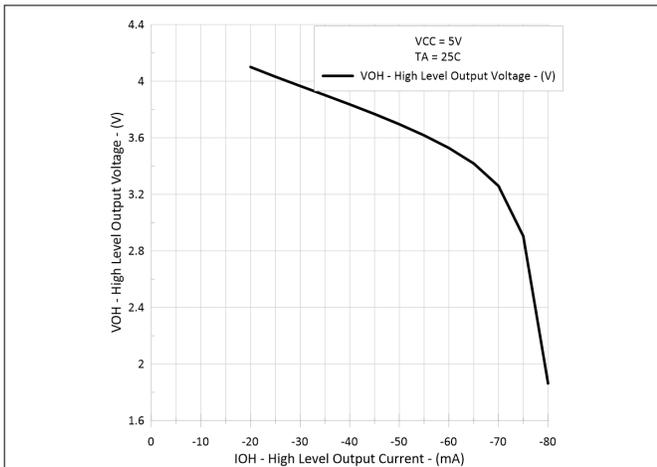


图 5-1. Drivers High-Level Output Voltage vs High-Level Output Voltage

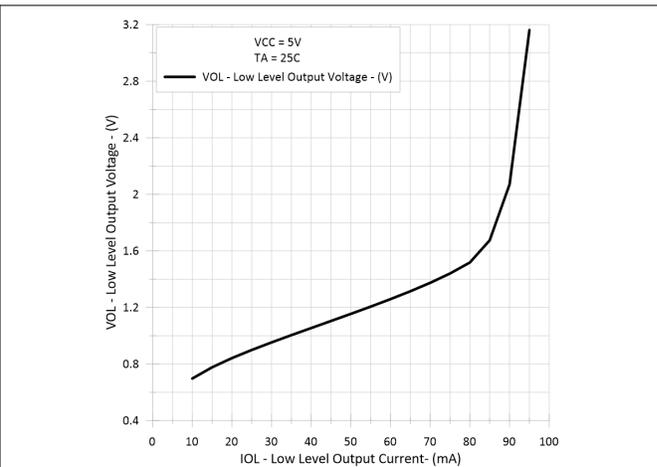


图 5-2. Drivers Low-Level Output Voltage vs Low-Level Output Current

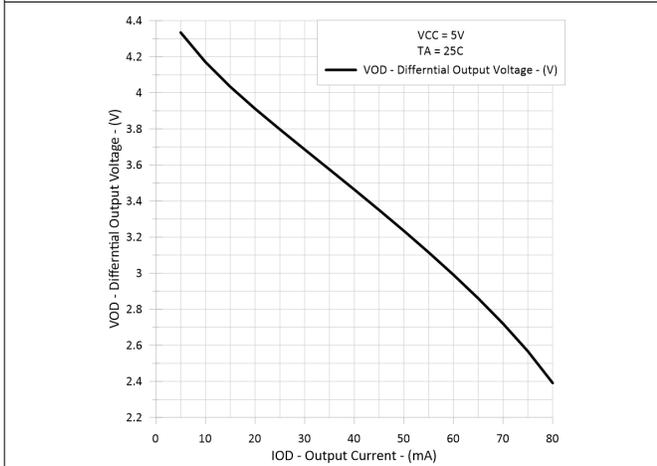


图 5-3. Drivers Differential Output Voltage vs Output Current

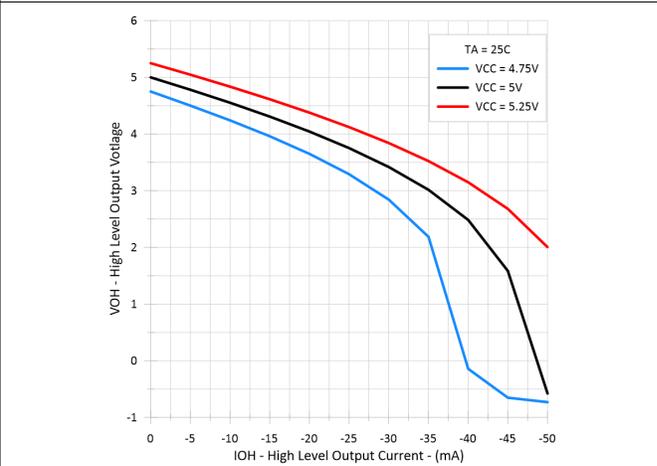


图 5-4. Receivers High-Level Output Voltage vs High-Level Output Current

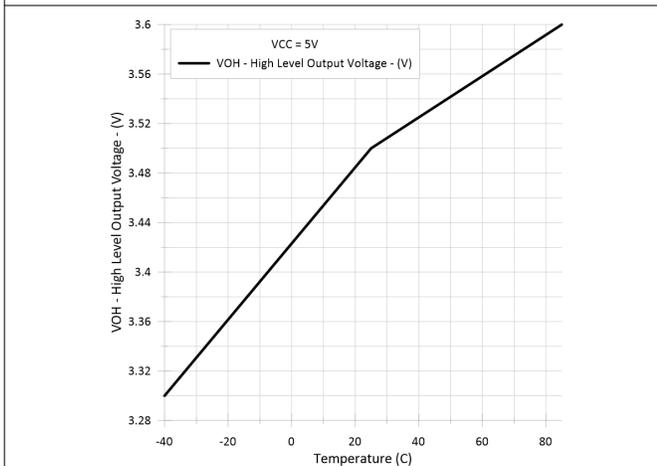


图 5-5. Receivers High-Level Output Voltage vs Free-Air Temperature

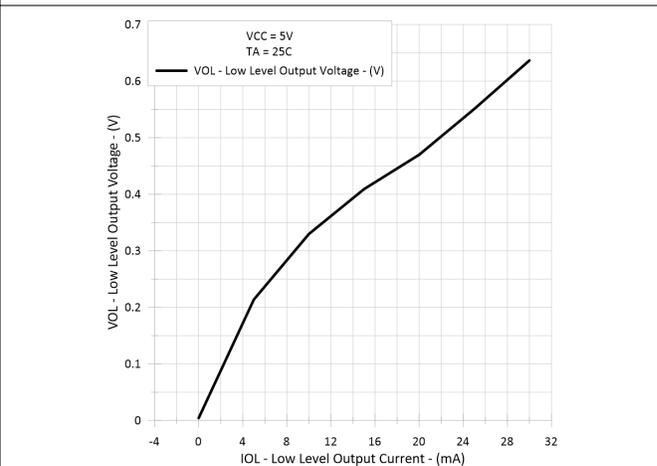
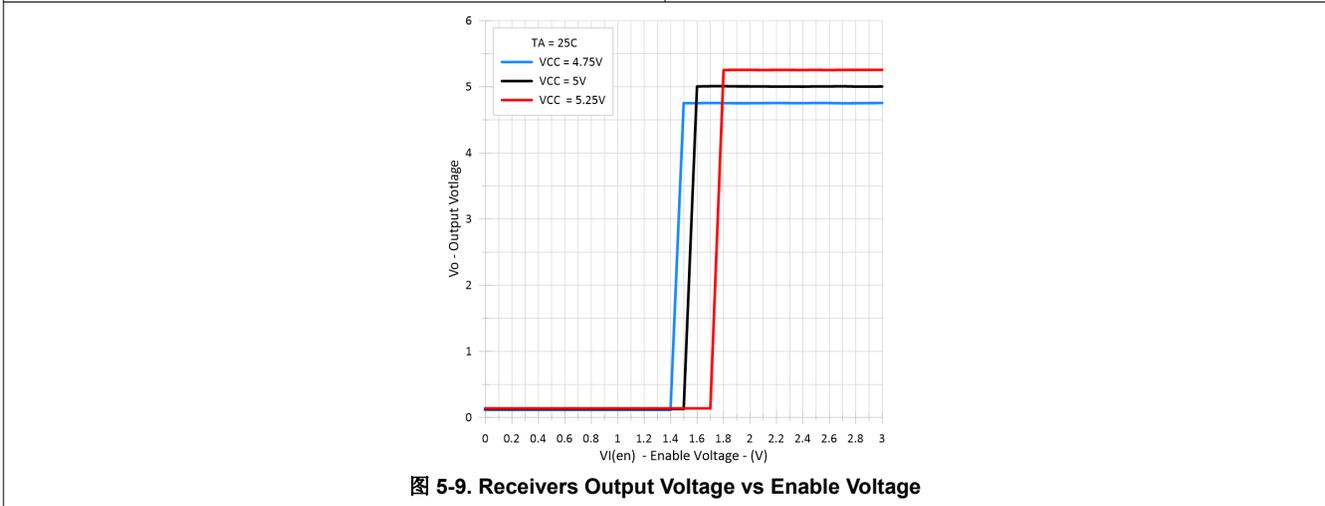
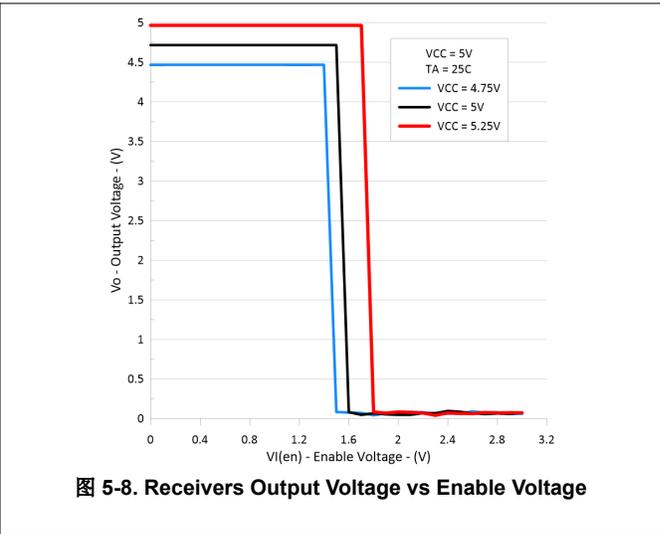
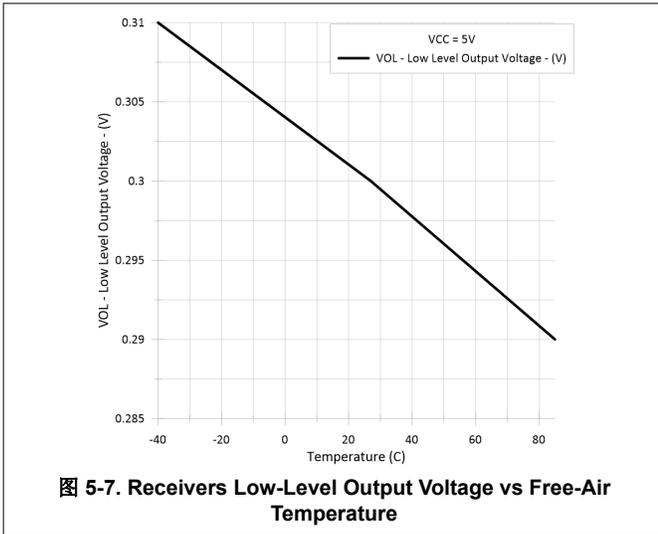


图 5-6. Receivers Low-Level Output Voltage vs Low-Level Output Current

5.9 Typical Characteristics (continued)



6 Parameter Measurement Information

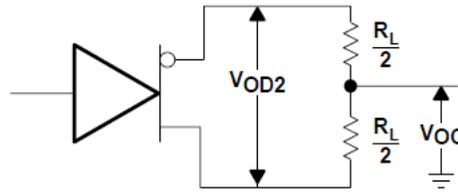


图 6-1. Driver V_{OD} and V_{OC}

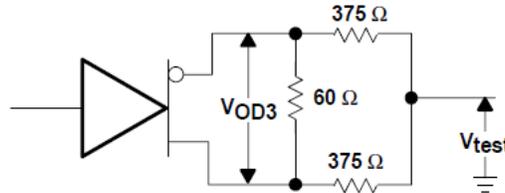
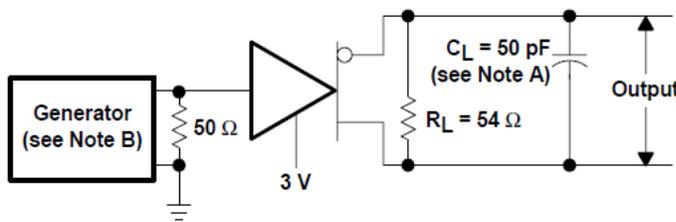
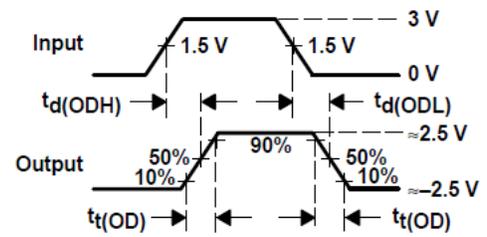


图 6-2. Driver V_{OD3}



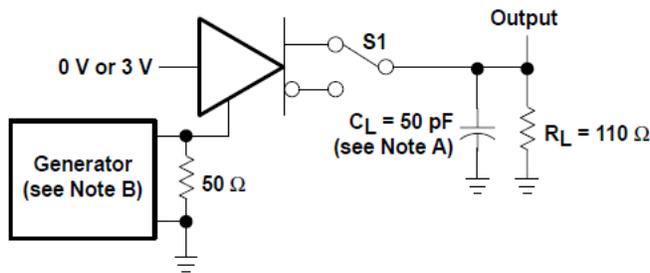
TEST CIRCUIT



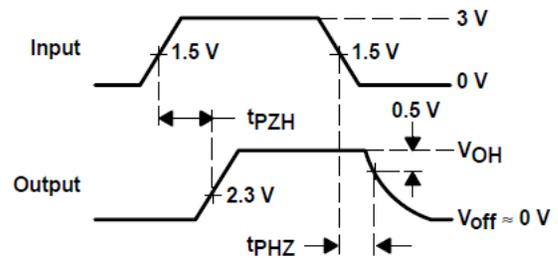
VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

图 6-3. Driver Test Circuit and Voltage Waveforms



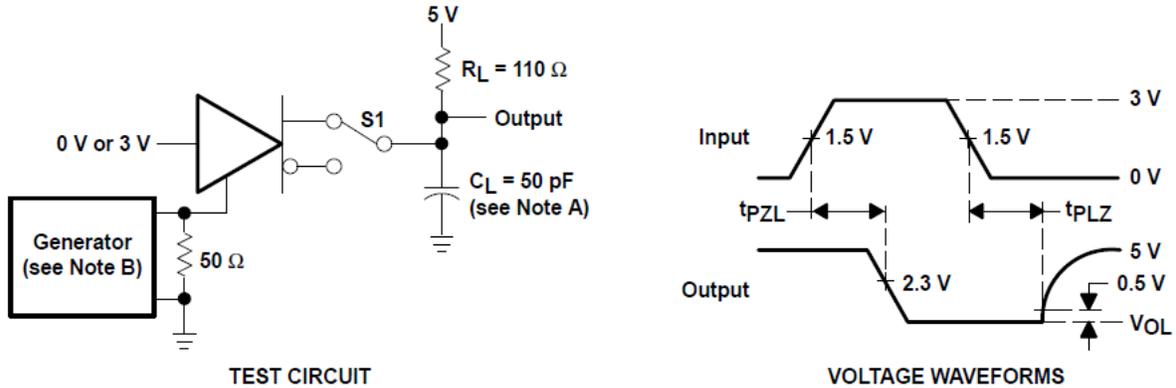
TEST CIRCUIT



VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

图 6-4. Driver Test Circuit and Voltage Waveforms



- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.

图 6-5. Driver Test Circuit and Voltage Waveforms

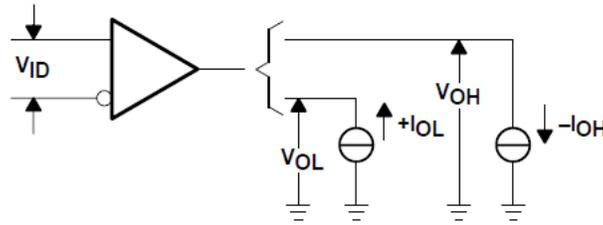
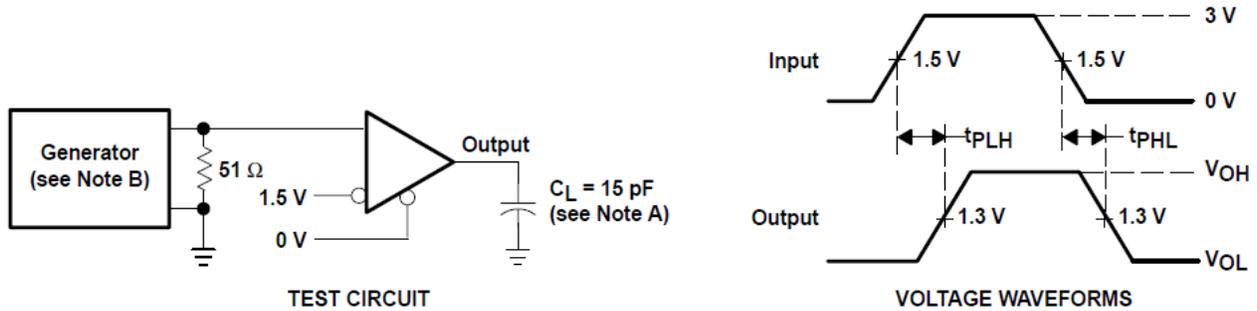
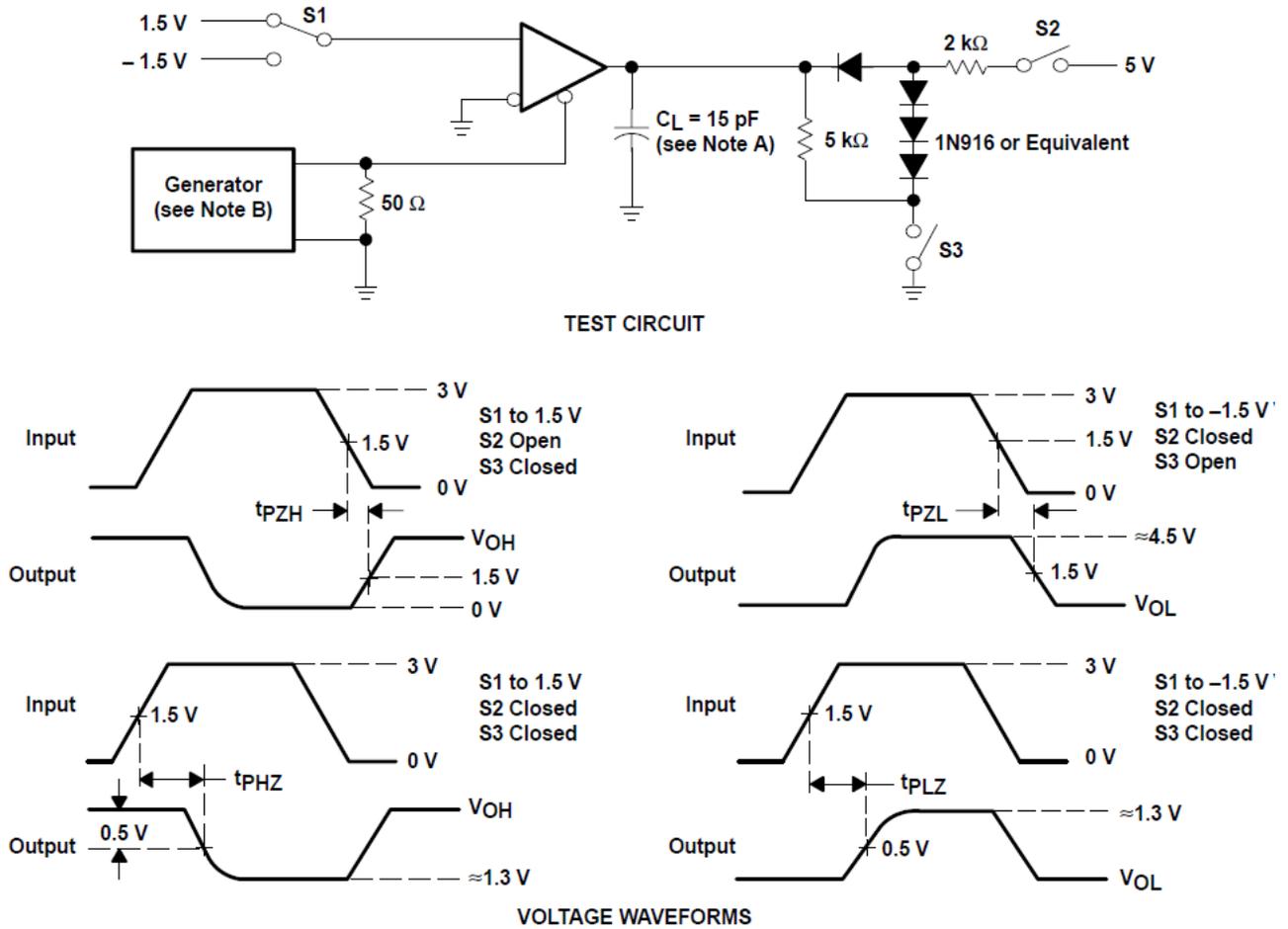


图 6-6. Receiver V_{OH} and V_{OL}



- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_O = 50 \Omega$.

图 6-7. Receiver Test Circuit and Voltage Waveforms



- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_0 = 50 \Omega$.

图 6-8. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

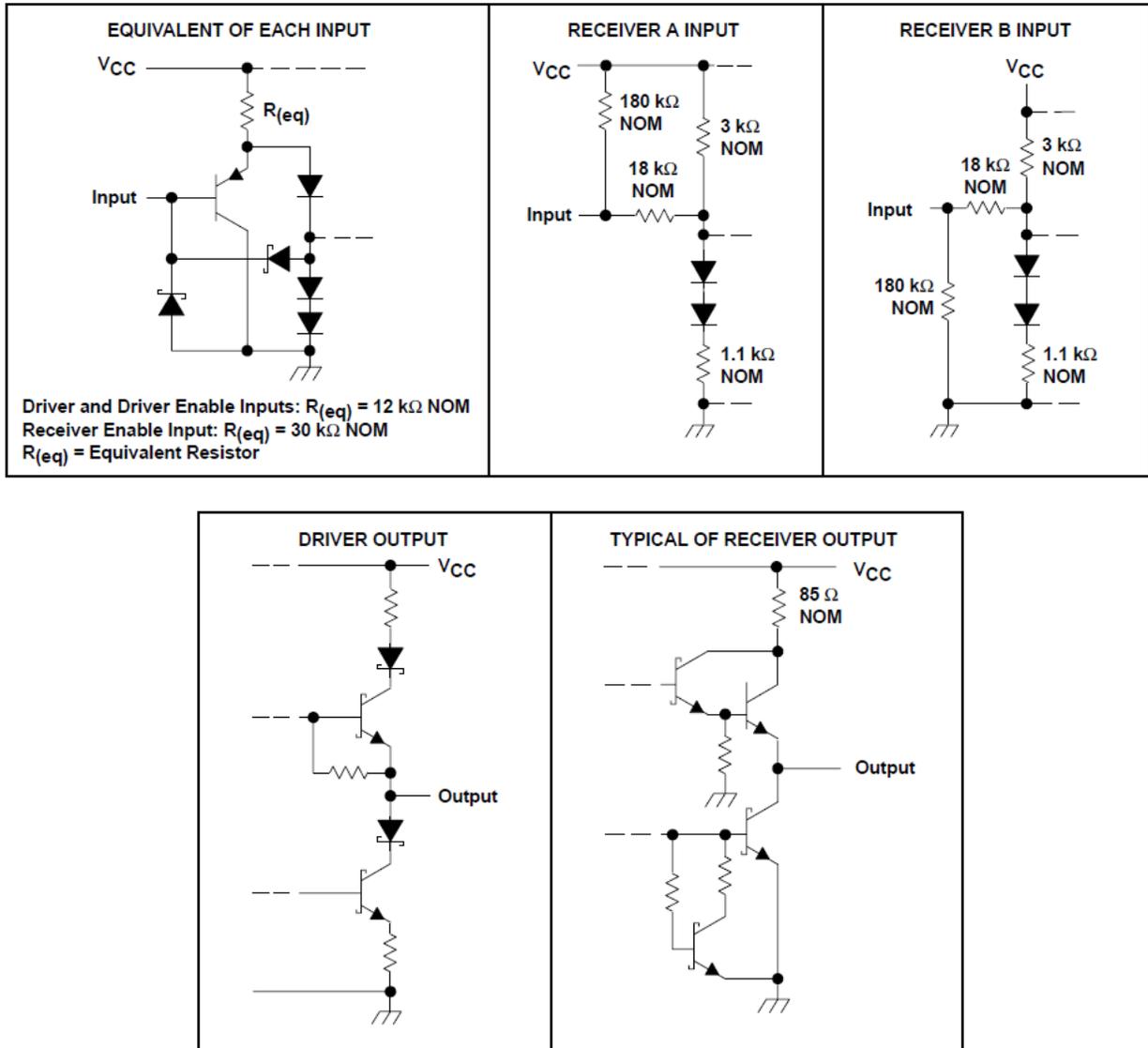


图 7-1. Schematic of Inputs and Outputs

7.2 Device Functional Modes

Function Tables

表 7-1. Driver⁽¹⁾

| INPUT D | ENABLE DE | OUTPUTS | |
|------------|--------------|---------|---|
| | | Y | Z |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

表 7-2. Receiver⁽¹⁾

| DIFFERENTIAL INPUTS A - B | ENABLE RE | OUTPUT R |
|---|--------------|-------------|
| $V_{ID} \geq 0.2 \text{ V}$ | L | H |
| $-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$ | L | ? |
| $V_{ID} \leq -0.2 \text{ V}$ | L | L |
| X | H | Z |
| Open | L | H |

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

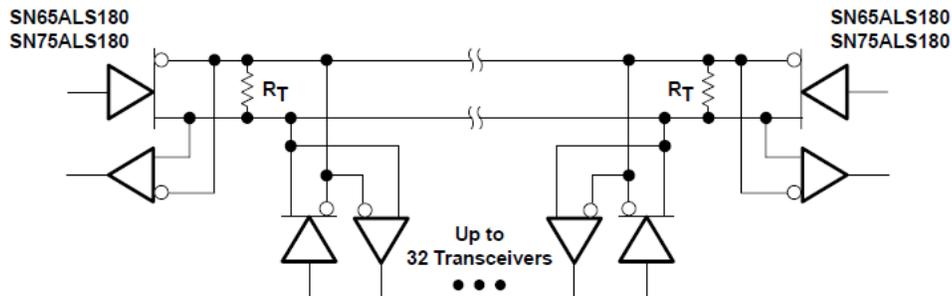
8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application



- A. The line should terminate at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

图 8-1. Typical Application Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN65ALS180D | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | -40 to 85 | 65ALS180 |
| SN65ALS180DR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65ALS180 |
| SN65ALS180DR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65ALS180 |
| SN65ALS180DRG4 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65ALS180 |
| SN75ALS180D | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | 0 to 70 | 75ALS180 |
| SN75ALS180DR | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | 0 to 70 | 75ALS180 |
| SN75ALS180N | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75ALS180N |
| SN75ALS180N.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75ALS180N |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

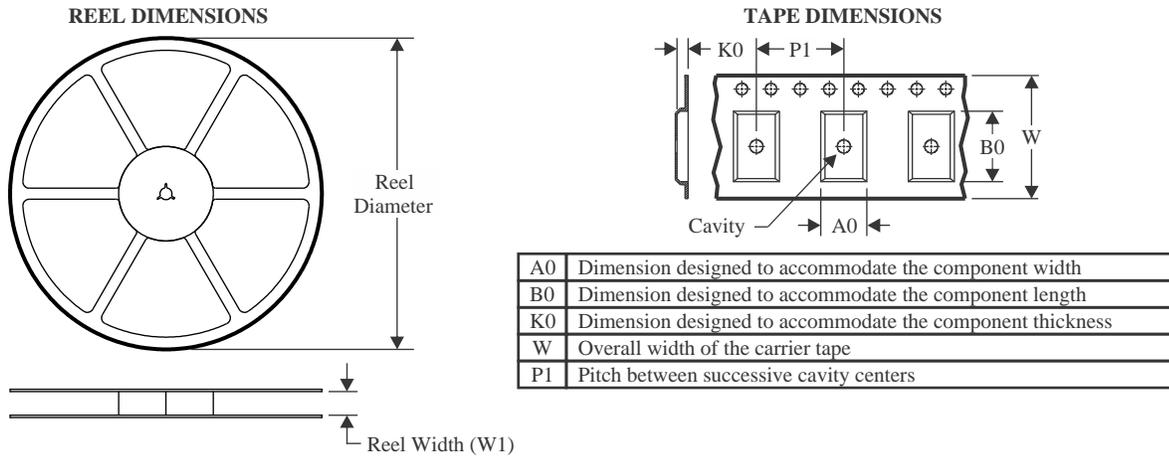
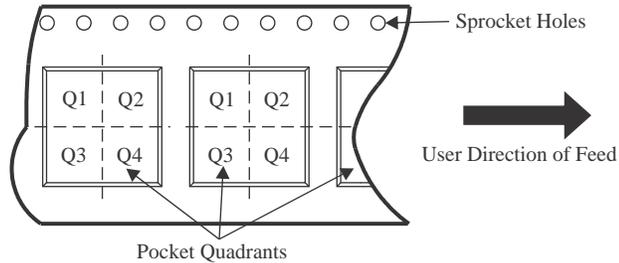
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


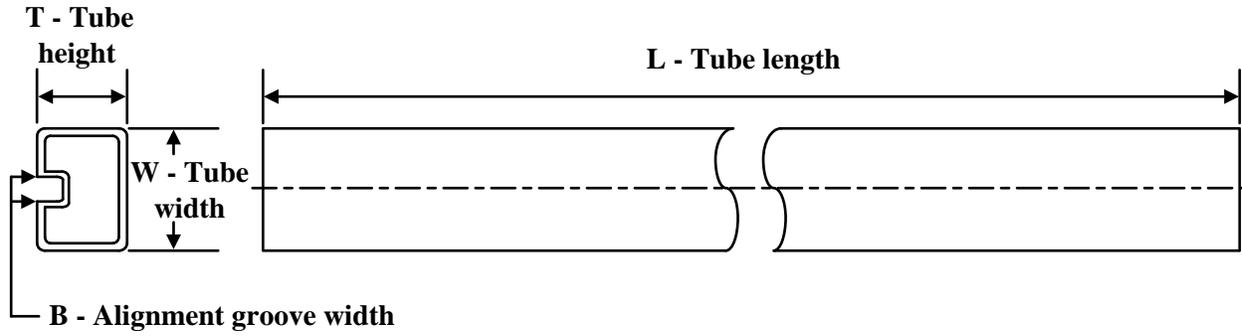
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65ALS180DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65ALS180DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN75ALS180N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN75ALS180N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

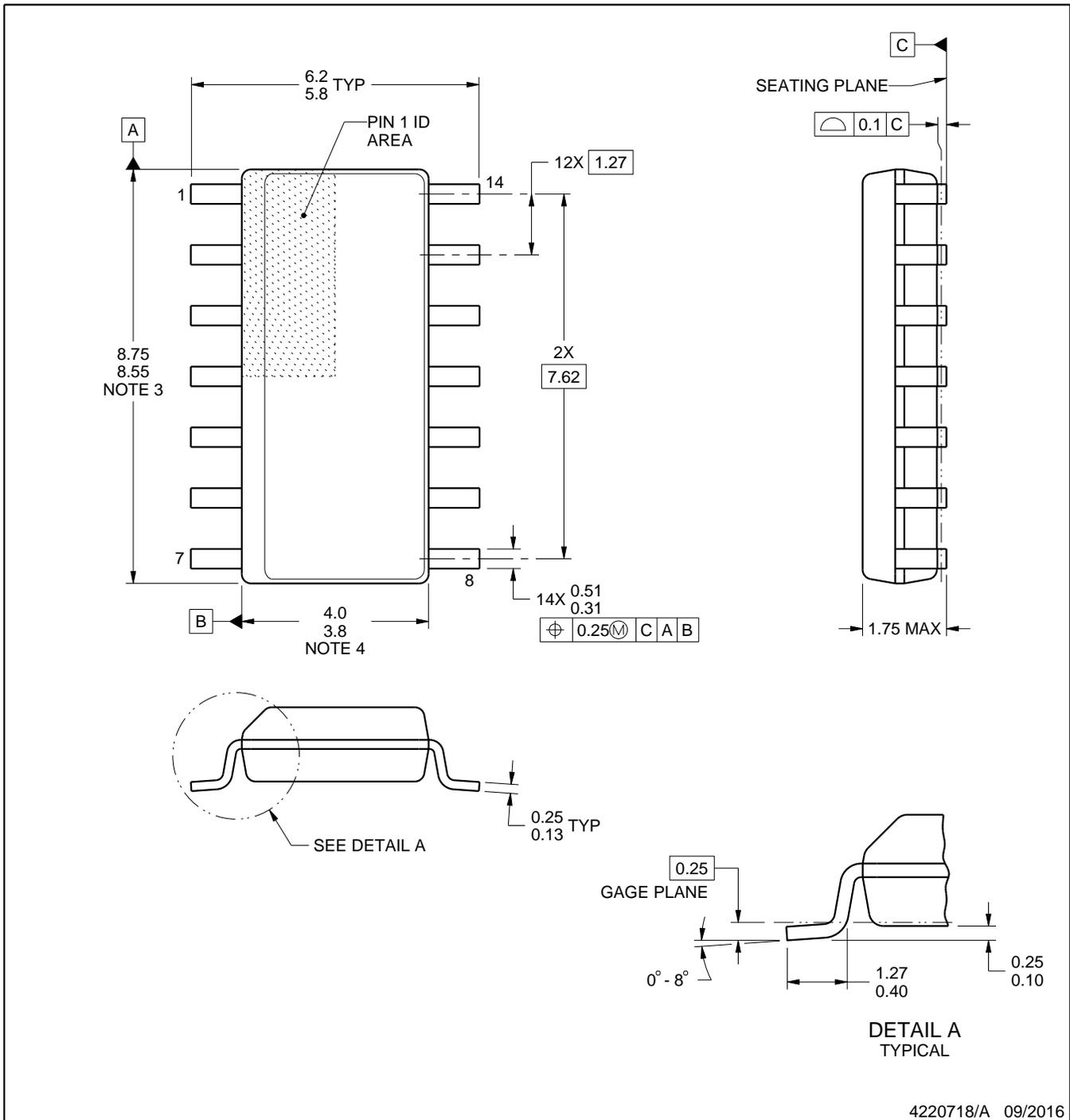


D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

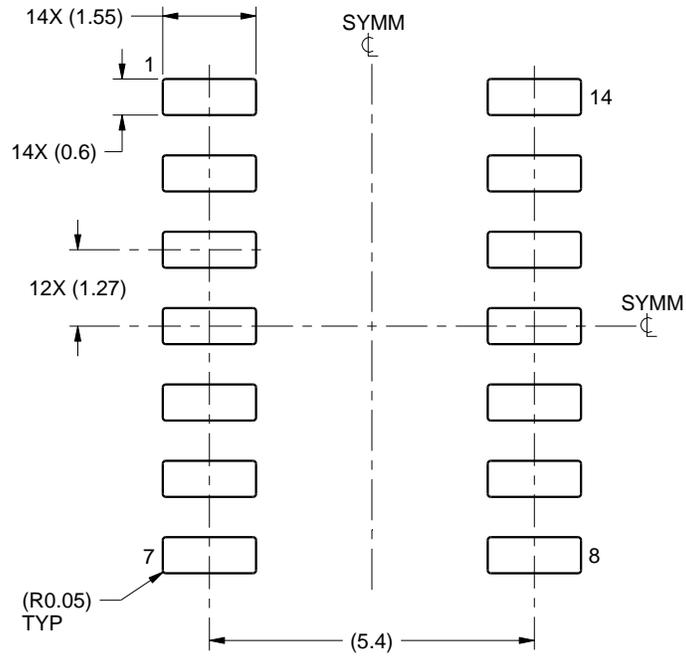
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

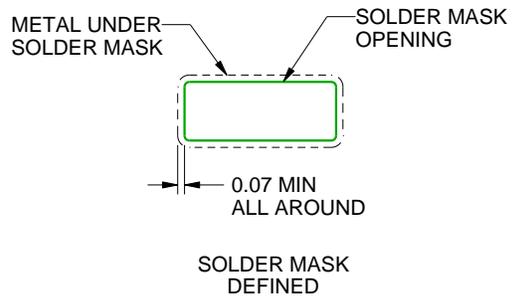
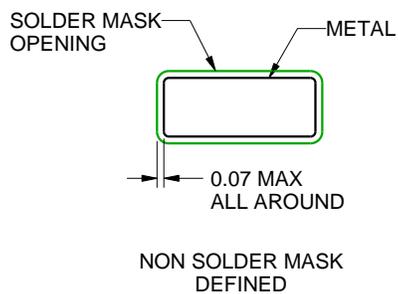
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

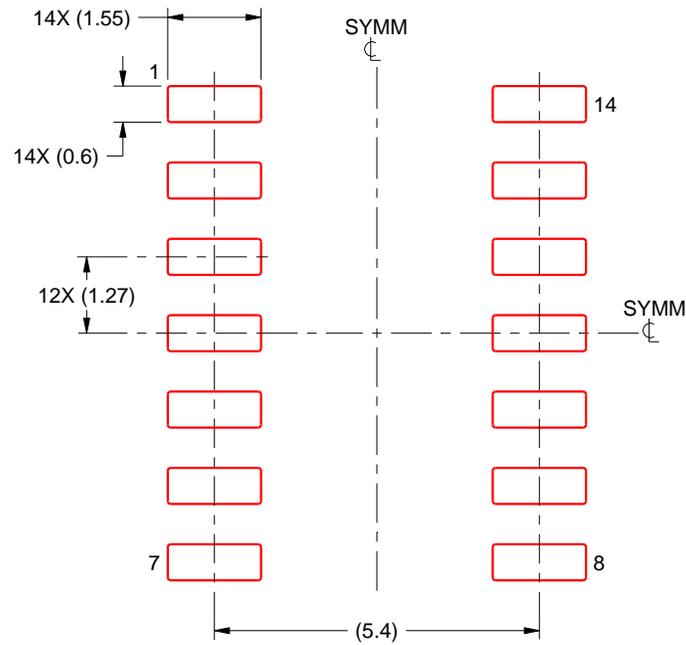
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

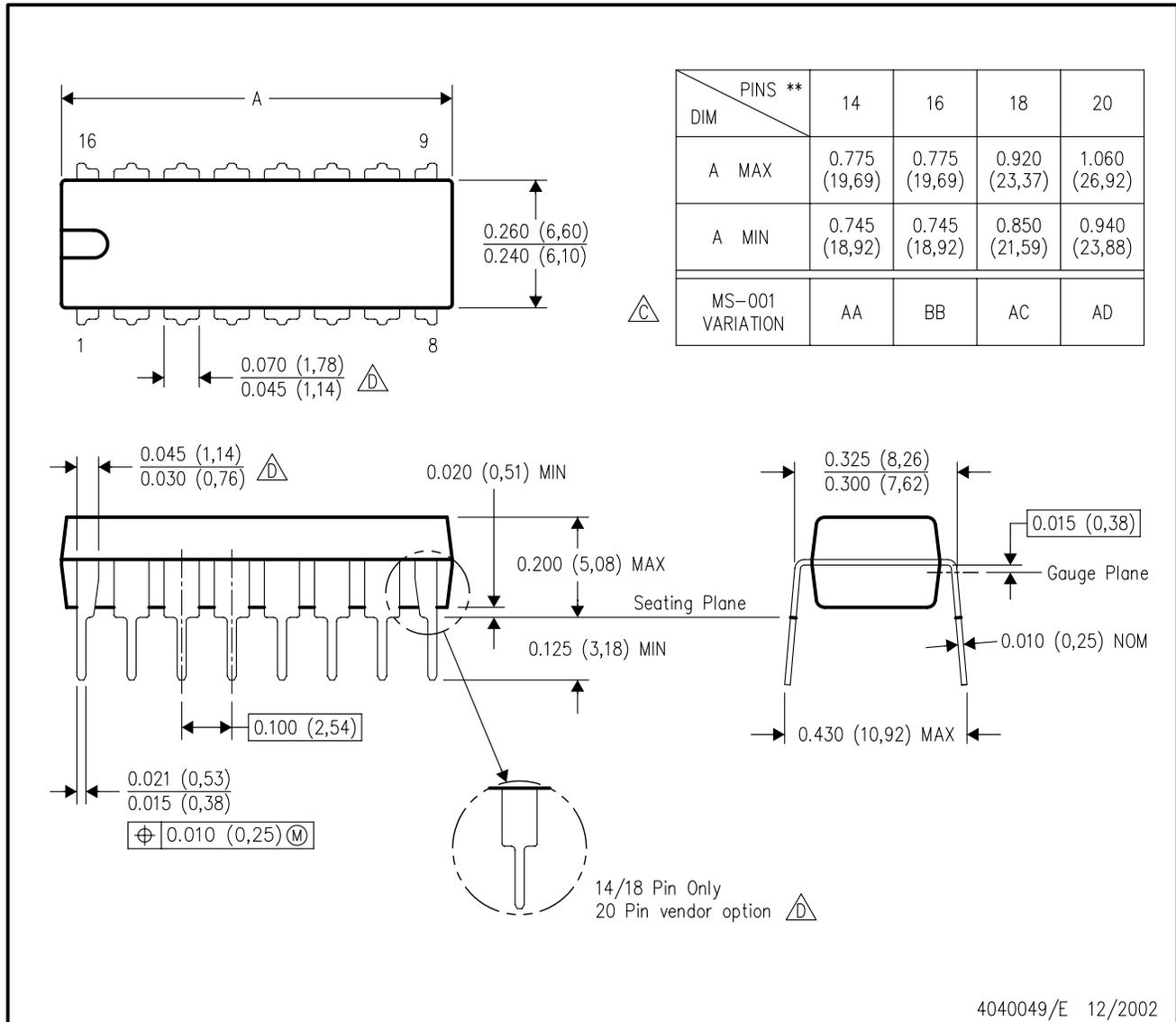
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月