SNx5LBC182 差分总线收发器

1 特性

- 四分之一单位负载允许一条总线上多达 128 个器件
- 符合或超出 ANSI 标准 TIA/EIA-485-A 和 ISO 8482 的要求：1987(E)
- 受控的驱动器输出电压压摆率允许更长的电缆残桩长度
- 专门针对信号传输速率而设计。
  - 线路的信号传输速率是每秒进行电压转换的次数，以单位 bps（每秒位数）来表示，最高 250kbps
- 低禁用电源电流：250 µA（最大值）
- 热关断保护
- 开路失效防护接收器设计
- 接收器输入迟滞：70mV（典型值）
- 无干扰上电和断电保护

2 应用

- 公用事业计量表
- 工业过程控制
- 楼宇自动化

3 说明

SN65LBC182 和 SN75LBC182 是差分数据线路收发器，提供高级别的 ESD 保护，采用 SN75176 的行业标准封装。这些器件专为平衡传输线路而设计，符合 ANSI 标准 TIA/EIA-485-A 和 ISO 8482。SN65LBC182 和 SN75LBC182 整合了一个三态差分线路驱动器和一个差分输入线路接收器，两者均采用 5V 单电源供电。驱动器和接收器分别具有高电平有效和低电平有效使能端，它们可以在外部连接在一起，用作方向控制。

驱动器输出和接收器输入在内部连接以形成差分输入/输出 (I/O) 总线端口，该端口用于为总线提供最小负载，可在宽共模电压范围内工作，使得该器件非常适合合用线应用。该器件还包含合用线数据总线的附加功能，适用于电气噪声环境应用，例如工业过程控制或电源逆变器。

SN75LBC182 和 SN65LBC182 总线引脚还具有与四分之一单位负载等效的高输入电阻，允许在总线上连接多达 128 个类似器件。高 ESD 容差可保护器件的电缆连接。（如需更高级别的保护，请参阅 SN65/75LBC184，文献编号 SLLS236。）

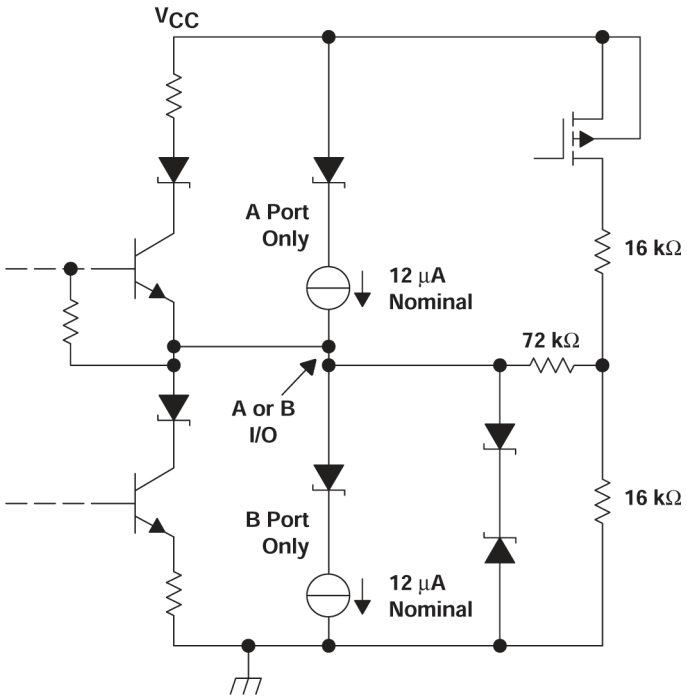
差动驱动器设计包含压摆率受控的输出，足以以高达 250kbps 的速率传输数据。与不受控制的电压转换相比，压摆率控制允许从主干部署更长的未端接电缆和更长的残桩线。该接收器设计可在输入保持悬空（开路）时提供高电平失效防护输出。可以通过禁用驱动器和接收器来实现超低的器件待机电源电流。

SN65LBC182 的额定工作温度范围为 −40°C 至 85°C，SN75LBC182 的额定工作温度范围为 0°C 至 70°C。

封装信息

器件型号	封装(1)	封装尺寸(2)
SN65LBC182、SN75LBC182	P（PDIP，8）	9.81mm × 9.43mm
	D（SOIC，8）	4.9mm × 6mm

(1) 有关详细信息，请参阅 节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



输入和输出原理图

Table of Contents

4 Pin Configuration and Functions

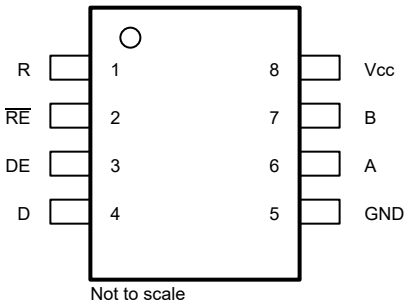


图 4-1. P (PDIP) or D (SOIC) Package (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
R	1	O	Receiver Output
$\overline{RE}$	2	I	Active Low Receiver Enable Input
DE	3	I	Active High Driver Enable Input
D	4	I	Driver Input
GND	5	GND	Device GND
A	6	I/O	Non-Inverting Differential Bus I/O
B	7	I/O	Inverting Differential Bus I/O
V_{CC}	8	PWR	Device VCC (4.75V to 5.25V)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free−air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range, (see (2))	−0.5	7	V
(A or B)	Voltage range at any bus terminal	−15	15	V
V_I (D, DE, R or $\overline{RE}$)	Input voltage	−0.3	7	V
I_O	Receiver output current		±20	mA
	Continuous total power dissipation		See *Dissipation Rating* table	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A, B, GND	±15	kV
			All pins	±3	
		IEC 61000-4-2 contact discharge	A, B, GND	±8	kV
		IEC 61000-4-2 Air-gap discharge	A, B, GND	±15	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Dissipation Rating

PACKAGE(2)	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature

5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus I/O terminal (separately or common mode) V_I or V_{IC}		−7		12	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$	2			V
Low-level input voltage, V_{IL}				0.8	
Differential input voltage, V_{ID} (see (1))		−12		12	V
Output current, I_O	Driver	−60		60	mA
	Receiver	−8		4	
Operating free-air temperature, T_A	SN65LBC182	−40		85	°C
	SN75LBC182	0		70	

(1) Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

5.5 Thermal Information

THERMAL METRIC[1]		D (SOIC)	P (PDIP)	UNIT
		8-PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	65.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	62.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	31.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	60.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.6 Driver Electrical Characteristics

over recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA		−1.5			V
V_O	Output voltage		I_O = 0		0		V_{CC}	V
$\lvert V_{OD}\rvert$	Differential output voltage		R_L = 54 Ω,	See 图 6-1	1.5	2.2	V_{CC}	V
			V_{test} = −7 V to 12 V,	See 图 6-2	1.5	2.2	V_{CC}	V
ΔV_{OD}	Change in magnitude of differential output voltage		See 图 6-1		−0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage				1		3	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		See 图 6-1 and 图 6-4		−0.2		0.2	
$V_{OC(PP)}$	Peak-to-peak change in common-mode output voltage during state transitions					0.8		V
I_{OZ}	High-impedance output current		See receiver input currents					
I_{IH}	High-level input current (D, DE)		V_I = 2.4 V				50	µA
I_{IL}	Low-level input current (D, DE)		V_I = 0.4 V		−50			µA
I_{OS}	Short-circuit output current		V_O = −7 V to 12 V		−250		250	mA
I_{CC}	Supply current	SN75LBC182	No load, DE at V_{CC},	$\overline{RE}$ at V CC		12	25	mA
		SN65LBC182				12	30	

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.7 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage					0.2	V
V_{IT-}	Negative-going input threshold voltage			−0.2			
V_{hys}	Hysteresis voltage (V_{IT+} − V_{IT-})				70		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA		−1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_O = −8 mA,	See 图 6-7	2.8			V

5.7 Receiver Electrical Characteristics（续）

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OL}	Low-level output voltage	V_{ID} = 200 mV, I_O = 4 mA,	See 图 6-7			0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 to 2.4 V				±1	μA
I_I	Bus input current	V_{IH} = 12 V, V_{CC} = 5 V	Other input at 0 V			250	μA
		V_{IH} = 12 V, V_{CC} = 0 V				250	
		V_{IH} = −7 V, V_{CC} = 5 V		−200			
		V_{IH} = −7 V, V_{CC} = 0 V		−200			
I_{IH}	High-level input current ($\overline{RE}$)	V_{IH} = 2 V				50	μA
I_{IL}	Low-level input current ($\overline{RE}$)	V_{IL} = 0.8 V		−50			μA
I_{CC}	Supply current	No load	DE at 0 V, $\overline{RE}$ at 0 V			3.5	mA
			DE at 0 V, $\overline{RE}$ at V_{CC}		175	250	μA

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.8 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Differential output signal rise time	R_L = 54 Ω, See 图 6-3	C_L = 50 pF,	0.25	0.72	1.2	μs
t_f	Differential output signal fall time			0.25	0.73	1.2	
t_{PLH}	Propagation delay time, low-to-high-level output					1.3	
t_{PHL}	Propagation delay time, high-to-low-level output					1.3	
$t_{sk(p)}$	Pulse skew (t_{PHL} − t_{PLH})				0.075	0.15	
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See 图 6-5			3.5	μs
t_{PHZ}	Output disable time from high level					3.5	
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See 图 6-6			3.5	μs
t_{PLZ}	Output disable time from low level					3.5	

5.9 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Differential output signal rise time	C_L = 50 pF,	See 图 6-7		20		ns
t_f	Differential output signal fall time				20		
t_{PLH}	Propagation delay time, low-to-high-level output					150	
t_{PHL}	Propagation delay time, high-to-low-level output					150	
t_{PZH}	Output enable time to high level	See 图 6-8				100	ns
t_{PZL}	Output enable time to low level					100	
t_{PHZ}	Output disable time from high level					100	ns
t_{PLZ}	Output disable time from low level					100	
$t_{sk(p)}$	Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$					50	ns

5.10 Typical Characteristics

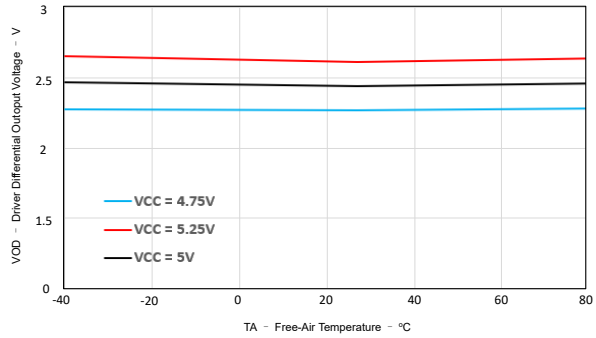


图 5-1. Driver Differential Output Voltage vs Temperature

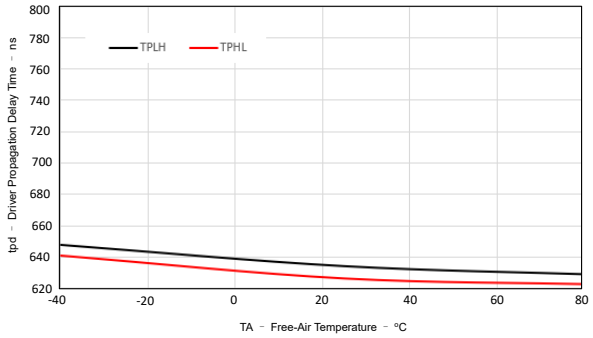


图 5-2. Driver Propagation Delay Time vs Temperature

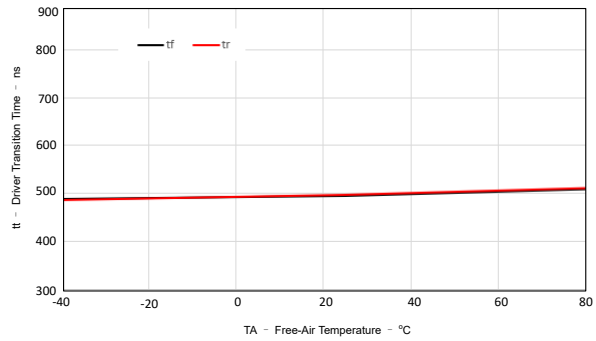


图 5-3. Driver Transition Time vs Temperature

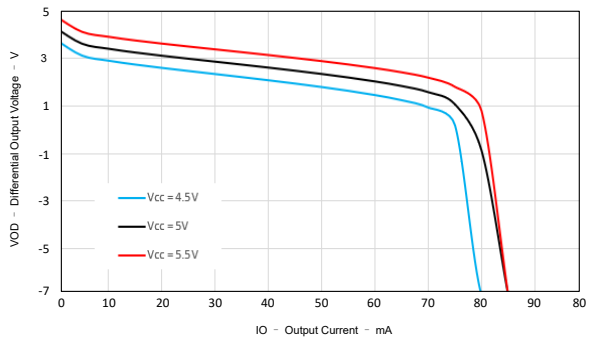


图 5-4. Differential Output Voltage vs Output Current

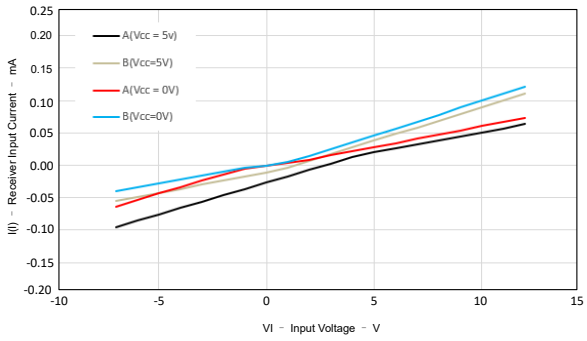
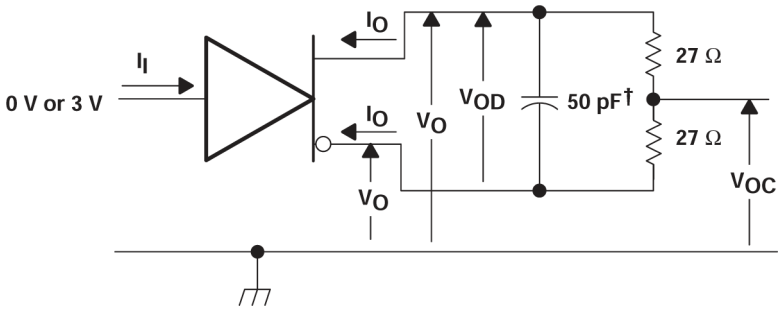


图 5-5. Receiver Input Current vs Input Voltage

6 Parameter Measurement Information



A. Includes probe and jig capacitance

图 6-1. Driver Test Circuit, v_{OD} And v_{OC} Without Common-Mode Loading

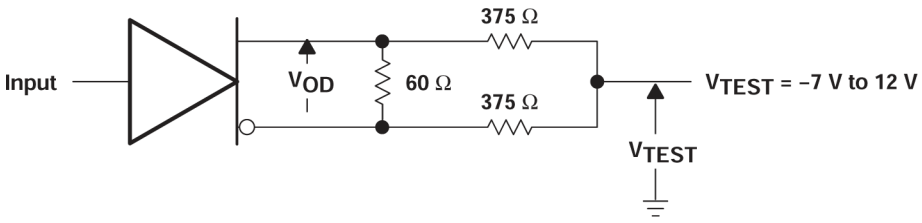
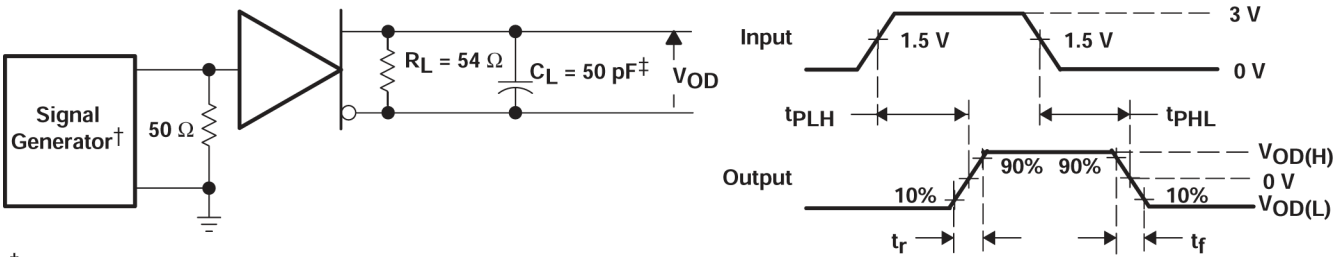


图 6-2. Driver Test Circuit, v_{OD} With Common-Mode Loading



A. PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_o = 50 Ω
B. Includes probe and jig capacitance

图 6-3. Driver Switching Test Circuit and Waveforms

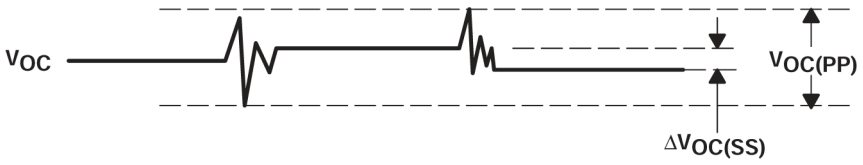
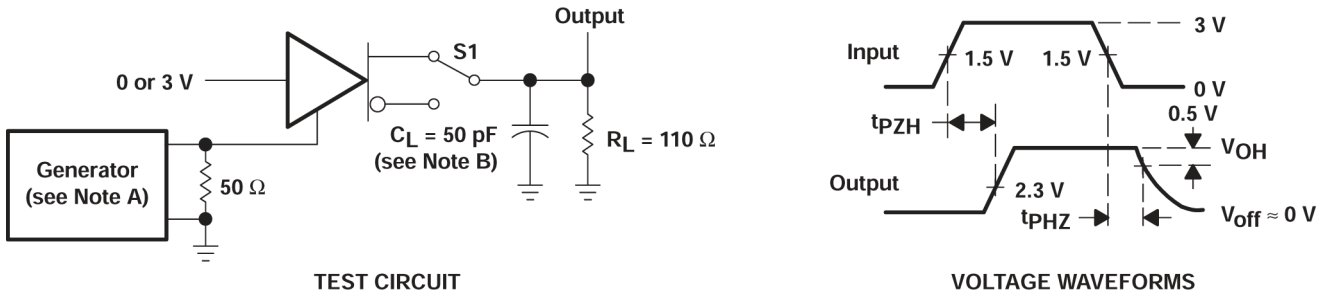


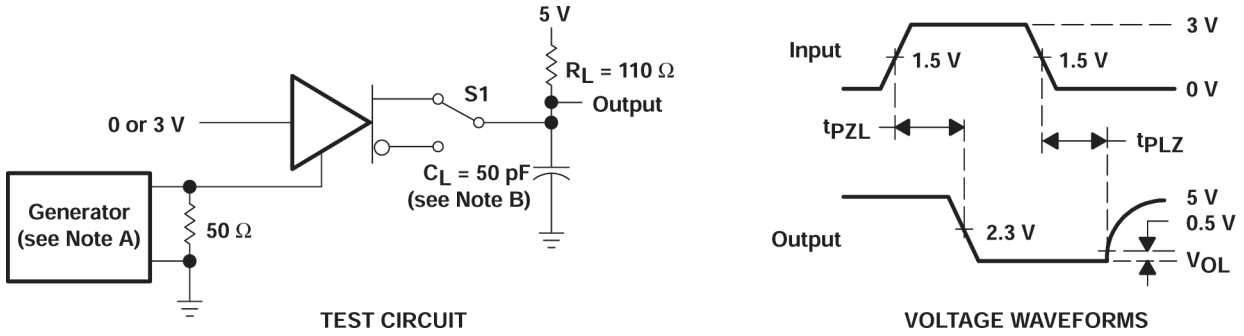
图 6-4. V_{OC} Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.

B. C_L includes probe and jig capacitance.

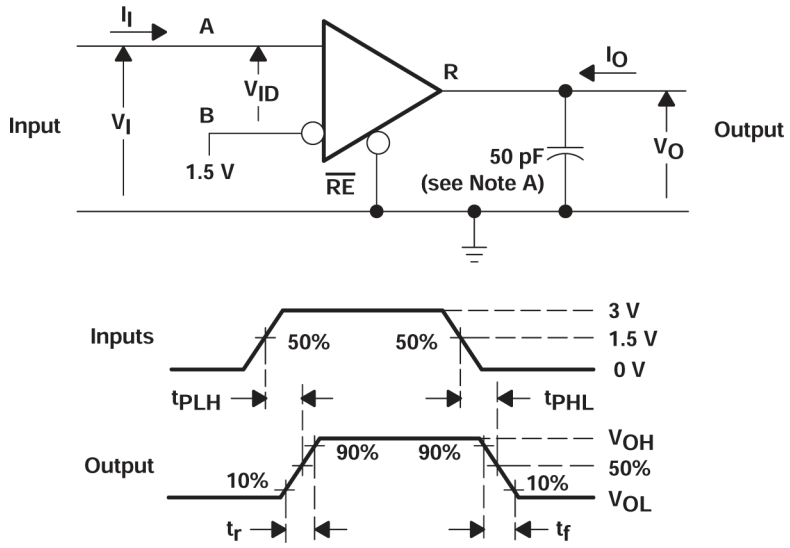
图 6-5. Driver T_{PZH} And T_{PHZ} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.

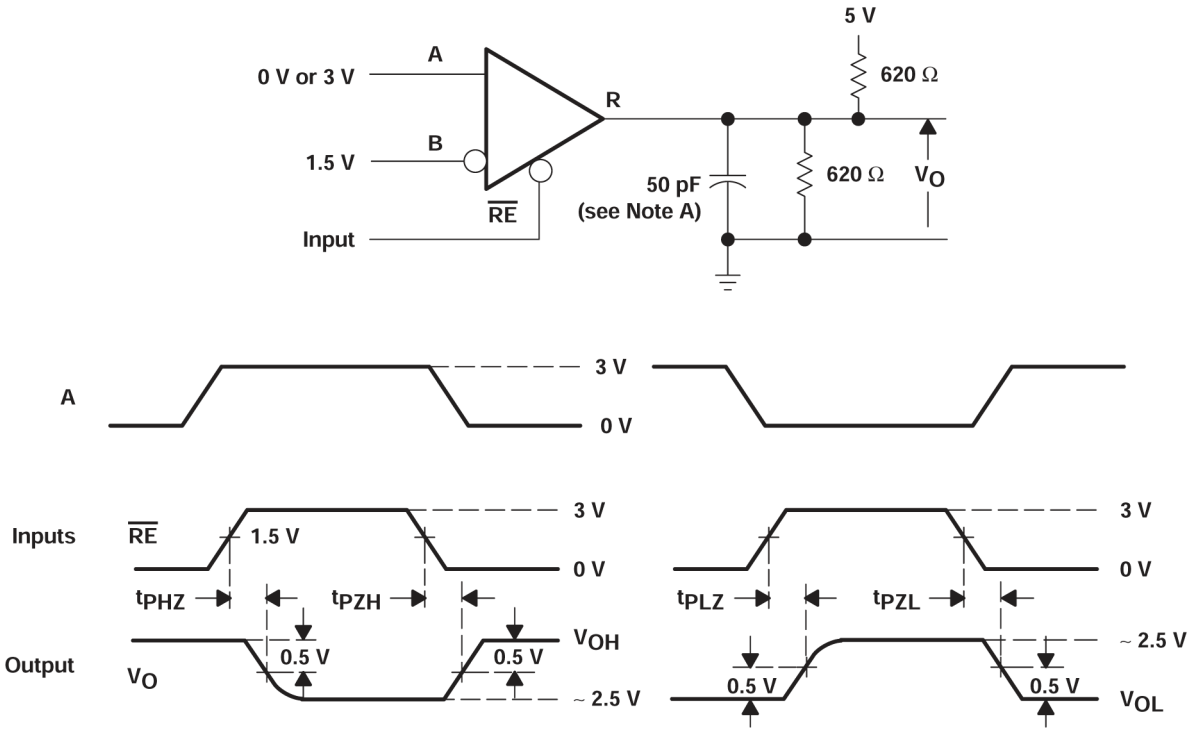
B. C_L includes probe and jig capacitance.

图 6-6. Driver T_{PZL} And T_{PLZ} Test Circuit and Voltage Waveforms



A. This value includes probe and jig capacitance (± 10%).

图 6-7. Receiver T_{PLH} And T_{PHL} Test Circuit and Voltage Waveforms

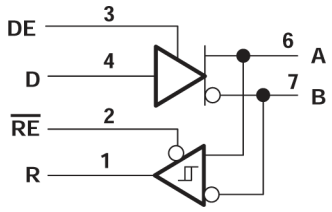


A. This value includes probe and jig capacitance (± 10%).

图 6-8. Receiver T_{PZL}, T_{PLZ}, T_{PZH}, And T_{PHZ} Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram



7.2 Device Functional Modes

表 7-1. Function Tables Driver

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

表 7-2. Function Tables Receiver

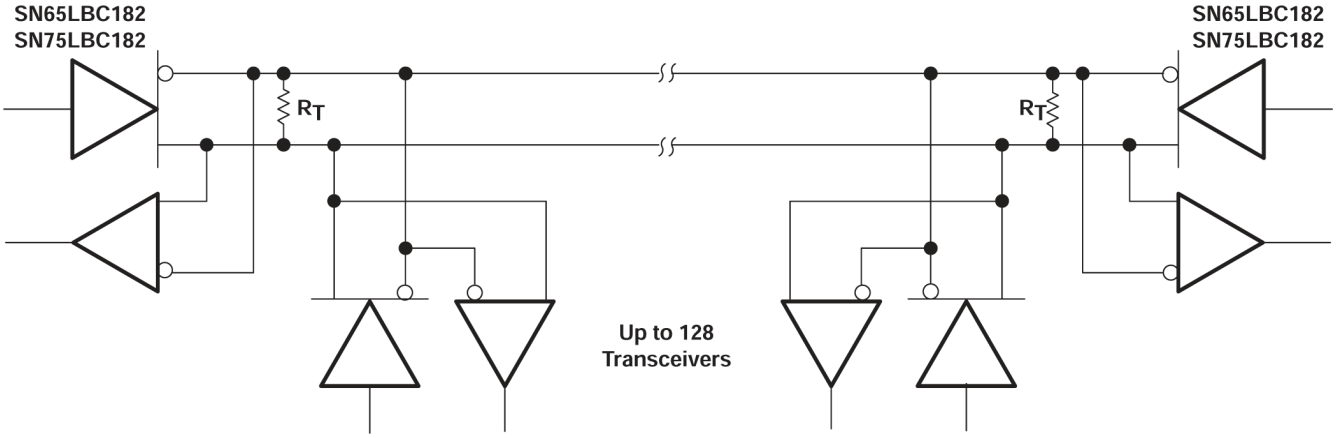
DIFFERENTIAL INPUTS	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geqslant$ 0.2 V	L	H
-0.2V < V_{ID} < 0.2 V	L	?
$V_{ID} \leqslant$ -0.2 V	L	L
X	H	Z
Open	L	H

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information



A. The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

图 8-1. Typical Application Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (March 2005) to Revision B (October 2023)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC182D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	6LB182	
SN65LBC182DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182	Samples
SN65LBC182DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB182	Samples
SN65LBC182P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC182	Samples
SN75LBC182DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB182	Samples
SN75LBC182P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	0 to 70	75LBC182	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

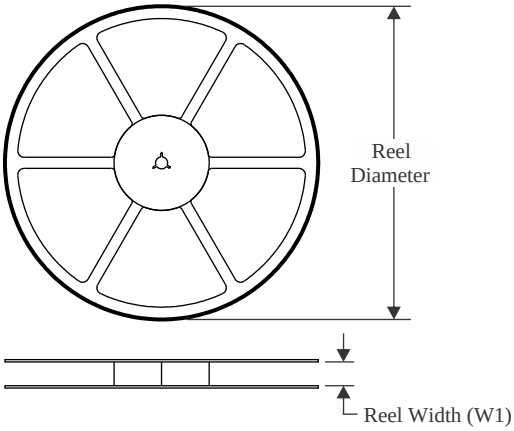
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

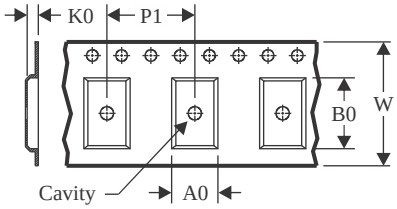
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

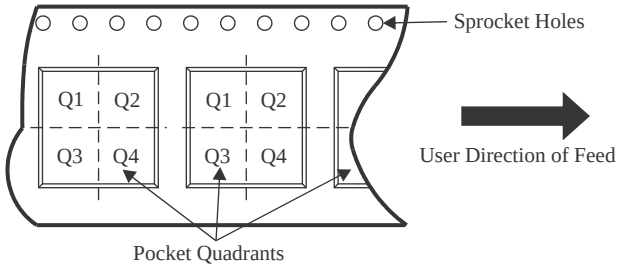


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

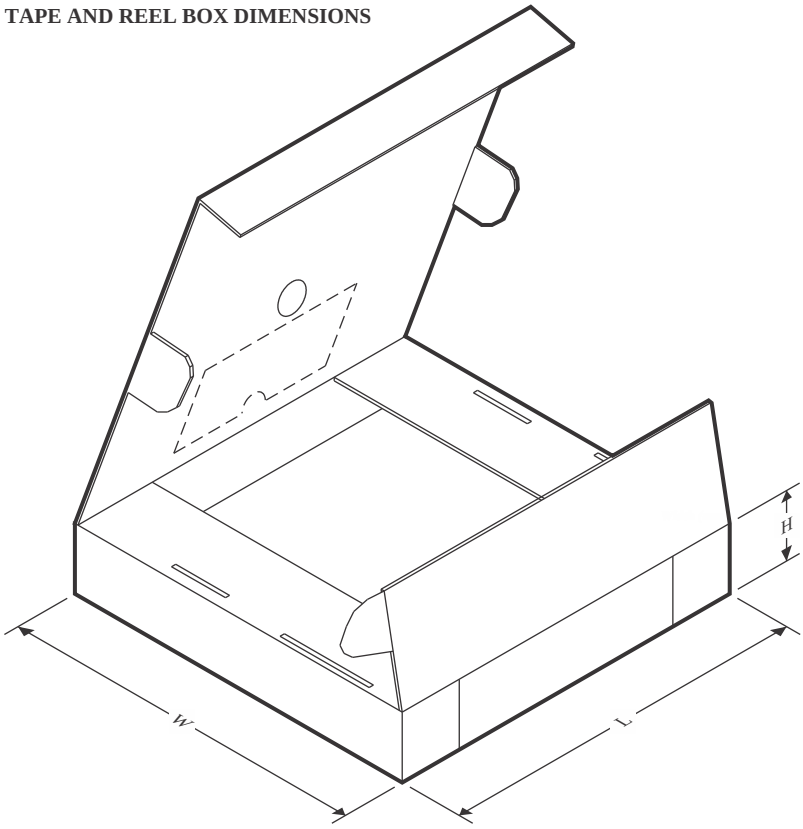
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC182DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

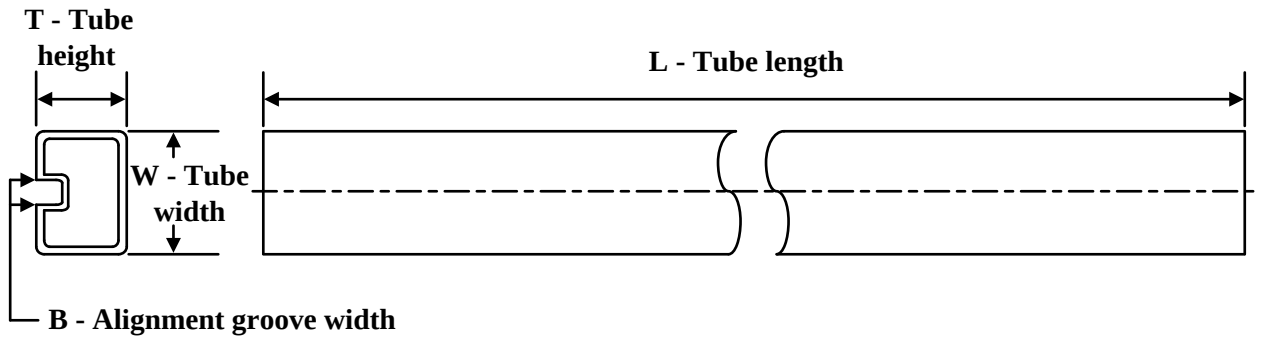
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

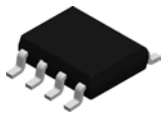
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC182DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65LBC182DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75LBC182DR	SOIC	D	8	2500	340.5	338.1	20.6
SN75LBC182DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC182D	D	SOIC	8	75	505.46	6.76	3810	4
SN65LBC182D	D	SOIC	8	75	507	8	3940	4.32
SN65LBC182P	P	PDIP	8	50	506	13.97	11230	4.32
SN75LBC182D	D	SOIC	8	75	507	8	3940	4.32
SN75LBC182DG4	D	SOIC	8	75	507	8	3940	4.32
SN75LBC182P	P	PDIP	8	50	506	13.97	11230	4.32

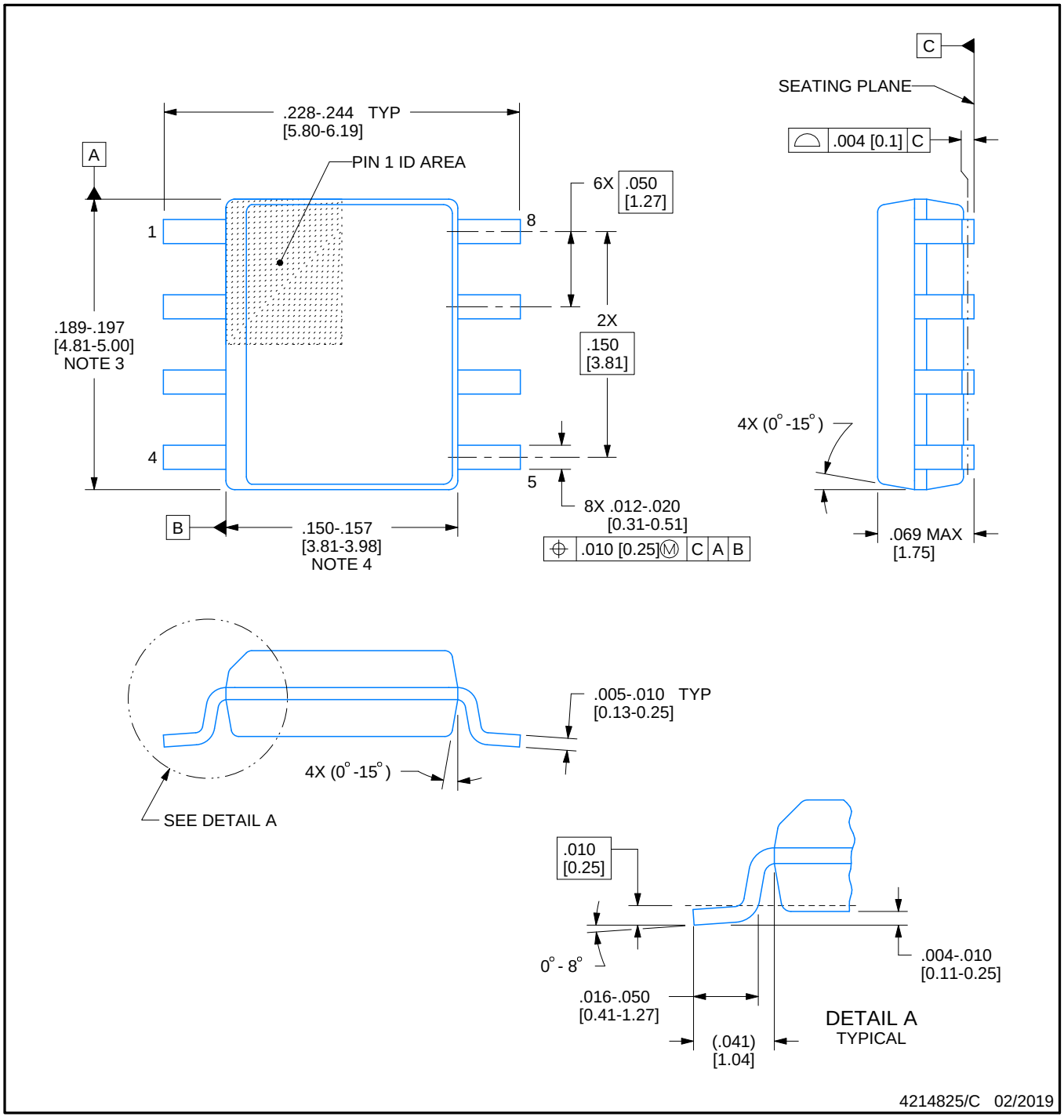


PACKAGE OUTLINE

D0008A

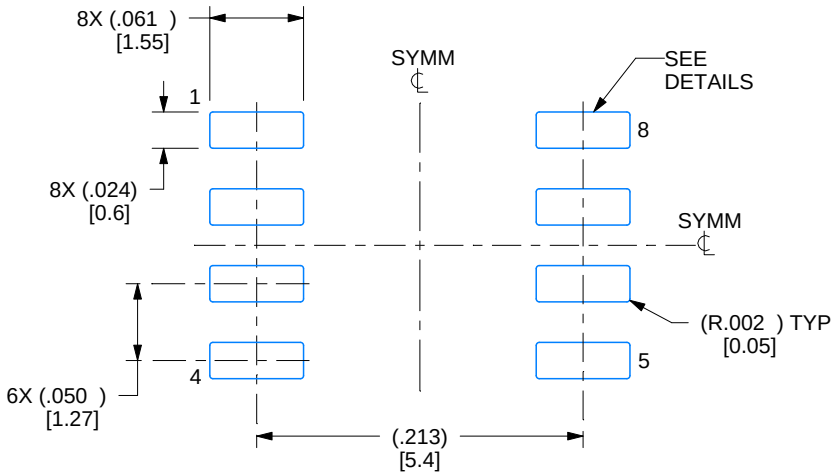
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

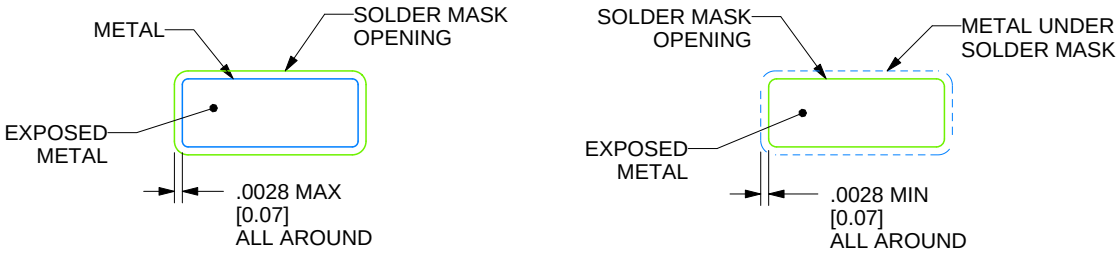


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

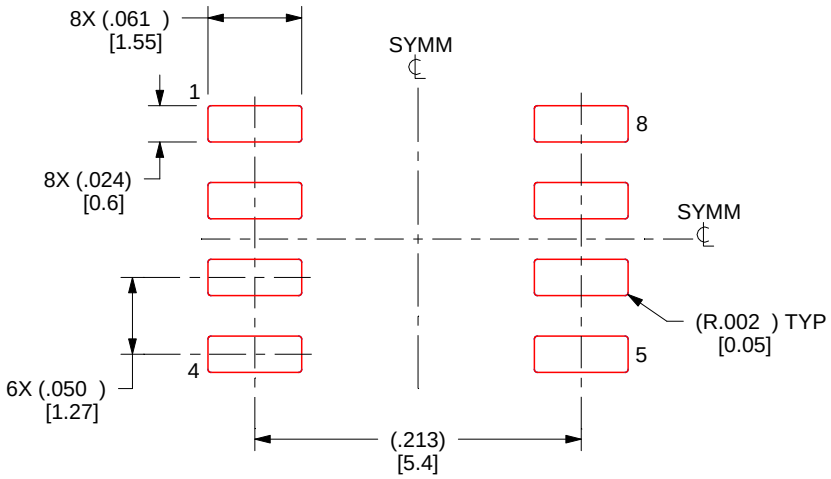
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



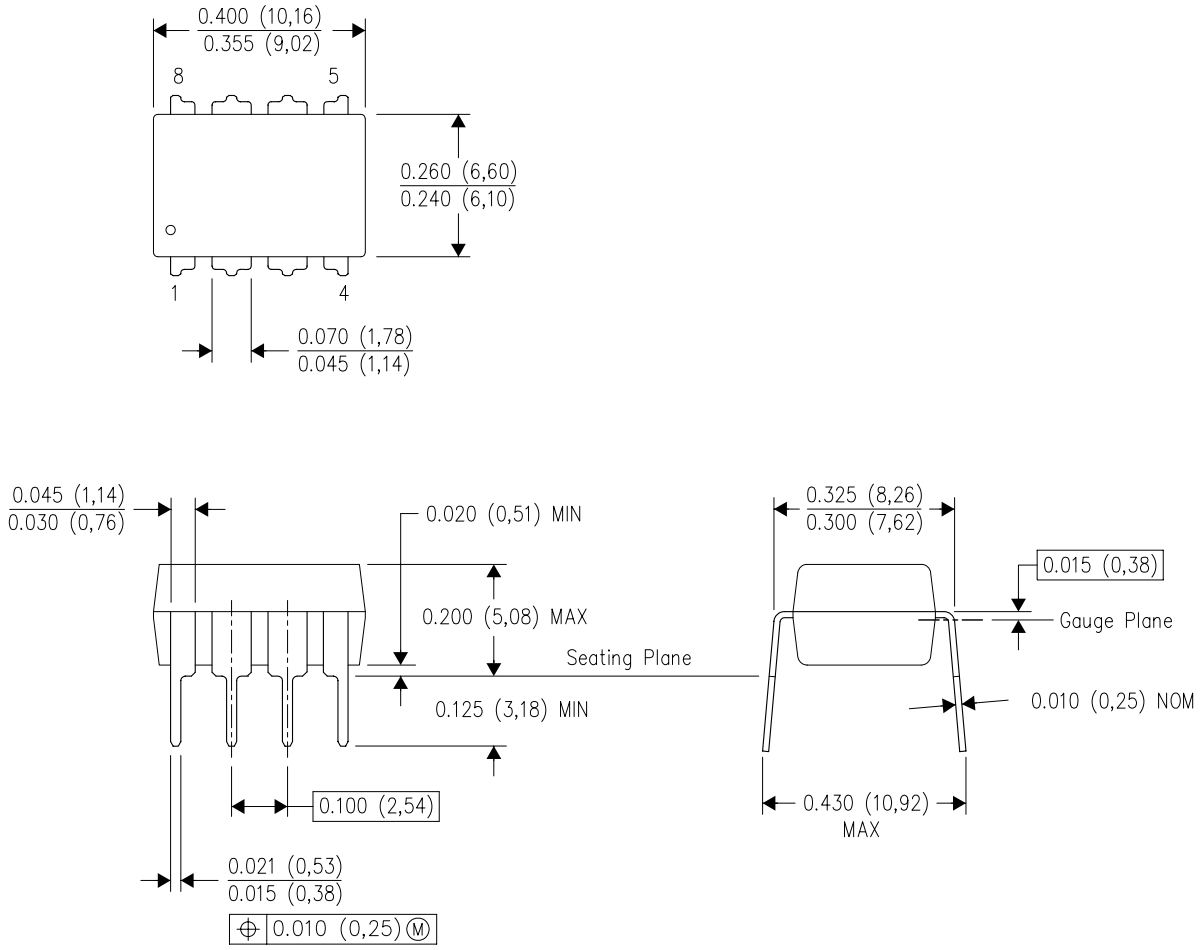
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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