14.2GBPS 双通道、双模线性均衡器

查询样品: **SN65LVCP1412**

特性

- 背板和线缆连接串行数据速率高达 **14.2Gbps** 的双通道、单向、多速率、双模线性均衡器
- 线性均衡增加了系统执行判决反馈均衡器 **(DFE)** 时的链路裕量
- 针对背板模式或者线缆模式，在具有 **1dB** 阶跃控制的 **7.1GHz** 上可实现 **18dB** 模拟均衡
- 输出线性动态范围：**1200mV**
- 带宽：**>20GHz -** 典型值
- **7.1GHz** 上，好于 **15dB** 的回波损耗
- 支持带外 **(OOB)** 信令
- 低功耗：**2.5V VCC** 时，每通道为 **75mW**（典型值）
- **24** 端子 **QFN**（四方扁平、无引线）
  4mm x 5mm x 0.75mm；**0.5mm** 端子间距

- 到 **100Ω** 差分印刷电路板 **(PCB)** 传输线路的出色阻抗匹配
- 通用输入输出接口 **(GPIO)** 或者 I²C 控制
- **2.5V** 和 **3.3V±5%** 单电源
- **2kV** 静电放电 **(ESD)** 人体模型 **(HBM)**
- 流经阳引脚的数据流简化了路由访问
- 小型封装尺寸节省了电路板空间

应用范围

- 电信和数据通信中的高速连接
- 针对 **10GbE，16GFC，10G SONET，SAS，SATA，CPRI，OBSAI，Infiniband，10GBase-KR**，和 **XFI/SFI** 的背板和线缆连接

说明

SN65LVCP1412 是一款异步、协议无关、低延迟、两通道线性均衡器，此均衡器针对高达 14.2Gbps 的数据速率和为背板或有源线缆应用中损耗的补偿进行了优化。 SN65LVCP1412 的架构设计用于与一个特定用途集成电路 (ASIC) 或者一个现场可编程栅极阵列 (FPGA)（采用判决反馈均衡器 (DFE) 来实现数字均衡）一起运行。 SN65LVCP1412 线性均衡器保持已发送信号的形状以确保最优 DFE 性能。 SN65LVCP1412 在充分发挥 DFE 效率的同时提供了一个低功耗的解决方案。

SN65LVCP1412 可经由 I²C 或者 GPIO 接口进行配置。 SN65LVCP1412 的 I²C 接口使得用户能够针对每个独立通道独立地控制均衡、路径增益和输出动态范围。 在 GPIO 模式下，通过使用 GPIO 输入引脚，可为所有通道设置均衡、路径增益、和输出动态范围。

SN65LVCP1412 输出可由 I²C 单独禁用。

SN65LVCP1412 在一个 2.5V 或者 3.3V 单电源下运行。

SN65LVCP1412 采用 24 引脚 4mm x 5mm x 0.75mm QFN（四方扁平无引线）无铅 0.5mm 焊球间距封装，额定运行温度 -40°C 至 85°C。

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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English Data Sheet: SLLSED2

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.
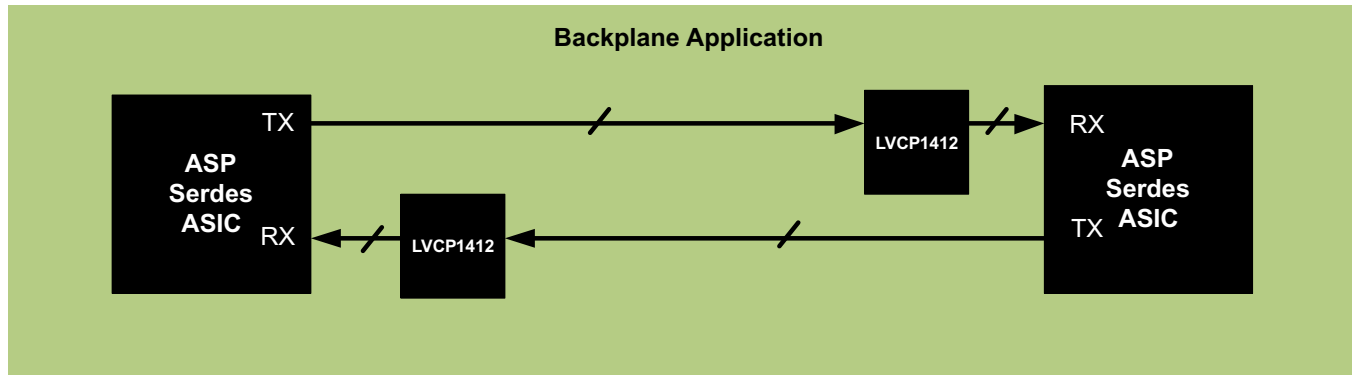
Backplane Application

Figure 1. Typical Backplane Application – Trace Mode
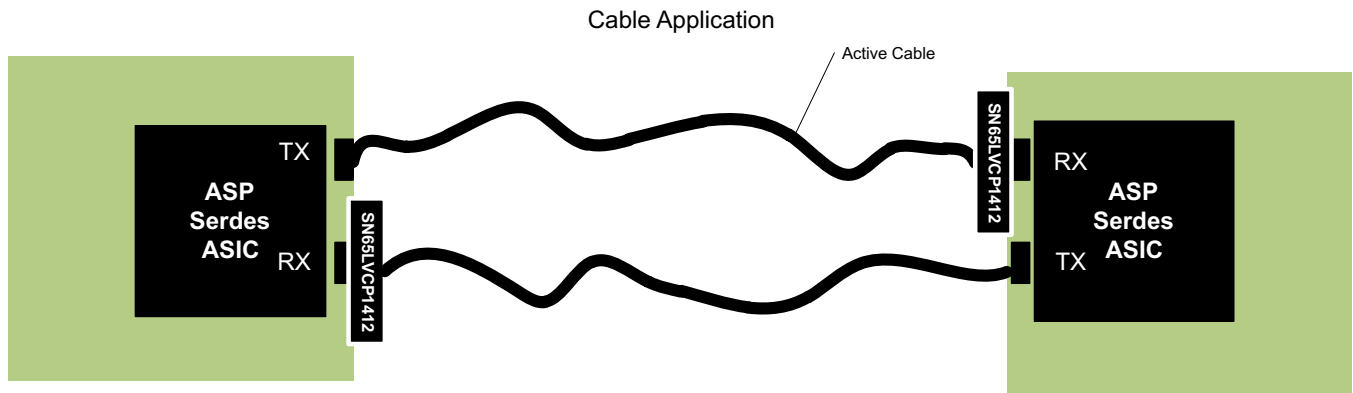
Cable Application

Figure 2. Typical Cable Application – Cable Mode

BLOCK DIAGRAM (GPIO or I²C Mode)

A simplified block diagram of the SN65LVCP1412 is shown in Figure 3 for GPIO or I²C input control mode. This compact, low power, 14.2Gbps daul-channel dual-mode linear analog equalizer consists of two high-speed data paths and an input GPIO pin logic-control block and a two-wire interface with a control-logic block.
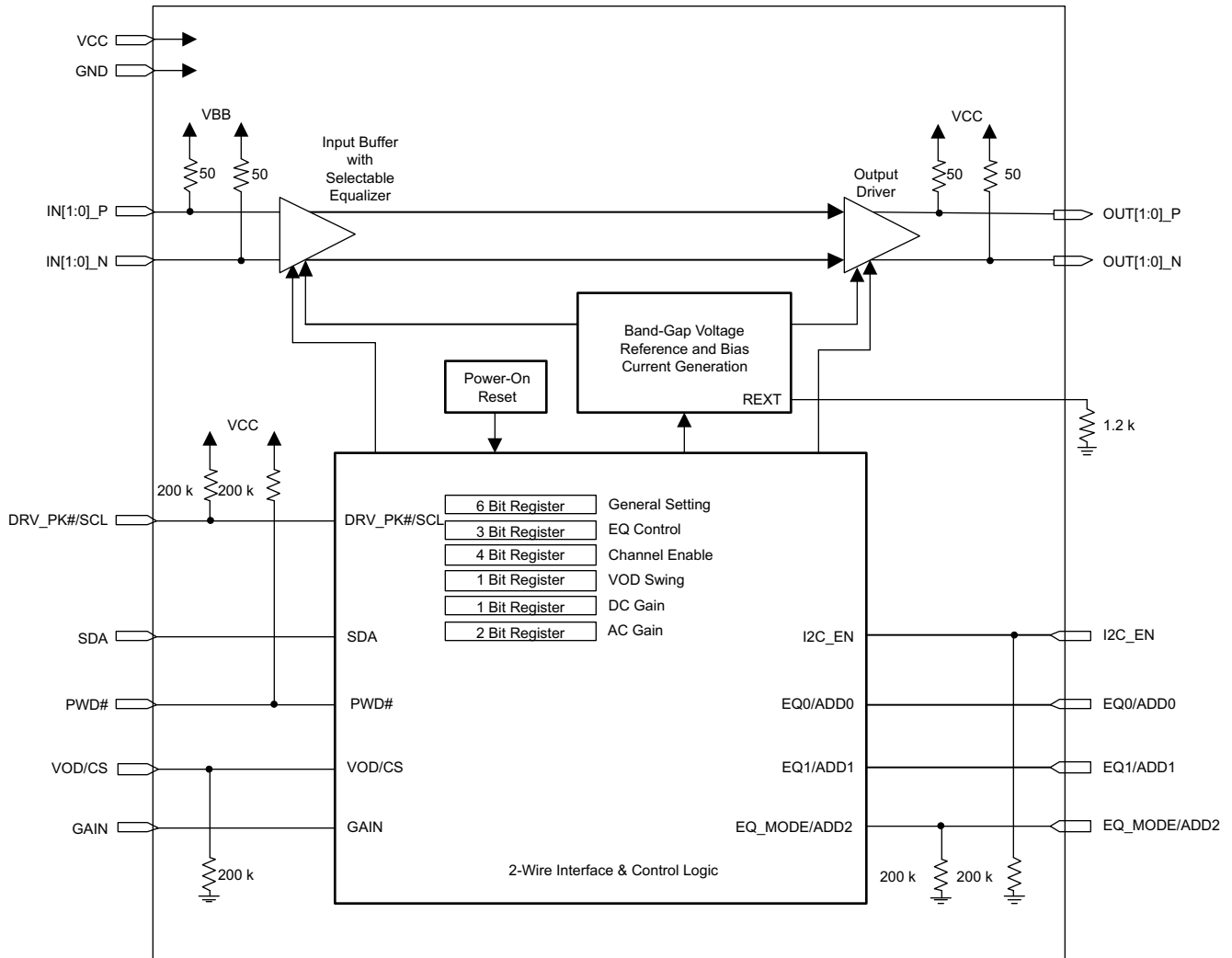

Figure 3. Simplified Block Diagram of the SN65LVCP1412

PACKAGE

The package pin locations and assignments are shown in Figure 4. The SN65LVCP1412 is packaged in a 4mm x 5mm x 0.75mm, 24 pin, 0.5mm pitch lead-free QFN.
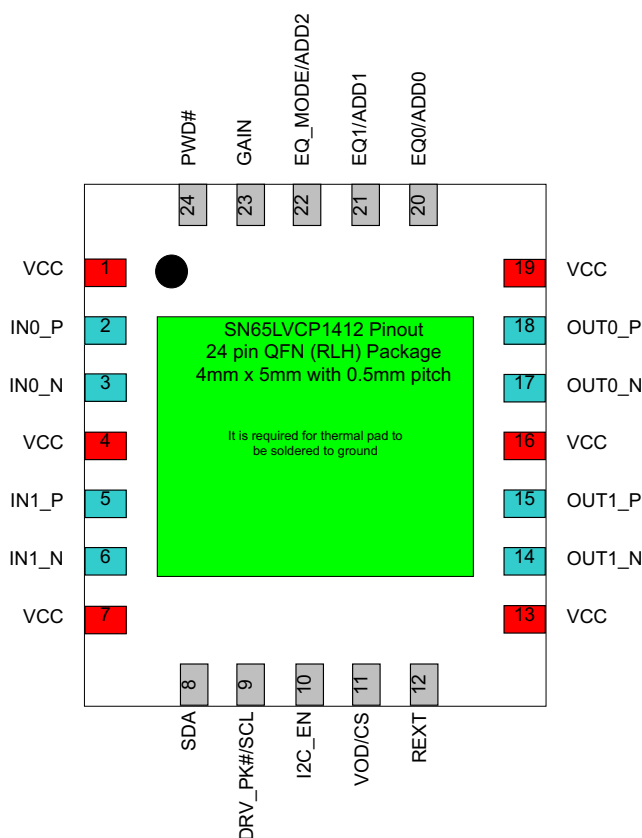

Figure 4. Package Drawing (Top View)

PIN DESCRIPTIONS

PINS		DIRECTION TYPE SUPPLY	DESCRIPTION	
NAME	NO.			
DIFFERENTIAL HIGH-SPEED I/O				
IN0_P IN0_N	2 3	Input, (with 50 Ω termination to input common mode)	Differential input, lane 0	
IN1_P IN1_N	5 6	Input, (with 50 Ω termination to input common mode)	Differential input, lane 1	
OUT0_P OUT0_N	18 17	Output	Differential output, lane 0	
OUT1_P OUT1_N	15 14	Output	Differential output, lane 1	
CONTROL SIGNALS				
SDA	8	Input Output, Open drain	**GPIO mode** No action needed	**I²C mode** I²C data. Connect a 10kΩ pull-up resistor externally
DRV_PK#/SCL	9	Input. (with 200kΩ pull-up)	**GPIO mode** HIGH: disable Driver peaking LOW: enables Driver 6dB AC peaking	**I²C mode** I²C clock. Connect a 10kΩ pull-up resistor externally
I2C_EN	10	Input, (wtih 200kΩ pull-down) 2.5V/3.3V CMOS	Configures the device operation for I²C or GPIO mode: HIGH: enables I²C mode LOW: enables GPIO mode	

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PIN DESCRIPTIONS (continued)

PINS		DIRECTION TYPE	DESCRIPTION		
NAME	NO.	SUPPLY			
VOD/CS	11	Input, (with 200kΩ pull-down) 2.5V/3.3V CMOS	**GPIO mode** HIGH: set high VOD range LOW: set low VOD range		**I²C mode** HIGH: acts as Chip Select LOW: disables I²C interface
REXT	12	Input, Analog	External Bias Resistor: 1,200 Ω to GND		
EQ0/ADD0	20	Input, 2.5V/3.3V CMOS - 3-state	**GPIO mode** Working with EQ1 to determine input EQ gain.		**I²C mode** ADD0 along with pins ADD1 and ADD2 comprise the three bits of I²C slave address. ADD2:ADD1:ADD0:XXX
EQ1/ADD1	21	Input, 2.5V/3.3V CMOS - 3-state	**GPIO mode** Working with EQ0 to determine input EQ gain steps of approximately 2dB		**I²C mode** ADD1 along with pins ADD0 and ADD2 comprise the three bits of I²C slave address ADD2:ADD1:ADD0:XXX

EQ1	EQ0	EQ GAIN
GND	GND	000
GND	HiZ	000
GND	VCC	001
HiZ	GND	010
HiZ	HiZ	011
HiZ	VCC	100
VCC	GND	101
VCC	HiZ	110
VCC	VCC	111

EQ1 and EQ0 work with AC_GAIN and DC_GAIN to determine final EQ gain as this:

EQ1/ EQ0	GAIN	DC GAIN (dB)	EQ GAIN (dB)
000 ~ 111	LOW	-6	1 ~ 9
000 ~ 111	HiZ	-6	7 ~ 17
000 ~ 111	HIGH	0	1 ~ 9

PINS		DIRECTION TYPE	DESCRIPTION		
EQ_MODE/ ADD2	22	Input, (with 200kΩ pull-down), 2.5V/3.3V CMOS	**GPIO mode** HIGH: Trace mode LOW: Cable mode		**I²C mode** ADD2 along with pins ADD1 and ADD0 comprise the three bits of I²C slave address. ADD2:ADD1:ADD0:XXX
GAIN	23	Input, 2.5V/3.3V CMOS - 3-state	**GPIO mode** Work with EQ1/EQ0 to set total EQ Gain. See table above.		**I²C mode** No action needed
PWD#	24	Input, (with 200kΩ pull-up), 2.5V/3.3V CMOS	HIGH: Normal Operation LOW: Powers down the device, inputs off and outputs disabled, resets I²C		
POWER SUPPLY					
VCC	1, 4, 7, 13, 16, 19	Power	Power supply 2.5V±5%, 3.3V±5%		
GND Center Pad		Ground	The ground center pad is the metal contact at the bottom of the package. This pad must be connected to the GND plane. At least 9 PCB vias are recommended to minimize inductance and provide a solid ground. Refer to the package drawing (RLH-package) for the via placement.		

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

		VALUES	UNIT
V_{CC}	Supply voltage range[2]	−0.3 to 4	V
$V_{IN,DIFF}$	Differential Voltage between INx_P and INx_N	±2.5	V
$V_{IN+, IN−}$	Voltage at Inx_P and fINx_N	−0.5 V to VCC+0.5	V
V_{IO}	Voltage on Control IO pins	−0.5 V to VCC+0.5	V
I_{IN+} $I_{IN−}$	Continuous Current at high speed differential data inputs (differential)	−25 to 25	mA
I_{OUT+} $I_{OUT−}$	Continuous Current at high speed differential data outputs	−25 to 25	mA
ESD	Human Body Model[3] (All Pins)	2.0	kV
	Charged-Device Model[4] (All Pins)	500	V
Moisture Sensitivity level		2	
Shelf Life Conditions In Moisture Barrier Bag		24 Months at <40ºC and <90% Humidity	
Reflow Temperature package soldering, 4 sec		260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

THERMAL INFORMATION

THERMAL METRIC[1]		SN65LVCP1412	UNITS
		RLH (24 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance[2]	34.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	33.8	
θ_{JB}	Junction-to-board thermal resistance[4]	12.5	
ψ_{JT}	Junction-to-top characterization parameter[5]	0.50	
ψ_{JB}	Junction-to-board characterization parameter[6]	12.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	2.00	

(1) 有关传统和新的热度量的更多信息，请参阅IC 封装热度量应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， ψ_JT，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_JA。
(6) 结至电路板特征参数， ψ_JB，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中描述的程序从仿真数据中 提取出该参数以便获得 θ_JA。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
dR	Operating Data Rate			14.2	Gbps
V_{CC}	Supply voltage	2.375	2.5	2.625	V
V_{CC}	Supply voltage	3.135	3.3	3.465	V
TC	Junction temperature	−10		125	°C
TB	Maximum board temperature			85	°C
CMOS DC SPECIFICATIONS					
V_{IH}	High-level input voltage	0.8×V_{CC}			V
V_{MID}	Mid-level input voltage	V_{CC}×0.4		V_{CC}×0.6	V
V_{IL}	Low-level input voltage	−0.5		0.2×V_{CC}	V
PSNR BG	Bandgap Circuit PSNR	20			dB

ELECTRICAL CHARACTERISTICS (VCC 2.5V ±5%)

over operating free-air temperature range. All parameters are referenced to package pins. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
POWER CONSUMPTION						
PD_L	Device power dissipation	VOD = LOW at 2.5V VCC with all 4 channels active.		150	250	mW
PD_H	Device power dissipation	VOD = HIGH, at 2.5V VCC with all 4 channels active.		225	400	mW
PD_{OFF}	Device power with all 4 channels switched off	Refer to I²C section for device configuration. 2.5V VCC		5		mW

(1) All typical values are at 25°C and with 2.5V supply unless otherwise noted.

ELECTRICAL CHARACTERISTICS (VCC 3.3V ±5%)

over operating free-air temperature range. All parameters are referenced to package pins. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
POWER CONSUMPTION						
PD_L	Device power dissipation	VOD = LOW at 3.3V VCC with all 4 channels active.		225	375	mW
PD_H	Device power dissipation	VOD = HIGH, at 3.3V VCC with all 4 channels active.		330	525	mW
PD_{OFF}	Device power with all 4 channels switched off	Refer to I²C section for device configuration. 3.3V VCC		5		mW

(1) All typical values are at 25°C and with 2.5V supply unless otherwise noted.

ELECTRICAL CHARACTERISTICS (VCC 2.5V ±5%, 3.3V ±5%)

over operating free-air temperature range. All parameters are referenced to package pins. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
CMOS DC SPECIFICATIONS						
I_{IH}	High level input current	VIN = 0.9 × V_{CC}	-40	17	40	µA
I_{IL}	Low level input current	VIN = 0.1 × V_{CC}	-40	17	40	µA
CML INPUTS (IN[3:0]_P, IN[3:0]_N)						
r_{IN}	Differential input resistance	INx_P to INx_N		100		Ω
V_{IN}	Input linear dynamic range	Gain = 0.5		1200		mV_{pp}
V_{ICM}	Input common mode voltage	Internally biased		V_{CC}−0.8		V
SCD11	Input differential to common mode conversion	100MHz to 7.1GHz		−20		dB
SDD11	Differential input return loss	100MHz to 7.1GHz		−15		dB

(1) All typical values are at 25°C and with 2.5V and 3.3V supply unless otherwise noted.

ELECTRICAL CHARACTERISTICS (VCC 2.5V ±5%, 3.3V ±5%) (continued)

over operating free-air temperature range. All parameters are referenced to package pins. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
CML OUTPUTS (OUT[3:0]_P, OUT[3:0]_N)						
V_{OD}	Output linear dynamic range	R_L = 100 Ω, V_{OD} = HIGH		1200		mV_{pp}
		R_L = 100 Ω, V_{OD} = LOW		600		mV_{pp}
V_{OS}	Output offset voltage	R_L = 100 Ω, 0 V applied at inputs		10		mV_{pp}
V_{OCM}	Output common mode voltage	See Figure 5		V_{CC}-0.4		V
$V_{CM,RIP}$	Common mode output ripple	K28.5 pattern at 14.2Gbps on all 4 channels, no interconnect loss, VOD = HIGH		10	20	mV_{RMS}
$V_{OD,RIP}$	Differential path output ripple	K28.5 pattern at 14.2Gbps on all channels, no interconnect loss, VIN = 1200mVpp.			20	mV_{pp}
$V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states				±10	mV
t_R	Rise time[2]	Input signal with 30ps rise time. 20% to 80%. See Figure 7		31		ps
t_F	Fall time[2]	Input signal with 30ps fall time. 20% to 80%. See Figure 7		32		ps
SDD22	Differential output return loss	100MHz to 7.1GHz		−15		dB
SCC22	Common-mode output return loss	100MHz to 7.1GHz		−8		dB
t_{PLH}	Low-to-high propagation delay	See Figure 6		65		ps
t_{PHL}	High-to-low propagation delay			65		ps
$t_{SK(O)}$	Inter-Pair (lane to lane) output skew[3]	All outputs terminated with 100 Ω, See Figure 8		3		ps
$t_{SK(PP)}$	Part-to-part skew[4]	All outputs terminated with 100 Ω			50	ps
r_{OT}	Single ended output resistance	Single ended on-chip termination to VCC. Outputs will be AC coupled.		50		Ω
r_{OM}	Output termination mismatch at 1MHz	$\Delta rom = 2 \times \dfrac{rp - rn}{rp + rn} \times 100$		5		%
Ch_{iso}	Channel-to-channel isolation	Frequency at 7.1GHz	35	45		dB
OUT_{NOISE}	Output referred noise[5]	10MHz to 7.1GHz. No other noise source present. VOD = LOW		400		µVRMS
		10MHz to 7.1GHz. No other noise source present. VOD = HIGH		500		µVRMS
EQUALIZATION						
EQ_{Gain}	At 7.1GHz input signal	Equalization Gain, EQ = MAX	15	18		dB
Vpre	Output pre-cursor pre-emphasis	Input signal with 3.75 pre-cursor and measure it on the output signal, Refer Figure 9. Vpre = 20log(V3/V2)		3.75		dB
Vpst	Output post-cursor pre-emphasis	Input signal with 12dB post-cursor and measure it on the output signal, Refer Figure 9. Vpst = 20log(V1/V2)		12		dB
DJ1	Residual deterministic jitter at 10.3125 Gbps	Transmit Side application Tx launch Amplitude = 0.6Vpp, EQ=0, ACGain and DCgain = Low and VOD = High, Trace Mode Test Channel -> 0". See Figure 11		0.016		UIp-p
DJ2	Residual deterministic jitter at 10.3125 Gbps	Receive Side Application Tx launch Amplitude = 0.6Vpp, EQ=7, ACGain and VOD = High and DCGain = High, Trace Mode Test Channel -> 12" (9dB loss at 5GHz) See Figure 10		0.11		UIp-p
DJ3	Residual Deterministic Jitter at 14.2 Gbps	Transmit Side Application Tx launch Amplitude = 0.6Vpp, EQ=0, ACGain and DCgain = Low and VOD = High, Trace Mode Test Channel -> 0". See Figure 11		0.041		UIp-p
DJ4	Residual Deterministic Jitter at 14.2 Gbps	Receive Side Application Tx launch Amplitude = 0.6Vpp, EQ=7, ACGain and VOD = High and DCGain = High, Trace Mode Test Channel -> 8" (9dB loss at 7GHz) See Figure 10		0.13		UIp-p

(2) Rise and Fall measurements include board and channel effects of the test environment, refer to Figure 10 and Figure 11
(3) $t_{SK(O)}$ is the magnitude of the time difference between the channels.
(4) $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
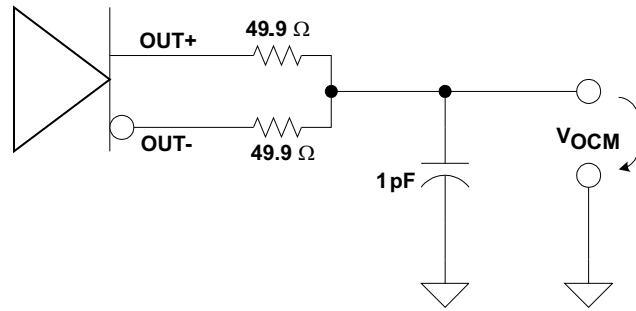(5) All noise sources added.

PARAMETER MEASUREMENT INFORMATION

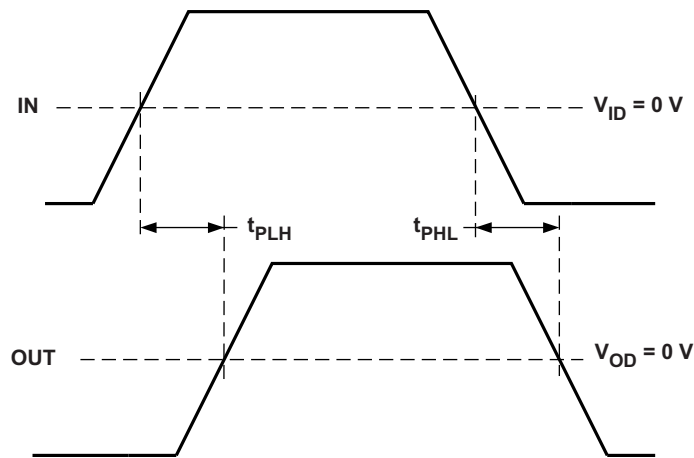**Figure 5. Common Mode Output Voltage Test Circuit**
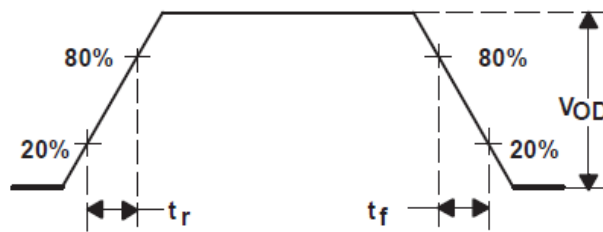

Figure 6. Propagation Delay Input to Output
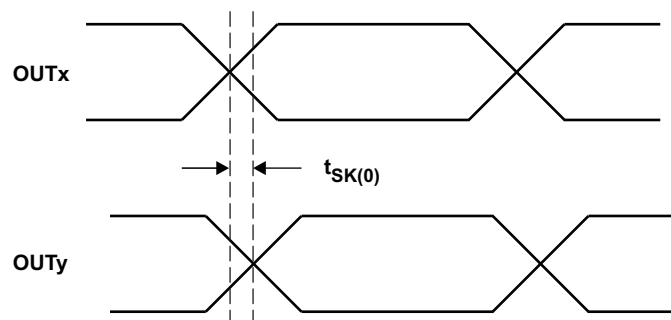

Figure 7. Output Rise and Fall Time

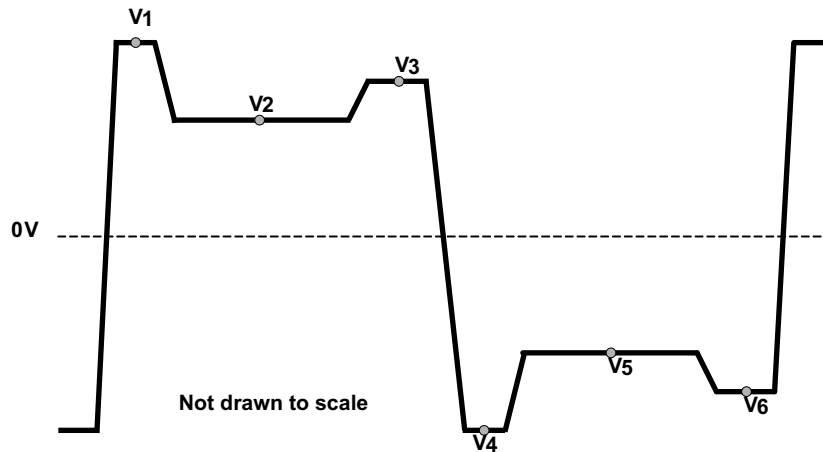**Figure 8. Output Inter-Pair Skew**

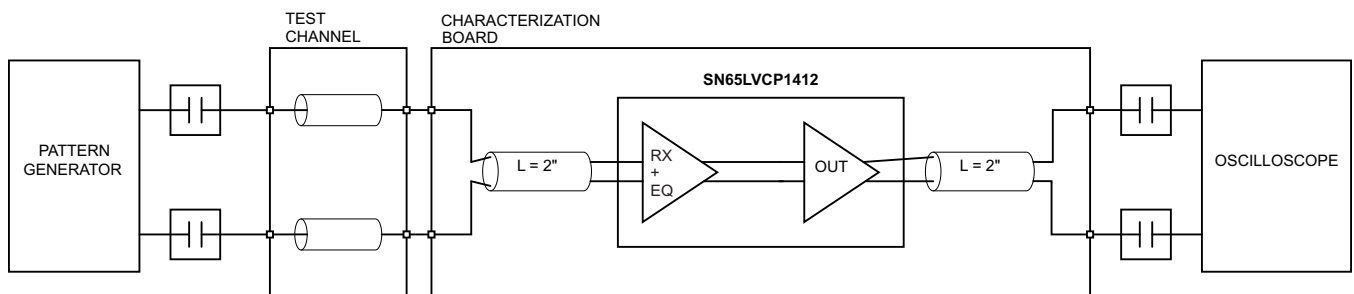**Figure 9. Vpre and Vpost (The test pattern is 1111111100000000 (8-1s, 8-0s))**

Figure 10. Receive Side Performance Test Circuit
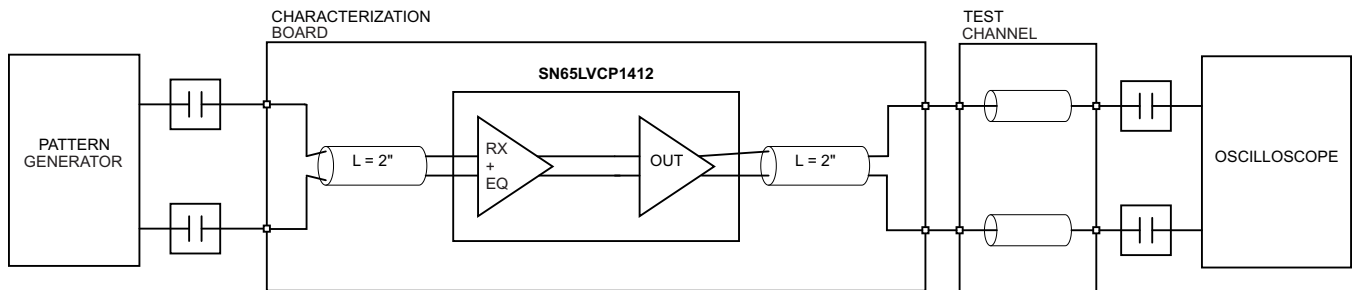
Figure 11. Transmit Side Performance Test Circuit

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS
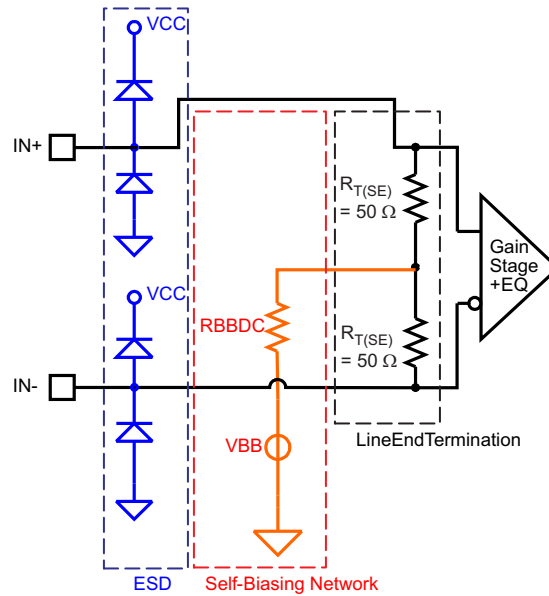
Figure 12. Equivalent Input Circuit Design
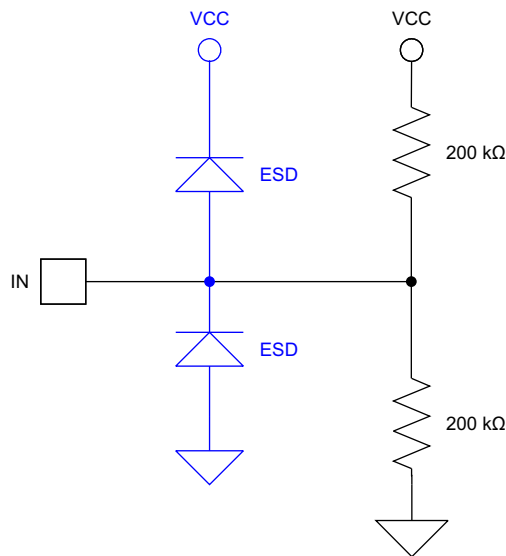
Figure 13. 3-Level Input Biasing Network

TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 2.5V and T_A = 25°C, no interconnect line at the output, and with default device settings (unless otherwise noted).
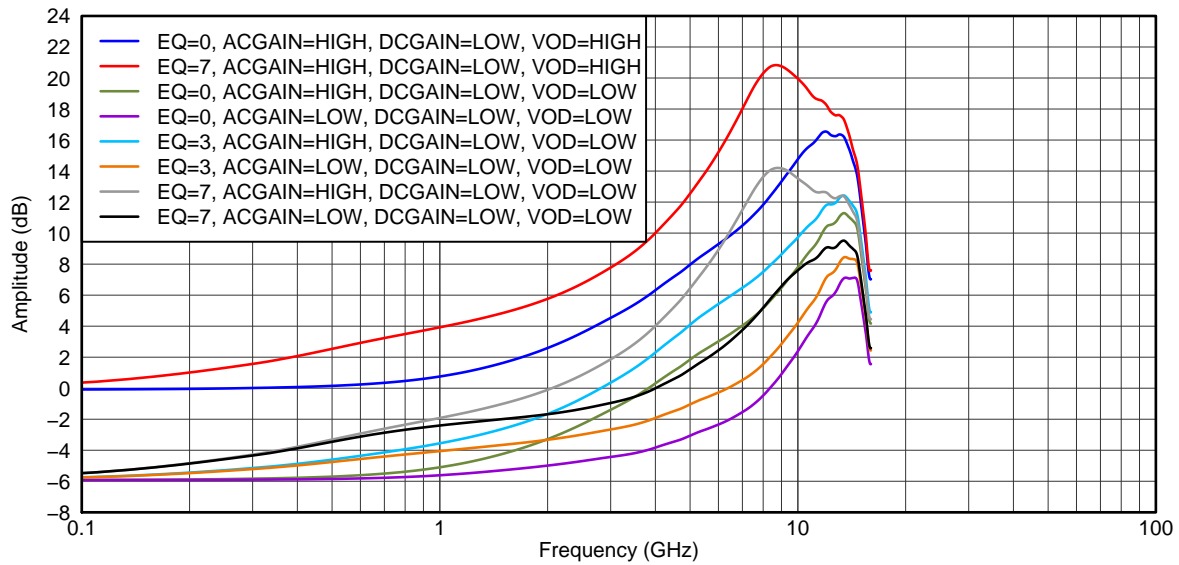
Figure 14. Typical EQ Gain Profile Curve
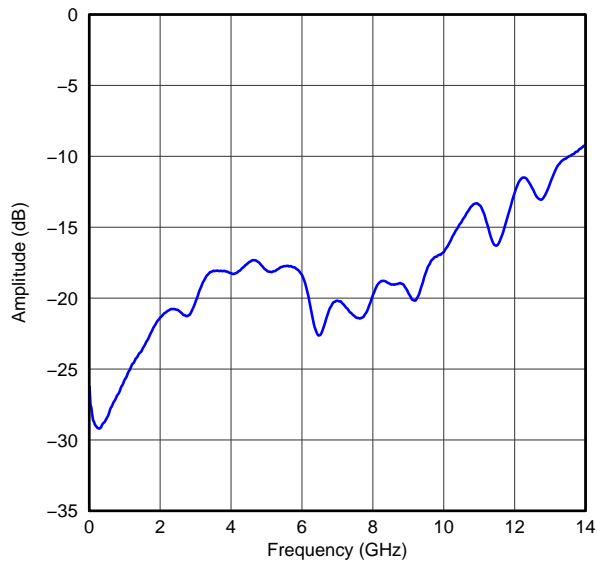
Figure 15. Differential Input Return Loss
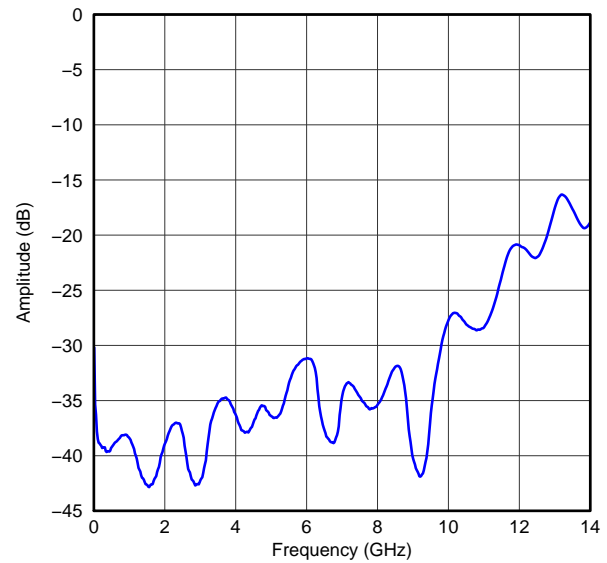
Figure 16. Differential to Common Mode Conversion

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 2.5V and T_A = 25°C, no interconnect line at the output, and with default device settings (unless otherwise noted).

Figure 17. Differential Output Return Loss
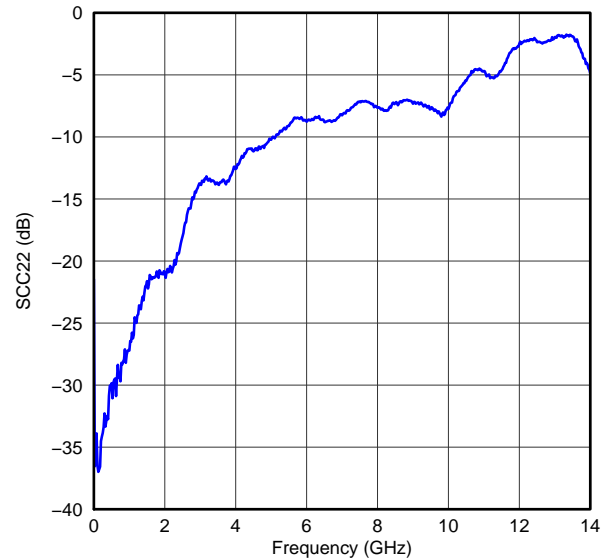
Figure 18. Common Mode Output Return Loss

A. With SN65LVCP1412 -> EQ = 4, VOD = High, ACGain = HiZ, DCGain = Low
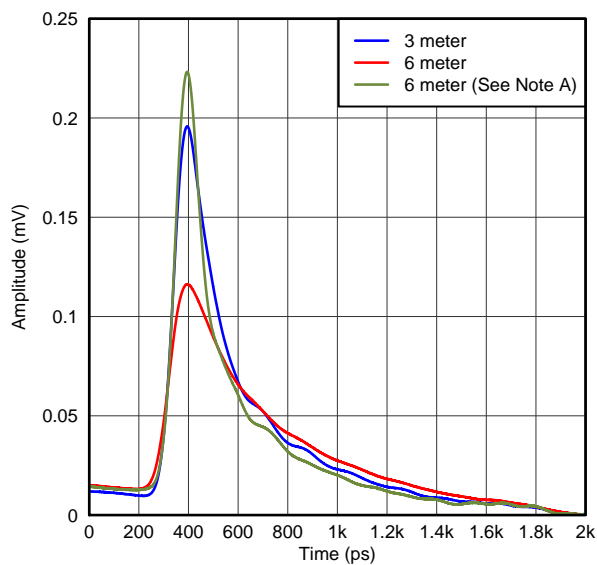
Figure 19. Cable Mode – Symbol Response

A. With SN65LVCP1412 -> EQ = 4, VOD = High, ACGain = HiZ, DCGain = Low
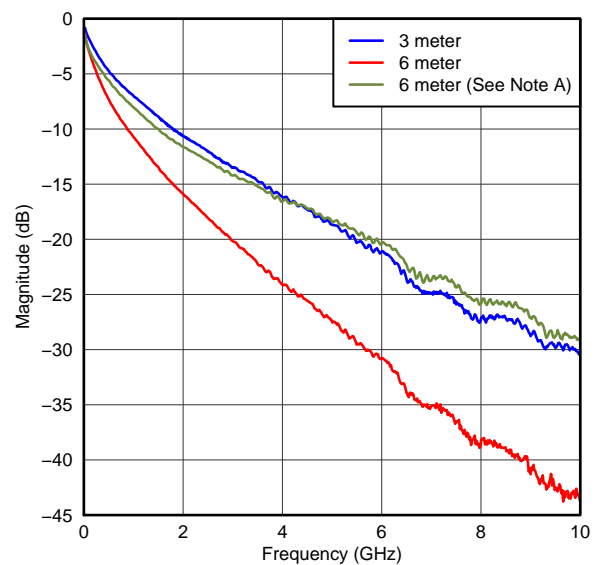
Figure 20. Cable Mode – Frequency Domain

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 2.5V and T_A = 25°C, no interconnect line at the output, and with default device settings (unless otherwise noted).
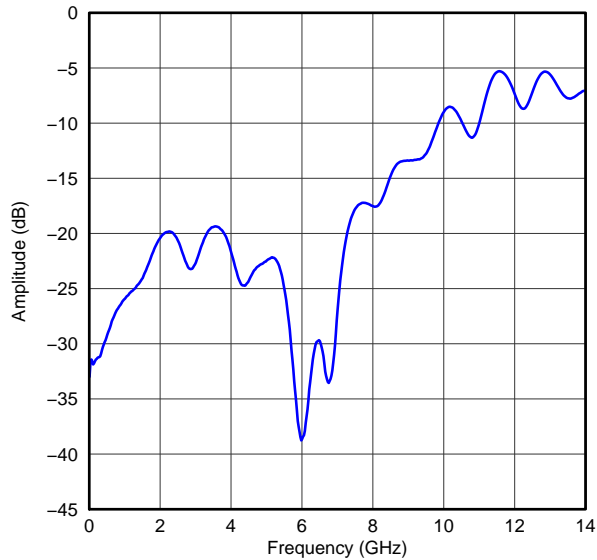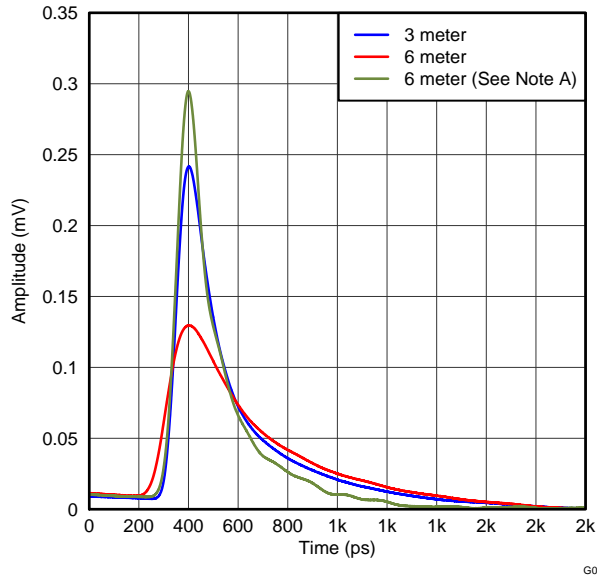

A. With SN65LVCP1412 -> EQ = 7, VOD = High, ACGain = High, DCGain = Low

Figure 21. Trace Mode – Symbol Response
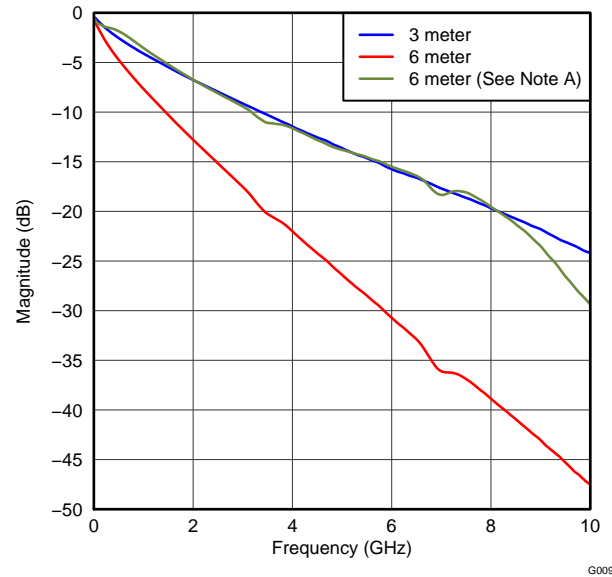
A. With SN65LVCP1412 -> EQ = 7, VOD = High, ACGain = High, DCGain = Low

Figure 22. Trace Mode - Frequency Domain

Table 1. Control Settings Descriptions

MODE	DCGAIN	ACGAIN<1:0>	EQ<2:0>	DC GAIN (dB)	EQ GAIN (dB)	APPLICATION
0	0	00	000 to 111	−6	1 to 9	Short Input Trace; Large Input Swing
0	0	11	000 to 111	−6	7 to 17	Long Input Trace; Large Input Swing
0	1	01	000 to 111	0	1 to 9	Short Input Trace; Small Input Swing
0	1	11	000 to 111	0	2 to 10	Short Input Trace; Small Input Swing
1	0	00	000 to 111	−6	1 to 9	Short Input Cable; Large Input Swing
1	0	11	000 to 111	−6	7 to 17	Long Input Cable; Large Input Swing
1	1	01	000 to 111	0	1 to 9	Short Input Cable; Small Input Swing
1	1	11	000 to 111	0	2 to 10	Short Input Cable; Small Input Swing

Table 2. Control Settings Descriptions

GAIN	DC GAIN	ACGAIN<1:0>
Low	0	00
HighZ	0	11
High	1	01

TWO-WIRE SERIAL INTERFACE AND CONTROL LOGIC

The SN65LVCP1412 uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCL, are driven, respectively, by the serial data and serial clock from a microcontroller, for example. The SDA and SCK pins require external 10kΩ pull-ups to VCC.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out control and status signals. The SN65LVCP1412 is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7 bit slave address (0000ADD[2:0]) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ. The ADD[2:0] address bits change with the status of the ADD2, ADD1, and ADD0 device pins, respectively. If the pins are left floating or pulled down, the 7 bit slave address is 0000000.
3. 8 bit register address
4. 8 bit register data word
5. STOP command

Regarding timing, the SN65LVCP1412 is I^{2}C compatible. The typical timing is shown in Figure 9 and a complete data transfer is shown in Figure 10. Parameters for Figure 9 are defined in Table 3.

Bus Idle: Both SDA and SCL lines remain HIGH

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.
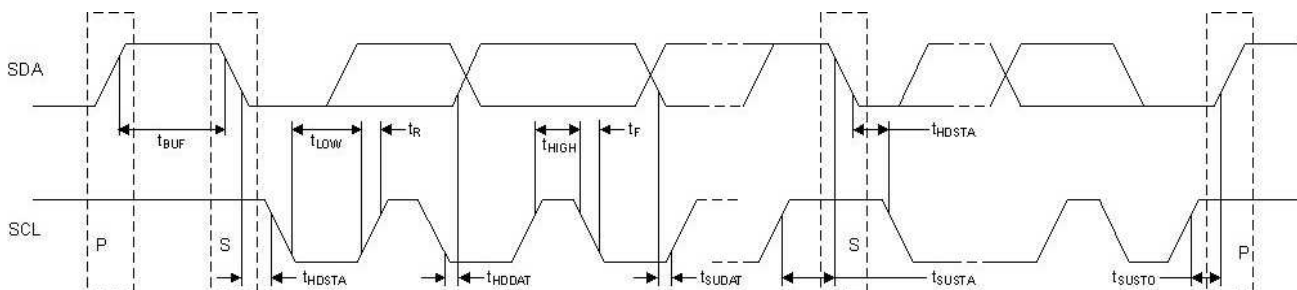
Figure 23. Two-wire Serial Interface Timing Diagram

Table 3. Two-Wire Serial Interface Timing Diagram Definitions

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency		400	kHz
t_{BUF}	Bus free time between START and STOP conditions	1.3		µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.6		µs
t_{LOW}	Low period of the SCL clock	1.3		µs
t_{HIGH}	High period of the SCL clock	0.6		µs
t_{SUSTA}	Setup time for a repeated START condition	0.6		µs
t_{HDDAT}	Data HOLD time	0		µs
t_{SUDAT}	Data setup time	100		ns
t_R	Rise time of both SDA and SCL signals		300	ns
t_F	Fall time of both SDA and SCL signals		300	ns
t_{SUSTO}	Setup time for STOP condition	0.6		µs
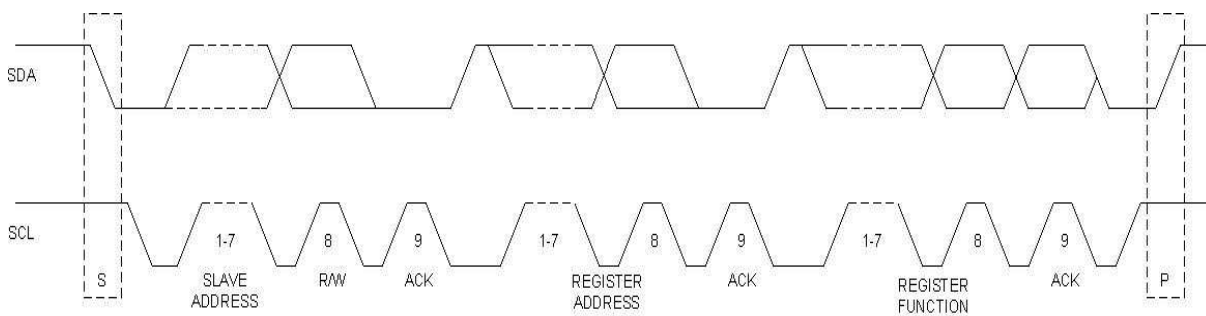
Figure 24. Two-wire Serial Interface Data Transfer

REGISTER MAPPING

The register mapping for read/write register addresses 0 (0x00) through 22 (0x18) are shown in Table 4. Table 5 describes the circuit functionality based on the register settings.

Table 4. SN65LVCP1412 Register Mapping Information

Register 0x00 (General Device Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	PWRDOWN	SYNC_01	RSVD	SYNC_ALL	EQ_MODE		RSVD

Register 0x01 (Channel Enable) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
					LN_EN_CH1	LN_EN_CH0	

Register 0x05 (Channel 0 Control Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	EQ2	EQ1	EQ0	VOD_CTRL	DC_GAIN	AC_GAIN1	AC_GAIN0

Register 0x06 (Channel 0 Enable Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
					DRV_PEAK	EQ_EN	DRV_EN

Register 0x08 (Channel 1 Control Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	EQ2	EQ1	EQ0	VOD_CTRL	DC_GAIN	AC_GAIN1	AC_GAIN0

Register 0x09 (Channel 1 Enable Settings) R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
					DRV_PEAK	EQ_EN	DRV_EN

Register 0x0F Read Only							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Register 0x11 R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	RSVD						

Register 0x12 R/W							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RSVD							

Table 5. SN65LVCP1412 Register Description

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x00	7	RSVD	Fot TI use only	00000000
	6	PWRDOWN	Power down the device: 0 = Normal operation 1 = Powerdown	
	5	SYNC_01	All settings from channel 1 will be used for channel 0 and 1: 0 = channel 0 tracking channel 1 settings 1 = no tracking tracking	
	4	RSVD	For TI use only	
	3	SYNC_ALL	All settings from channel 1 will be used on all channels: 0 = all channels tracking channel 1 1 = no channel tracking Overwrites SYNC_01	
	2	EQ_MD	Set EQ Mode: 0 = Cable Mode 1 = Trace Mode	
	1			
	0	RSVD	For TI use only	

Table 5. SN65LVCP1412 Register Description (continued)

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x01	7			00000000
	6			
	5			
	4			
	3			
	2	LN_EN_CH1	Channel 1 Enable: 0 = Enable 1 = Disable	
	1	LN_EN_CH0	Channel 0 Enable: 0 = Enable 1 = Disable	
	0			
0x05 0x08	7	RSVD		00000000
	6	EQ2	Equalizer Adjustment Setting 000 = Minimum equalization setting 111 = Maximum equalization setting	
	5	EQ1		
	4	EQ0		
	3	VOD_CTRL	Channel [x] VOD control: 0 = low VOD range 1 = high VOD range	
	2	DC_GAIN_CTRL	Channel [x] EQ DC Gain: 0 = set EQ DC Gain to 0.5x 1 = set EQ DC Gain to 1x	
	1	AC_GAIN_CTRL1	AC Gain Control: 00 = Low 01 = HiZ 11 = High	
	0	AC_GAIN_CTRL0		
0x06 0x09	7			00000000
	6			
	5			
	4			
	3			
	2	DRV_PEAK	Channel [x] Driver Peaking: 0 = disables driver Peaking 1 = enables driver 6db AC Peaking	
	1	EQ_EN	Channel [x] EQ stage enable: 0 = Enable 1 = Disable	
	0	DRV_EN	Channel [x] Driver stage enable: 0 = Enable 1 = Disable	
0x0F	7	RSVD	For TI use only	00110000
	6	RSVD	For TI use only	
	5	RSVD	For TI use only	
	4	RSVD	For TI use only	
	3	RSVD	For TI use only	
	2	RSVD	For TI use only	
	1	RSVD	For TI use only	
	0	RSVD	For TI use only	

Table 5. SN65LVCP1412 Register Description (continued)

REGISTER	BIT	SYMBOL	FUNCTION	DEFAULT
0x11	7			00000000
	6	RSVD	For TI use only	
	5			
	4			
	3			
	2			
	1			
	0			
0x12	7	RSVD	For TI use only	00000000
	6			
	5			
	4			
	3			
	2			
	1			
	0			

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVCP1412RLHR	Obsolete	Production	WQFN (RLH) | 24	-	-	Call TI	Call TI	-40 to 85	LVCP 1412
SN65LVCP1412RLHT	Obsolete	Production	WQFN (RLH) | 24	-	-	Call TI	Call TI	-40 to 85	LVCP 1412

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.
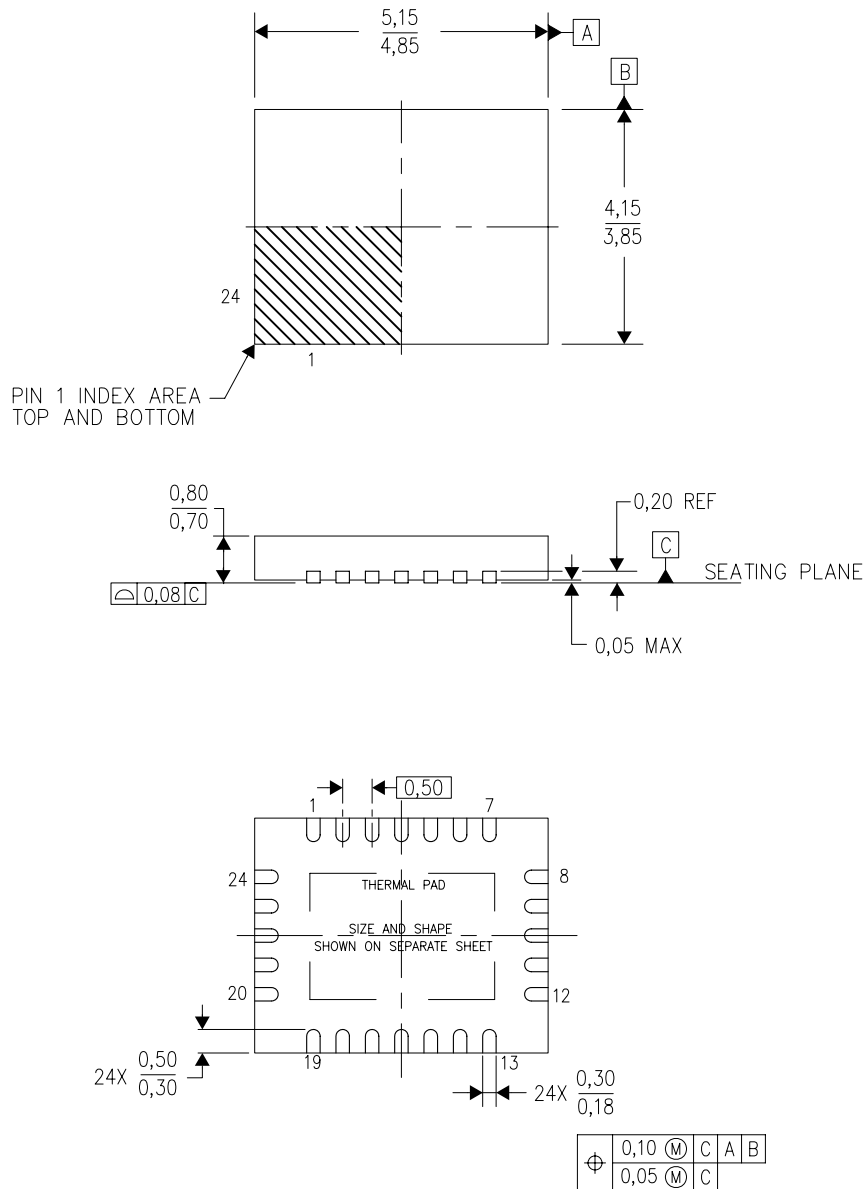
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RLH (R−PWQFN−N24)　　　　　PLASTIC QUAD FLATPACK NO−LEAD

5,15
4,85

A

B

4,15
3,85

24

1

PIN 1 INDEX AREA
TOP AND BOTTOM

0,80
0,70

0,20 REF

C

SEATING PLANE

0,08 C

0,05 MAX

0,50

1   7

24   8

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

20   12

19   13

24X 0,50
0,30

24X 0,30
0,18

⊕ 0,10 Ⓜ C A B
0,05 Ⓜ C

4212455/A 01/12

NOTES:　A.　All linear dimensions are in millimeters.　Dimensioning and tolerancing per ASME Y14.5M−1994.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　QFN (Quad Flatpack No−Lead) Package configuration.
　　　　　D.　The package thermal pad must be soldered to the board for thermal and mechanical performance.
　　　　　E.　See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
　　　　　F.　Falls within JEDEC MO−220.

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