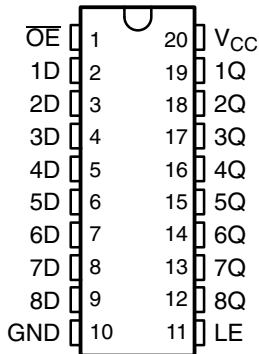


# SN54ABT573, SN74ABT573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

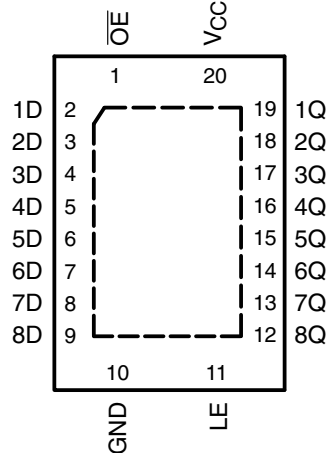
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- Typical  $V_{OLP}$  (Output Ground Bounce)  $<1$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

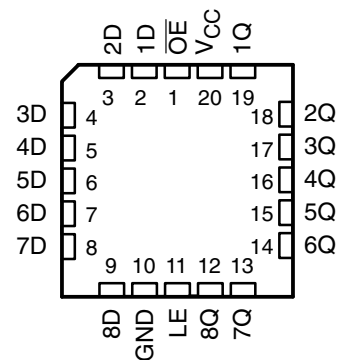
SN54ABT573 . . . J OR W PACKAGE  
SN74ABT573A . . . DB, DW, N, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74ABT573A . . . RGY PACKAGE  
(TOP VIEW)



SN54ABT573 . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74ABT573AN	SN74ABT573AN
	QFN – RGY	Tape and reel	SN74ABT573ARGYR	AB573A
	SOIC – DW	Tube	SN74ABT573ADW	ABT573A
		Tape and reel	SN74ABT573ADWR	
	SOP – NS	Tape and reel	SN74ABT573ANSR	ABT573A
	SSOP – DB	Tape and reel	SN74ABT573ADBR	AB573A
	TSSOP – PW	Tube	SN74ABT573APW	AB573A
		Tape and reel	SN74ABT573APWR	
VFBGA – GQN	Tape and reel	SN74ABT573AGQNR	AB573A	
VFBGA – ZQN (Pb-free)		SN74ABT573AZQNR		
-55°C to 125°C	CDIP – J	Tube	SNJ54ABT573J	SNJ54ABT573J
	CFP – W	Tube	SNJ54ABT573W	SNJ54ABT573W
	LCCC – FK	Tube	SNJ54ABT573FK	SNJ54ABT573FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54ABT573, SN74ABT573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## description/ordering information (continued)

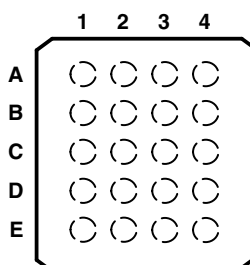
A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### SN74ABT573A . . . GQN OR ZQN PACKAGE (TOP VIEW)



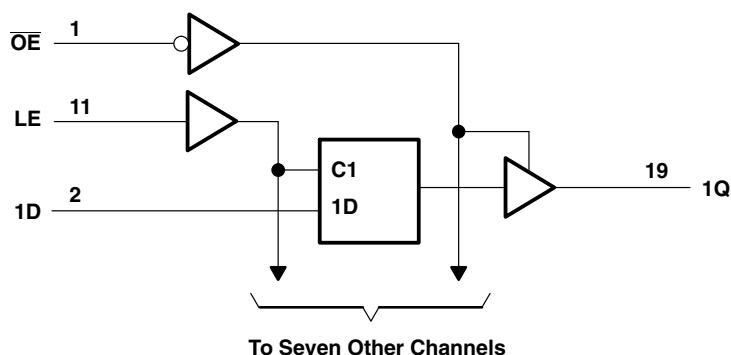
### terminal assignments

	1	2	3	4
A	1D	$\overline{OE}$	$V_{CC}$	1Q
B	3D	3Q	2D	2Q
C	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
E	GND	8D	LE	8Q

### FUNCTION TABLE (each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

### logic diagram (positive logic)



Pin numbers shown are for the DB, DW, FK, J, N, NS, PW, RGY, and W packages.

# SN54ABT573, SN74ABT573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT573 .....	96 mA
SN74ABT573A .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package .....	70°C/W
(see Note 2): DW package .....	58°C/W
(see Note 2): GQN/ZQN package .....	78°C/W
(see Note 2): N package .....	69°C/W
(see Note 2): NS package .....	60°C/W
(see Note 2): PW package .....	83°C/W
(see Note 3): RGY package .....	37°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.  
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

## recommended operating conditions (see Note 4)

		SN54ABT573		SN74ABT573A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5	5	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN54ABT573, SN74ABT573A

## OCTAL TRANSPARENT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT573		SN74ABT573A		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V	
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$			2.5		2.5		2.5	V	
	$V_{CC} = 5\text{ V}$ , $I_{OH} = -3\text{ mA}$			3		3		3		
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -24\text{ mA}$			2			2		
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$				0.55		0.55	V	
		$I_{OL} = 64\text{ mA}$				0.55*		0.55		
$V_{hys}$				100					mV	
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}$ or GND			$\pm 1$		$\pm 1$		$\pm 1$	$\mu\text{A}$	
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$			$10^\ddagger$		$10^\ddagger$		$10^\ddagger$	$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0.5\text{ V}$			$-10^\ddagger$		$-10^\ddagger$		$-10^\ddagger$	$\mu\text{A}$	
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O \leq 4.5\text{ V}$			$\pm 100$				$\pm 100$	$\mu\text{A}$	
$I_{CEX}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$	Outputs high				50		50	$\mu\text{A}$	
$I_O^§$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$			-50	-100	-180		-50	-180	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high		1	250			250	$\mu\text{A}$	
		Outputs low		24	30			30	30	mA
		Outputs disabled		0.5	250			250	250	$\mu\text{A}$
$\Delta I_{CC}^{\parallel}$	$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND					1.5		1.5	mA	
$C_i$	$V_I = 2.5\text{ V}$ or $0.5\text{ V}$			3.5					pF	
$C_o$	$V_O = 2.5\text{ V}$ or $0.5\text{ V}$			6.5					pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at  $V_{CC} = 5\text{ V}$ .

‡ This data sheet limit may vary among suppliers.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54ABT573				UNIT	
		$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		MIN	MAX		
		MIN	MAX				
$t_w$	Pulse duration, LE high			3.3		3.3	ns
$t_{su}$	Setup time, data before LE↓	High		1.9		2.5	ns
		Low		1.5		2.5	
$t_h$	Hold time, data after LE↓			1		2.5	ns



# SN54ABT573, SN74ABT573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN74ABT573A		UNIT
		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		
		MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	3.3	3.3	ns
t <sub>su</sub>	Setup time, data before LE↓	High	1.9	ns
		Low	1.5	
t <sub>h</sub>	Hold time, data after LE↓	1.8†	1.8†	ns

† This data-sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT573				UNIT	
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C					
			MIN	TYP	MAX	MIN		MAX
t <sub>PLH</sub>	D	Q	1.9	3.2	5.4	1.4	6.4	ns
t <sub>PHL</sub>			2.2	4.2	5.7	1.6	6.7	
t <sub>PLH</sub>	LE	Q	2.2	4	6.1	2	7.1	ns
t <sub>PHL</sub>			3.2	5.2	6.7	2.8	7.5	
t <sub>PZH</sub>	OE	Q	1.2	3.2	4.7	0.8	6.2	ns
t <sub>PZL</sub>			2.7	4.7	6.2	2	7.2	
t <sub>PHZ</sub>	OE	Q	2.5	4.9	6.4	2.2	7.7	ns
t <sub>PLZ</sub>			2	4.2	6	1.4	7	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT573A				UNIT	
			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C					
			MIN	TYP	MAX	MIN		MAX
t <sub>PLH</sub>	D	Q	1.9	3.2	5.4	1.9	5.9	ns
t <sub>PHL</sub>			2.2	4.2	5.7	2.2	6.2	
t <sub>PLH</sub>	LE	Q	2.2	4	6.1	2.2	6.6	ns
t <sub>PHL</sub>			3.2	5.2	6.7	3.2	7.2	
t <sub>PZH</sub>	OE	Q	1.2	3.2	4.7	1.2	5.2	ns
t <sub>PZL</sub>			2.5†	4.7	6.2	2.5†	6.7	
t <sub>PHZ</sub>	OE	Q	2.5	4.9	6.4	2.5	7.1†	ns
t <sub>PLZ</sub>			2	4.2	6	2	6.5	

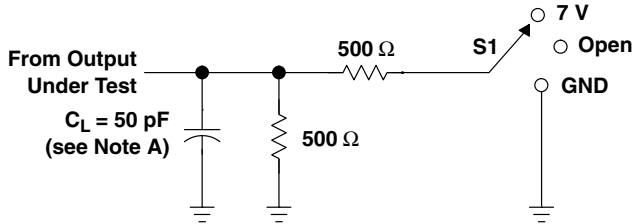
† This data-sheet limit may vary among suppliers.



# SN54ABT573, SN74ABT573A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

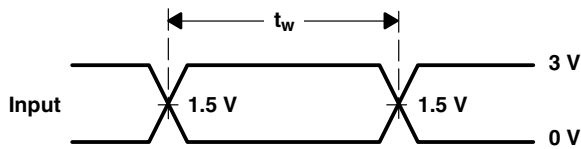
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## PARAMETER MEASUREMENT INFORMATION

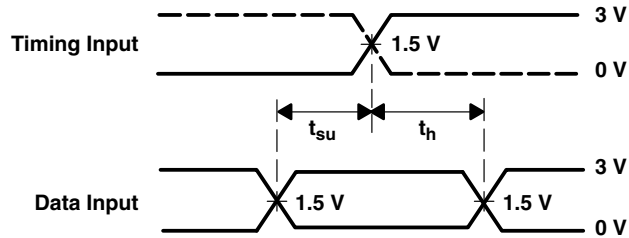


LOAD CIRCUIT

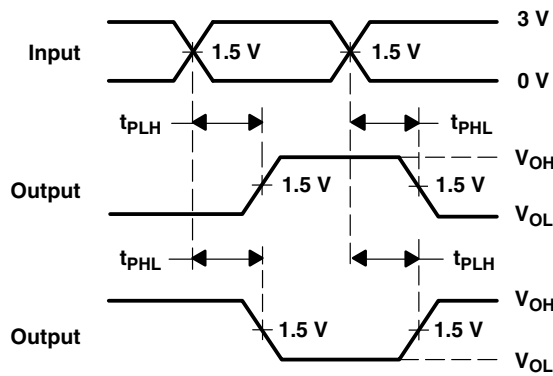
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



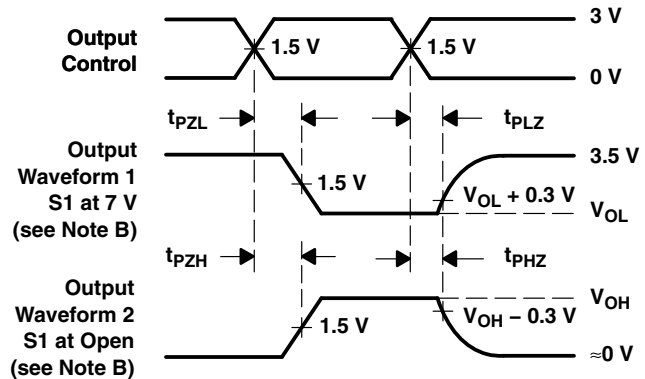
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9321901Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9321901Q2A SNJ54ABT 573FK	<a href="#">Samples</a>
5962-9321901QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9321901QR A SNJ54ABT573J	<a href="#">Samples</a>
5962-9321901QSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9321901QS A SNJ54ABT573W	<a href="#">Samples</a>
SN74ABT573ADBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB573A	<a href="#">Samples</a>
SN74ABT573ADW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT573A	<a href="#">Samples</a>
SN74ABT573ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT573A	<a href="#">Samples</a>
SN74ABT573AN	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABT573AN	<a href="#">Samples</a>
SN74ABT573APW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB573A	<a href="#">Samples</a>
SN74ABT573APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB573A	<a href="#">Samples</a>
SN74ABT573ARGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AB573A	<a href="#">Samples</a>
SNJ54ABT573FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9321901Q2A SNJ54ABT 573FK	<a href="#">Samples</a>
SNJ54ABT573J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9321901QR A SNJ54ABT573J	<a href="#">Samples</a>
SNJ54ABT573W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9321901QS A SNJ54ABT573W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT573ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT573ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ABT573APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74ABT573ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT573ADBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74ABT573ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ABT573APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74ABT573ARGYR	VQFN	RGY	20	3000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9321901Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9321901QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ABT573ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABT573AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ABT573APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54ABT573FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ABT573W	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

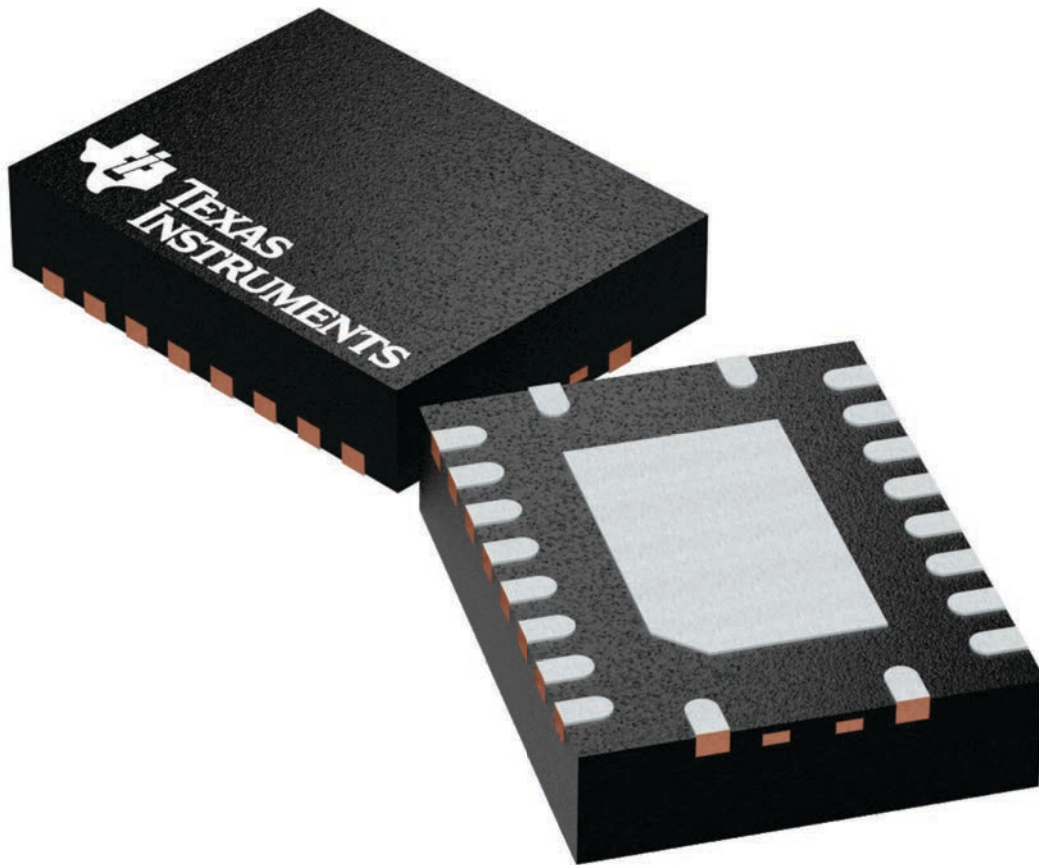
**RGY 20**

**VQFN - 1 mm max height**

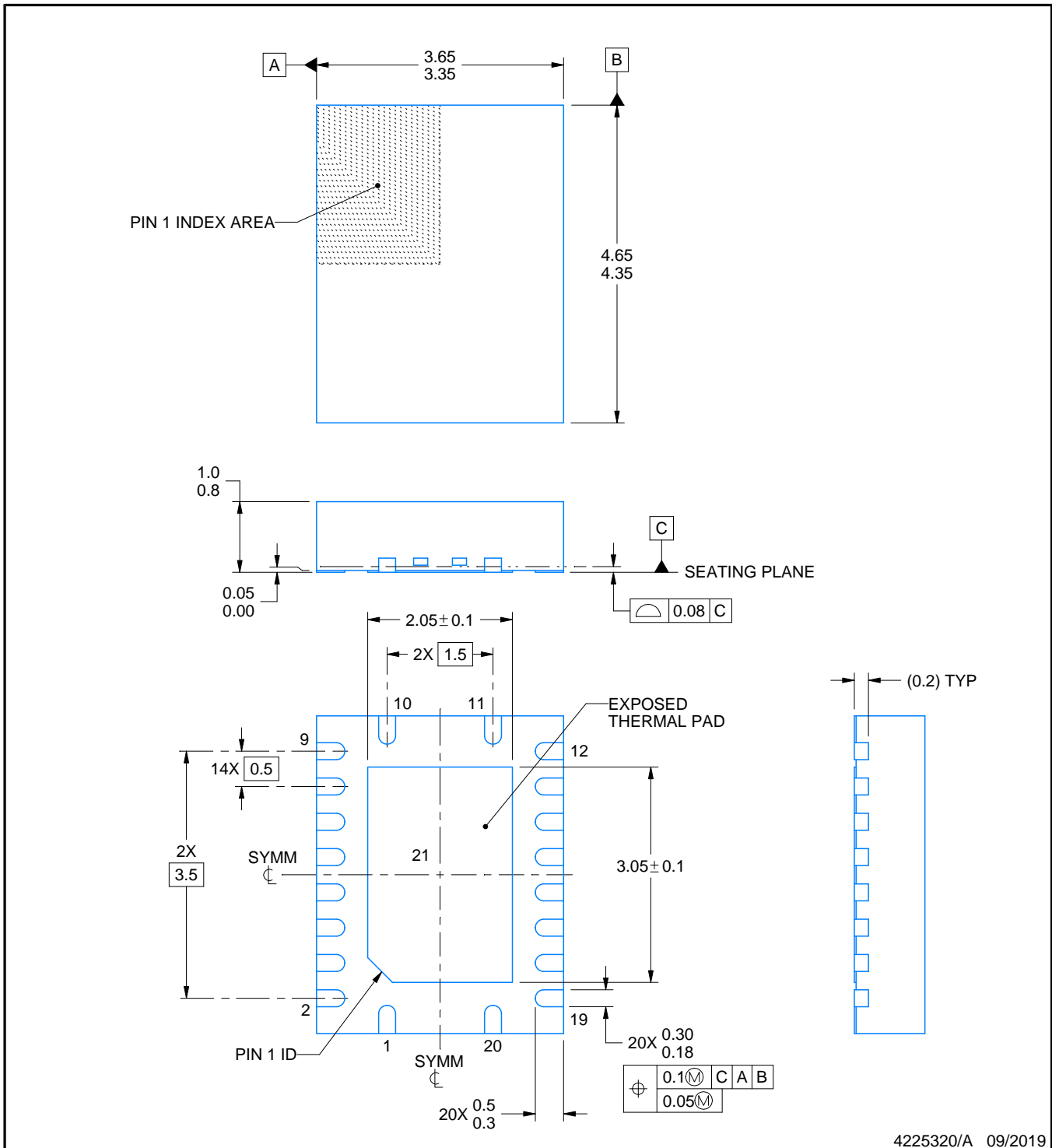
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:18X



**SOLDER MASK DETAILS**

4225320/A 09/2019

NOTES: (continued)

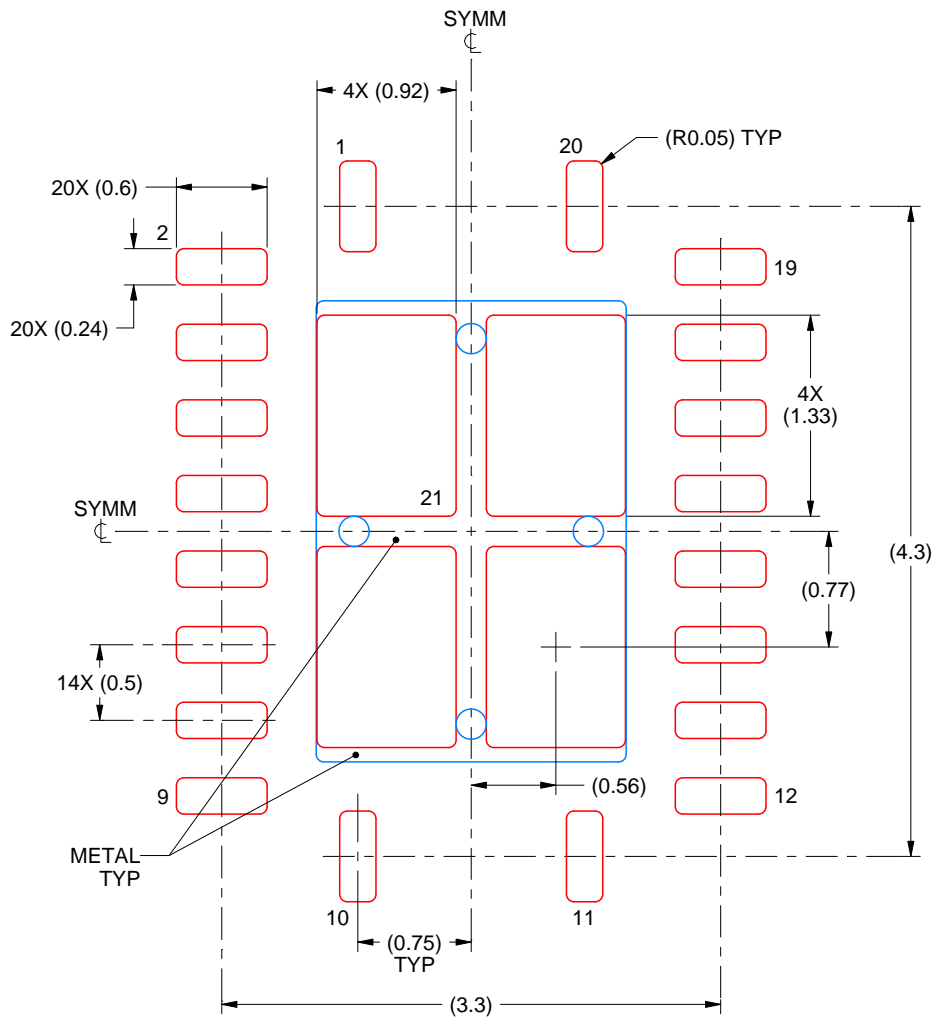
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21  
 78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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