

SN74AHC139 Dual 2- to 4-Bit Decoders/Demultiplexers

1 Features

- Operating range 2V to 5.5V
- Designed specifically for high-speed memory decoders and data-transmission systems
- Incorporate two enable inputs to simplify cascading or data reception
- Latch-up performance exceeds 250mA per JESD 17
- ESD protection exceeds JESD 22:
 - 2000V human-body model (A114-A)
 - 1000V charged-device model (C101)

2 Description

The SN74AHC139 are dual 2-line to 4-line decoders/demultiplexers designed for 2V to 5.5V V_{CC} operation. These devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When used with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

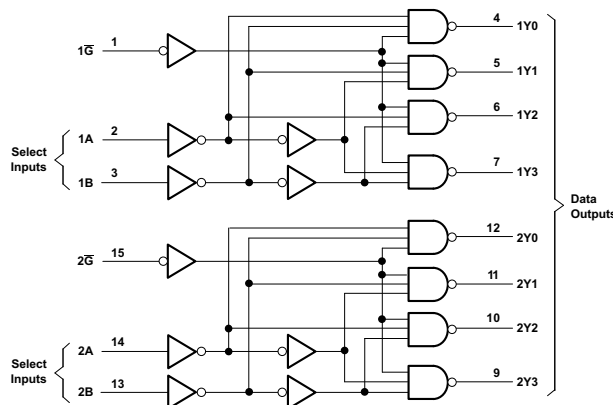
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74AHC139	D (SOIC, 16)	9.90 mm × 6mm	9.90 mm × 3.90 mm
	DB (SSOP, 16)	6.20 mm × 7.8mm	6.20 mm × 5.30 mm
	N (PDIP, 16)	19.31 mm × 9.4mm	19.31 mm × 6.35 mm
	NS (SOP, 16)	5mm × 6.4mm	5mm × 4.4mm
	PW (TSSOP, 16)	5.00 mm × 6.4mm	5.00 mm × 4.40 mm
	DGV (TVSOP, 16)	3.6mm × 6.4mm	3.6mm × 4.4mm
	RGY (VQFN, 16)	4mm × 3.5mm	4mm × 3.5mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable

(3) The body size (length × width) is a nominal value and does not include pins.



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

Logic Diagram, Each Gate (Positive Logic)



Table of Contents

1 Features	1	6.4 Device Functional Modes.....	9
2 Description	1	7 Application and Implementation	10
3 Pin Configuration and Functions	3	7.1 Application Information.....	10
4 Specifications	4	7.2 Typical Application.....	10
4.1 Absolute Maximum Ratings.....	4	7.3 Power Supply Recommendations.....	13
4.2 ESD Ratings.....	4	7.4 Layout.....	13
4.3 Recommended Operating Conditions.....	4	8 Device and Documentation Support	15
4.4 Thermal Information.....	5	8.1 Documentation Support.....	15
4.5 Electrical Characteristics.....	5	8.2 Receiving Notification of Documentation Updates....	15
4.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	5	8.3 Support Resources.....	15
4.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	6	8.4 Trademarks.....	15
4.8 Operating Characteristics.....	6	8.5 Electrostatic Discharge Caution.....	15
5 Parameter Measurement Information	7	8.6 Glossary.....	15
6 Detailed Description	8	9 Revision History	15
6.1 Overview.....	8	10 Mechanical, Packaging, and Orderable Information	16
6.2 Functional Block Diagram.....	8		
6.3 Feature Description.....	8		

3 Pin Configuration and Functions

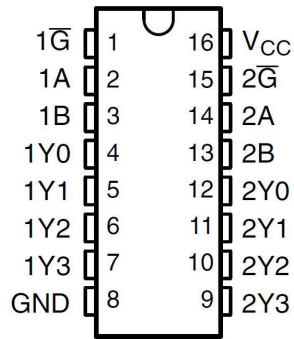


Figure 3-1. SN74AHC139 D, DB, DGV, N, NS, or PW Package (Top View)

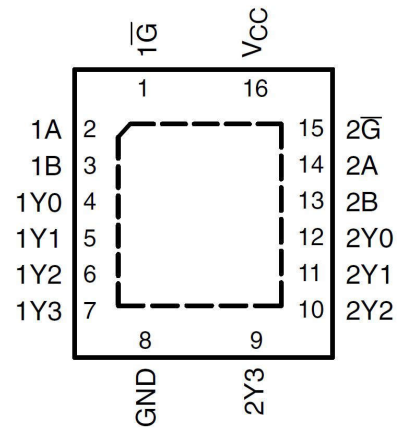


Figure 3-2. SN74AHC139 RGY Package (Top View)

Table 3-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	D, DB, DGV, N, NS, PW, RGY		
NC	—	I	Output enable input 1, active low
$\overline{1G}$	1	I	Input for channel 1
1A	2	I	Input for channel 2
1B	3	I	Input for channel 3
1Y0	4	I	Input for channel 4
NC	—	I	Input for channel 5
1Y1	5	I	Input for channel 6
1Y2	6	I	Input for channel 7
1Y3	7	I	Input for channel 8
GND	8	G	Ground
NC	—	O	Output for channel 8
2Y3	9	O	Output for channel 7
2Y2	10	O	Output for channel 6
2Y1	11	O	Output for channel 5
2Y0	12	O	Output for channel 4
NC	—	O	Output for channel 3
2B	13	O	Output for channel 2
2A	14	O	Output for channel 1
$\overline{2G}$	15	I	Output enable input 2, active low
V _{CC}	16	P	Positive supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	-0.5	7	V
V_I ⁽²⁾	Input voltage	-0.5	7	V
V_O ⁽²⁾	Output voltage	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current		-20	mA
				($V_I < 0$)
I_{OK}	Output clamp current		±20	mA
				($V_O < 0$ or $V_O > V_{CC}$)
I_O	Continuous output current		±25	mA
				($V_O = 0$ to V_{CC})
	Continuous current through V_{CC} or GND		±75	mA
T_{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101	±1000

4.3 Recommended Operating Conditions

		SN54AHC139		SN74AHC139		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	1.5		V
		$V_{CC} = 3\text{ V}$	2.1	2.1		
		$V_{CC} = 5.5\text{ V}$	3.85	3.85		
V_{IL}	Low-level Input voltage	$V_{CC} = 2\text{ V}$		0.5	0.5	V
		$V_{CC} = 3\text{ V}$		0.9	0.9	
		$V_{CC} = 5.5\text{ V}$		1.65	1.65	
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$		-50	-50	mA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		-4	-4	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		-8	-8	
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$		50	50	mA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		4	4	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		8	8	
$\Delta t/\Delta v$	Input Transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		100	100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		20	20	
T_A	Operating free-air temperature	-55	125	-40	125	°C

4.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHC139							UNIT
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	
		16							
R _{θJA}	Junction-to-ambient thermal resistance	73	82	120	67	64	135.9	52.9	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

4.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = -40°C TO 85°C		T _A = -40°C TO 125°C		UNIT
						SN74AHC139		Recommended		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2	1.9	1.9	1.9	1.9	V	
		3 V	2.9	3	2.9	2.9	2.9	2.9		
		4.5 V	4.4	4.5	4.4	4.4	4.4	4.4		
	I _{OH} = -4 mA	3 V	2.58		2.48	2.48	2.48	2.48		
		4.5 V	3.94		3.8	3.8	3.8	3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1	0.1	0.1	0.1	V	
		3 V			0.1	0.1	0.1	0.1		
		4.5 V			0.1	0.1	0.1	0.1		
	I _{OH} = 4 mA	3 V			0.36	0.44	0.5	0.5		
		4.5 V			0.36	0.44	0.5	0.5		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1	±1	±1	±1	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4	40	40	40	μA	
C _i	V _I = V _{CC} or GND	5 V			2	10	10	10	pF	

4.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Figure 5-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C		T _A = -40°C TO 85°C		T _A = -40°C TO 125°C		UNIT
						SN74AHC139		Recommended		
				TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 15 pF	7.2 ⁽¹⁾	11 ⁽¹⁾	1	13	1	13	ns
t _{PHL}				7.2 ⁽¹⁾	11 ⁽¹⁾	1	13	1	13	
t _{PLH}	G̅	Y	C _L = 15 pF	6.4 ⁽¹⁾	9.2 ⁽¹⁾	1	11	1	11	ns
t _{PHL}				6.4 ⁽¹⁾	9.2 ⁽¹⁾	1	11	1	11	
t _{PLH}	A or B	Y	C _L = 50 pF	9.7	14.5	1	16.5	1	16.5	ns
t _{PHL}				9.7	14.5	1	16.5	1	16.5	
t _{PLH}	G̅	Y	C _L = 50 pF	8.9	12.7	1	14.5	1	14.5	ns
t _{PHL}				8.9	12.7	1	14.5	1	14.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

4.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Figure 5-1](#))

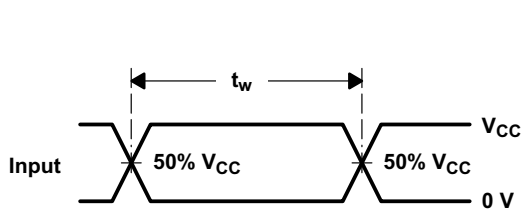
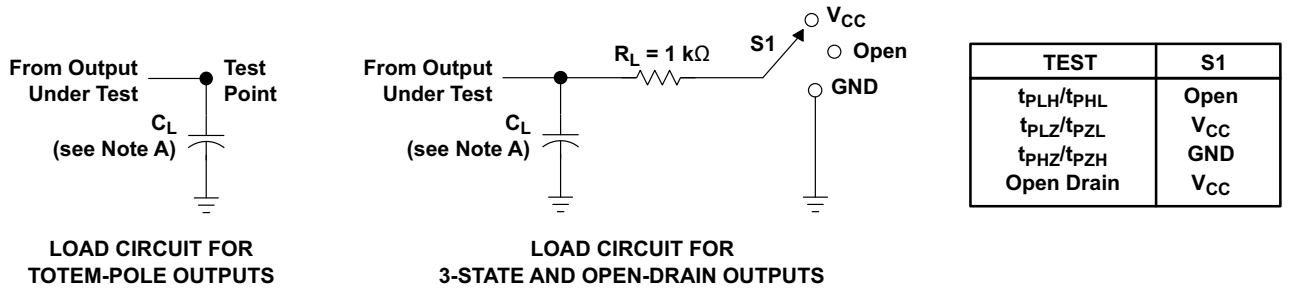
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		UNIT
				TYP	MAX	Recommended		Recommended		
						SN74AHC139		SN74AHC139		
					MIN	MAX	MIN	MAX		
t_{PLH}	A or B	Y	$C_L = 15\text{ pF}$	5 ⁽¹⁾	7.2 ⁽¹⁾	1	8.5	1	8.5	ns
t_{PHL}				5 ⁽¹⁾	7.2 ⁽¹⁾	1	8.5	1	8.5	
t_{PLH}	\bar{G}	Y	$C_L = 15\text{ pF}$	4.4 ⁽¹⁾	6.3 ⁽¹⁾	1	7.5	1	7.5	ns
t_{PHL}				4.4 ⁽¹⁾	6.3 ⁽¹⁾	1	7.5	1	7.5	
t_{PLH}	A or B	Y	$C_L = 50\text{ pF}$	6.5	9.5	1	10.5	1	10.5	ns
t_{PHL}				6.5	9.5	1	10.5	1	10.5	
t_{PLH}	\bar{G}	Y	$C_L = 50\text{ pF}$	5.9	8.3	1	9.5	1	9.5	ns
t_{PHL}				5.9	8.3	1	9.5	1	9.5	

4.8 Operating Characteristics

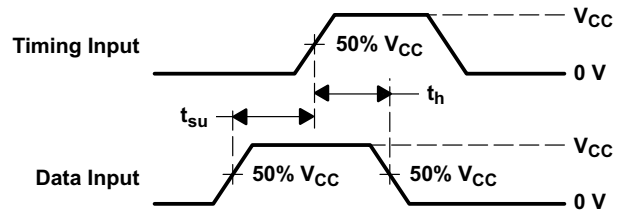
$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	13	pF

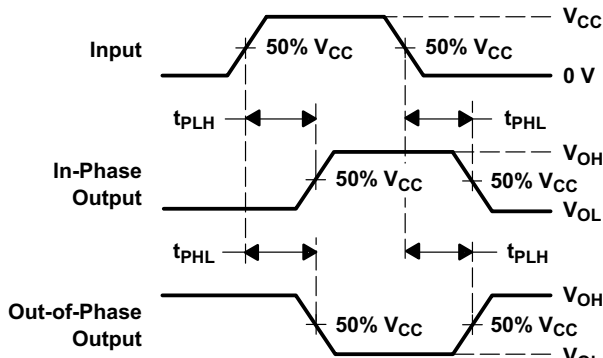
5 Parameter Measurement Information



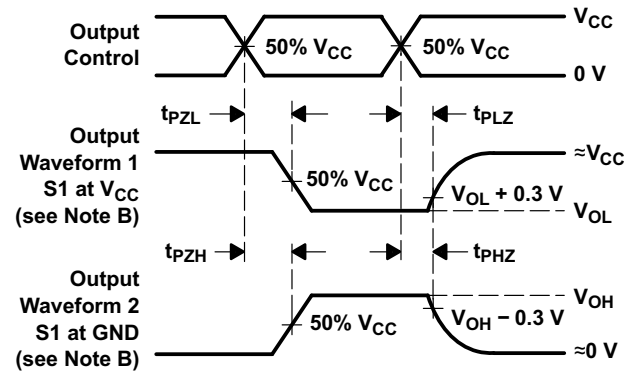
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
- The outputs are measured one at a time with one input transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms

6 Detailed Description

6.1 Overview

The SN74AHC139 is a high speed silicon gate CMOS decoder well suited to memory address decoding or data routing applications. It contains two 2:4 decoders.

Each channel of the SN74AHC139 has two address select inputs (A1 and A0). The circuit functions as a normal one-of-four decoder.

One strobe input (\overline{G}) is provided for each channel to simplify cascading and to facilitate demultiplexing. When the input strobe for a channel is active, that channel's outputs are forced into the high state.

The demultiplexing function is accomplished by first using the select inputs to choose the desired output, and then using the strobe input as the data input.

The outputs for the SN74AHC139 are normally high, and low when selected.

6.2 Functional Block Diagram

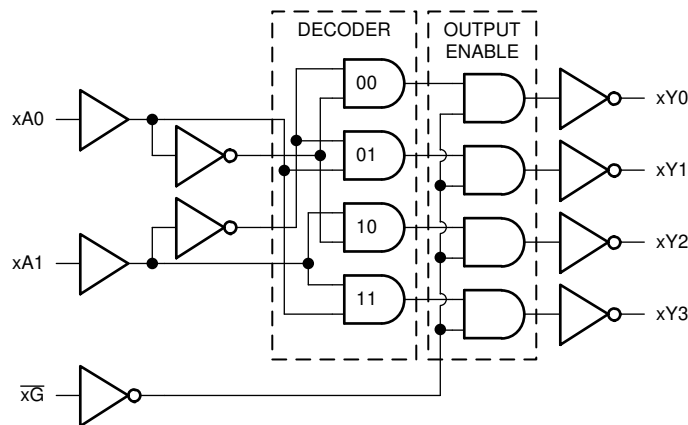


Figure 6-1. Logic Diagram, Each Gate (Positive Logic)

6.3 Feature Description

6.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10k Ω resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

6.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in [Implications of Slow or Floating CMOS Inputs](#).

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10k Ω resistor, however, is recommended and will typically meet all requirements.

6.4 Device Functional Modes

Function Table (each channel)

INPUTS ¹			OUTPUT ²			
\bar{G}	SELECT		Y0	Y1	Y2	Y3
	A1	A0				
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

1. L = Low; H = High; X = Don't care
2. L = Driving low; H = Driving high

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The SN74AHC139 device is used to control multiple devices that operate on a shared data bus. A decoder allows a binary encoded input to activate only one of the device's outputs. This makes this device an excellent choice for solid state memory applications where multiple devices have to be read or written to with a limited number of GPIO pins used on the system controller. The decoder is used to activate the chip select (CS) input to the selected memory device, and the controller can then read or write from that device alone when using a shared bus.

7.2 Typical Application

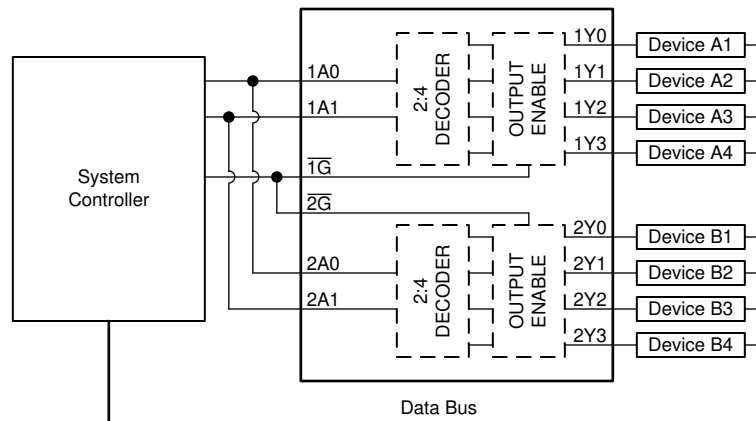


Figure 7-1. Typical Application Block Diagram

7.2.1 Design Requirements

7.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AHC139 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AHC139 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AHC139 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74AHC139 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

7.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AHC139 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k Ω resistor value is often used due to these factors.

The SN74AHC139 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

7.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

7.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is $\leq 50\text{pF}$. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AHC139 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

7.2.3 Application Curve

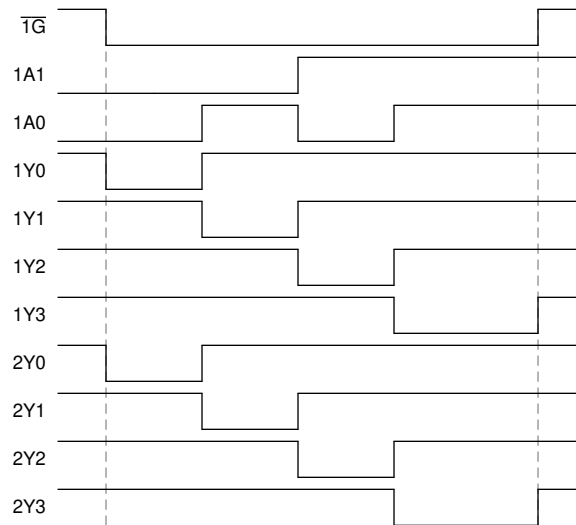


Figure 7-2. Application Timing Diagram

7.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\mu\text{F}$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.4 Layout

7.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

7.4.2 Layout Example

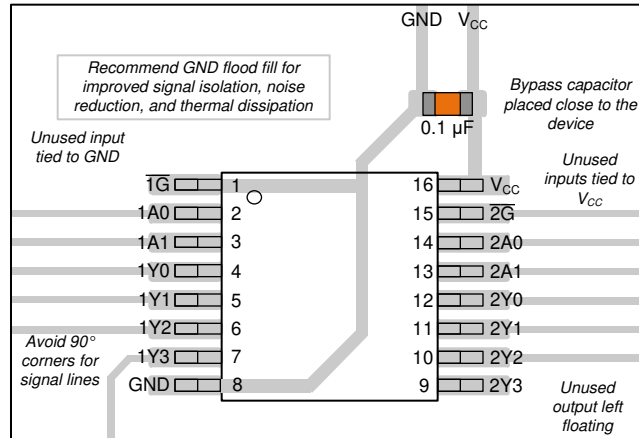


Figure 7-3. Example Layout for the SN74AHC139

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Understanding Schmitt Triggers](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)
- Texas Instruments, [CMOS Power Consumption and Cpd Calculation](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#)

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (June 2013) to Revision M (July 2024)	Page
• Deleted machine model from <i>Features</i> section.....	1
• Added <i>Package Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , Application and Implementation section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Updated thermal values for RθJA: PW = 108 to 135.9, RGY = 39 to 52.9, all values in °C/W	5

Changes from Revision K (March 2003) to Revision L (June 2013)	Page
• Extended operating temperature range to 125°C.....	4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated