SNx4AHCT02 四路双输入正或非门

1 特性

- 工作电压范围为 4.5V 至 5.5V
- 低功耗，I_{CC} 最大值为 10μA
- 5V 时，输出驱动为 ±8mA
- 输入兼容 TTL 电压
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- 启用或禁用数字信号
- 控制指示灯 LED
- 通信模块和系统控制器之间的转换

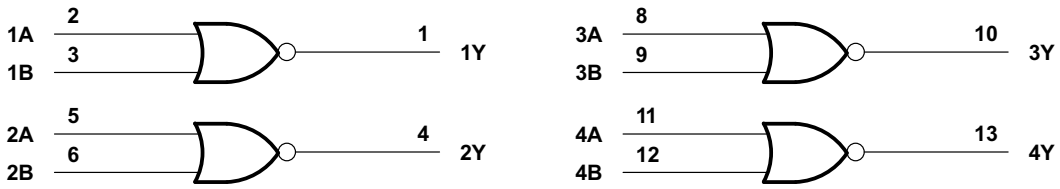
3 说明

这些器件包含四个独立的双输入或非门，这些门以正逻辑执行布尔函数 $Y = \overline{A} \times \overline{B}$ 或 $Y = \overline{A + B}$。

器件信息

器件型号	等级	封装尺寸(1)
SN54AHCT02	军用级	J（CDIP，14）
		W（CFP，14）
		FK（LCCC，20）
SN74AHCT02	商用级	D（SOIC，14）
		DB（SSOP，14）
		DGV（TVSOP，14）
		N（PDIP，14）
		NS（SOP，14）
		PW（SOP，14）
		RGY（VQFN，14）
		BQA（WQFN，14）

(1) 更多相关信息，请参阅第 11 节。



逻辑图（正逻辑）

内容

4 引脚配置和功能

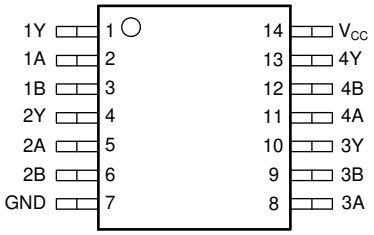


图 4-1. SN54AHCT02 J 或 W 封装，14 引脚（顶视图）
SN74AHCT02 D、DB、DGV、N、NS 或 PW 封装，14 引脚（顶视图）

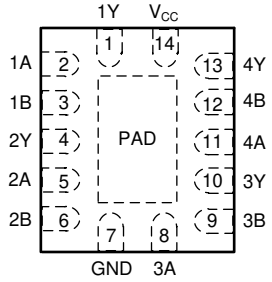


图 4-2. SN74AHCT02 RGY 或 BQA 封装，14 引脚（顶视图）

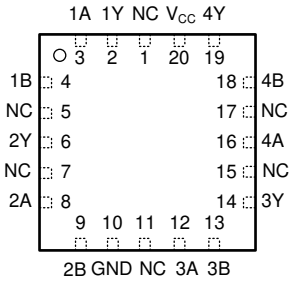


图 4-3. SN54AHCT02 FK 封装，20 引脚（顶视图）

表 4-1. 引脚功能

引脚				类型[1]	说明
名称	SN74AHCT02	SN54AHCT02			
	D、DB、DGV、N、NS、PW、RGY、BQA	J、W	FK		
1A	2	2	3	I	1A 输入
1B	3	3	4	I	1B 输入
1Y	1	1	2	O	1Y 输出
2A	5	5	8	I	2A 输入
2B	6	6	9	I	2B 输入
2Y	4	4	6	O	2Y 输出
3A	8	8	12	I	3A 输入
3B	9	9	13	I	3B 输入
3Y	10	20	14	O	3Y 输出
4A	11	11	16	I	4A 输入
4B	12	12	18	I	4B 输入
4Y	13	13	19	O	4Y 输出
GND	7	7	10	—	接地引脚
NC	—	—	1、5、7、11、15、17	—	无连接

表 4-1. 引脚功能（续）

引脚				类型(1)	说明
名称	SN74AHCT02	SN54AHCT02			
	D、DB、DGV、N、NS、PW、RGY、BQA	J、W	FK		
V_{CC}	14	14	20	—	电源引脚

(1) I = 输入，O = 输出

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

	最小值	最大值	单位
电源电压范围，V_{CC}	−0.5	7	V
输入电压范围，V_I (2)	−0.5	7	V
输出电压范围，V_O (2)	−0.5	V_{CC}+0.5	V
输入钳位电流，I_{IK} (V_I < 0)		-20	mA
输出钳位电流，I_O（V_O < 0 或者 V_O > V_{CC}）		±20	mA
持续输出电流，I_O（V_O = 0 至 V_{CC}）		±25	mA
通过 V_{CC} 或 GND 的持续电流		±50	mA
储存温度范围，T_{stg}	−65	150	°C

(1) 应力超出*绝对最大额定值*下所列的值可能会对器件造成永久损坏。这些列出的值仅仅是应力等级，这并不表示器件在这些条件下以及在*建议运行条件*以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

5.2 ESD 等级

		值	单位
$V_{(ESD)}$ 静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准(1)	±2000	V
	充电器件模型 (CDM)，符合 ANSI/ESDA/JEDEC JS-002 标准(2)	±1000	

(1) JEDEC 文档 JEP155 指出：500V HBM 能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文件 JEP157 指出：250V CDM 可实现在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

		SN54AHCT02		SN74AHCT02		单位
		最小值	最大值	最小值	最大值	
V_{CC}	电源电压	4.5	5.5	4.5	5.5	V
V_{IH}	高电平输入电压	2		2		V
V_{IL}	低电平输入电压		0.8		0.8	V
V_I	输入电压	0	5.5	0	5.5	V
V_O	输出电压	0	V_{CC}	0	V_{CC}	V
I_{OH}	高电平输出电流		−8		-8	mA
I_{OL}	低电平输出电流		8		8	mA
$\Delta t/\Delta v$	输入转换上升或下降速率		20		20	ns/V
T_A	自然通风工作温度	−55	125	−40	125	°C

5.4 热性能信息

热指标(1)	SNx4AHCT02					单位
	D	DB	NS	PW	RGY	
	14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	
$R_{\theta JA}$ 结至环境热阻	86	96	76	113	87.1	°C/W

(1) 有关新旧热指标的更多信息，请参阅 *IC 封装热指标* 应用报告 SPRA953。

5.5 电气特性

在推荐的自然通风条件下的工作温度范围（除非另外注明）

参数	测试条件	VCC	TA = 25°C			SN54AHCT02		SN74AHCT02		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V_{OH}	I_{OH} = -50μA	4.5V	4.4	4.5		4.4		4.4		V
	I_{OH} = -8 mA		3.94			3.8		3.8		
V_{OL}	I_{OL} = 50μA	4.5V			0.1		0.1		0.1	V
	I_{OL} = 8mA				0.36		0.44		0.44	
I_I	V_I=5.5V 或 GND	0 V 至 5.5 V			±0.1		±1(1)		±1	μA
I_{CC}	V_I = V_{CC} 或 GND，I_O = 0	5.5V			2		20		20	μA
ΔI_{CC} (2)	一个输入为 3.4V，GND 或 VCC 上的其他输入	5.5V			1.35		1.5		1.5	mA
C_i	VI = VCC 或 GND	5V		4	10				10	pF

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试（在 V_{CC} = 0V 时）。
(2) 这是每个输入在指定的一个 TTL 电压电平下（而不是 0V 或 V_{CC} 时）电源电流的增加情况。

5.6 开关特性

在推荐的自然通风条件下的工作温度范围内测得，V_{CC} = 5V ± 0.5V（除非另有说明）。请参阅图 6-1

参数	从（输入）	至（输出）	负载电容	TA = 25°C			SN54AHCT02		SN74AHCT02		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{PLH}	A 或 B	Y	C_L = 15 pF		2.4(1)	5.5(1)	1(1)	6.5(1)	1	6.5	ns
t_{PHL}					3.5(1)	5.5(1)	1(1)	6.5(1)	1	6.5	
t_{PLH}	A 或 B	Y	C_L = 50pF		3.4	7.5	1	8.5	1	8.5	ns
t_{PHL}					4.5	7.5	1	8.5	1	8.5	

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试。

5.7 噪声特性

V_{CC} = 5V，C_L = 50pF，T_A = 25°C（除非另有说明）(1)

参数	SN74AHCT02			单位
	最小值	典型值	最大值	
$V_{OL(P)}$ 安静输出，最大动态 V_{OL}			0.8	V
$V_{OL(V)}$ 安静输出，最小动态 V_{OL}			-0.8	V
$V_{OH(V)}$ 安静输出，最小动态 V_{OH}		4.7		V
$V_{IH(D)}$ 高电平动态输入电压	2			V
$V_{IL(D)}$ 低电平动态输入电压			0.8	V

(1) 特性仅适用于表面贴装封装。

5.8 工作特性

V_{CC} = 5V，T_A = 25°C

参数	测试条件	典型值	单位
C_{pd} 功率耗散电容	空载，f = 1MHz	17	pF

5.9 典型特性

T_A = 25°C（除非另有说明）

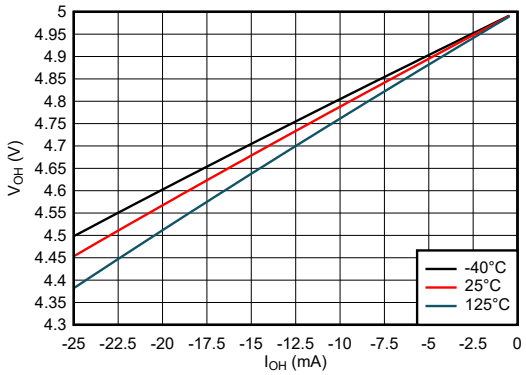


图 5-1. 高电平状态下输出电压与电流间的关系；5V 电源

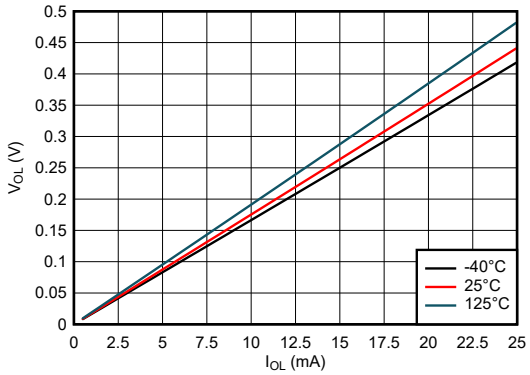
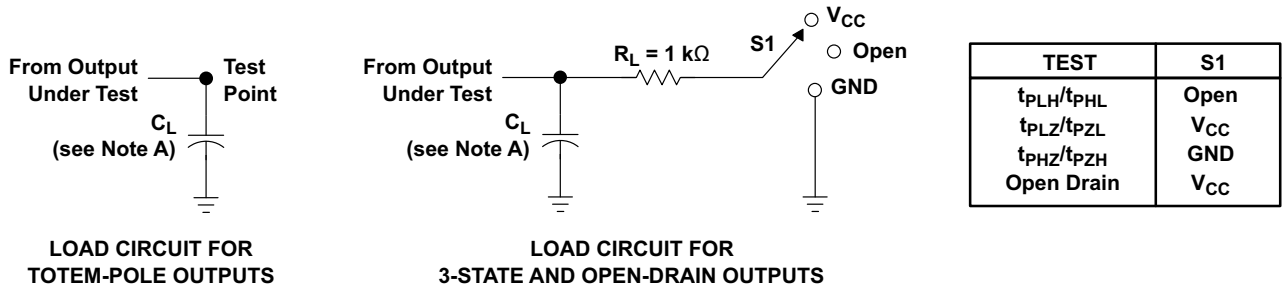


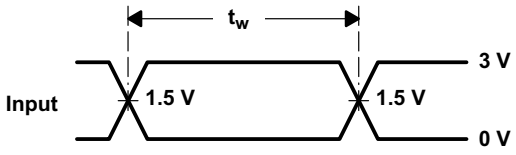
图 5-2. 低电平状态下输出电压与电流间的关系；5V 电源

6 参数测量信息

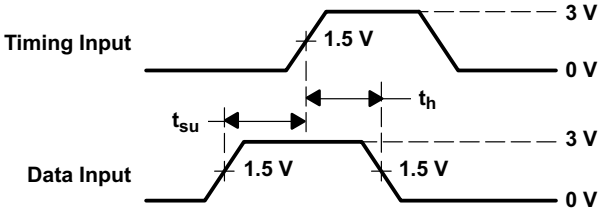


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

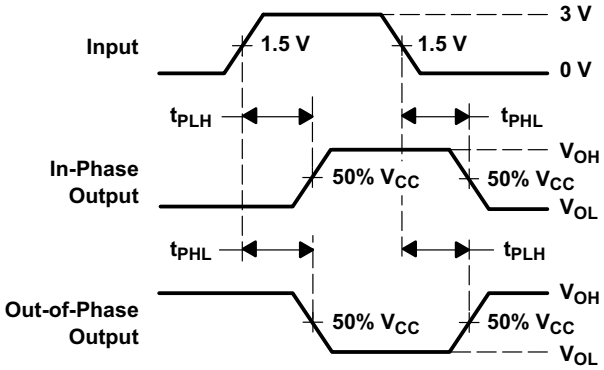
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



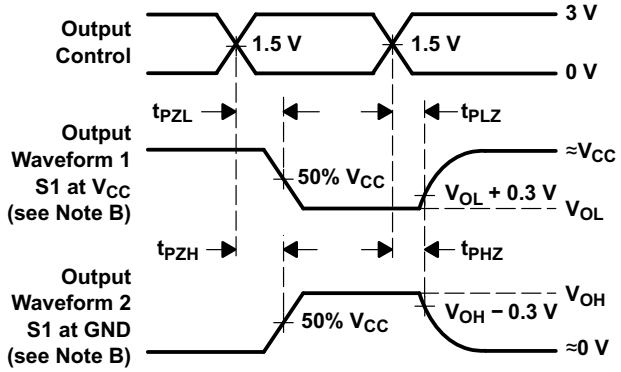
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

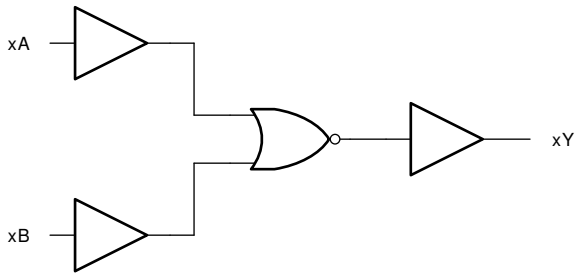
图 6-1. 负载电路和电压波形

7 详细说明

7.1 概述

此器件包含四个独立双输入或非门。每个逻辑门以正逻辑执行布尔函数 $Y = \overline{A + B}$。

7.2 功能方框图



7.3 特性说明

7.3.1 TTL 兼容型 CMOS 输入

此器件包括 TTL 兼容型 CMOS 输入。这些输入专门设计为通过降低的输入电压阈值与 TTL 逻辑器件连接。

TTL 兼容型 CMOS 输入为高阻抗，通常建模为与输入电容并联的电阻器，如*电气特性* 中所示。最坏情况下的电阻是根据*绝对最大额定值* 中给出的最大输入电压和*电气特性* 中给出的最大输入漏电流，使用欧姆定律 (R = V ÷ I) 计算得出的。

TTL 兼容型 CMOS 输入要求输入信号在有效逻辑状态之间快速转换，如*建议的工作条件* 表中的输入转换时间或速率所定义。不符合此规范将导致功耗过大并可能导致振荡。有关更多详细信息，请参阅 *CMOS 输入缓慢变化或悬空的影响* 应用报告。

在运行期间，任何时候都不要让 TTL 兼容型 CMOS 输入悬空。未使用的输入必须在 V_{CC} 或 GND 端接。如果系统不会一直主动驱动输入，可以添加上拉或下拉电阻器，以在这些时间段提供有效的输入电压。电阻值将取决于多种因素；但建议使用 10kΩ 电阻器，这通常可以满足所有要求。

7.3.2 平衡 CMOS 推挽式输出

该器件包括平衡 CMOS 推挽输出。术语*平衡* 表示器件可以灌入和拉出相似的电流。此器件的驱动能力可能在轻负载时产生快速边缘，因此应考虑布线和负载条件以防止振铃。此外，该器件的输出能够驱动的电流比此器件能够承受的电流更大，而不会损坏器件。务必限制器件的输出功率，以避免因过流而损坏器件。必须始终遵守*绝对最大额定值* 中规定的电气和热限值。

未使用的推挽 CMOS 输出应保持断开状态。

7.3.3 钳位二极管结构

该器件的输出同时具有正负钳位二极管，而该器件的输入只有负钳位二极管，如图 7-1 所示。

小心

电压超出*绝对最大额定值* 表中规定的值可能会损坏器件。如果遵守输入和输出钳制电流额定值，输入和输出电压可超过额定值。

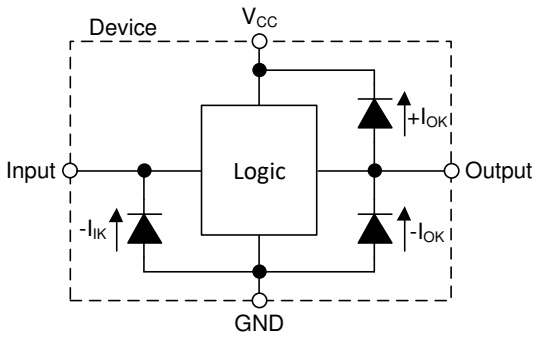


图 7-1. 每个输入和输出的钳位二极管的电气布置

7.4 器件功能模式

表 7-1. 功能表

输入(1)		输出 Y
A	B	
H	X	L
X	H	L
L	L	H

(1) H = 高电压电平，L = 低电压电平，X = 不用考虑

8 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 应用信息

在该应用中，使用两个双输入与非门来创建 SR 锁存器，如图 8-1 所示。可以对第二个 SR 锁存器使用两个额外的逻辑门，或者可将输入接地且两个通道均未使用。

SNx4AHCT02 用于驱动篡改指示灯 LED 并为系统控制器提供一位数据。当防拆开关输出低电平时，输出 Q 变为高电平。此输出保持高电平，直到系统控制器处理该事件并向 R 输入发送高电平信号，使 Q 输出恢复至低电平。

用户可以在或非门的反馈路径中添加一个小 RC，以将输出设为特定默认状态，这可能会产生较慢的转换速率。SNx4AHCT02 具有无输入转换速率要求的施密特触发输入，因此非常适合该应用。

8.2 典型应用

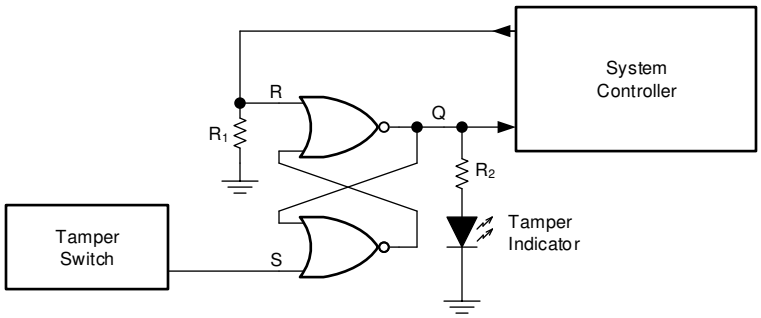


图 8-1. 典型应用框图

8.2.1 设计要求

8.2.1.1 电源注意事项

确保所需电源电压在*建议运行条件*中规定的范围内。电源电压按照*电气特性*部分所述设置器件的电气特性。

正电压电源必须能够提供的电流等于 最大静态电源电流 I_{CC}（在*电气特性*中列出）以及开关所需的任何瞬态电流之和。

地必须能够灌入的电流等于 SNx4AHCT02 所有输出端灌入的总电流加上最大电源电流 I_{CC}（在*电气特性*中列出）以及开关所需的任何瞬态电流之和。逻辑器件只能灌入其所接的地可灌入的大小相同的电流。确保不要超过*绝对最大额定值*中列出的通过 GND 的最大总电流。

SNx4AHCT02 可以驱动总电容小于或等于 50pF 的负载，同时仍满足所有数据表规格。可以施加更大的容性负载；但建议不要超过 50pF。

SNx4AHCT02 可以驱动由 $R_L \geq V_O/I_O$ 描述的总电阻负载，输出电压和电流在*电气特性*表中用 V_{OL} 定义。在高电平状态下输出时，公式中的输出电压定义为测量的输出电压与 V_{CC} 引脚处的电源电压之间的差值。

总功耗可以使用 *CMOS 功耗与 Cpd 计算*中提供的信息进行计算。

可以使用*标准线性和逻辑 (SLL) 封装和器件的热特性*中提供的信息计算热增量。

小心

绝对最大额定值 中列出的最高结温 $T_{J(max)}$ 是防止损坏器件的附加限制。请勿违反*绝对最大额定值* 中列出的任何值。提供这些限制是为了防止损坏器件。

8.2.1.2 输入注意事项

输入信号必须超过 才能被视为逻辑低电平，超过 才能被视为逻辑高电平。不要超过*绝对最大额定值* 中的最大输入电压范围。

未使用的输入必须端接至 V_{CC} 或地。如果输入完全不使用，则可以直接端接未使用的输入，如果有时要使用输入，但并非始终使用，则可以使用上拉或下拉电阻器连接输入。上拉电阻用于默认高电平状态，下拉电阻用于默认低电平状态。控制器的驱动电流、进入 SNx4AHCT02 的漏电流（如*电气特性* 中所规定）以及所需输入转换率会限制电阻大小。由于这些因素，通常使用 10kΩ 的电阻值。

有关此器件的输入的附加信息，请参阅*特性描述* 部分。

8.2.1.3 输出注意事项

接地电压用于产生输出低电平电压。根据*电气特性* 中 V_{OL} 规范的规定，向输出端灌入电流将提高输出电压。

未使用的输出可以保持悬空状态。不要将输出直接连接到 V_{CC} 或地。

有关此器件的输出的附加信息，请参阅*特性描述* 部分。

8.2.2 详细设计过程

1. 在 V_{CC} 至 GND 之间添加一个去耦电容器。此电容器需要在物理上靠近器件，在电气上靠近 V_{CC} 和 GND 引脚。*布局* 部分中展示了示例布局。
2. 确保输出端的容性负载 ≤ 50pF。这不是硬性限制；但是，根据设计，该限制将优化性能。这可以通过从 SNx4AHCT02 向一个或多个接收器件提供适当大小的短布线来实现。
3. 确保输出端的电阻负载大于 $(V_{CC}/I_{O(max)})$Ω。这可防止超出*绝对最大额定值* 中的最大输出电流。大多数 CMOS 输入具有以 MΩ 为单位的电阻负载；远大于之前计算的最小值。
4. 逻辑门很少关注热问题；然而，可以使用应用报告 *CMOS 功耗与 Cpd 计算* 中提供的步骤计算功耗和热增量。

8.2.3 应用曲线

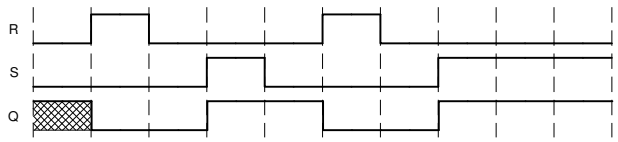


图 8-2. 应用时序图

8.3 电源相关建议

电源可以是*建议运行条件*中最小和最大电源电压额定值之间的任何电压。每个 V_{CC} 端子均应具有一个良好的旁路电容器，以防止功率干扰。建议为该器件使用 0.1 µF 电容。可以并联多个旁路电容器以抑制不同的噪声频率。0.1 µF 和 1 µF 电容器通常并联使用。旁路电容器应安装在尽可能靠近电源端子的位置，以获得更佳效果，如给定的示例布局图所示。

8.4 布局

8.4.1 布局指南

使用多输入和多通道逻辑器件时，输入不得悬空。在许多情况下，未使用数字逻辑器件的功能或部分功能；例如，当仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个时。此类未使用的输入引脚不得悬空，因为外部连接处的未定义电压会导致未定义的操作状态。数字逻辑器件的所有未使用输入必须连接到由输入电压规范定义的逻辑高电平电压或逻辑低电平电压，以防止其悬空。必须应用于任何特定未使用输入的逻辑电平取决于器件的功能。通常，输入连接到 GND 或 V_{CC}，以对逻辑功能更有意义或更方便者为准。

8.4.2 布局示例

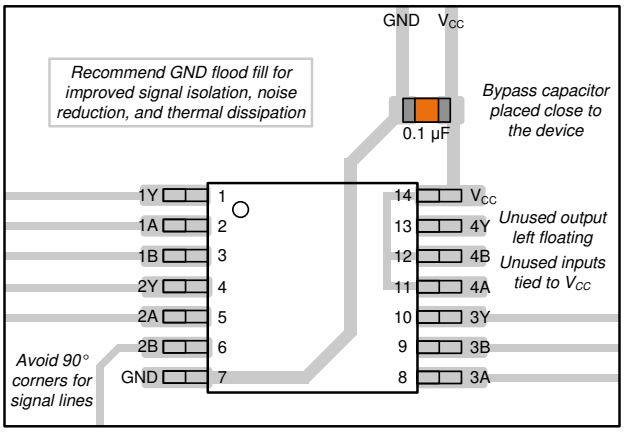


图 8-3. SNx4AHCT02 的示例布局

9 器件和文档支持

9.1 文档支持

9.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*CMOS 功耗与 Cpd 计算* 应用手册
- 德州仪器 (TI)，*CMOS 输入缓慢或悬空的影响* 应用手册
- 德州仪器 (TI)，*标准线性和逻辑 (SLL) 封装和器件的热特性* 应用手册

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision M (May 2023) to Revision N (February 2024)	Page
• 更新了 $R_{\theta JA}$ 值：RGY = 47 至 87.1，所有值均以 °C/W 为单位	5

Changes from Revision L (July 2003) to Revision M (May 2023)	Page
• 更新了*特性* 部分	1
• 添加了*应用* 部分	1
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 更新了*器件信息* 表以包含*通道数*	1
• 向数据表添加了 *BQA* 封装	1
• 添加了*引脚配置和功能* 部分	3

11 机械、封装和可订购信息

下述页面包含机械、封装和订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9757101Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9757101Q2A SNJ54AHCT 02FK	Samples
5962-9757101QCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9757101QC A SNJ54AHCT02J	Samples
5962-9757101QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9757101QD A SNJ54AHCT02W	Samples
SN74AHCT02BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT02	Samples
SN74AHCT02D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	AHCT02	
SN74AHCT02DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB02	Samples
SN74AHCT02DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB02	Samples
SN74AHCT02DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT02	Samples
SN74AHCT02N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHCT02N	Samples
SN74AHCT02NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT02	Samples
SN74AHCT02PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	HB02	
SN74AHCT02PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HB02	Samples
SN74AHCT02RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HB02	Samples
SNJ54AHCT02FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9757101Q2A SNJ54AHCT 02FK	Samples
SNJ54AHCT02J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9757101QC A SNJ54AHCT02J	Samples
SNJ54AHCT02W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9757101QD A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54AHCT02W	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54AHCT02, SN74AHCT02 :

- Catalog : SN74AHCT02

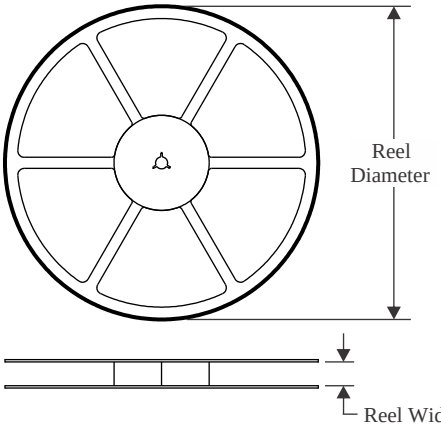
- Automotive : SN74AHCT02-Q1, SN74AHCT02-Q1
- Military : SN54AHCT02

NOTE: Qualified Version Definitions:

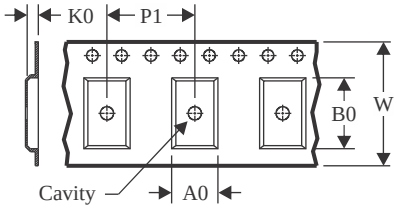
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

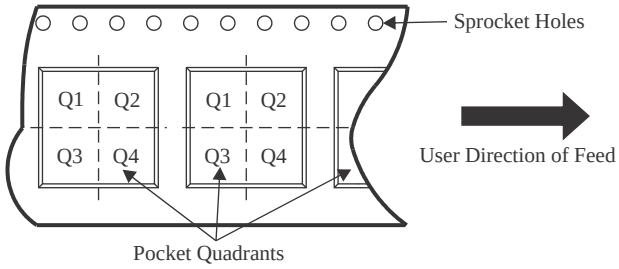


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

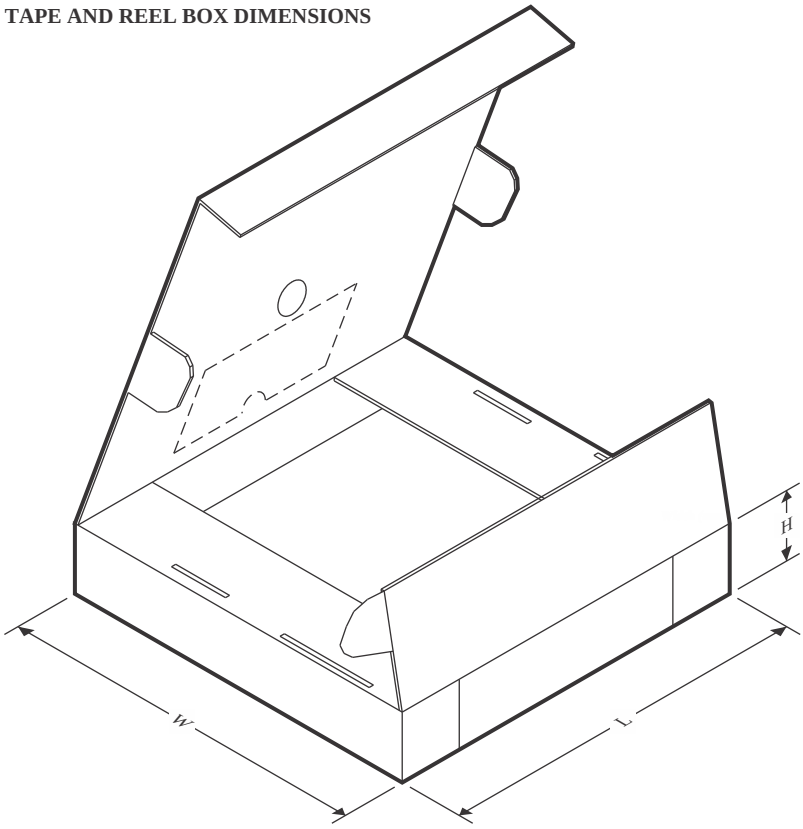
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT02BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHCT02DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT02DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHCT02DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHCT02NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHCT02PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT02PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT02RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

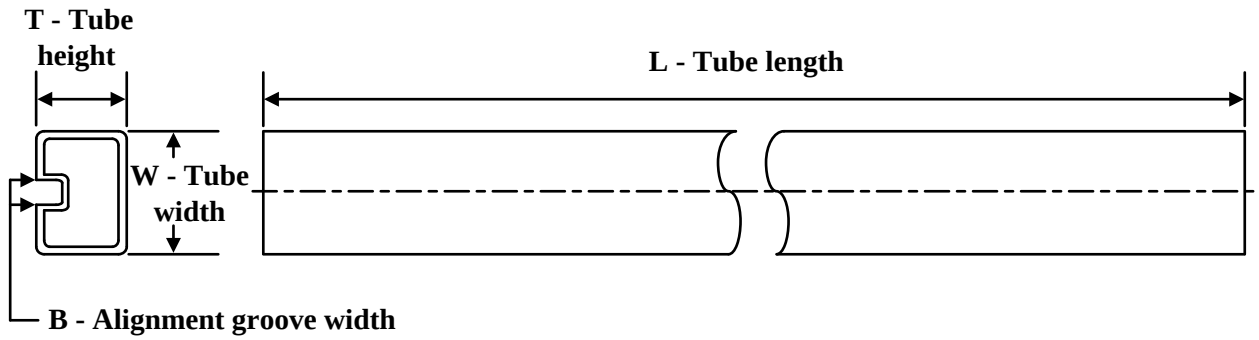
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT02BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHCT02DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHCT02DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHCT02DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AHCT02NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74AHCT02PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHCT02PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHCT02RGYR	VQFN	RGY	14	3000	360.0	360.0	36.0

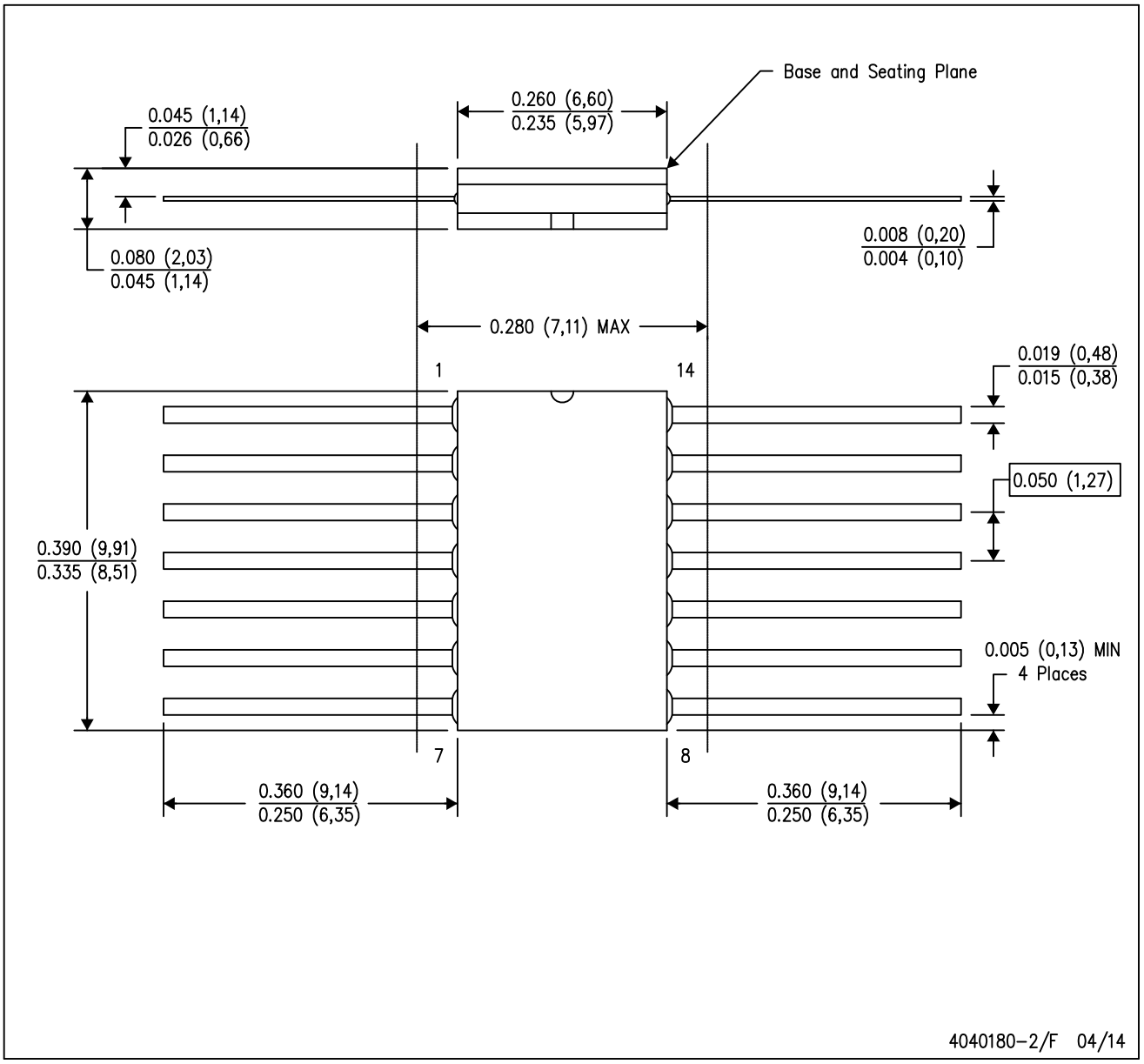
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9757101Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9757101QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHCT02N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHCT02N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHCT02FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT02W	W	CFP	14	25	506.98	26.16	6220	NA

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



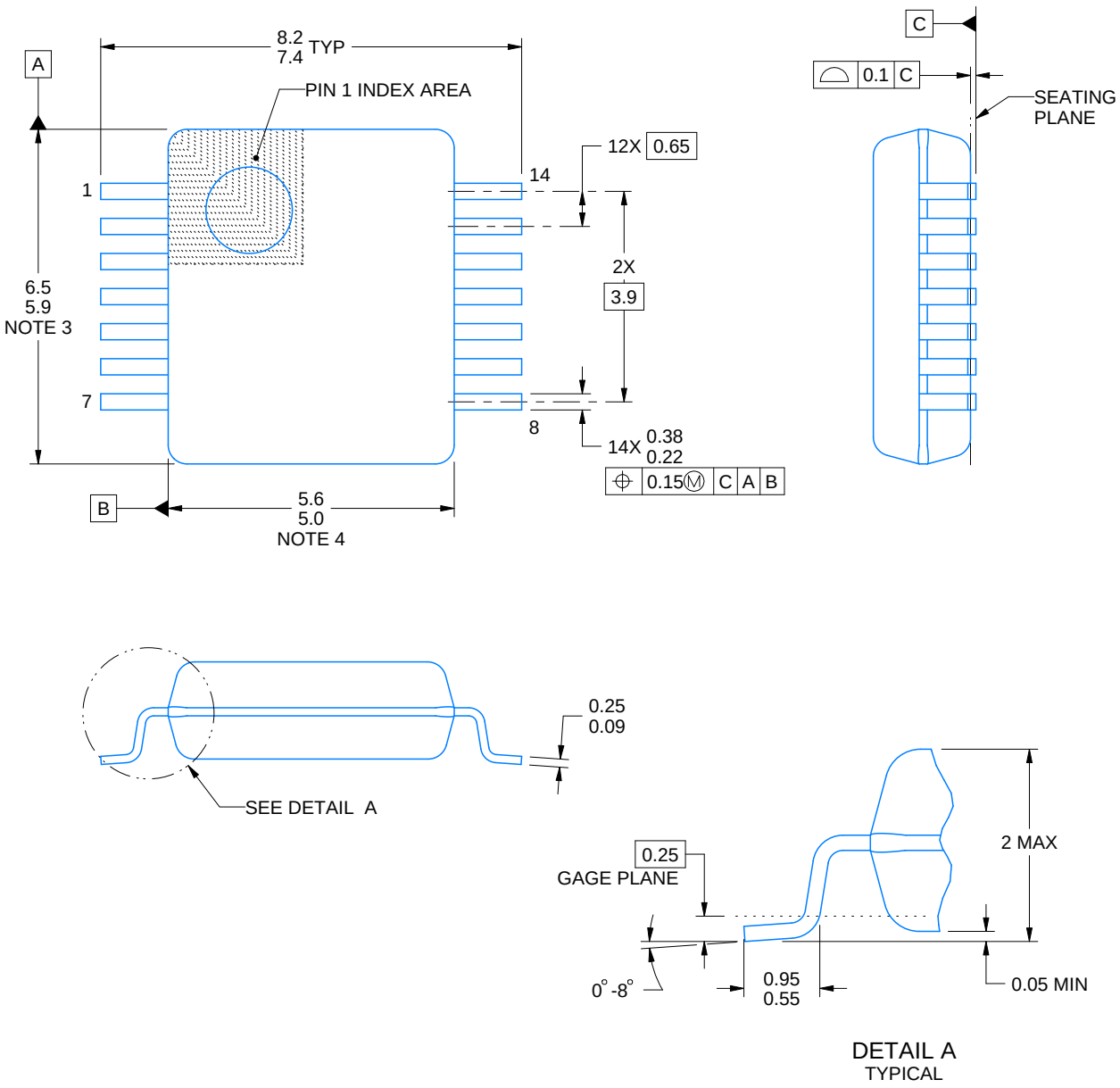
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



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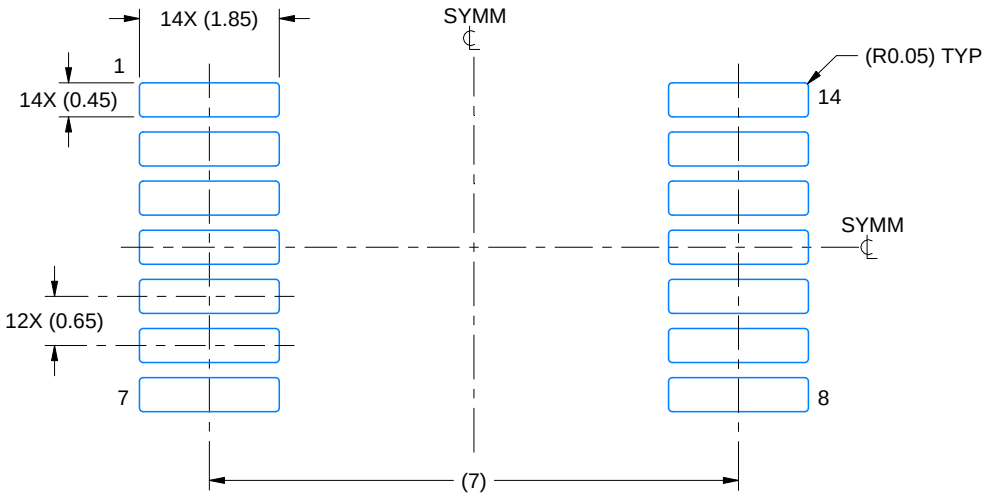
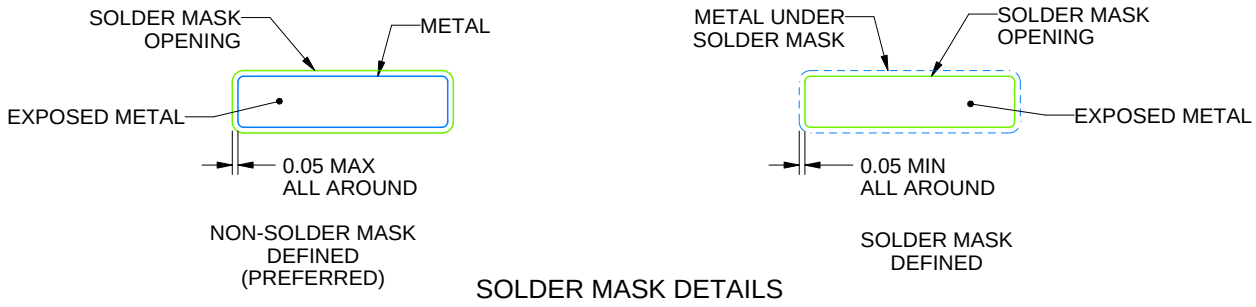
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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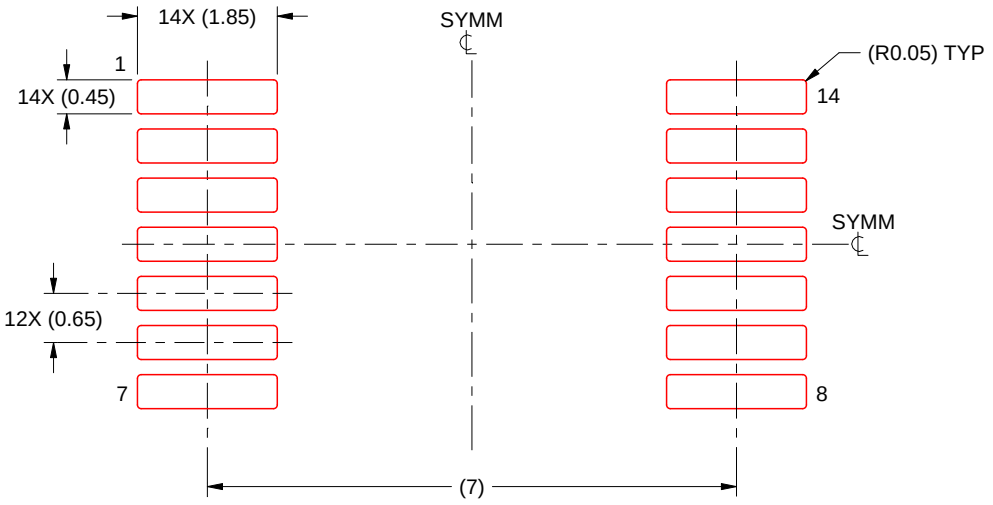
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

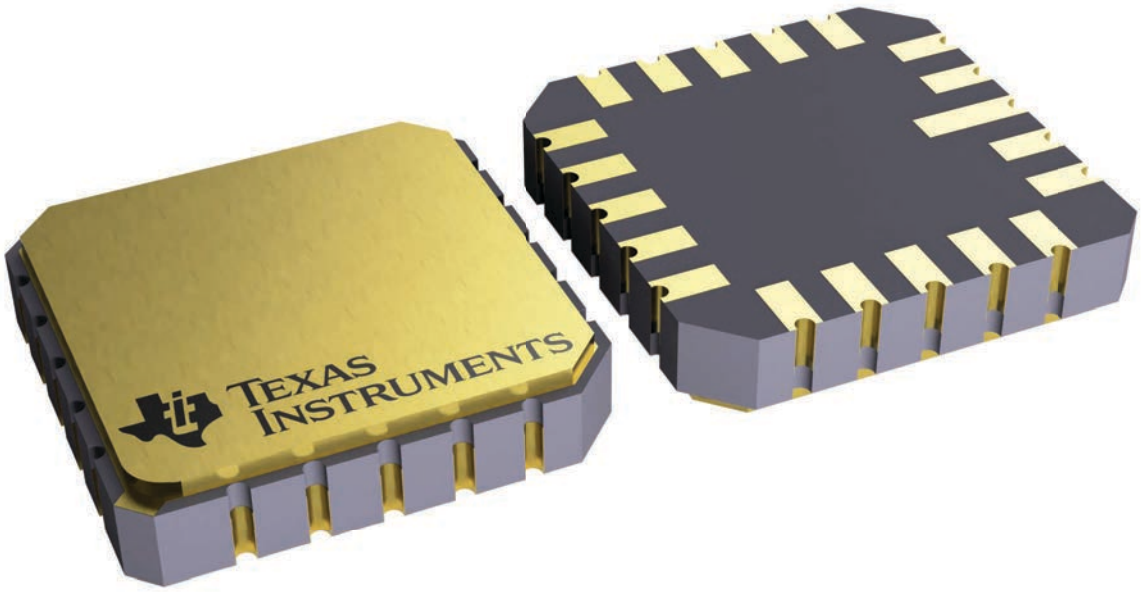
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

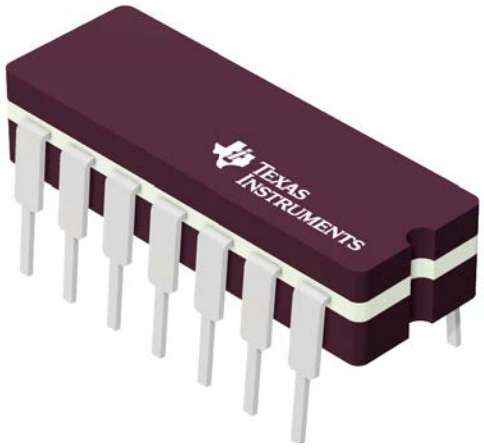


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

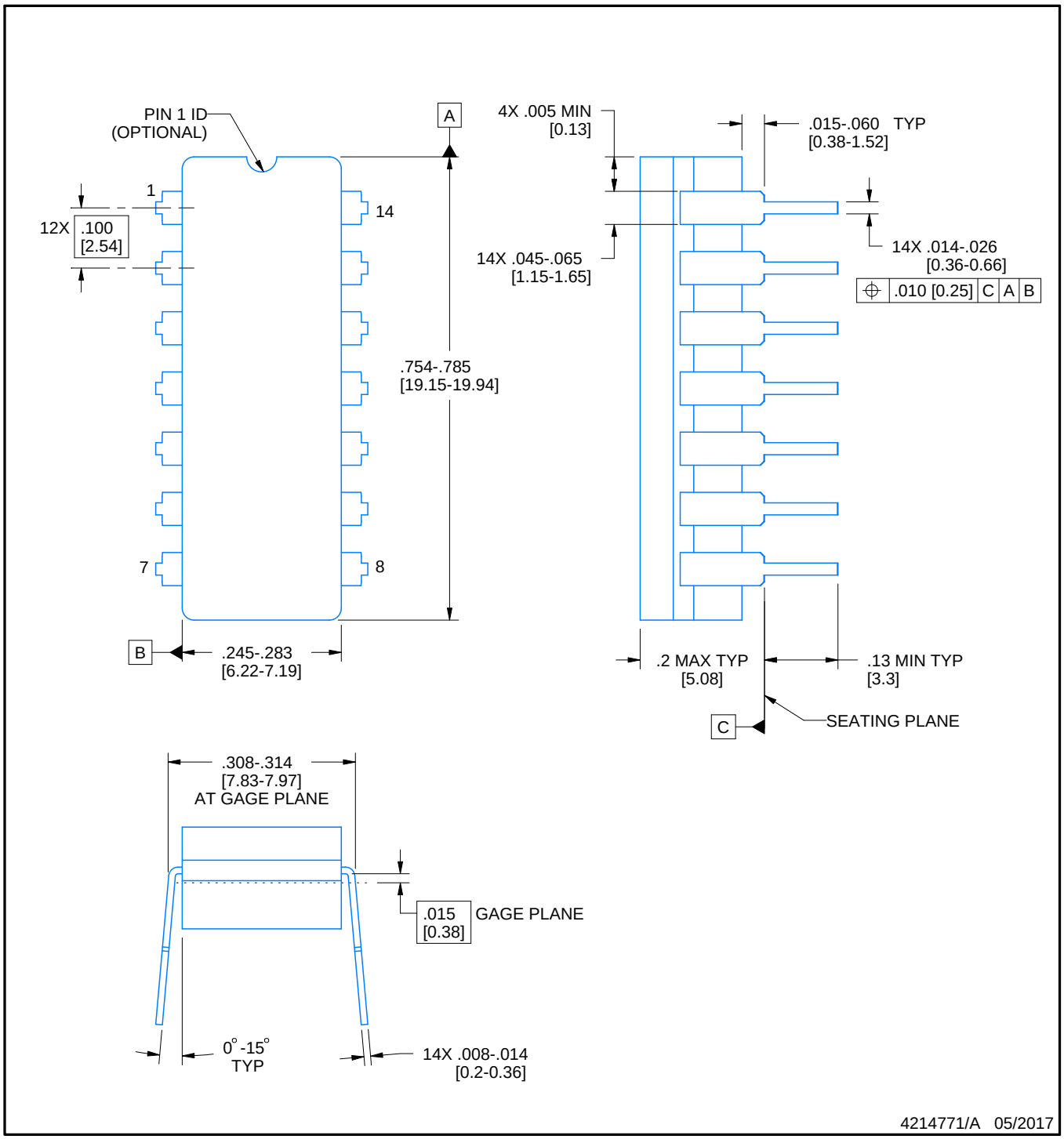
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

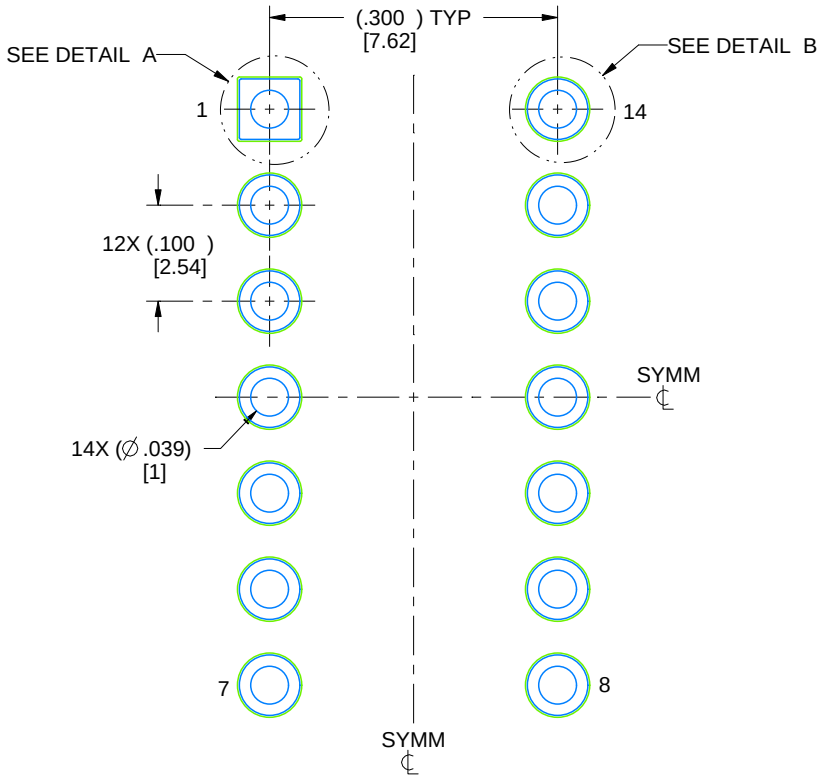
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

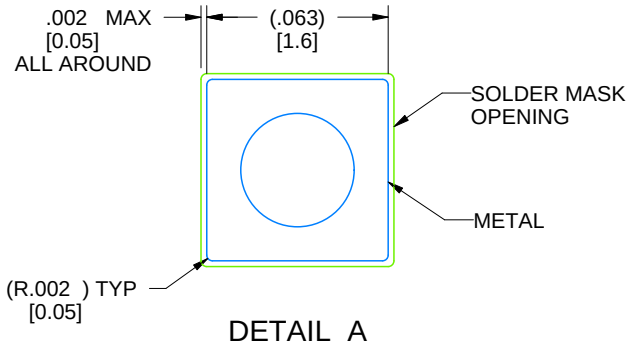
J0014A

CDIP - 5.08 mm max height

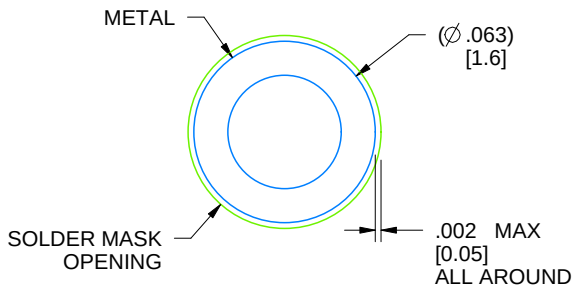
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



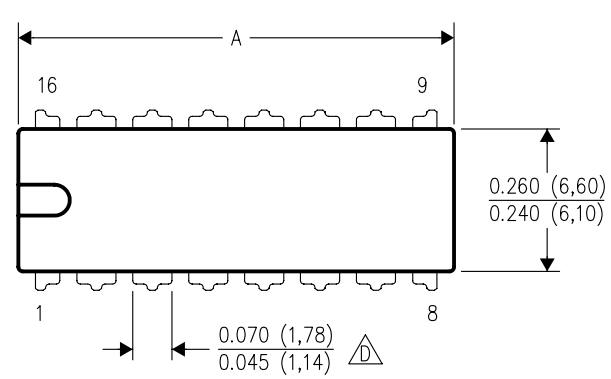
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

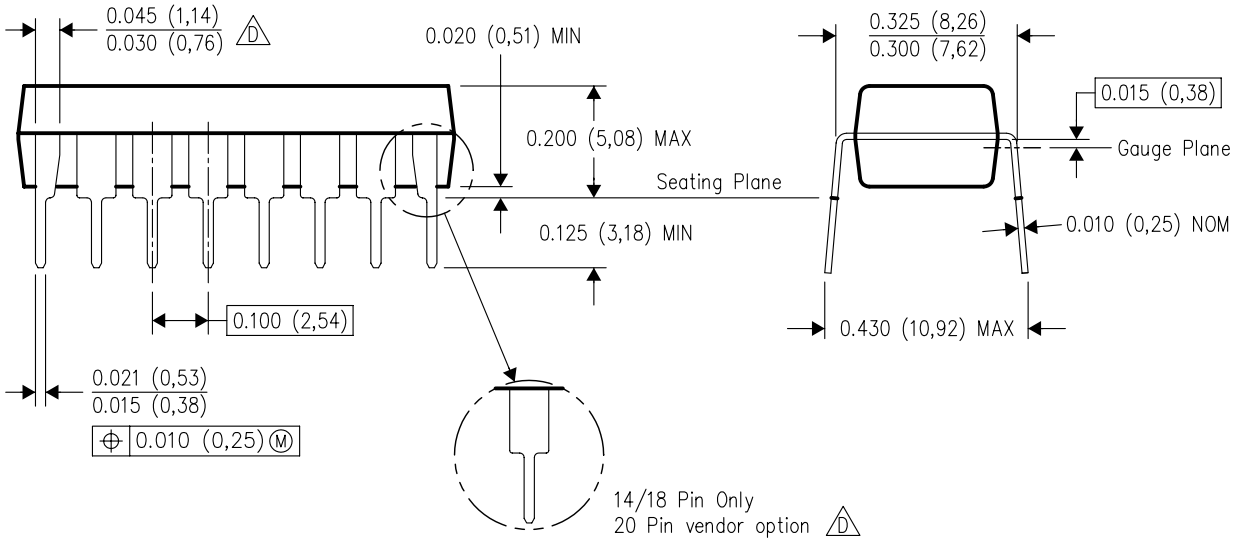
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

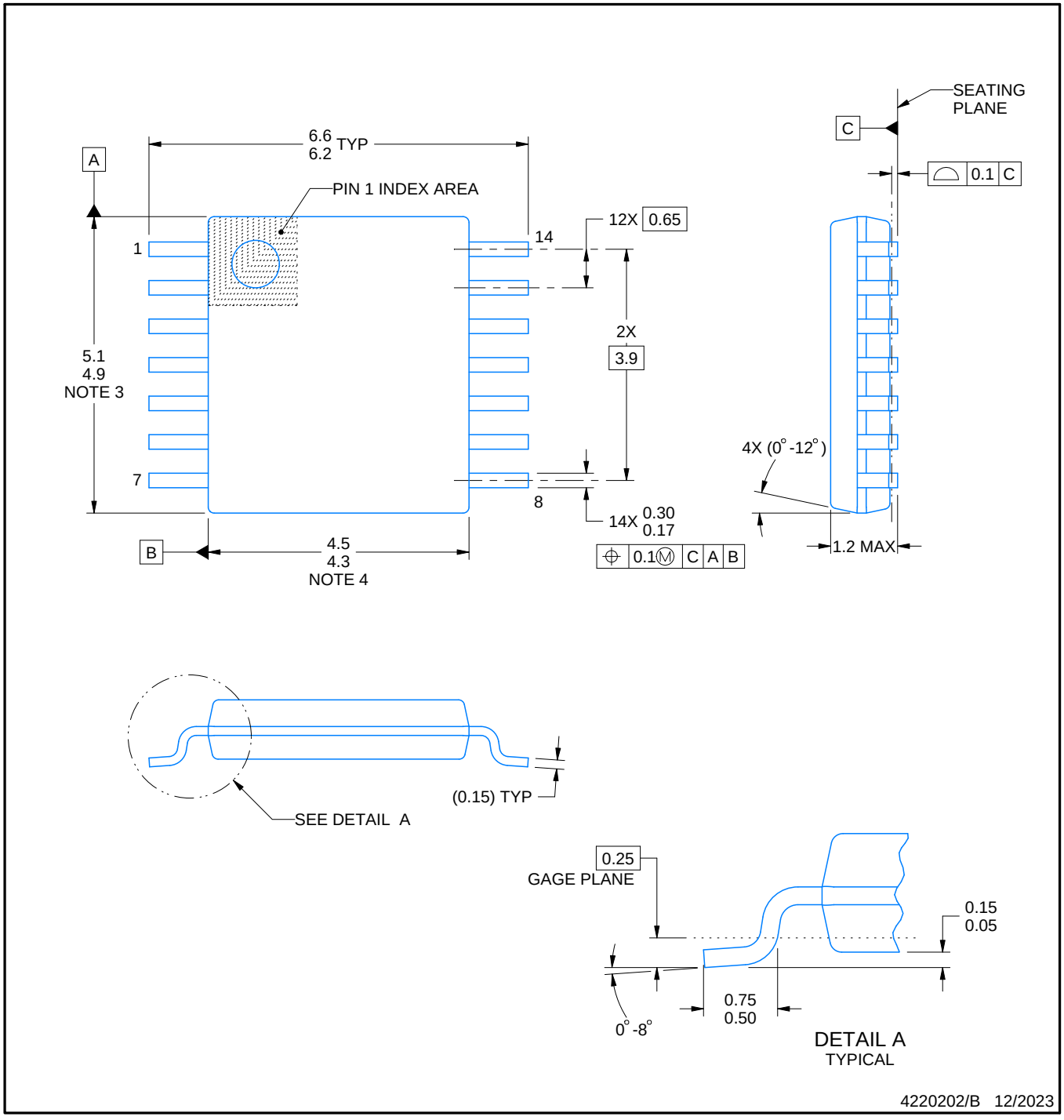
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

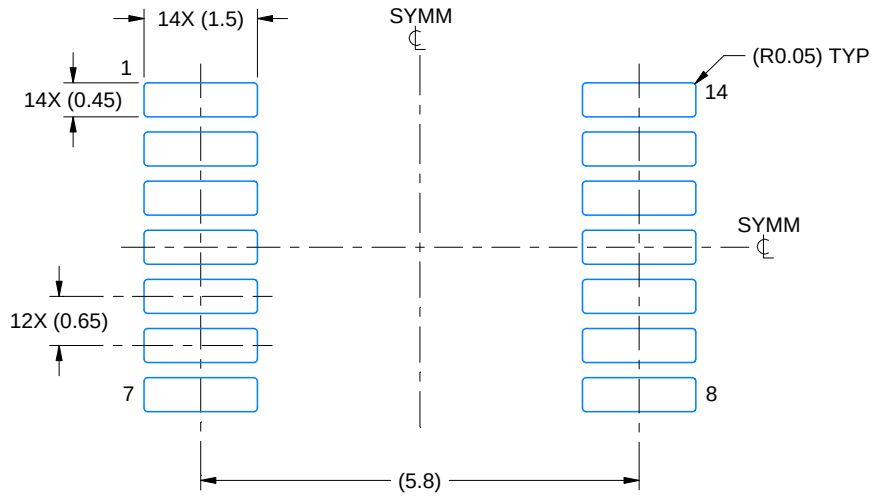
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

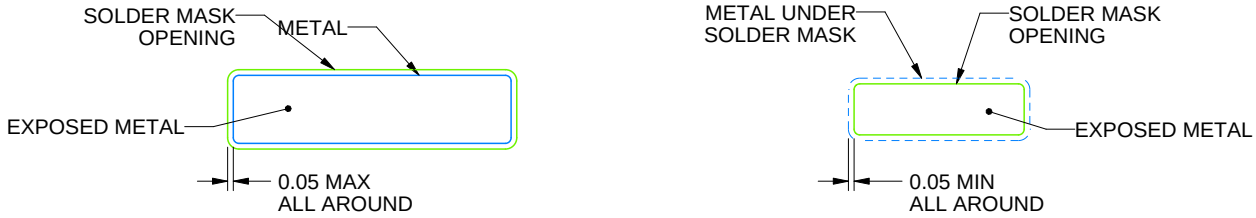


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

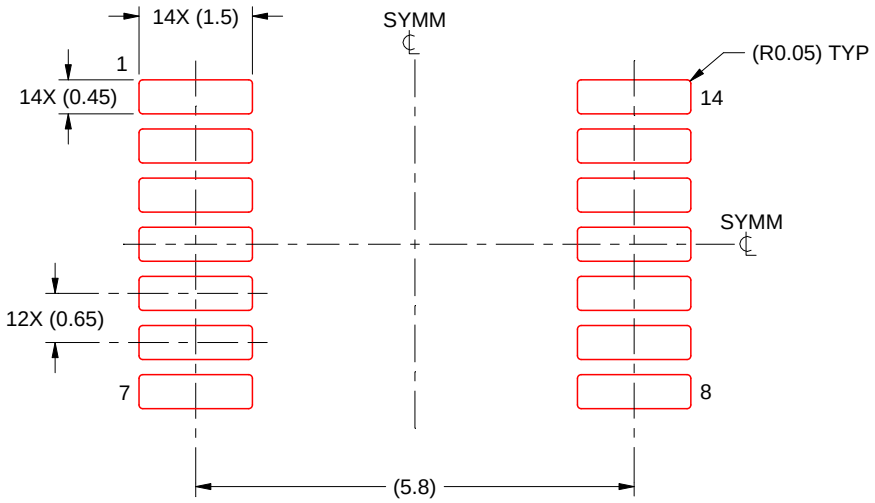


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

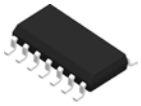


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

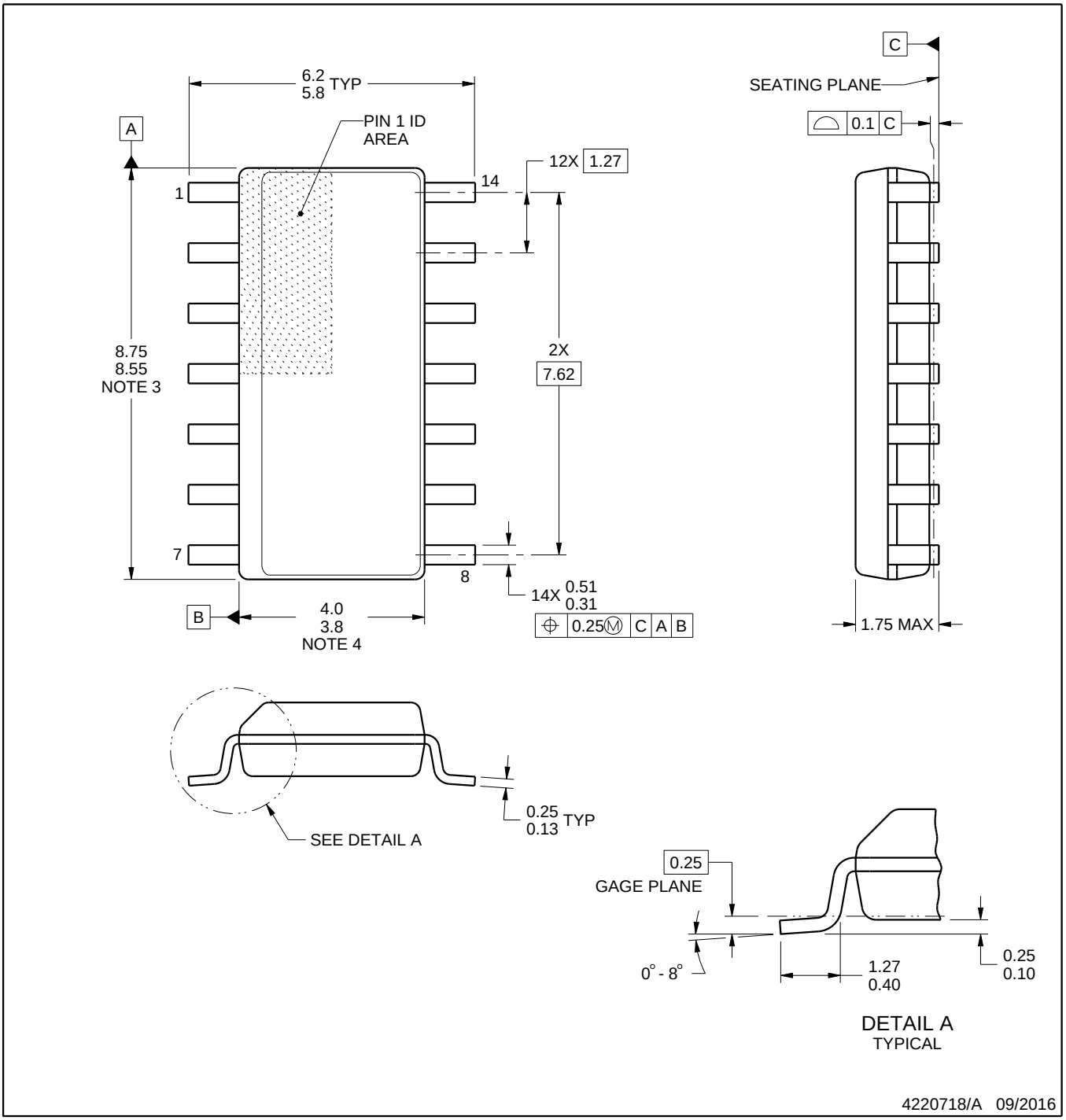


PACKAGE OUTLINE

D0014A

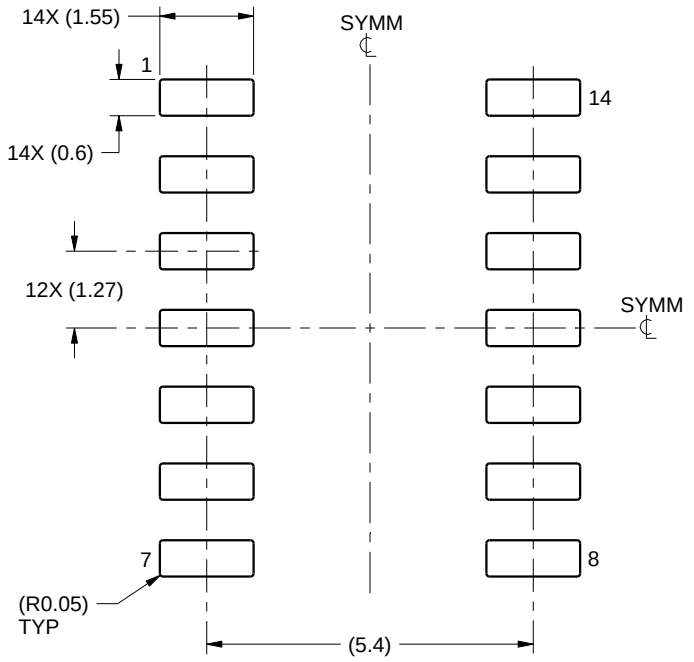
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

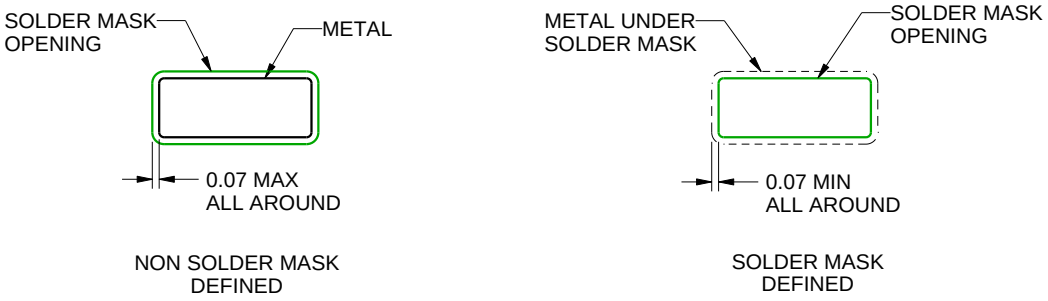


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

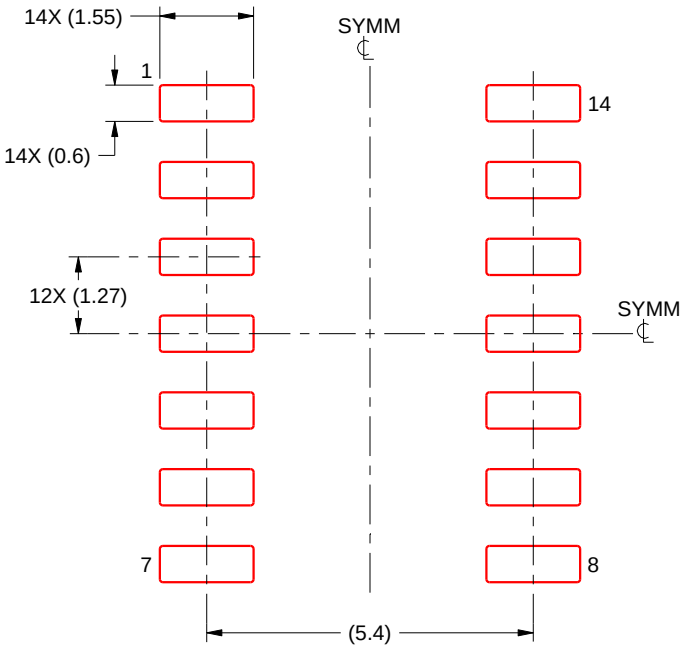
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



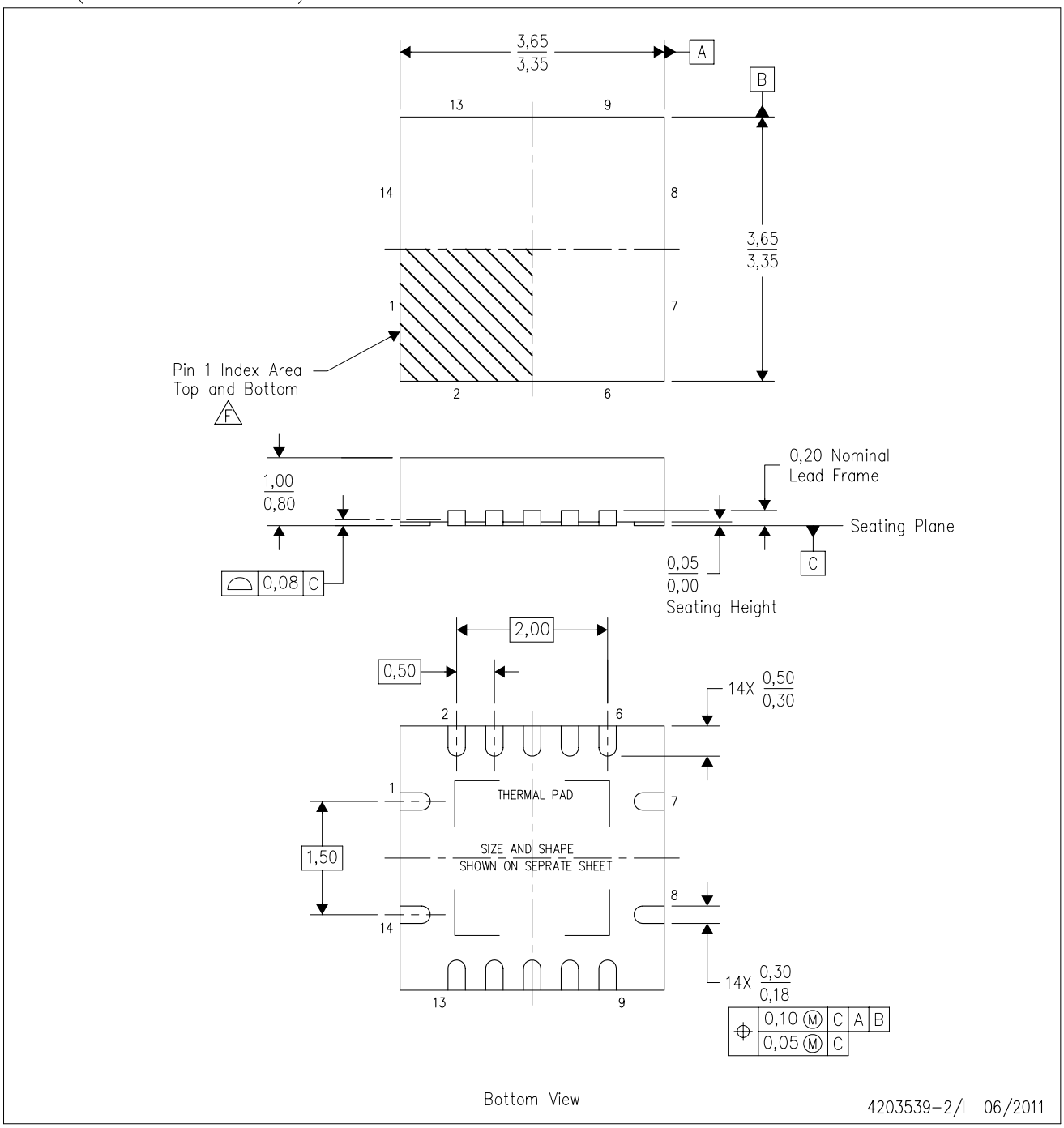
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

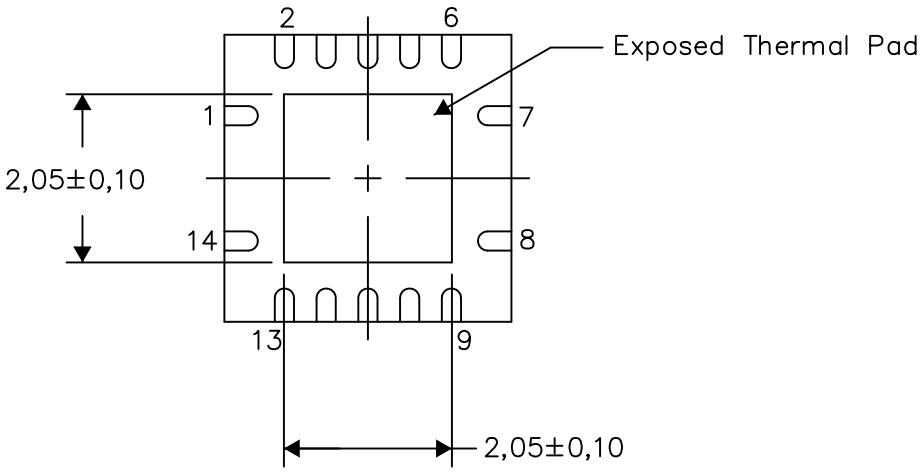
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



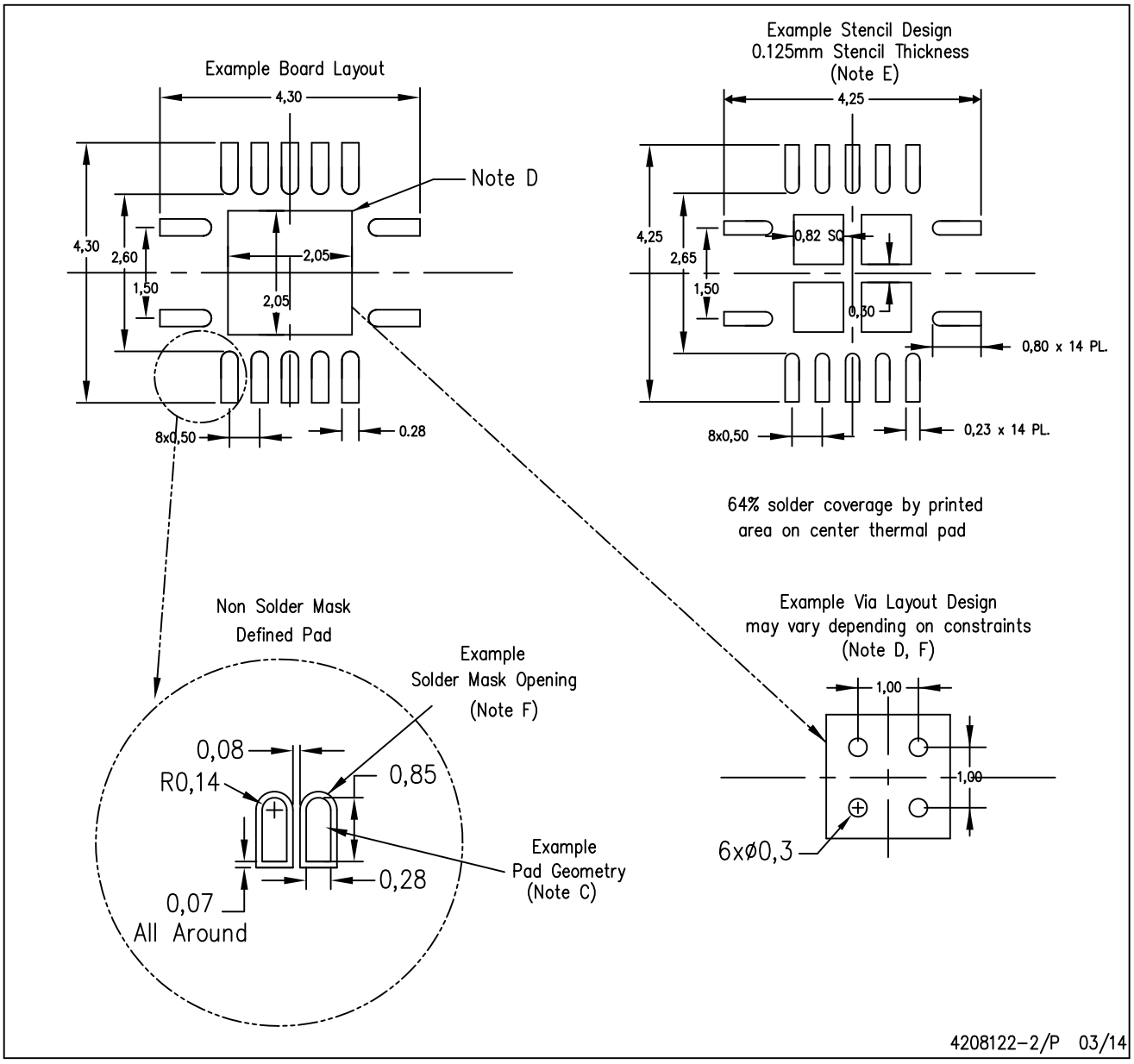
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

GENERIC PACKAGE VIEW

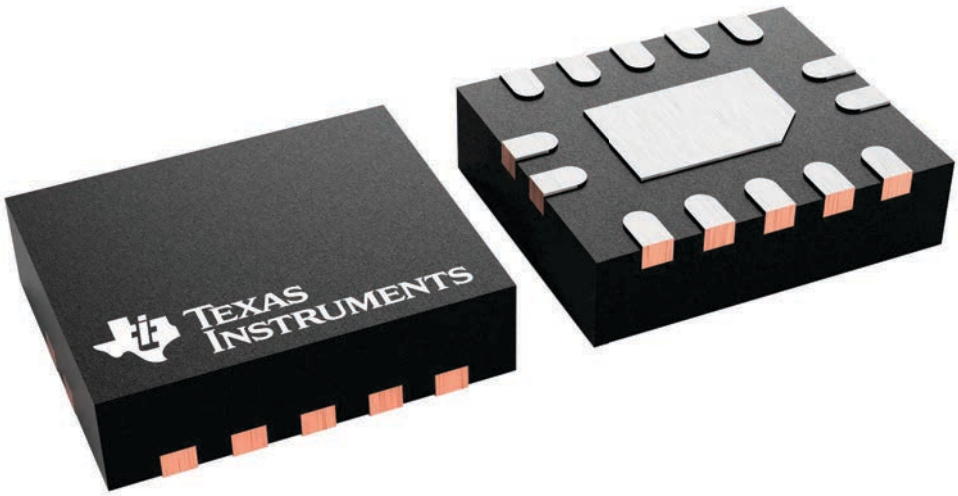
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

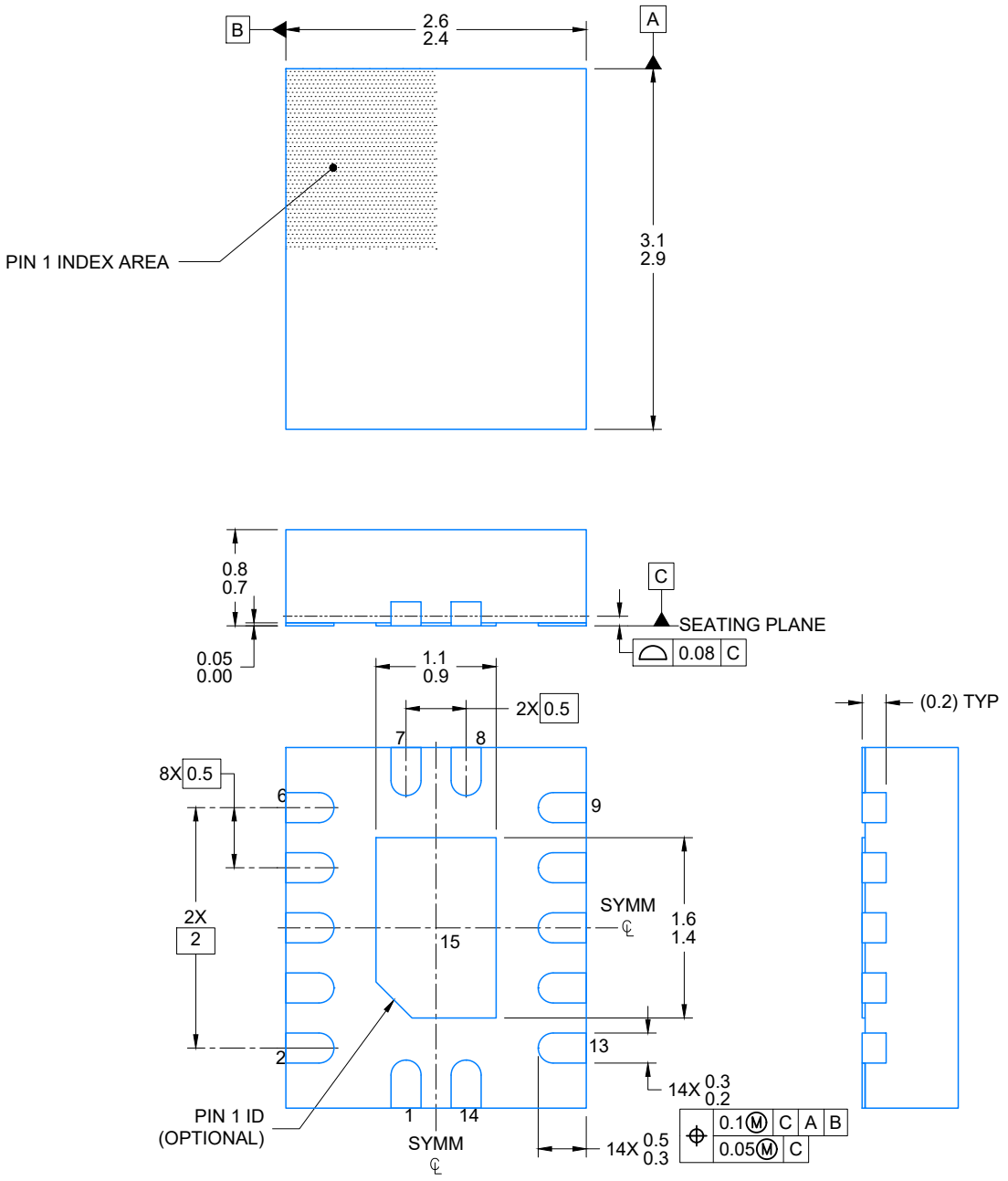


PACKAGE OUTLINE

BQA0014A

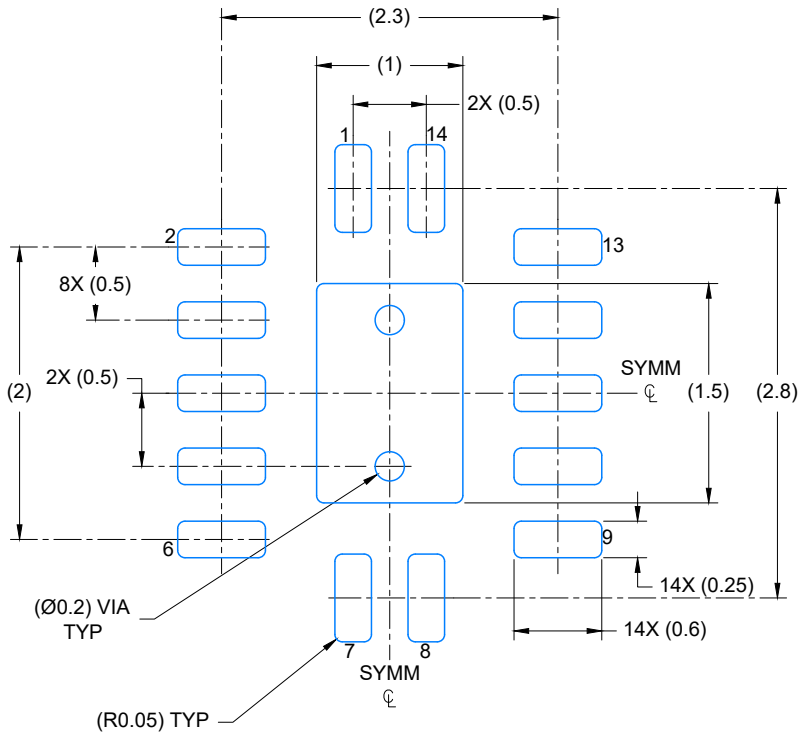
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

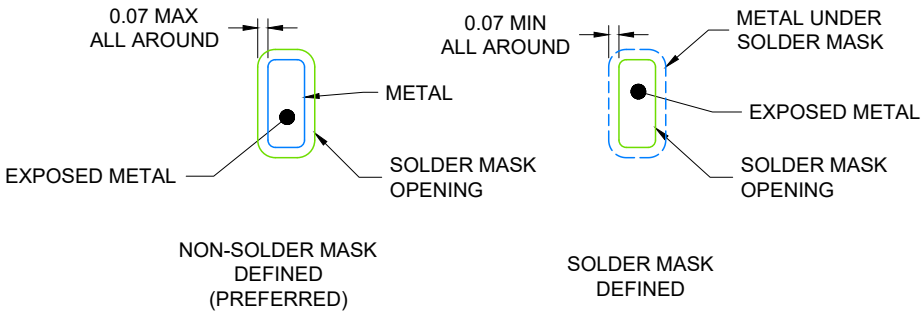


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



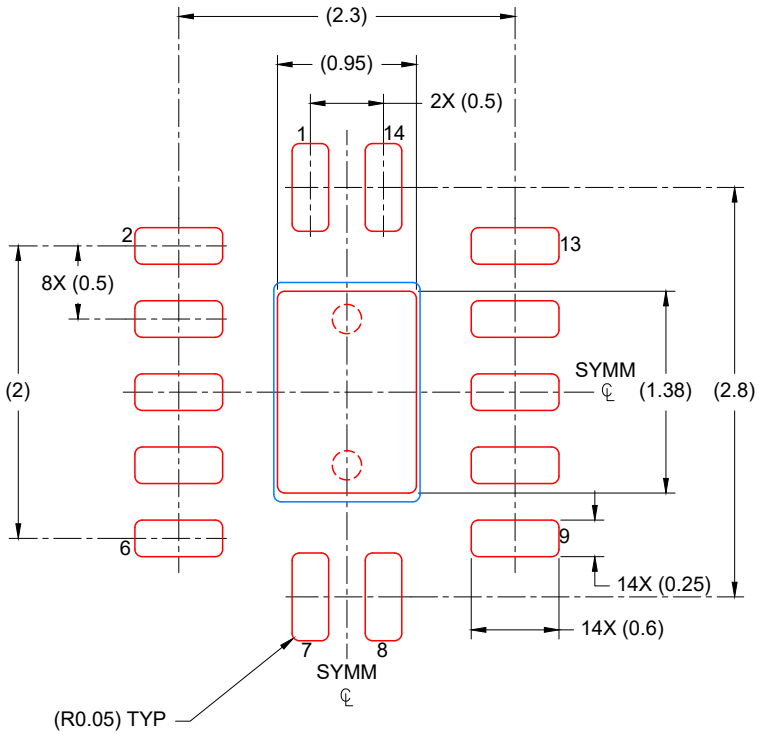
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

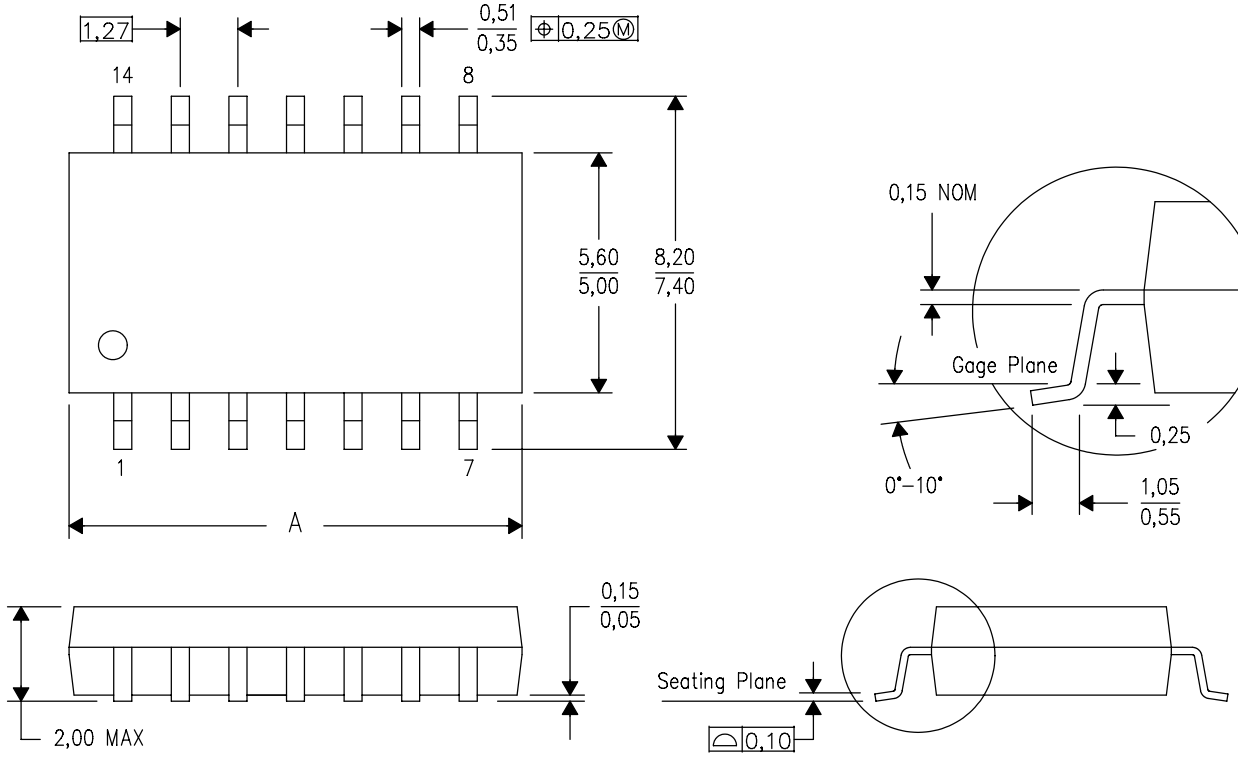
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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