

SN74AHCT1G125 具有三态输出的单路总线缓冲门

1 特性

- 工作电压范围为 4.5V 至 5.5V
- 电压为 5V 时， t_{pd} 最大值为 6ns
- 低功耗， I_{CC} 最大值为 10 μ A
- 电压为 5V 时，输出驱动为 ± 8 mA
- 输入兼容 TTL 电压
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- 无线基础设施
- 服务器
- 电力基础设施
- PC/笔记本电脑
- 可编程逻辑控制器
- 测试和测量

3 说明

SN74AHCT1G125 器件是一款具有三态输出的单通道总线缓冲门/线路驱动器。当输出使能 (\overline{OE}) 输入为高电平时，输出被禁用。当 \overline{OE} 为低电平时，数据从 A 输入传递到 Y 输出。

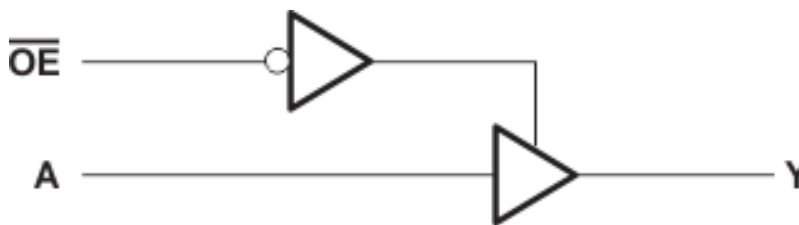
封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
SN74AHCT1G125	DBV (SOT-23 , 5)	2.9mm x 2.8mm	2.9mm x 1.6mm
	DCK (SC-70 , 5)	2mm x 2.1mm	2mm x 1.25mm
	DRL (SOT-553 , 5)	1.6mm x 1.6mm	1.6mm x 1.2mm

(1) 如需了解更多信息，请参阅第 11 节。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。

(3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



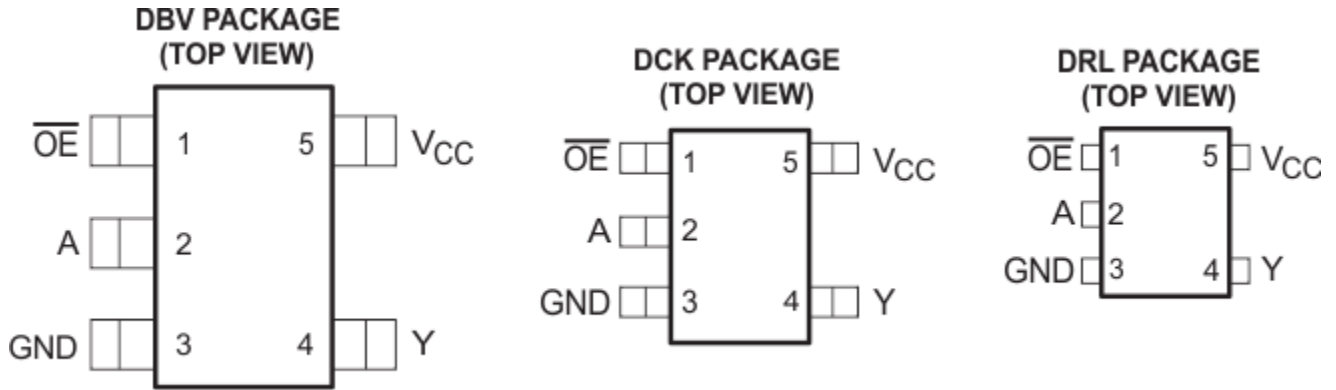
简化原理图



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4 Pin Configuration and Functions



See mechanical drawings for dimensions.

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	\overline{OE}	I	Output Enable
2	A	I	Input A
3	GND	—	Ground Pin
4	Y	O	Output Y
5	V_{CC}	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	- 0.5	7	V
V _I ⁽²⁾	Input voltage range	- 0.5	7	V
V _O ⁽²⁾	Output voltage range	- 0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		- 20 mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}		±20 mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±25 mA
	Continuous channel current through V _{CC} or GND			±50 mA
T _{stg}	Storage temperature range	- 65	150	°C
T _j	Junction temperature		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [# 5.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±1000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current		- 8	mA
I _{OL}	Low-level output current		8	mA
Δt/Δv	Input transition rise or fall rate		20	ns/V
T _A	Operating free-air temperature	- 40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* ([SCBA004](#)).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DBV	DCK	DRL	UNIT
		5 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278	289.2	328.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	180.5	205.8	105.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	184.4	176.2	150.3	
ψ_{JT}	Junction-to-top characterization parameter	115.4	117.6	6.9	
ψ_{JB}	Junction-to-board characterization parameter	183.4	175.1	148.4	
$R_{\theta JC(bot)}$	Junction-to-case (bot) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High level output voltage	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4	4.5		4.4	4.4	V	
				$I_{OH} = -8 \text{ mA}$	3.94		3.8	3.8		
V_{OL}	Low level output voltage	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1	0.1	0.1	V	
		$I_{OL} = 8 \text{ mA}$			0.36	0.44	0.44			
I_I	Input leakage current	$V_I = 5.5 \text{ V or GND}$	0 V to 5.5 V			± 0.1	± 1	± 1	μA	
I_{OZ}	Off-State (High-Impedance State) Output Current (of a 3-State Output)	$V_O = V_{CC} \text{ or GND}$	5.5 V			± 0.25	± 2.5	± 2.5	μA	
I_{CC}	Supply current	$V_I = V_{CC} \text{ or GND, } I_O = 0$	5.5 V			1	10	10	μA	
$\Delta I_{CC}^{(1)}$	Supply-current change	One input at 3.4 V, Other input at V_{CC} or GND	5.5 V			1.35	1.5	1.5	mA	
C_i	Input capacitance	$V_I = V_{CC} \text{ or GND}$	5 V		4	10	10	10	pF	
C_o	Output capacitance	$V_O = V_{CC} \text{ or GND}$	5 V		10				pF	

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC} .

5.6 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.8	5.5		1	6.5	1	7	ns
t_{PHL}				3.8	5.5	1	6.5	1	7		
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	3.6	5.1		1	6	1	6.5	ns
t_{PZL}				3.6	5.1	1	6	1	6.5		
t_{PHZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	4.6	6.8		1	8	1	8.5	ns
t_{PLZ}				4.6	6.8	1	8	1	8.5		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.3	7.5		1	8.5	1	9.5	ns
t_{PHL}				5.3	7.5	1	8.5	1	9.5		
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	5.1	7.1		1	8	1	9	ns
t_{PZL}				5.1	7.1	1	8	1	9		
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	6.1	8.8		1	10	1	11	ns
t_{PLZ}				6.1	8.8	1	10	1	11		

5.7 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	14	pF

5.8 Typical Characteristics

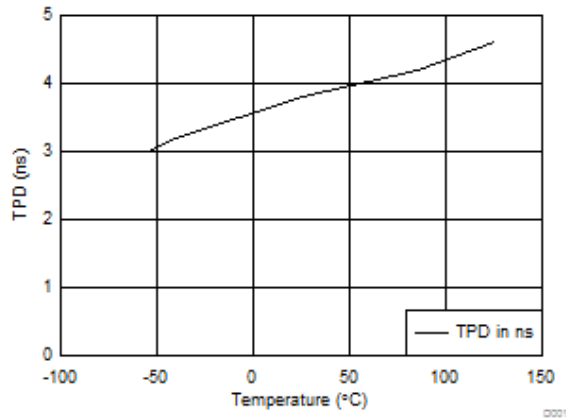
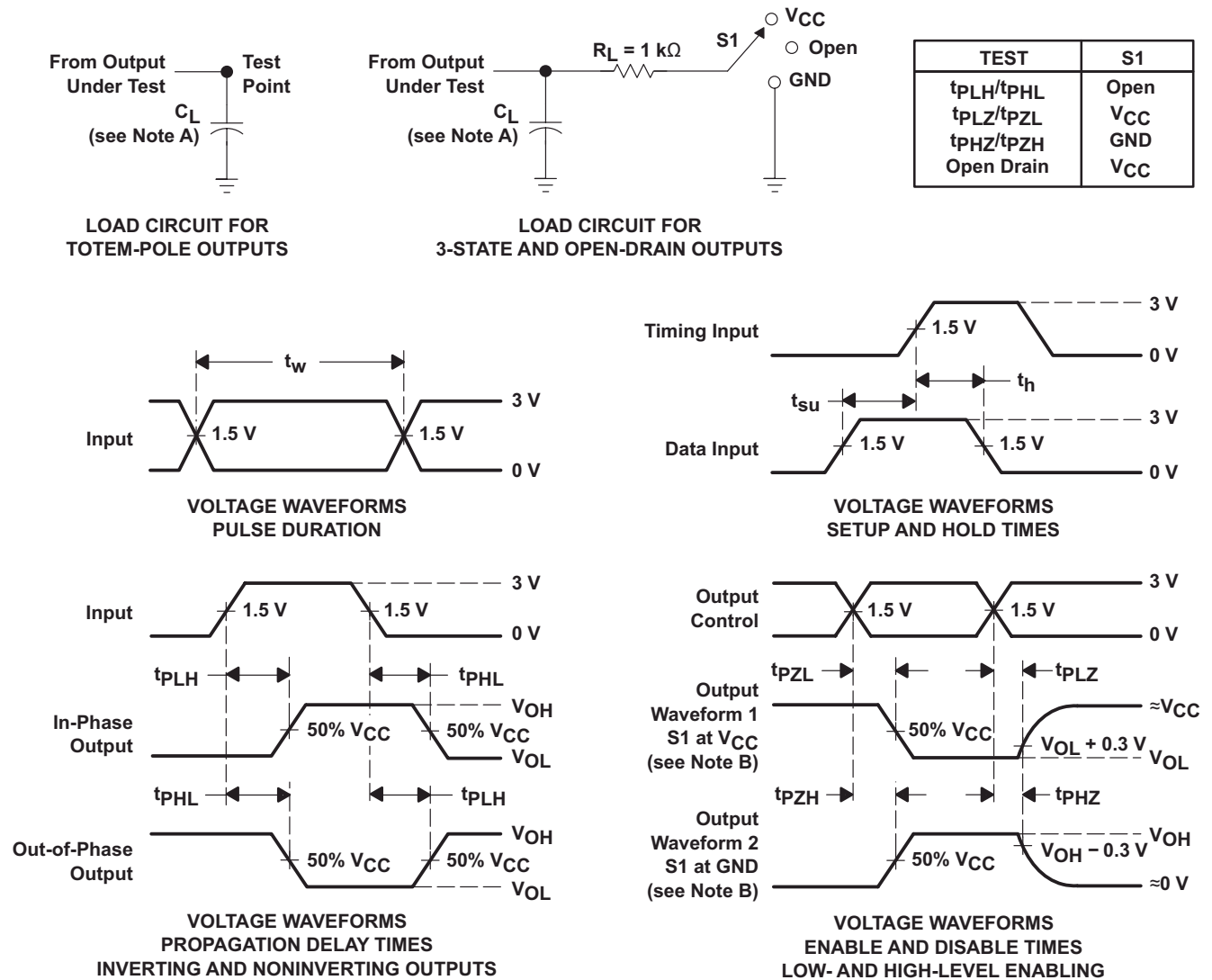


图 5-1. TPD vs Temperature

6 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 D. The outputs are measured one at a time, with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74AHCT1G125 device is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (\overline{OE}) input is high. When \overline{OE} is low, data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

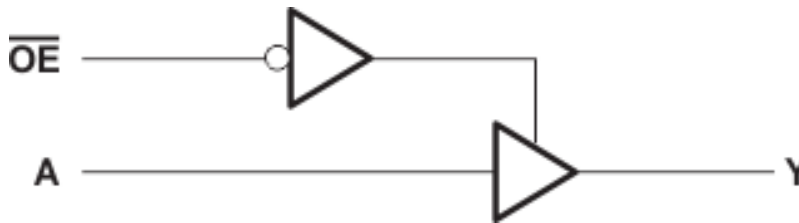


图 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

- TTL inputs
 - Lowered switching threshold allows up translation 3.3 V to 5 V
- Slow edges reduce output ringing

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS ⁽¹⁾		OUTPUT ⁽²⁾
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Don' t Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The SN74AHCT1G125 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8 V_{IL} and 2 V_{IH} . This feature makes it ideal for translating up from 3.3 V to 5 V . 图 8-1 shows this type of translation.

8.2 Typical Application

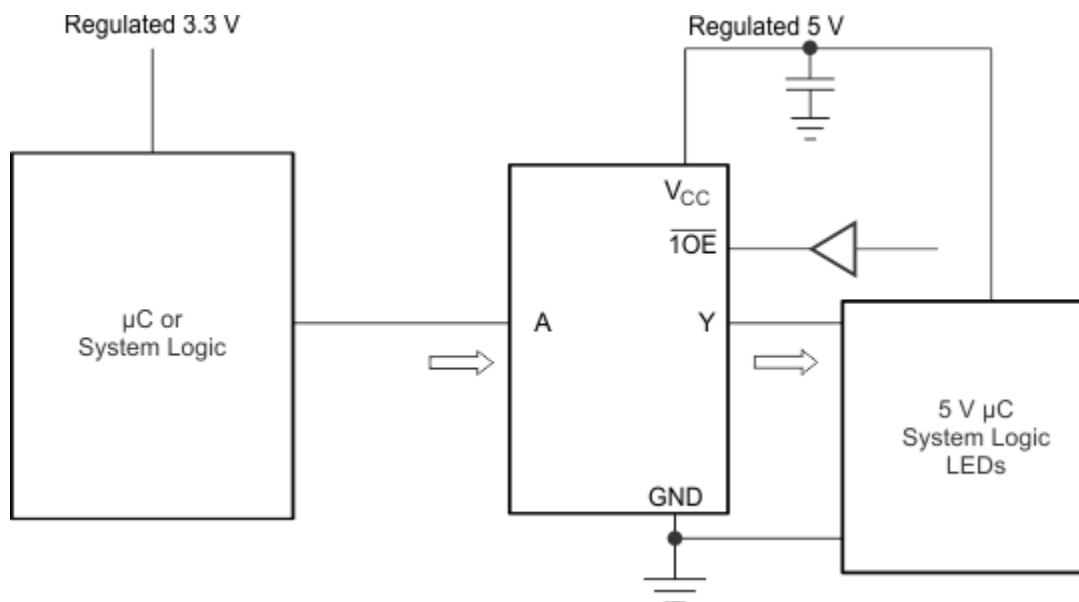


图 8-1. Typical Application Schematic

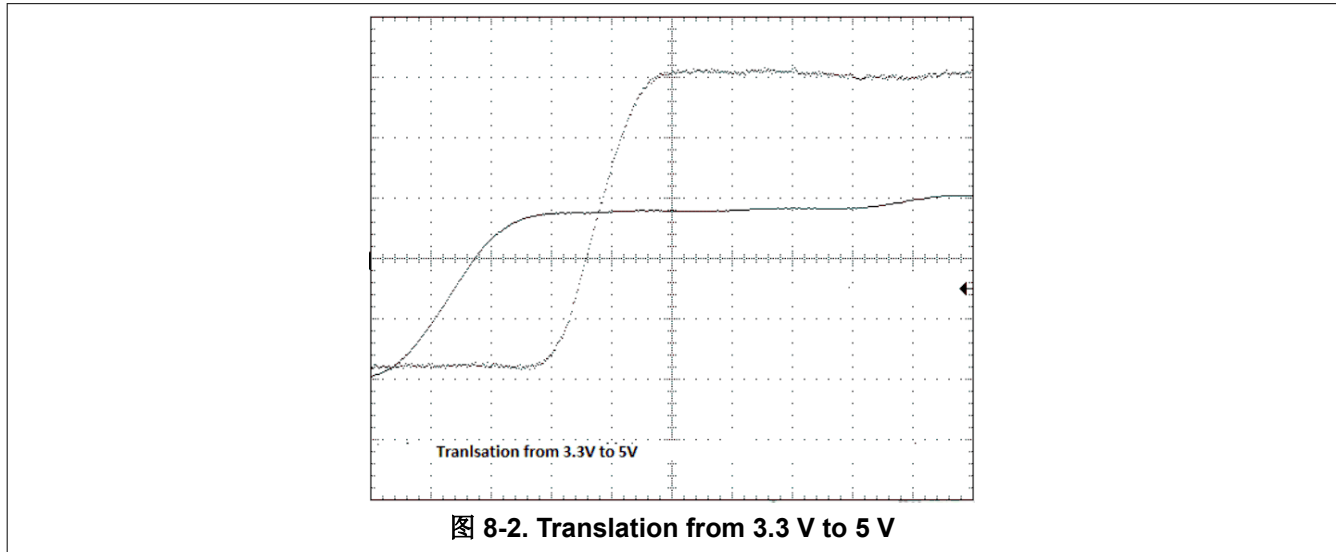
8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended Input Conditions
 - For rise time and fall time specifications, see $\Delta t / \Delta V$ in the 节 5.3 table.
 - For specified High and low levels, see V_{IH} and V_{IL} in the 节 5.3 table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

8.2.3 Application Curves



8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [表 5.3](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [图 8-3](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.4.1.1 Layout Example

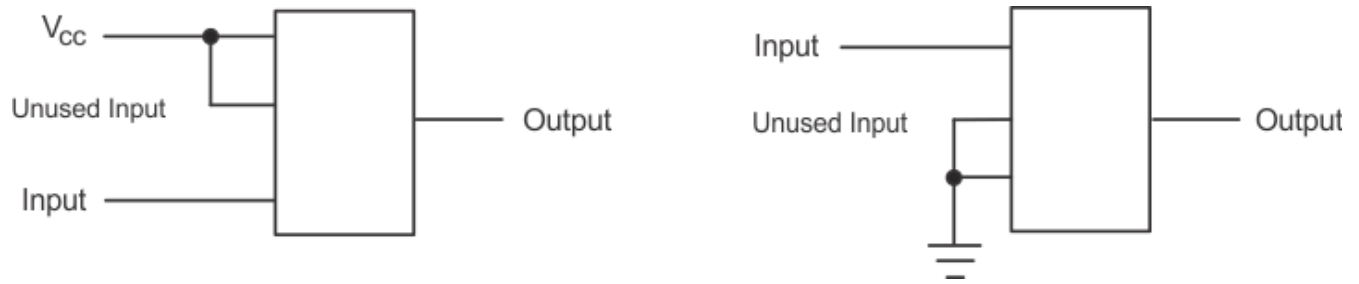


图 8-3. Layout Diagram

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

Changes from Revision O (October 2023) to Revision P (March 2024) Page

- 向 [封装信息](#) 表中添加了本体尺寸 1
- Updated thermal values for DBV package from $R_{\theta JA} = 231.3$ to 278, $R_{\theta JC(top)} = 119.9$ to 180.5, $R_{\theta JB} = 60.6$ to 184.4, $\Psi_{JT} = 17.8$ to 115.4, $\Psi_{JB} = 60.1$ to 183.4, $R_{\theta JC(bot)} = N/A$, all values in °C/W 5

Changes from Revision N (January 2016) to Revision O (October 2023) Page

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- Updated thermal values for DCK package from $R_{\theta JA} = 287.6$ to 289.2, $R_{\theta JC(top)} = 97.7$ to 205.8, $R_{\theta JB} = 65$ to 176.2, $\Psi_{JT} = 2.0$ to 117.6, $\Psi_{JB} = 64.2$ to 175.1, $R_{\theta JC(bot)} = N/A$, all values in °C/W 5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AHCT1G125DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B25G	Samples
74AHCT1G125DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B25G	Samples
74AHCT1G125DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM3	Samples
74AHCT1G125DCKTE4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM3	Samples
74AHCT1G125DCKTG4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BM3	Samples
SN74AHCT1G125DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(37QH, 3BEF, B253, B25G, B25J, B25L, B25S)	Samples
SN74AHCT1G125DCK3	ACTIVE	SC70	DCK	5	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 85	BMY	Samples
SN74AHCT1G125DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(BM3, BMG, BMJ, BML, BMS)	Samples
SN74AHCT1G125DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(BMB, BMS)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHCT1G125 :

- Automotive : [SN74AHCT1G125-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AHCT1G125DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHCT1G125DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
74AHCT1G125DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
74AHCT1G125DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHCT1G125DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHCT1G125DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AHCT1G125DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74AHCT1G125DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
74AHCT1G125DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
74AHCT1G125DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHCT1G125DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AHCT1G125DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHCT1G125DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0

DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



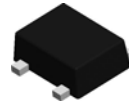
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

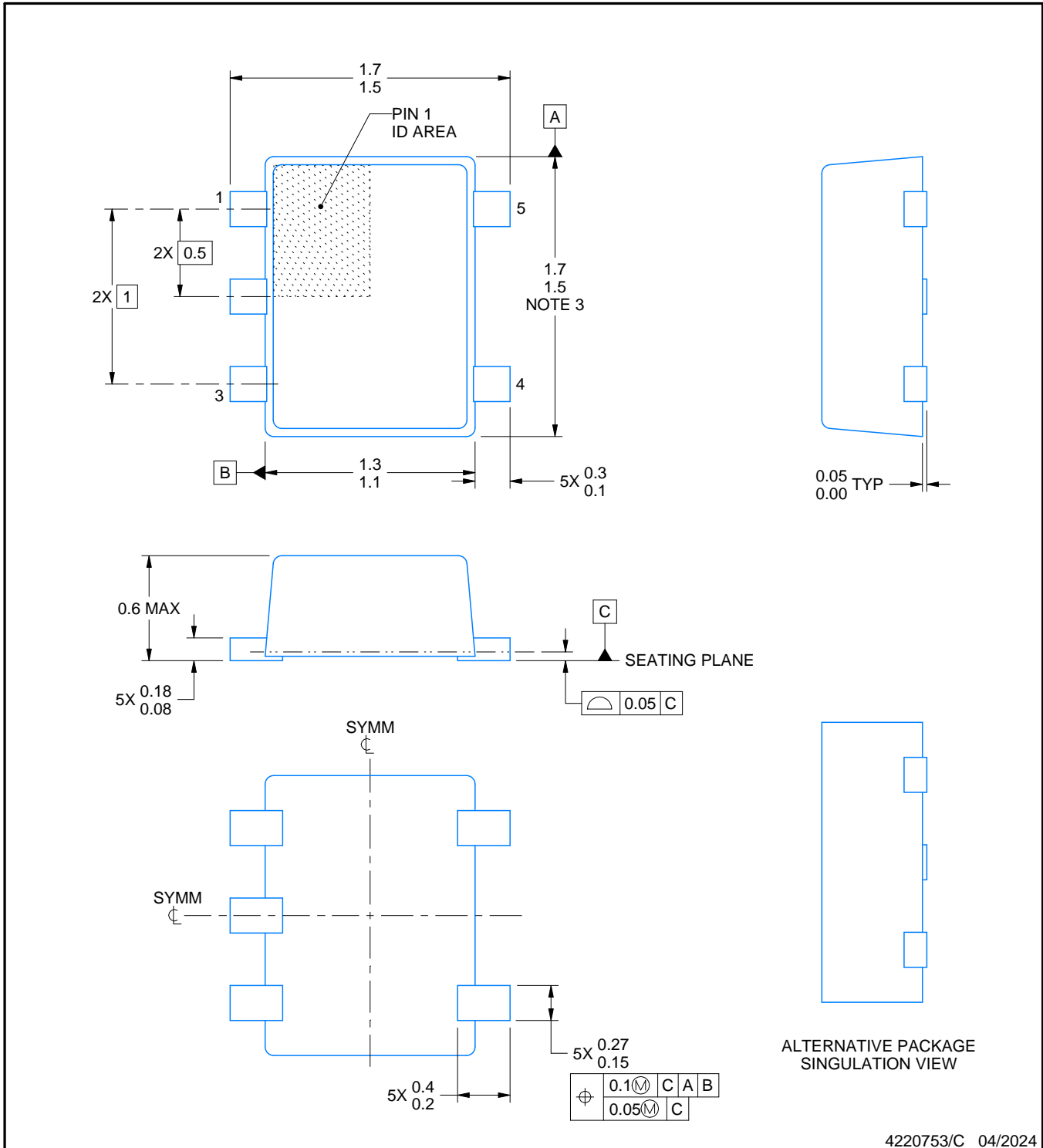
DRL0005A



PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4220753/C 04/2024

NOTES:

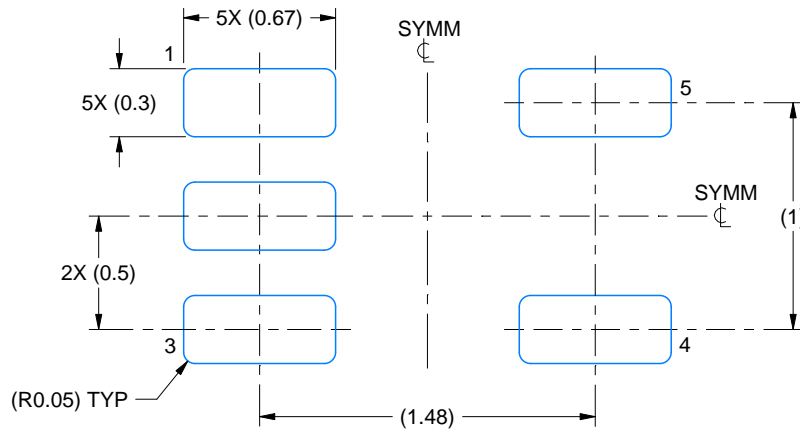
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

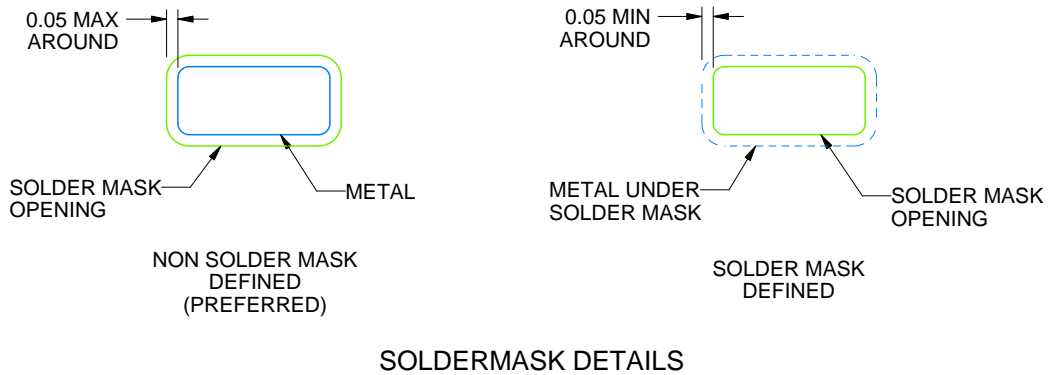
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/C 04/2024

NOTES: (continued)

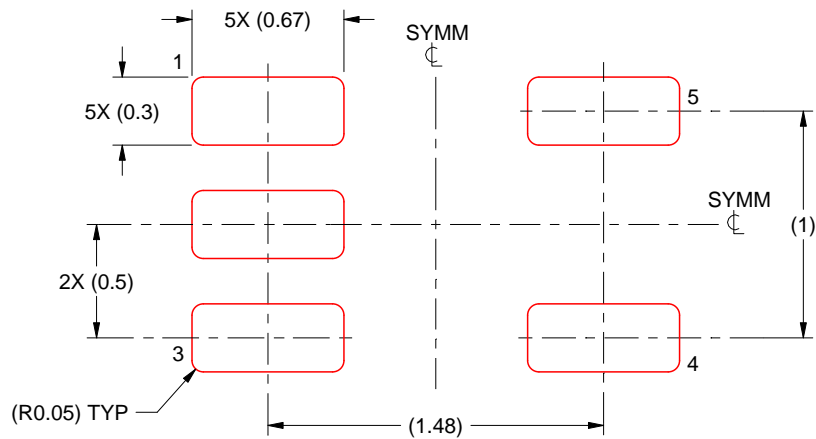
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/C 04/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

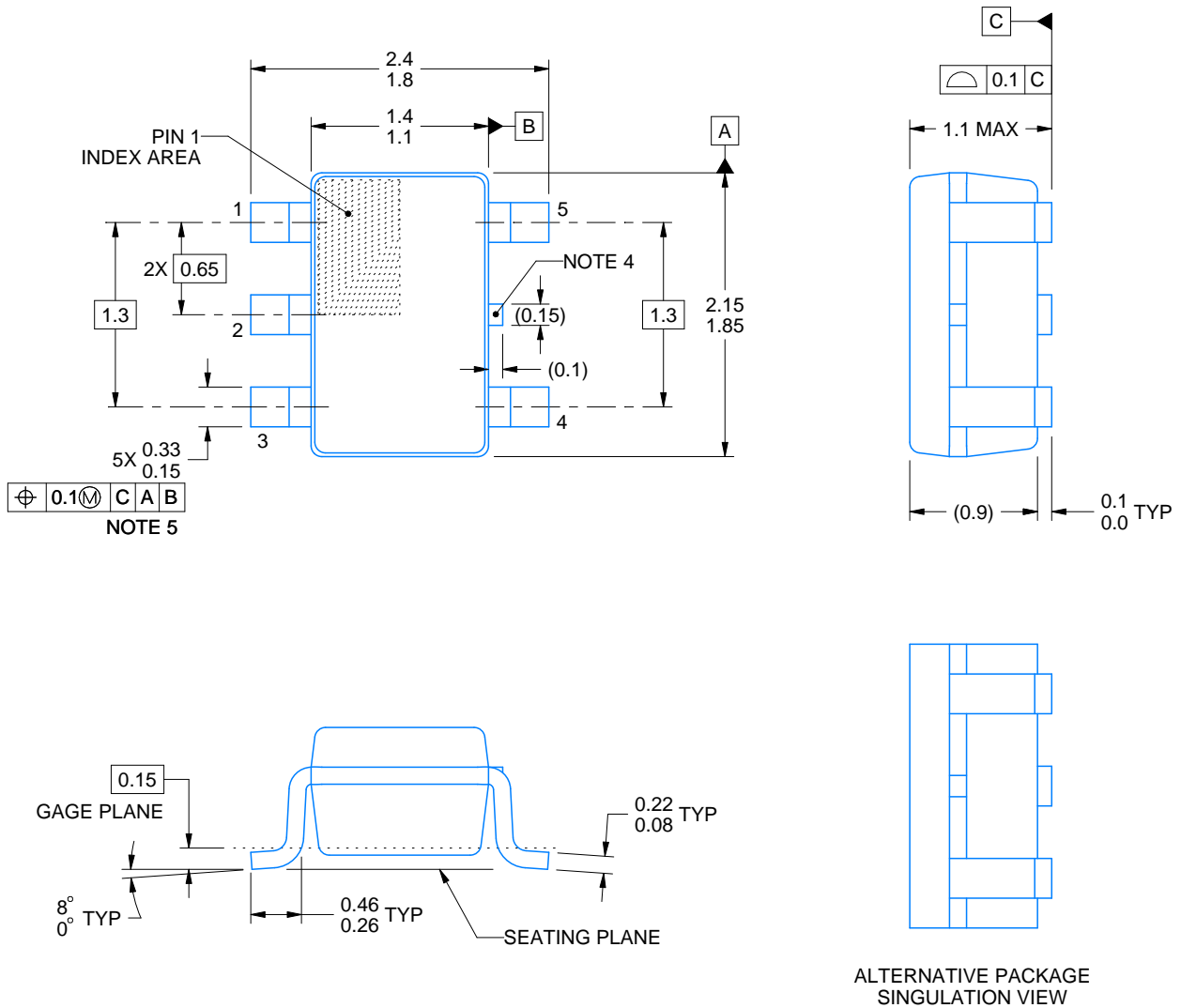
DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/E 06/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/E 06/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE: 18X

4214834/E 06/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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