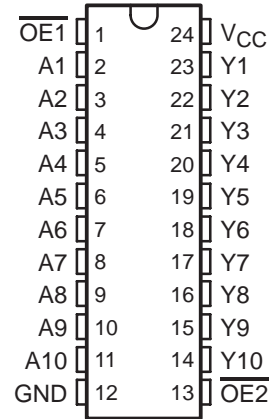


# SN54BCT2827C, SN74BCT2827C 10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS

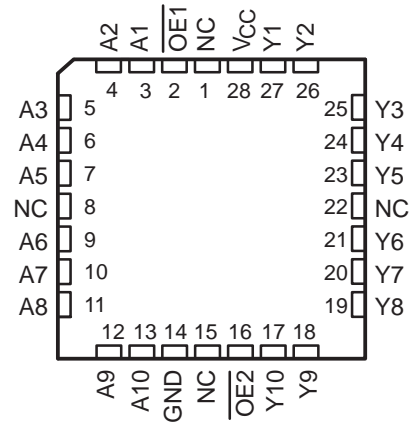
SCBS007E – APRIL 1987 – REVISED NOVEMBER 1993

- BiCMOS Design Substantially Reduces  $I_{CCZ}$
- Output Ports Have Equivalent 25- $\Omega$  Resistors; No External Resistors Are Required
- Specifically Designed to Drive MOS DRAMs
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Flow-Through Architecture Optimizes PCB Layout
- Power-Up High-Impedance State
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPs (JT, NT)

SN54BCT2827C . . . JT OR W PACKAGE  
SN74BCT2827C . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54BCT2827C . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

## description

These 10-bit buffers and bus drivers are specifically designed to drive the capacitive input characteristics of MOS DRAMs. They provide high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all ten outputs are in the high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down.

The SN54BCT2827C is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74BCT2827C is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

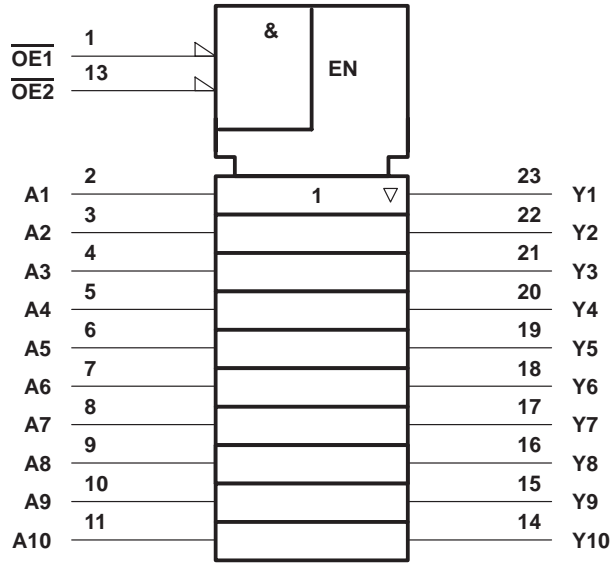
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

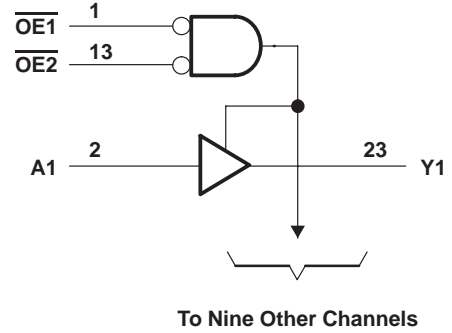
# SN54BCT2827C, SN74BCT2827C 10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS

SCBS007E – APRIL 1987 – REVISED NOVEMBER 1993

## logic symbol†

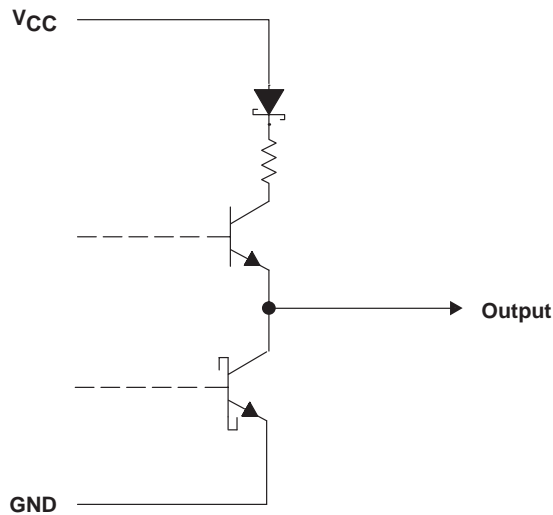


## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the DW, JT, NT, and W packages.

## schematic of each output



# SN54BCT2827C, SN74BCT2827C 10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS

SCBS007E – APRIL 1987 – REVISED NOVEMBER 1993

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ .....	–0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$ .....	–0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ .....	–30 mA
Current into any output in the low state .....	24 mA
Operating free-air temperature range: SN54BCT2827C .....	–55°C to 125°C
SN74BCT2827C .....	0°C to 70°C
Storage temperature range .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

## recommended operating conditions

		SN54BCT2827C			SN74BCT2827C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			–18			–18	mA
$I_{OH}$	High-level output current			–1			–1	mA
$I_{OL}$	Low-level output current			12			12	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54BCT2827C			SN74BCT2827C			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			–1.2			–1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $I_{OH} = -1\text{ mA}$	$V_{CC}-2$			$V_{CC}-2$			V
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 1\text{ mA}$	0.15	0.5	0.15	0.5		V
		$I_{OL} = 12\text{ mA}$	0.35	0.8	0.35	0.8		
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.7\text{ V}$			20			20	μA
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 0.5\text{ V}$			–20			–20	μA
$I_{OL(sink)}$	$V_{CC} = 4.5\text{ V}$ , $V_O = 2\text{ V}$	50			50			mA
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			20			20	μA
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.5\text{ V}$			–0.2			–0.2	mA
$I_{O}^{\S}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	–30		–112	–30		–112	mA
$I_{CCL}$	$V_{CC} = 5.5\text{ V}$ , Outputs open		28	40		28	40	mA
$I_{CCZ}$	$V_{CC} = 5.5\text{ V}$ , Outputs open		3.8	6		3.8	6	mA
$C_i$	$V_{CC} = 5\text{ V}$ , $V_I = 2.5\text{ V or } 0.5\text{ V}$		5			5		pF
$C_o$	$V_{CC} = 5\text{ V}$ , $V_I = 2.5\text{ V or } 0.5\text{ V}$		8			8		pF

‡ All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current,  $I_{OS}$ .



# SN54BCT2827C, SN74BCT2827C 10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS

SCBS007E – APRIL 1987 – REVISED NOVEMBER 1993

## switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			74BCT2827C			SN54BCT2827C		SN74BCT2827C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	0.9	3.6	5.2	0.9	6.6	0.9	6	ns
t <sub>PHL</sub>			2	5.1	7.2	2	8.2	2	7.8	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Y	2.8	5.6	8	2.8	10.7	2.8	10.7	ns
t <sub>PZL</sub>			5	8.9	11	5	13.7	5	12.9	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Y	3.2	6.7	8.5	3.2	14	3.2	13	ns
t <sub>PLZ</sub>			2.7	5.3	10.5	2.7	11	2.7	10	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74BCT2827CDW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT2827C	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74BCT2827CDW	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated