

SN74CBTLV3126 低电压四通道 FET 总线开关

1 特性

- 标准 126 型引脚
- 两个端口间使用 5Ω 开关连接
- 支持在数据 I/O 端口进行轨到轨开关
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范

2 应用

- 数据中心和企业计算
- 宽带固定线路接入
- 楼宇自动化
- 有线网络
- 电机驱动器

3 说明

SN74CBTLV3126 四通道 FET 总线开关具有独立的线路开关。当每个开关的相关输出使能 (OE) 输入为低电平时，开关被禁用。

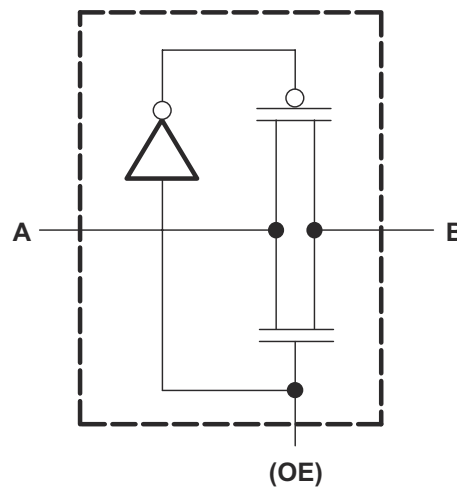
该器件专用于使用 I_{off} 的局部断电应用。 I_{off} 特性确保在关断时防止损坏电流通过器件回流。SN74CBTLV3126 器件可在电源关断时提供隔离。

为确保在上电或掉电期间均处于高阻抗状态，应将 OE 通过下拉电阻器接地；该电阻器的最小值取决于驱动器的灌电流能力。

封装信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
SN74CBTLV3126	SOIC (D , 14)	8.65mm × 3.91mm
	TVSOP (DGV , 14)	3.60mm × 4.40mm
	TSSOP (PW , 14)	5.00mm × 4.40mm
	VQFN (RGY , 14)	4.00mm × 3.50mm
	SSOP (DBQ , 16)	4.90mm × 3.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



每个 FET 开关的简化版原理图



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision K (June 2021) to Revision L (August 2022)	Page
• Updated the <i>Overview</i> section.....	8

Changes from Revision J (January 2019) to Revision K (June 2021)	Page
• 更新了整个文档中的表格、图和交叉引用的编号格式.....	1
• Changed <i>active low</i> to <i>active high</i> in the <i>Pin Configurations and Functions</i> section to reflect logic description change.....	3

Changes from Revision I (October 2003) to Revision J (January 2019)	Page
• 添加了器件信息表、ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分。.....	1
• Added V_{IH} MAX values in the <i>Recommended Operating Conditions</i> table.....	5

5 Pin Configuration and Functions

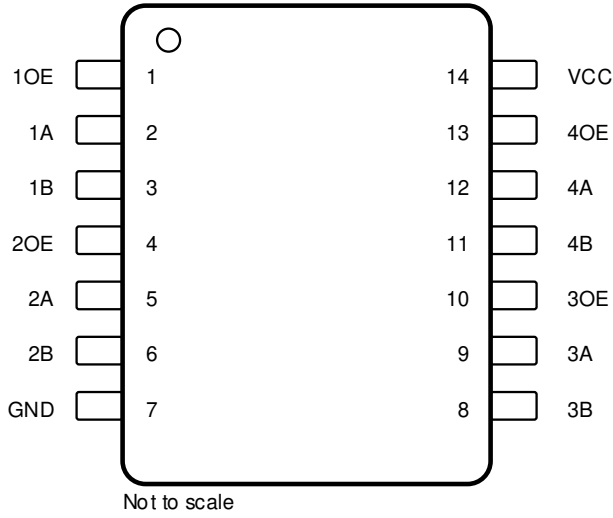


图 5-1. D, DGV, and PW Package, 14 Pin SOIC, TVSOP, and TSSOP (Top View)

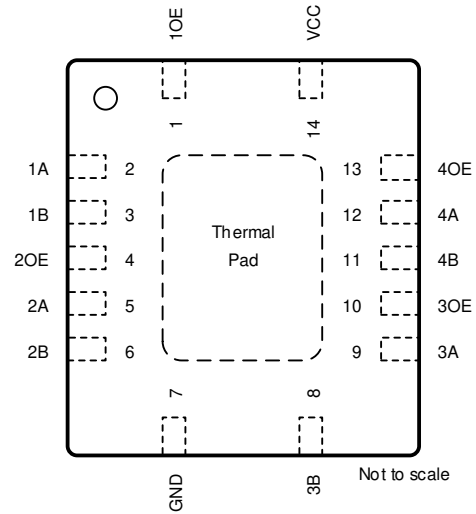


图 5-2. RGY Package, 14 Pin VQFN (Top View)

表 5-1. Pin Functions, D, DGV, PW, RGY

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1A	2	I/O	Channel 1 input or output
1B	3	I/O	Channel 1 input or output
1OE	1	I	Output enable, active high
2A	5	I/O	Channel 2 input or output
2B	6	I/O	Channel 2 input or output
2OE	4	I	Output enable, active high
3A	9	I/O	Channel 3 input or output
3B	8	I/O	Channel 3 input or output
3OE	10	I	Output enable, active high
4A	12	I/O	Channel 4 input or output
4B	11	I/O	Channel 4 input or output
4OE	13	I	Output enable, active high
GND	7	—	Ground
V _{CC}	14	P	Power supply
Thermal Pad		—	Exposed thermal pad. There is no requirement to solder this pad; if connected, it should be left floating or tied to GND.

(1) I = input, O = output, I/O = input and output, P = power

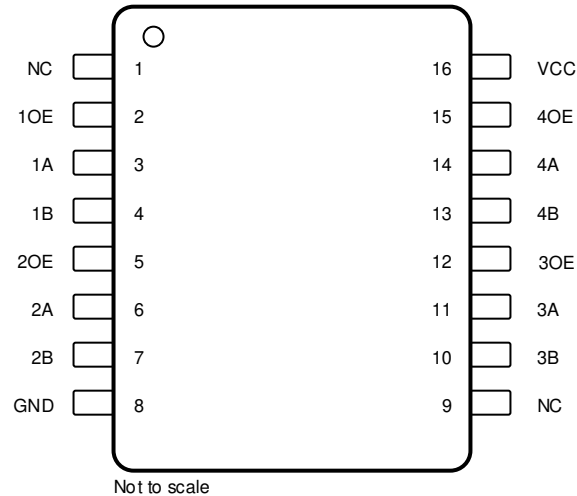


图 5-3. DBQ Package, 16 Pin SSOP (Top View)

表 5-2. Pin Functions, DBQ

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1A	3	I/O	Channel 1 input or output
1B	4	I/O	Channel 1 input or output
1OE	2	I	Output enable, active high
2A	6	I/O	Channel 2 input or output
2B	7	I/O	Channel 2 input or output
2OE	5	I	Output enable, active high
3A	11	I/O	Channel 3 input or output
3B	10	I/O	Channel 3 input or output
3OE	12	I	Output enable, active high
4A	14	I/O	Channel 4 input or output
4B	13	I/O	Channel 4 input or output
4OE	15	I	Output enable, active high
GND	8	—	Ground
NC	9	—	No internal connection
V _{CC}	16	P	Power supply

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	- 0.5	4.6	V
V _I	Input voltage range ⁽²⁾	- 0.5	4.6	V
I _{I/O}	Continuous channel current		128	mA
I _{IK}	Input clamp current	V _{I/O} < 0	- 50	mA
T _{stg}	Storage temperature range	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	V _{CC}
		V _{CC} = 2.7 V to 3.6 V	2	V _{CC}
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V	0.7	V
		V _{CC} = 2.7 V to 3.6 V	0.8	
T _A	Operating free-air temperature	- 40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74CBTLV3126					UNIT
		D (SOIC)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	DBQ (SSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	16 Pins	
R _{θJA}	Junction-to-ambient thermal resistance	100.6	154.8	123.3	59.6	118.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	55.5	64.5	53.0	71.3	66.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	56.8	88.4	66.3	35.6	62.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	17.0	11.1	9.3	4.2	20.9	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	56.4	87.4	65.7	35.7	61.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	16.1	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	$V_{CC} = 3\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
I_I	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$ or GND			± 1	μA
I_{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 3.6 V			10	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$,	$I_O = 0$,			10	μA
ΔI_{CC} ⁽²⁾	Control inputs $V_{CC} = 3.6\text{ V}$,	One input at 3 V ,			300	μA
C_i	Control inputs $V_I = 3\text{ V}$ or 0			2.5		pF
$C_{io(OFF)}$	$V_O = 3\text{ V}$ or 0 ,	OE = GND		7		pF
r_{on} ⁽³⁾	$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5	8	Ω
			$I_I = 24\text{ mA}$	5	8	
		$V_I = 1.7\text{ V}$,	$I_I = 15\text{ mA}$	27	40	
	$V_{CC} = 3\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5	7	
			$I_I = 24\text{ mA}$	5	7	
		$V_I = 2.4\text{ V}$,	$I_I = 15\text{ mA}$	10	15	

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

(2) This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

(3) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

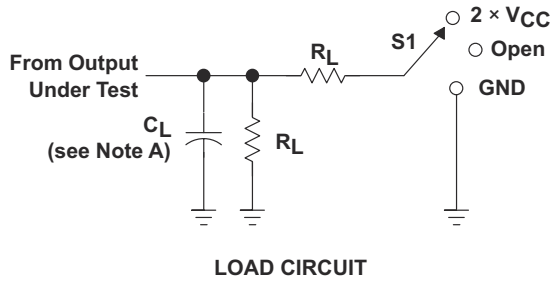
6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [图 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd} ⁽¹⁾	A or B	B or A		0.15		0.25	ns
t_{en}	OE	A or B	1.6	4.5	1.9	4.2	ns
t_{dis}	OE	A or B	1.3	4.7	1	4.8	ns

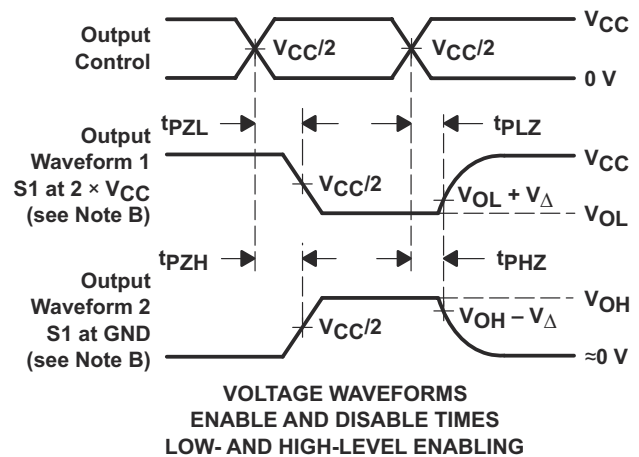
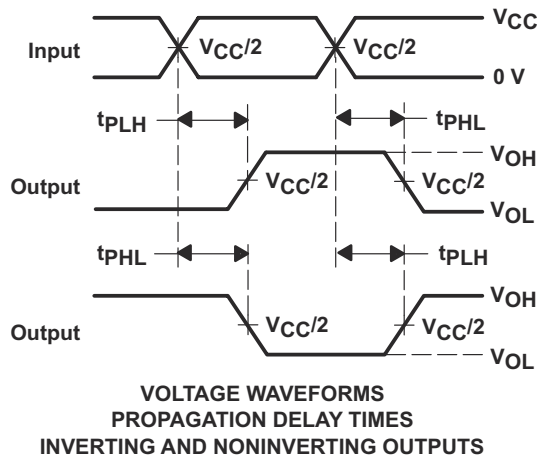
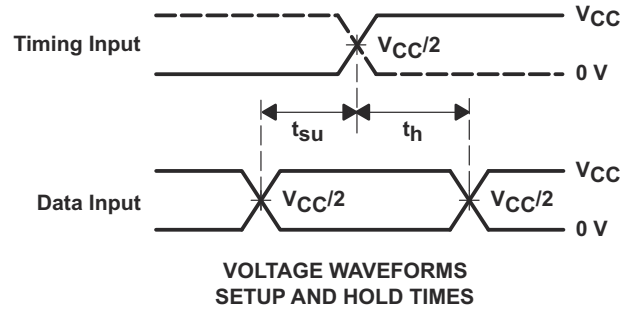
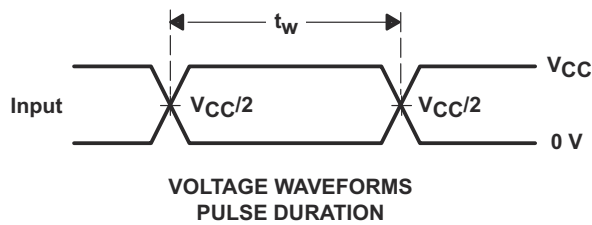
(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

7 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{Δ}
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	50 pF	500 Ω	0.3 V



- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .
- All parameters and waveforms are not applicable to all devices.

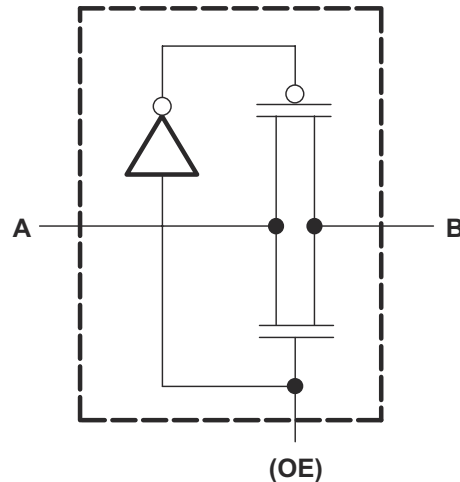
图 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74CBTLV3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The SN74CBTLV3126 device has isolation during power off. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull down resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



8.3 Feature Description

The SN74CBTLV3126 features $5\text{-}\Omega$ switch connection between ports, allowing for low signal loss across the switch. Rail-to-rail switching on data I/O allows for full voltage swing outputs. I_{off} supports partial-power-down mode operation, protecting the chip from voltages at output ports when it is not powered on. Latch-up performance exceeds 100 mA per JESD 78, Class II.

8.4 Device Functional Modes

8.4.1 Function Table (Each Bus Switch)

表 8-1 provides the truth table for the SN74CBTLV3126.

表 8-1. Truth Table

INPUT OE	FUNCTION
L	Disconnect
H	A port = B port

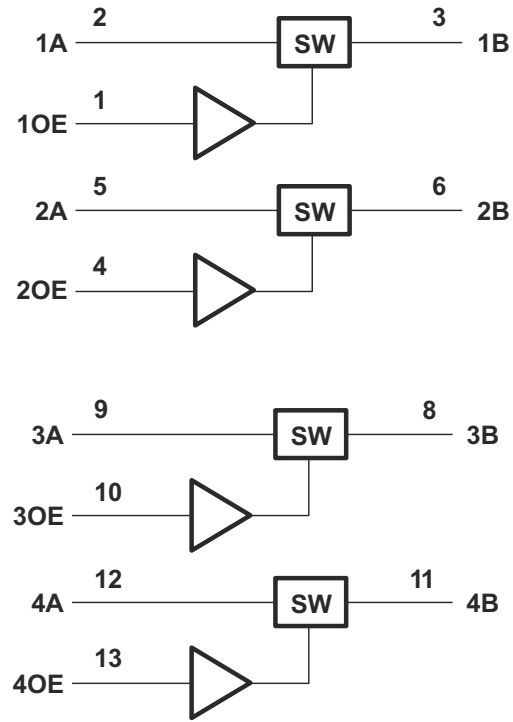


图 8-1. Logic Diagram (Positive Logic)

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

One useful application to take advantage of the SN74CBTLV3126 features is isolating various protocols from a processor or MCU such as JTAG, SPI, or standard GPIO signals. The device provides excellent isolation performance when the device is powered. The added benefit of powered-off protection allows a system to minimize complexity by eliminating the need for power sequencing in hot-swap and live insertion applications.

9.2 Typical Application

9.2.1 Protocol and Signal Isolation

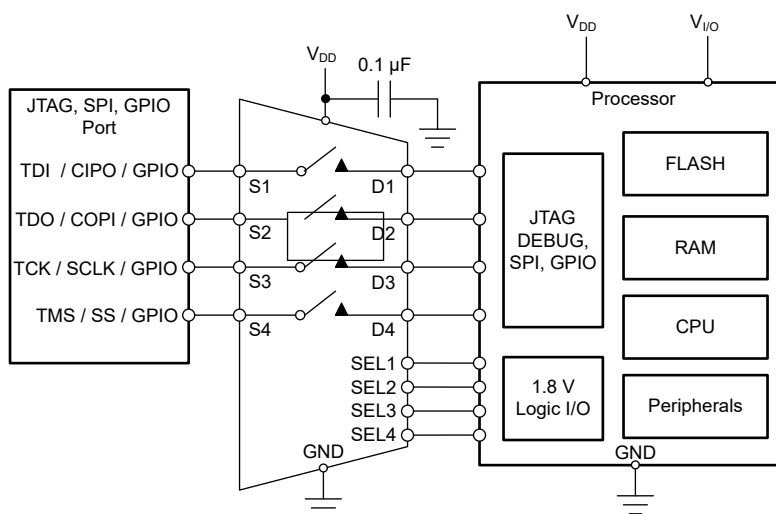


图 9-1. Typical Application

9.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	3.3 V
Input or output signal range	0 V to 3.3 V
Control logic thresholds	1.8 V compatible

9.2.1.2 Detailed Design Procedure

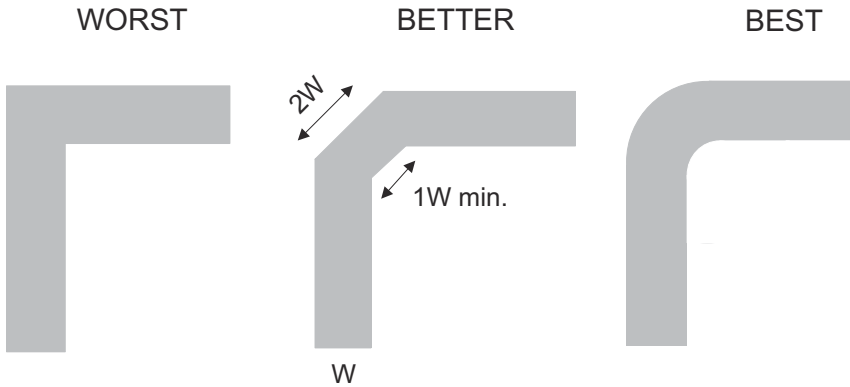
The SN74CBTLV3126 can operate without any external components except for the supply decoupling capacitors. TI recommends that the digital control pins (OE) be pulled up to V_{CC} or down to GND to avoid an undesired switch state that could result from the floating pin. All input signals passing through the switch must fall within the *Recommend Operating Conditions* of the SN74CBTLV3126 including signal range and continuous current. For this design example, with a supply of 3.3 V, the signals can range from 0 V to 3.3 V when the device is powered. This example can also utilize the Powered-off Protection feature, and the inputs can range from 0 V to 3.3 V when $V_{DD} = 0$ V.

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions* table. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F bypass capacitor is recommended. If multiple pins are labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight, and therefore; some traces must turn corners.  shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

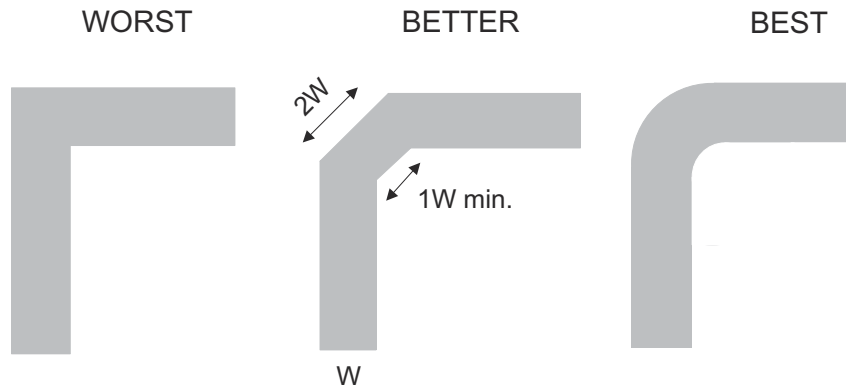


图 11-1. Trace Example

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Do not route high speed signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

- Avoid stubs on the high-speed signals traces because they cause signal reflections.
- Route all high-speed signal traces over continuous GND planes, with no interruptions.
- Avoid crossing over anti-etch, commonly found with plane splits.

- When working with high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in [图 11-2](#).

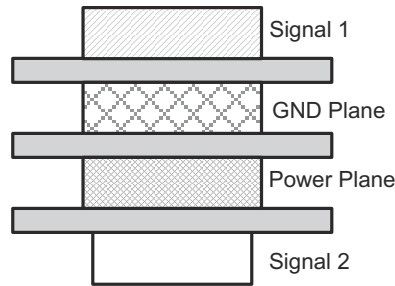


图 11-2. Example Layout

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

[图 11-3](#) shows an example of a PCB layout with the SN74CBTLV3126. Some key considerations are:

Decouple the V_{DD} pin with a 0.1- μ F capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.

High-speed switches require proper layout and design procedures for optimum performance.

Keep the input lines as short as possible.

Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.

Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

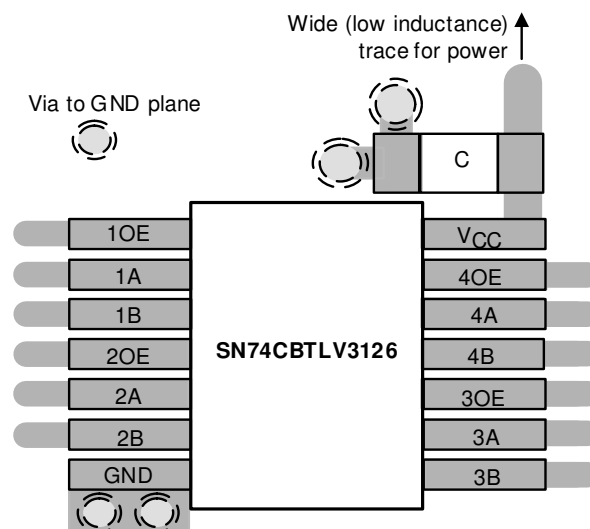


图 11-3. Example Layout

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CBTLV3126RGYRG4	LIFEBUY	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126	
SN74CBTLV3126D	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3126	
SN74CBTLV3126DBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126	Samples
SN74CBTLV3126DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126	Samples
SN74CBTLV3126DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3126	Samples
SN74CBTLV3126PW	LIFEBUY	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126	
SN74CBTLV3126PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126	Samples
SN74CBTLV3126RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTLV3126DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBTLV3126DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CBTLV3126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTLV3126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3126RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTLV3126DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
SN74CBTLV3126DGVR	TVSOP	DGV	14	2000	367.0	367.0	35.0
SN74CBTLV3126DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74CBTLV3126PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74CBTLV3126RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBTLV3126D	D	SOIC	14	50	506.6	8	3940	4.32
SN74CBTLV3126PW	PW	TSSOP	14	90	530	10.2	3600	3.5

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - △ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

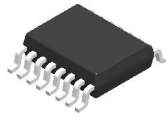
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

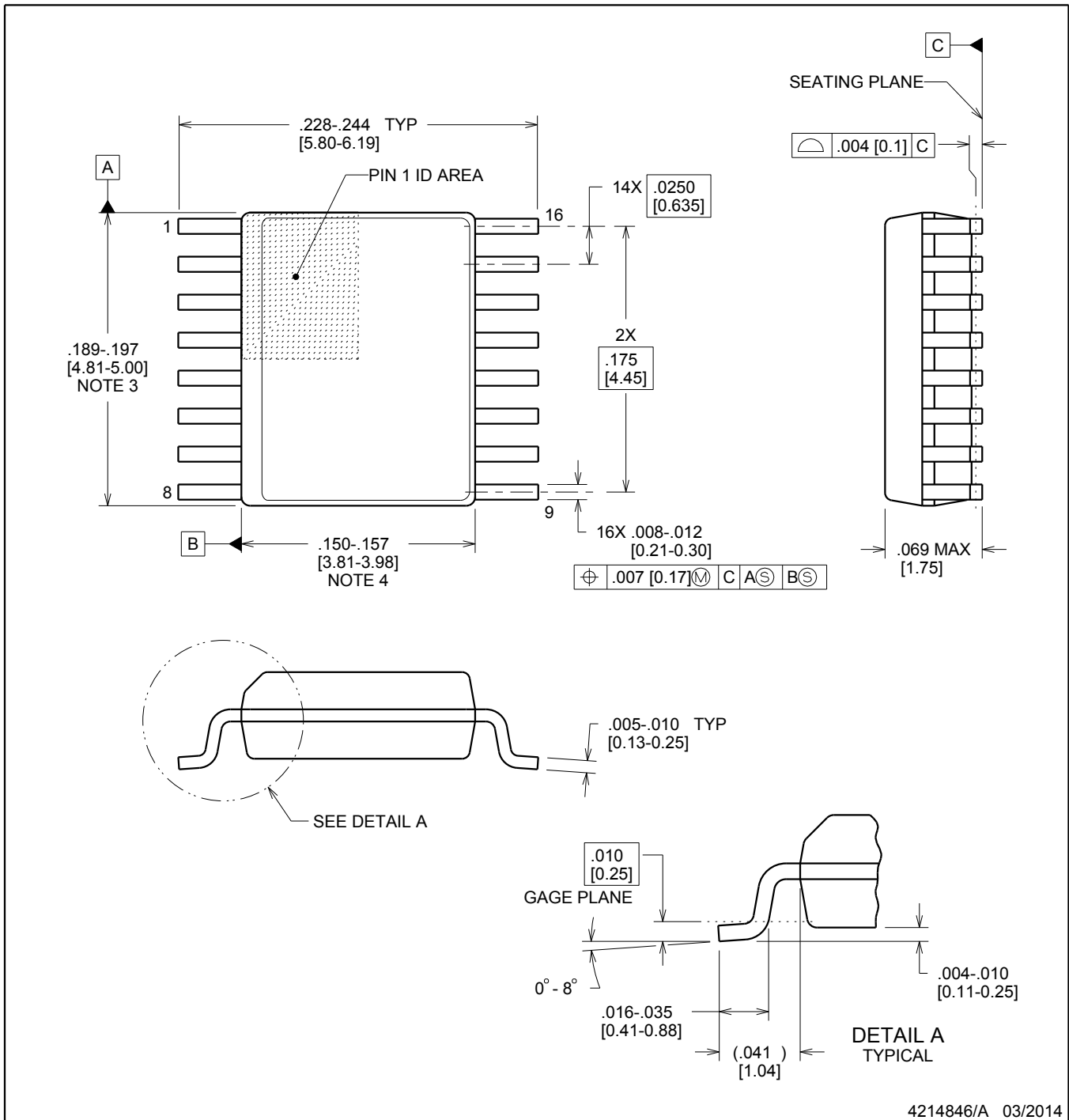


DBQ0016A

PACKAGE OUTLINE

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



4214846/A 03/2014

NOTES:

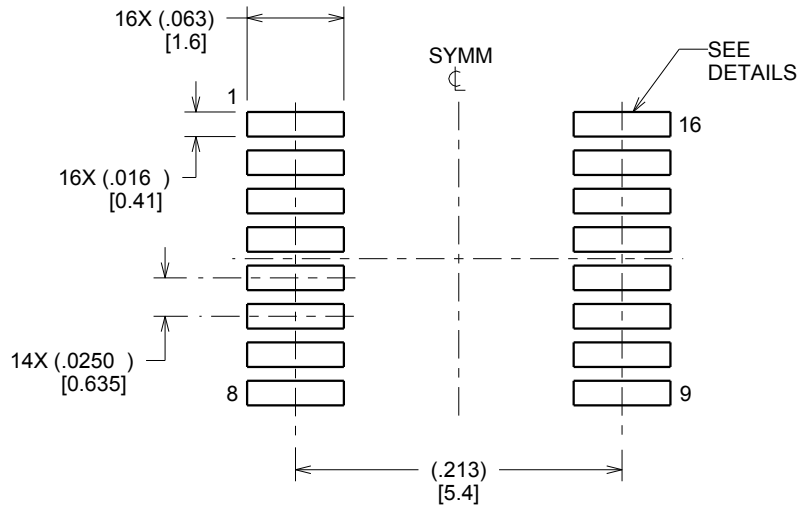
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT

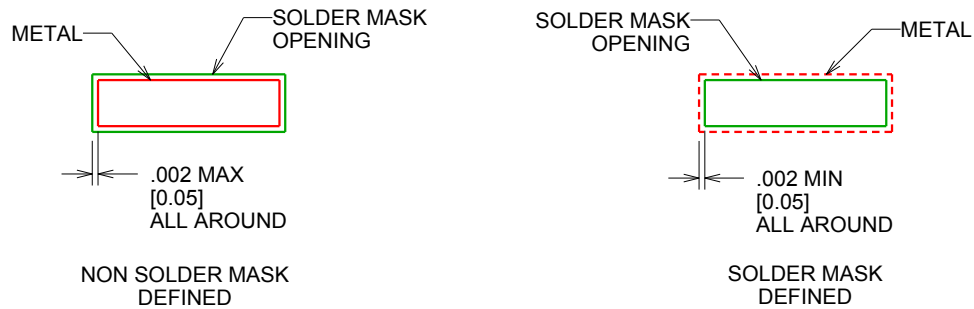
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

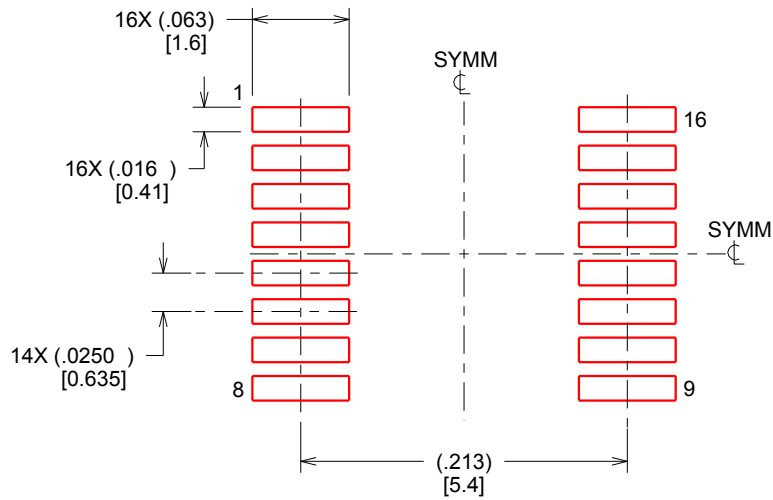
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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