

SNx4HC368 具有三态输出的六路反相缓冲器和线路驱动器

1 特性

- 2V 至 6V 的宽工作电压范围
- 高电流三态输出驱动总线、缓冲存储器地址寄存器或驱动多达 15 个 LSTTL 负载
- 反相输出
- 低功耗， I_{CC} 最大值为 80 μ A
- t_{pd} 典型值 = 10ns
- 电压为 5V 时，输出驱动为 ± 6 mA
- 低输出电流，最大值 1 μ A

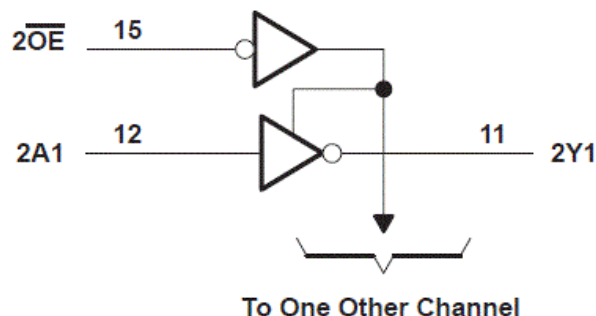
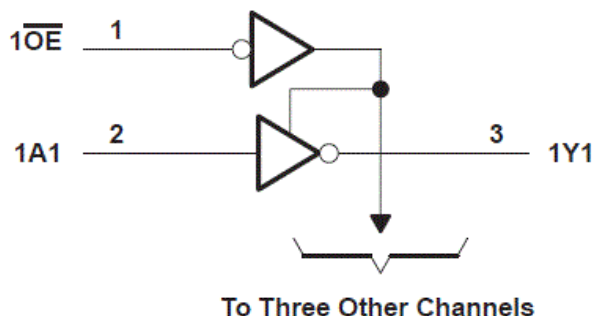
2 说明

这些六路反相缓冲器和线路驱动器专门用于提高三态存储器地址驱动器、时钟驱动器以及总线导向接收器和发送器的性能和密度。'HC368 器件配置为具有低电平有效输出使能 ($\overline{1OE}$ 和 $\overline{2OE}$) 输入的双路 4 线和 2 线缓冲器/驱动器。当 \overline{OE} 为低电平时，该器件将来自 A 输入的反相数据传递到 Y 输出。当 \overline{OE} 为高电平时，输出处于高阻态。

器件信息

| 器件型号 | 封装 ⁽¹⁾ | 封装尺寸 (标称值) |
|-------------|----------------------|------------------|
| SN54HC368J | 陶瓷双列直插封装 (CDIP) (16) | 24.38mm × 6.92mm |
| SN74HC368D | SOIC (16) | 9.90mm × 3.90mm |
| SN74HC368N | PDIP (16) | 19.31mm × 6.35mm |
| SN74HC368NS | SO (16) | 6.20mm × 5.30mm |
| SN74HC368PW | TSSOP (16) | 5.00mm × 4.40mm |
| SN54HC368FK | LCCC (20) | 8.89mm × 8.45mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能方框图



Table of Contents

| | | | |
|---|---|--|----|
| 1 特性 | 1 | 7.2 Functional Block Diagram..... | 9 |
| 2 说明 | 1 | 7.3 Device Functional Modes..... | 9 |
| 3 Revision History | 2 | 8 Power Supply Recommendations | 10 |
| 4 Pin Configuration and Functions | 3 | 9 Layout | 10 |
| 5 Specifications | 4 | 9.1 Layout Guidelines..... | 10 |
| 5.1 Absolute Maximum Ratings..... | 4 | 10 Device and Documentation Support | 11 |
| 5.2 Recommended Operating Conditions ⁽¹⁾ | 4 | 10.1 Documentation Support..... | 11 |
| 5.3 Thermal Information..... | 4 | 10.2 接收文档更新通知..... | 11 |
| 5.4 Electrical Characteristics..... | 6 | 10.3 支持资源..... | 11 |
| 5.5 Switching Characteristics..... | 6 | 10.4 Trademarks..... | 11 |
| 5.6 Operating Characteristics..... | 7 | 10.5 Electrostatic Discharge Caution..... | 11 |
| 6 Parameter Measurement Information | 8 | 10.6 术语表..... | 11 |
| 7 Detailed Description | 9 | 11 Mechanical, Packaging, and Orderable Information | 11 |
| 7.1 Overview..... | 9 | | |

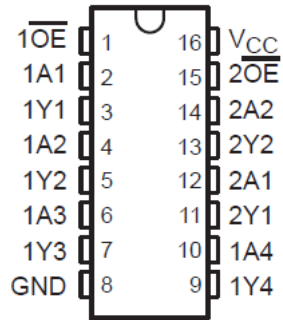
3 Revision History

注：以前版本的页码可能与当前版本的页码不同

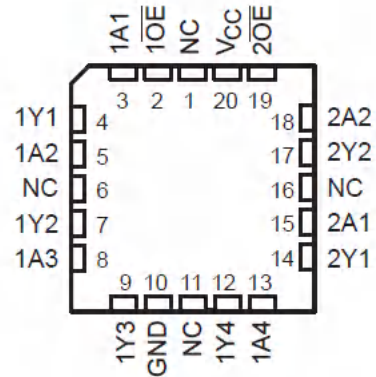
| Changes from Revision E (February 2022) to Revision F (June 2022) | Page |
|---|-------------|
| • Junction-to-ambient thermal resistance values increased. D was 73 is now 117.2, N was 67 is now 68.6, NS was 64 is now 87.4, PW was 108 is now 137.5..... | 4 |

| Changes from Revision D (October 2003) to Revision E (February 2022) | Page |
|---|-------------|
| • 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准..... | 1 |

4 Pin Configuration and Functions



J, D, N, NS, PW package
16-Pin CDIP, SOIC, PDIP, SO, TSSOP
Top View



NC – No internal connection
FK package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|---|-----|--------|
| V _{CC} | Supply voltage range | -0.5 | 7 | V |
| I _{IK} | Input clamp current ⁽²⁾ | (V _I < 0 or V _I > V _{CC}) | | ±20 mA |
| I _{OK} | Output clamp current ⁽²⁾ | (V _O < 0 or V _O > V _{CC}) | | ±20 mA |
| I _O | Continuous output current | (V _O = 0 to V _{CC}) | | ±25 mA |
| | Continuous current through V _{CC} or GND | | | ±50 mA |
| T _J | Junction temperature | | | 150 °C |
| T _{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

| | | SN54HC368 | | | SN74HC368 | | | UNIT |
|-----------------|---------------------------------|-------------------------|-----|-----------------|-----------|-----|-----------------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | | 1.5 | 1.5 | | V | |
| | | V _{CC} = 4.5 V | | 3.15 | 3.15 | | | |
| | | V _{CC} = 6 V | | 4.2 | 4.2 | | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | | 0.5 | | V | |
| | | V _{CC} = 4.5 V | | | 1.35 | | | |
| | | V _{CC} = 6 V | | | 1.8 | | | |
| V _I | Input voltage | 0 | | V _{CC} | 0 | | V _{CC} | V |
| V _O | Output voltage | 0 | | V _{CC} | 0 | | V _{CC} | V |
| t _t | Input transition rise/fall time | V _{CC} = 2 V | | | 1000 | | ns | |
| | | V _{CC} = 4.5 V | | | 500 | | | |
| | | V _{CC} = 6 V | | | 400 | | | |
| T _A | Operating free-air temperature | - 55 | | 125 | - 40 | | 85 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

5.3 Thermal Information

| THERMAL METRIC | | D (SOIC) | N (PDIP) | NS (SO) | PW (TSSOP) | UNIT |
|-----------------------|---|----------|----------|---------|------------|------|
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance ⁽¹⁾ | 117.2 | 68.6 | 87.4 | 137.5 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 77.2 | 61.1 | 44.9 | 75.3 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 75.6 | 48.6 | 49.6 | 82.2 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 38.1 | 33.9 | 12.2 | 25.1 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 75.3 | 48.4 | 49.2 | 81.8 | °C/W |

5.3 Thermal Information (continued)

| THERMAL METRIC | | D (SOIC) | N (PDIP) | NS (SO) | PW (TSSOP) | UNIT |
|----------------------|--|----------|----------|---------|------------|------|
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} (V) | T _A = 25°C | | | SN74HC368 | | SN74HC368 | | UNIT |
|-----------------|---|----------------------------|---------------------|-----------------------|-------|------|-----------|-------|-----------|-------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = - 20 μA | 2 | 1.9 | 1.998 | | 1.9 | | 1.9 | V | |
| | | | 4.5 | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | 6 | 5.9 | 5.999 | | 5.9 | | 5.9 | | | |
| | | I _{OH} = 6 mA | 4.5 | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | I _{OH} = - 7.8 mA | 6 | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | 6 | | 0.001 | 0.1 | | 0.1 | | 0.1 | | |
| | | I _{OL} = 6 mA | 4.5 | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | I _{OL} = 7.8 mA | 6 | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| I _I | V _I = V _{CC} or 0 | | 6 | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| I _{OZ} | V _O = V _{CC} or 0 | | 6 | | ±0.01 | ±0.5 | | ±10 | | ±5 | μA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | | 6 | | | 8 | | 160 | | 80 | μA |
| C _i | | | 2 to 6 | | 3 | 10 | | 10 | | 10 | pF |

5.5 Switching Characteristics

Over recommended operating free-air temperature range, C_L = 50 pF. See [Parameter Measurement Information](#)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} (V) | T _A = 25°C | | | SN54HC368 | | SN74HC368 | | |
|------------------|--------------|-------------|---------------------|-----------------------|-----|-----|-----------|-----|-----------|-----|----|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A | Y | 2 | | 50 | 95 | | 145 | | 120 | ns |
| | | | 4.5 | | 12 | 19 | | 29 | | 24 | |
| | | | 6 | | 10 | 16 | | 25 | | 20 | |
| t _{en} | OE | Y | 2 | | 100 | 190 | | 285 | | 238 | ns |
| | | | 4.5 | | 26 | 38 | | 57 | | 48 | |
| | | | 6 | | 21 | 32 | | 48 | | 41 | |
| t _{dis} | OE | Y | 2 | | 50 | 175 | | 265 | | 240 | ns |
| | | | 4.5 | | 21 | 35 | | 53 | | 48 | |
| | | | 6 | | 19 | 30 | | 45 | | 41 | |
| t _t | | Any | 2 | | 28 | 60 | | 90 | | 75 | ns |
| | | | 4.5 | | 8 | 12 | | 18 | | 15 | |
| | | | 6 | | 6 | 10 | | 15 | | 13 | |

5.5 Switching Characteristics

Over recommended operating free-air temperature range, $C_L = 150$ pF. See [Parameter Measurement Information](#)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} (V) | $T_A = 25^\circ\text{C}$ | | | SN54HC368 | | SN74HC368 | | |
|-----------|-----------------|-------------|--------------|--------------------------|------|-----|-----------|-----|-----------|-----|--|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A | Y | 2 | 70 | 120 | 180 | 150 | ns | | | |
| | | | 4.5 | 17 | 24 | 36 | 30 | | | | |
| | | | 6 | 14 | 20 | 31 | 25 | | | | |
| t_{en} | \overline{OE} | Y | 2 | 140 | 1230 | 345 | 285 | ns | | | |
| | | | 4.5 | 30 | 46 | 69 | 57 | | | | |
| | | | 6 | 28 | 39 | 59 | 48 | | | | |
| t_t | | Any | 2 | 45 | 210 | 315 | 265 | ns | | | |
| | | | 4.5 | 17 | 42 | 63 | 53 | | | | |
| | | | 6 | 13 | 36 | 53 | 45 | | | | |

5.6 Operating Characteristics

$T_A = 25^\circ\text{C}$

| | | Test Conditions | TYP | UNIT |
|----------|---|-----------------|-----|------|
| C_{pd} | Power dissipation capacitance per buffer/driver | No load | 35 | pF |

6 Parameter Measurement Information

t_{pd} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{THL}

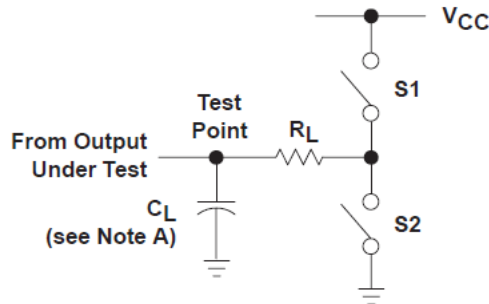


图 6-1.

| PARAMETER | | R_L | C_L | S1 | S2 |
|-------------------|-----------|--------------|-----------------|--------|--------|
| t_{en} | t_{PZH} | 1 k Ω | 50 pF or 150 pF | Open | Closed |
| | t_{PZL} | | | Closed | Open |
| t_{dis} | t_{PHZ} | 1 k Ω | 50 pF | Open | Closed |
| | t_{PLZ} | | | Closed | Open |
| t_{pd} or t_t | | -- | 50 pF or 150 pF | Open | Open |

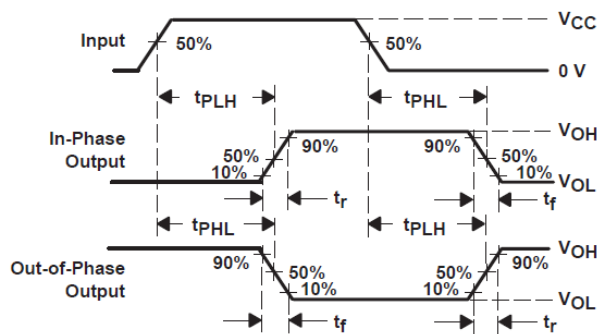


图 6-2. Voltage Waveforms
Propagation Delay and Output Transition Times

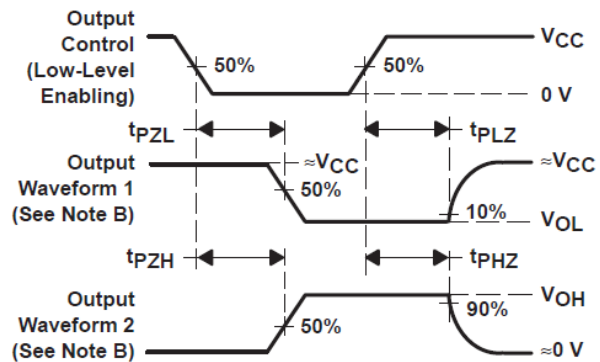


图 6-3. Voltage Waveforms
Enable and Disable Times for 3-State Outputs

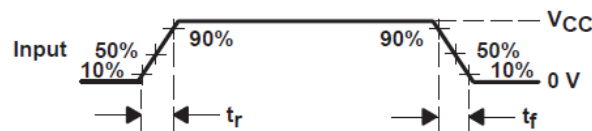


图 6-4. Voltage Waveform
Input Rise and Fall Times

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

7 Detailed Description

7.1 Overview

These hex inverting buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The ' HC368 devices are organized as dual 4-line and 2-line buffers/drivers with active-low output-enable ($\overline{1OE}$ and $\overline{2OE}$) inputs. When \overline{OE} is low, the device passes inverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

7.2 Functional Block Diagram

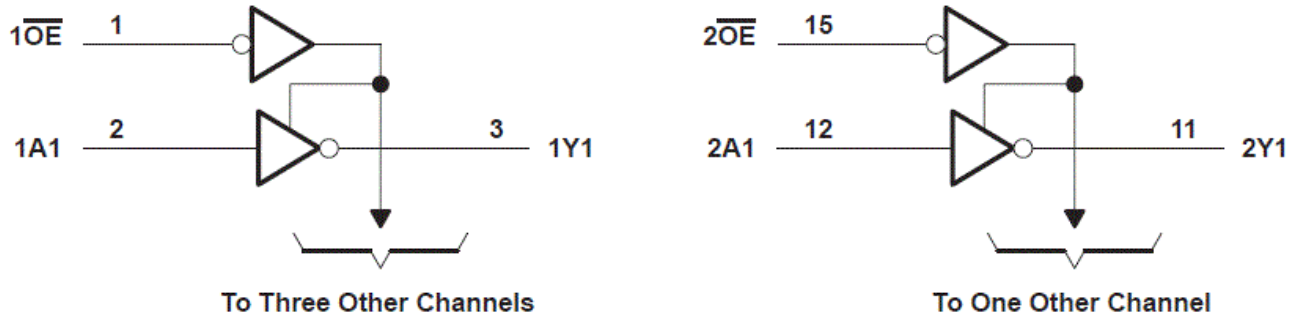


图 7-1. Functional Block Diagram

7.3 Device Functional Modes

Function Table
(Each buffer/driver)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| H | X | Z |
| L | H | L |
| L | L | H |

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ [支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|--------------------------------|-------------------------|
| 5962-86812012A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-86812012A SNJ54HC368FK | Samples |
| 5962-8681201EA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8681201EA SNJ54HC368J | Samples |
| JM38510/65709BEA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65709BEA | Samples |
| M38510/65709BEA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65709BEA | Samples |
| SN54HC368J | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54HC368J | Samples |
| SN74HC368D | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -40 to 85 | HC368 | |
| SN74HC368DR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | HC368 | Samples |
| SN74HC368N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC368N | Samples |
| SN74HC368NE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC368N | Samples |
| SN74HC368NSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC368 | Samples |
| SN74HC368PW | OBSOLETE | TSSOP | PW | 16 | | TBD | Call TI | Call TI | -40 to 85 | HC368 | |
| SN74HC368PWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC368 | Samples |
| SNJ54HC368FK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-86812012A SNJ54HC368FK | Samples |
| SNJ54HC368J | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8681201EA SNJ54HC368J | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC368, SN74HC368 :

● Catalog : [SN74HC368](#)

● Military : [SN54HC368](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC368DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC368NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC368PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC368PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC368DR | SOIC | D | 16 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74HC368NSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC368PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC368PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-86812012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SN74HC368N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC368N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC368NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC368NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54HC368FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

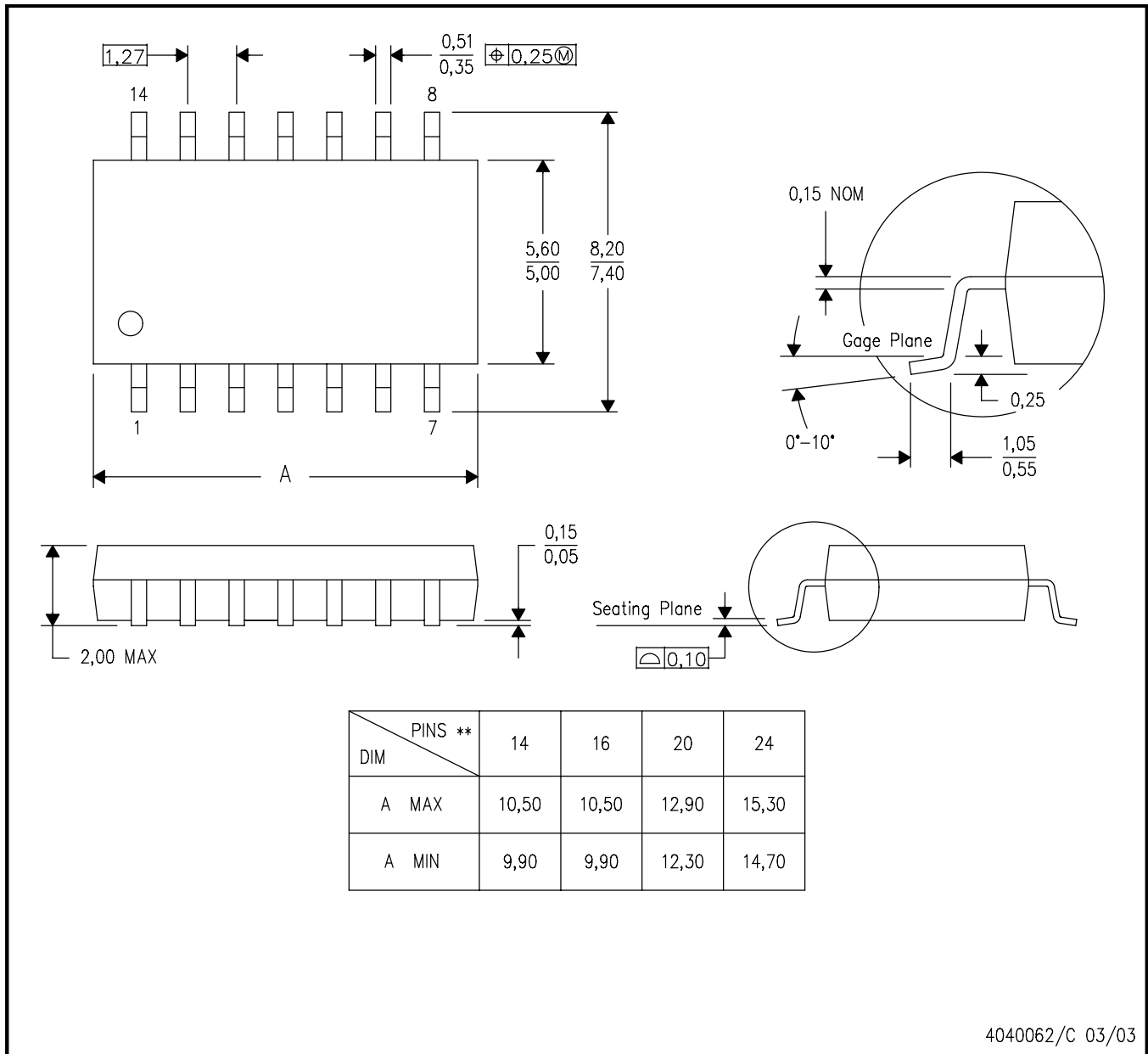
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)
14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024，德州仪器 (TI) 公司