SN74LV126A 具有三态输出的四通道总线缓冲门

1 特性

- 2V 至 5.5V V_{CC} 运行
- 5V 时，t_{pd} 最大值为 6.5ns
- V_{OLP}（输出接地反弹）典型值 <0.8V（V_{CC} = 3.3V、T_A = 25°C）
- V_{CC} = 3.3V、T_A = 25°C 时，V_{OHV}（输出 V_{OH} 下冲）典型值 >2.3V
- I_{off} 支持带电插入、局部关断模式和后驱动保护
- 所有端口上均支持混合模式电压运行
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- 服务器
- 网络交换机
- 电子销售终端
- 电视
- 机顶盒

3 说明

这款 SN74LV126A 四路总线缓冲门可在 2V 至 5.5V V_{CC} 下运行。

这款四路总线缓冲门可在 2V 至 5.5V V_{CC} 下运行。

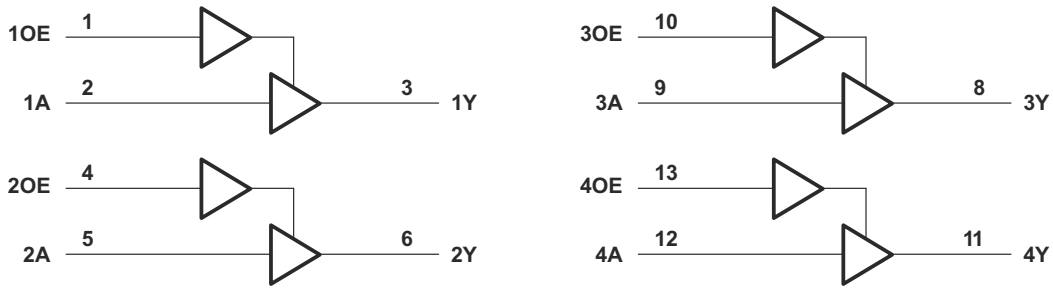
SN74LV126A 器件采用具有三态输出的独立线路驱动器。当每个输出的相关输出使能 (OE) 输入为低电平时，输出被禁用。

为了确保加电或断电期间的高阻抗状态，OE 应该通过一个下拉电阻器接在接地 (GND) 上；此电阻器的最小值由驱动器电流供源能力决定。

封装信息

器件型号	封装(1)	封装尺寸(2)
SN74LV126A	D（SOIC，14）	8.65mm × 6mm
	NS（SOP，14）	10.2mm × 7.8mm
	DB（SSOP，14）	6.2mm × 7.8mm
	PW（TSSOP，14）	5mm × 6.4mm

(1) 有关更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）

Table of Contents

4 Pin Configuration and Functions

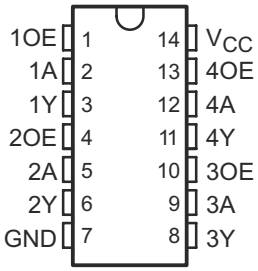


图 4-1. SN74LV126A: D, DB, DGV, NS, or PW Package, 14-Pin SOIC, SSOP, TVSOP, SOP, or TSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1OE	1	I	Channel 1, Output Enable
1A	2	I	Channel 1, Input A
1Y	3	O	Channel 1, Output Y
2OE	4	I	Channel 2, Output Enable
2A	5	I	Channel 2, Input A
2Y	6	O	Channel 2, Output Y
GND	7	—	Ground
3Y	8	O	Channel 3, Output Y
3A	9	I	Channel 3, Input A
3OE	10	I	Channel 3, Output Enable
4Y	11	O	Channel 4, Output Y
4A	12	I	Channel 4, Input A
4OE	13	I	Channel 4, Output Enable

表 4-1. Pin Functions（续）

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
V_{CC}	14	—	Positive Supply

(1) I = input, O = output, P = power, G = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	– 0.5	7	V
V_I	Input voltage(2)	– 0.5	7	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	– 0.5	7	V
V_O	Output voltage(2) (3)	– 0.5	V_{CC} + 0.5V	V
I_{IK}	Input clamp current, V_I < 0		– 20	mA
I_{OK}	Output clamp current, V_O < 0		– 50	mA
I_O	Continuous output current, V_O = 0 to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND		±70	mA
T_{stg}	Storage temperature	– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5V maximum.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

see (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2V	1.5		V
		V_{CC} = 2.3 to 2.7V	V_{CC} × 0.7		
		V_{CC} = 3 to 3.6V	V_{CC} × 0.7		
		V_{CC} = 4.5 to 5.5V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2V		0.5	V
		V_{CC} = 2.3 to 2.7V		V_{CC} × 0.3	
		V_{CC} = 3 to 3.6V		V_{CC} × 0.3	
		V_{CC} = 4.5 to 5.5V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2V		– 50	µA
		V_{CC} = 2.3 to 2.7V		– 2	mA
		V_{CC} = 3 to 3.6V		– 8	
		V_{CC} = 4.5 to 5.5V		– 16	

5.3 Recommended Operating Conditions（续）

see (1)

			MIN	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 2V		50	μA
		V_{CC} = 2.3 to 2.7V		2	mA
		V_{CC} = 3 to 3.6V		8	
		V_{CC} = 4.5 to 5.5V		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 to 2.7V		200	ns/V
		V_{CC} = 3 to 3.6V		100	
		V_{CC} = 4.5 to 5.5V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.4 Thermal Information

THERMAL METRIC(1)		D	DB	DGV	NS	PW	UNIT
		14 PINS					
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	92.7	105.0	127.6	89.6	119.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.1	57.5	50.7	47.2	48.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	47.0	52.3	60.5	48.4	61.5	
ψ_{JT}	Junction-to-top characterization parameter	18.9	19.1	6.1	14.0	5.7	
ψ_{JB}	Junction-to-board characterization parameter	46.7	51.8	59.8	48.1	61.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –50μA	2 to 5.5V	V_{CC} – 0.1			V
	I_{OH} = –2mA	2.3V	2			
	I_{OH} = –8mA	3V	2.48			
	I_{OH} = –16mA	4.5V	3.8			
V_{OL}	I_{OL} = 50μA	2 to 5.5V			0.1	V
	I_{OL} = 2mA	2.3V			0.4	
	I_{OL} = 8mA	3V			0.44	
	I_{OL} = 16mA	4.5V			0.55	
I_I	V_I = 5.5V or GND	0 to 5.5V			±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5V			±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5V			20	μA
I_{off}	V_I or V_O = 0 to 5.5V	0V			±5	μA
C_i	V_I = V_{CC} or GND	3.3V		1.6		pF

5.6 Switching Characteristics, V_{CC} = 2.5V ±0.2V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	A	Y	C_L = 15pF		7.1	13	1	15.5	ns
t_{en}	OE				7.4	13	1	15.5	
t_{dis}	OE				5.7	14.7	1	17	
t_{pd}	A	Y	C_L = 50pF		9.2	16.5	1	18.5	ns
t_{en}	OE				9.5	16.5	1	18.5	
t_{dis}	OE				8.1	18.2	15	20.5	
$t_{sk(o)}$						2		2	

5.7 Switching Characteristics, V_{CC} = 3.3V ±0.3V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	A	Y	C_L = 15pF		5	8	1	9.5	ns
t_{en}	OE				5.1	8	1	9.5	
t_{dis}	OE				4.4	9.7	1	11.5	
t_{pd}	A	Y	C_L = 50pF		6.4	11.5	1	13	ns
t_{en}	OE				6.6	11.5	1	13	
t_{dis}	OE				6.1	13.2	1	15	
$t_{sk(o)}$						1.5		1.5	

5.8 Switching Characteristics, V_{CC} = 5V ±0.5V

over recommended operating free-air temperature range (unless otherwise noted) (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	A	Y	C_L = 15pF		3.5	5.5	1	6.5	ns
t_{en}	OE				3.6	5.1	1	6	
t_{dis}	OE				3.3	6.8	1	8	
t_{pd}	A	Y	C_L = 50pF		4.6	7.5	1	8.5	ns
t_{en}	OE				4.6	7.1	1	8	
t_{dis}	OE				4.3	8.8	1	10	
$t_{sk(o)}$						1		1	

5.9 Noise Characteristics

V_{CC} = 3.3V, C_L = 50pF, T_A = 25°C (see (1))

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.2	–0.8	
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.1		
$V_{IH(D)}$	High-level dynamic input voltage	2.31			
$V_{IL(D)}$	Low-level dynamic input voltage			0.97	

(1) Characteristics are for surface-mount packages only.

5.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enable; C_L = 50pF, f = 10MHz	3.3V	14.4	pF
			5V	15.9	

5.11 Typical Characteristics

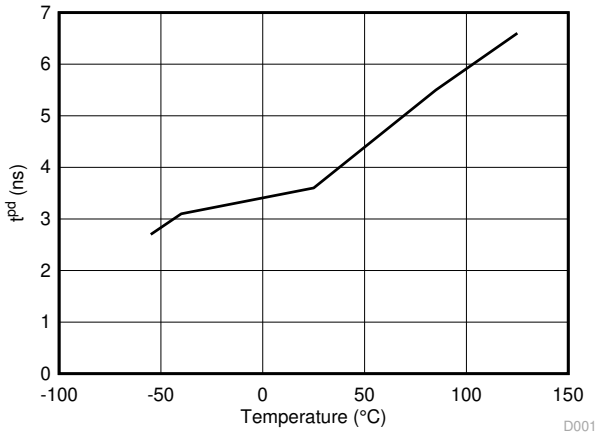


图 5-1. SN74LV126A t_{PD} vs Temperature at 5V

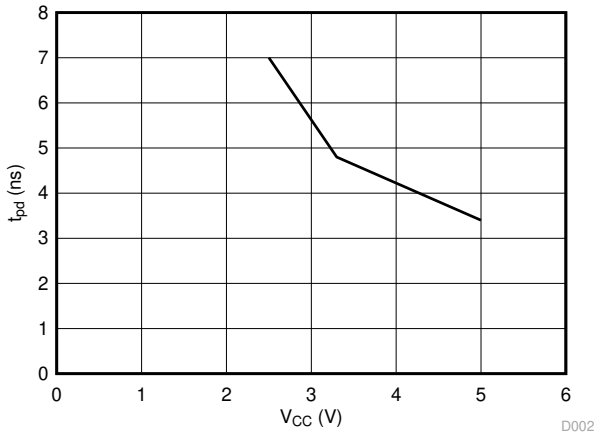
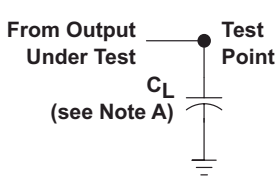
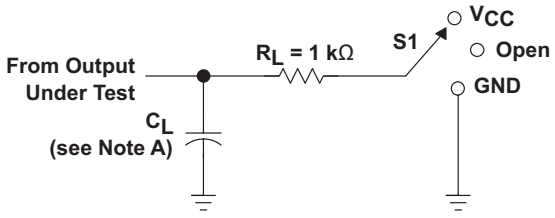


图 5-2. SN74LV126A t_{PD} vs V_{CC} at 25°C

6 Parameter Measurement Information

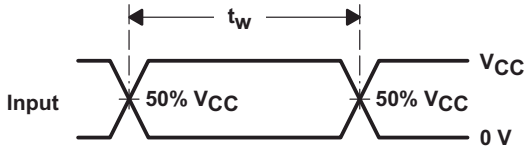


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

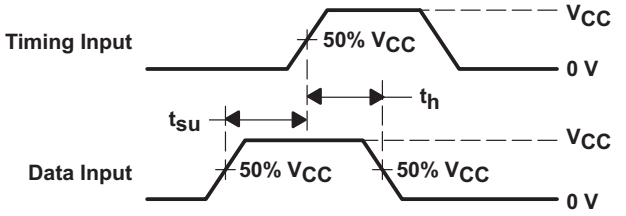


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

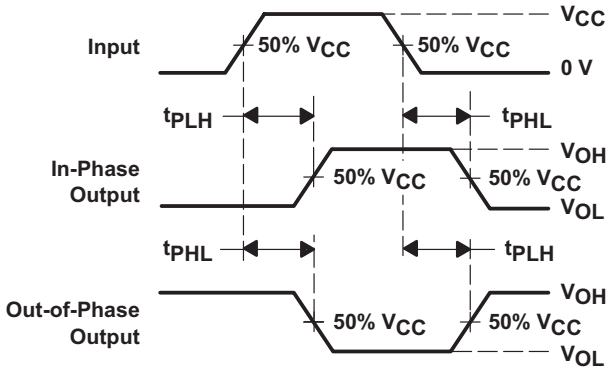
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



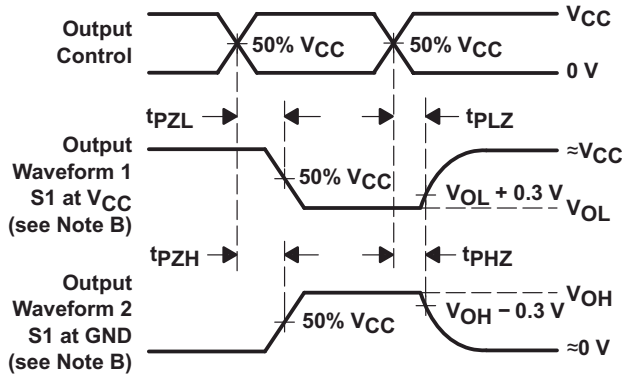
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1MHz, Z_O = 50 Ω, t_r ⩽ 3ns, t_f ⩽ 3ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

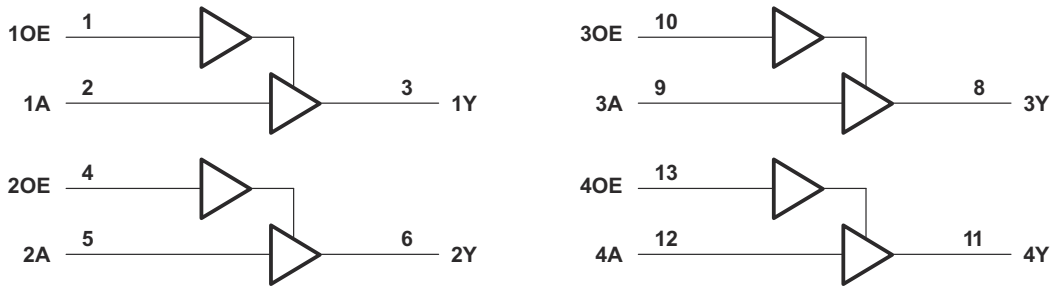
图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LV126A devices are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low. When OE is high, the respective gate passes the data from the A input to its Y output. To put the device in the high-impedance state during power up or power down, tie OE to GND through a pulldown resistor; the current-sourcing capability of the driver determines the minimum value of the resistor.

7.2 Functional Block Diagram



A. Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, and W packages.

图 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

- Wide operating voltage range, operates from 2 to 5.5V
- Allows down voltage translation, inputs accept voltages to 5.5V
- Ioff supports live insertion, partial power down mode, and back drive protection

7.4 Device Functional Modes

表 7-1. Function Table (Each Buffer)

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The SN74LV126A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates minimize overshoot and undershoot on the outputs. The inputs are 5.5V tolerant at any valid V_{CC} making this device an excellent choice for translating down to V_{CC}.

8.2 Typical Application

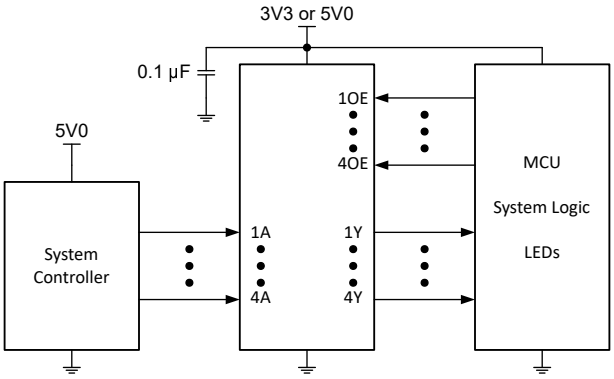


图 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended input conditions
   - Rise time and fall time specifications, see ($\Delta t/\Delta V$) in *Recommended Operating Conditions*.
   - Specified High and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
2. Recommend output conditions
   - Load currents should not exceed 35mA per output and 70mA total for the part
   - Outputs should not be pulled above V_{CC}

8.2.3 Application Curve

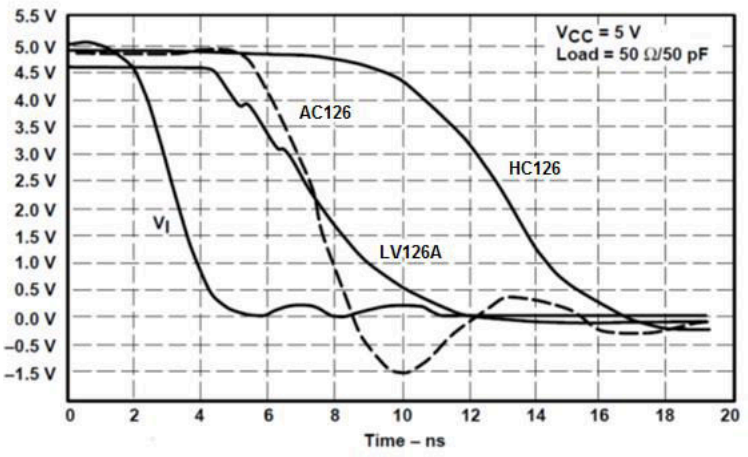


图 8-2. Switching Characteristics Comparison

8.3 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended and if there are multiple V_{CC} terminals then .01 or .022 μF is recommended for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever makes more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, then it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs so they also cannot float when disabled.

8.4.2 Layout Example

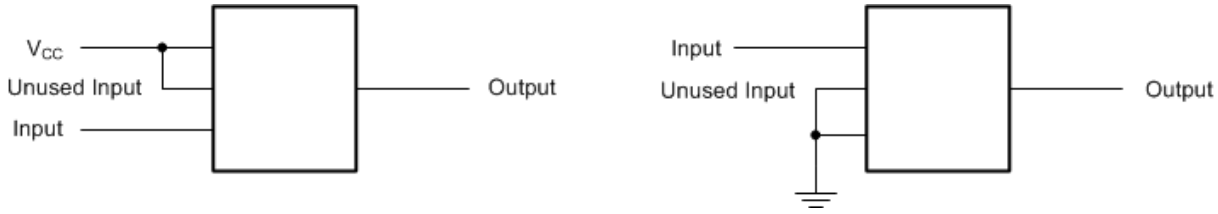


图 8-3. Layout Recommendation

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision I (February 2015) to Revision J (April 2024)	Page
• 删除了数据表中的 *SN54LV126A* 器件	1
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Changed the 125 function table with the correct 126 function table	9

Changes from Revision H (April 2005) to Revision I (February 2015)	Page
• 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分	1
• Updated operating free-air temperature maximum from 85°C to 125°C for SN74LV126A	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV126ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A	Samples
SN74LV126ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A	Samples
SN74LV126ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LV126A	Samples
SN74LV126ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV126A	Samples
SN74LV126APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LV126A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

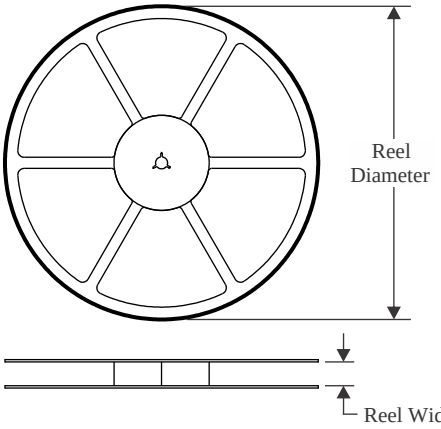
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

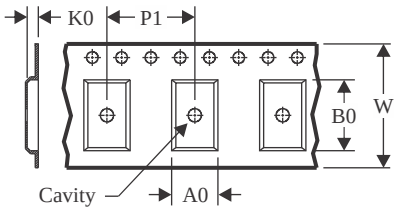
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

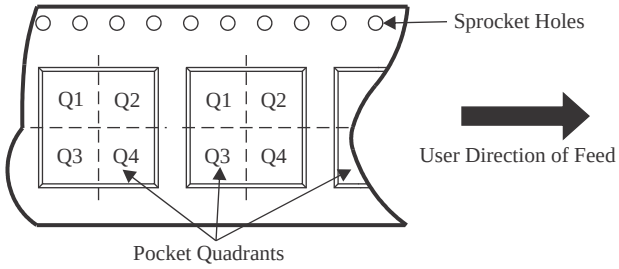


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

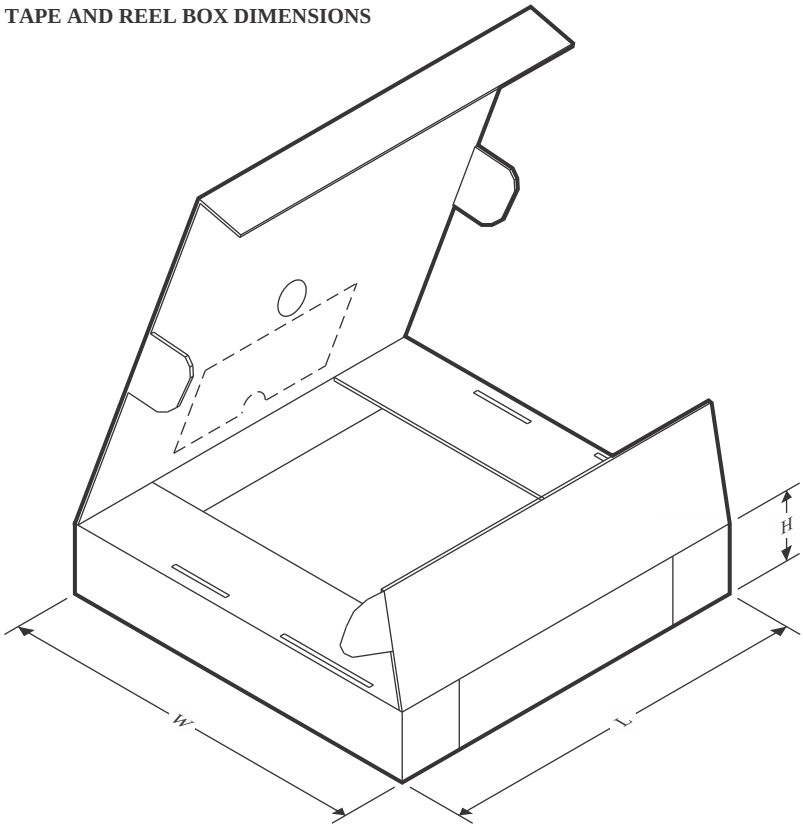
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV126ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV126ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV126ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV126ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV126ADR	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74LV126ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV126APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV126APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



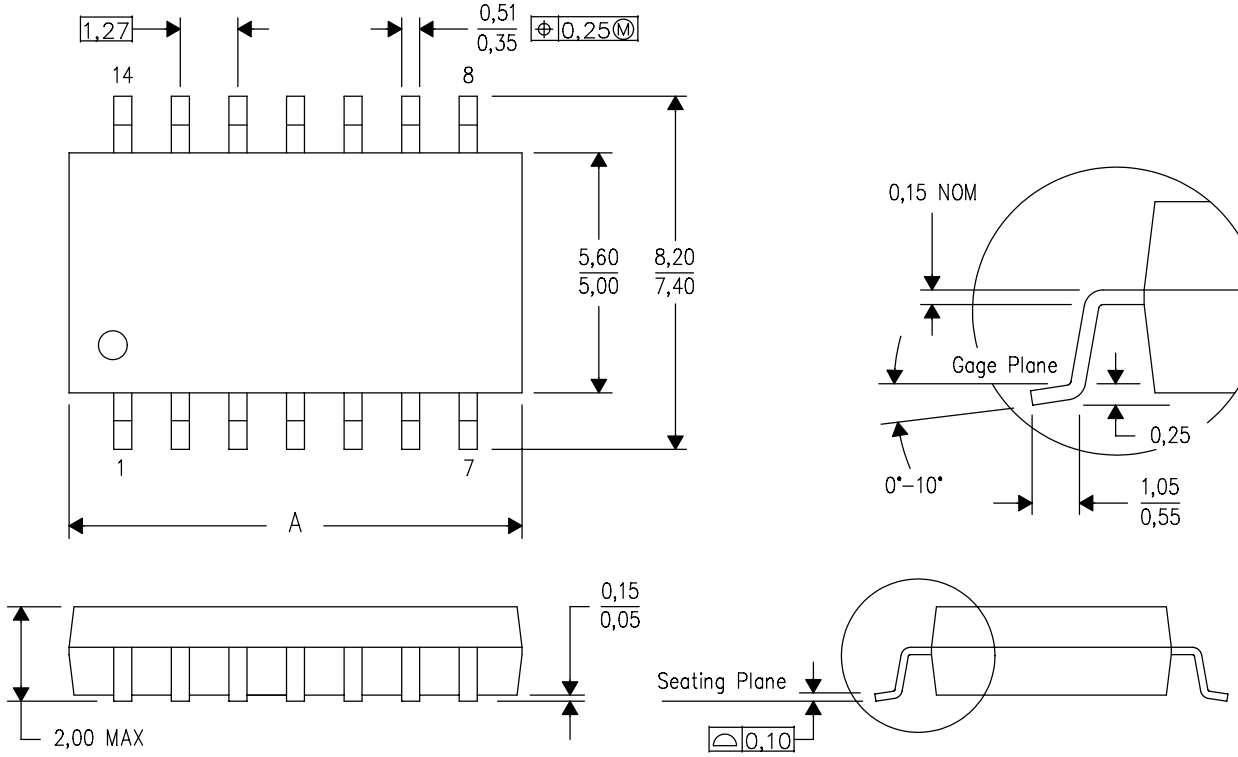
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV126ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV126ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV126ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV126ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV126ADR	SOIC	D	14	2500	366.0	364.0	50.0
SN74LV126ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LV126APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV126APWR	TSSOP	PW	14	2000	356.0	356.0	35.0

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



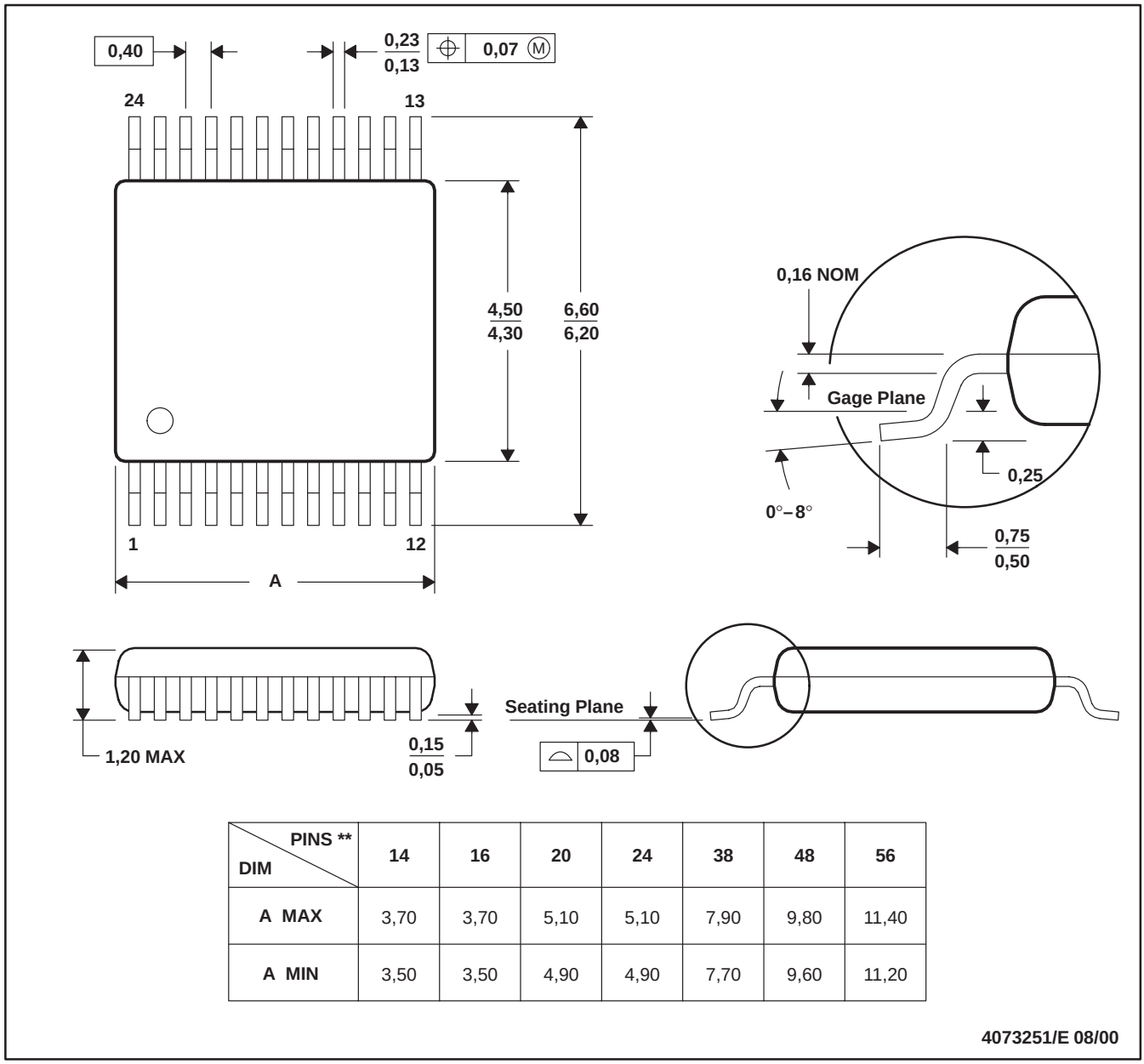
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

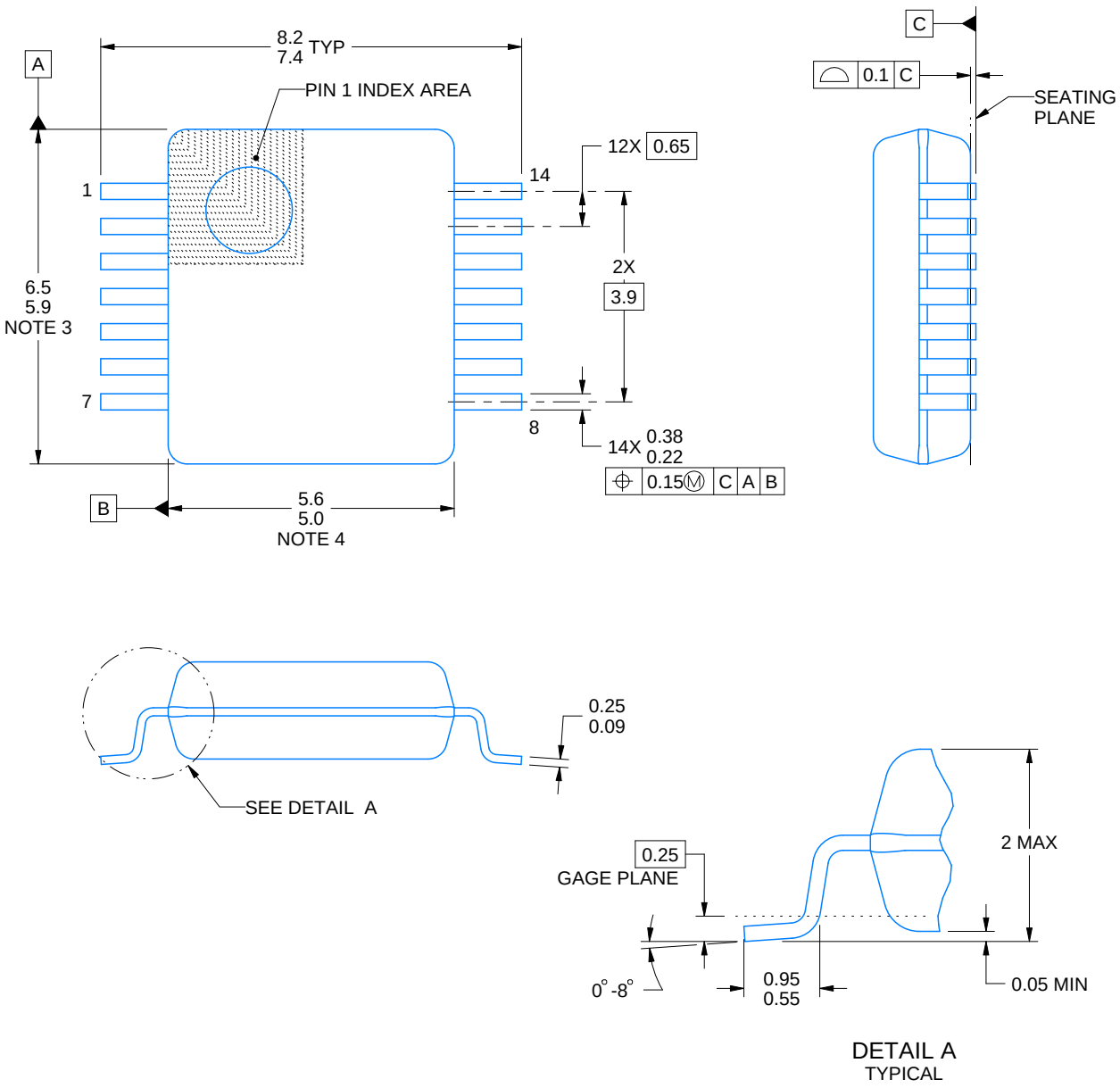
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

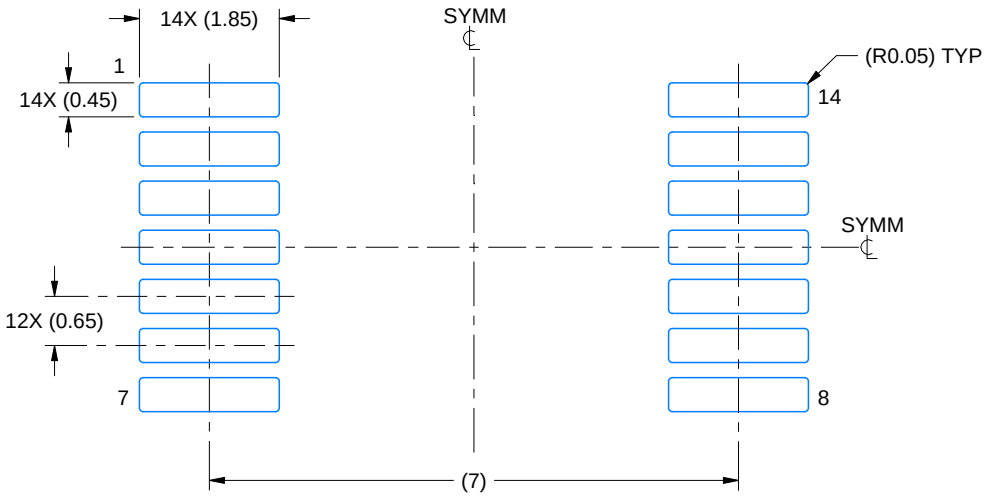
SMALL OUTLINE PACKAGE



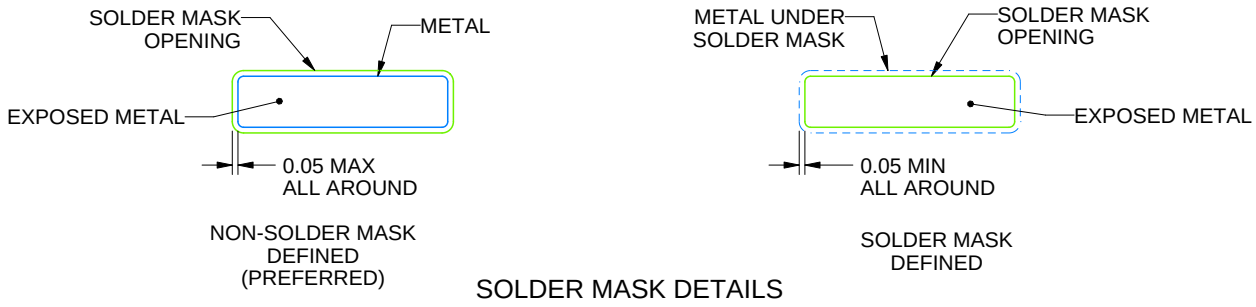
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

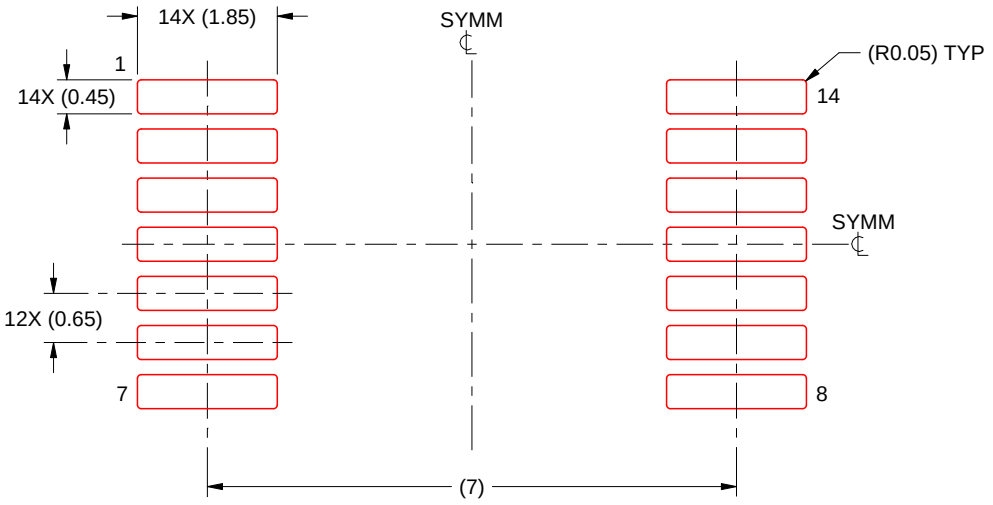


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



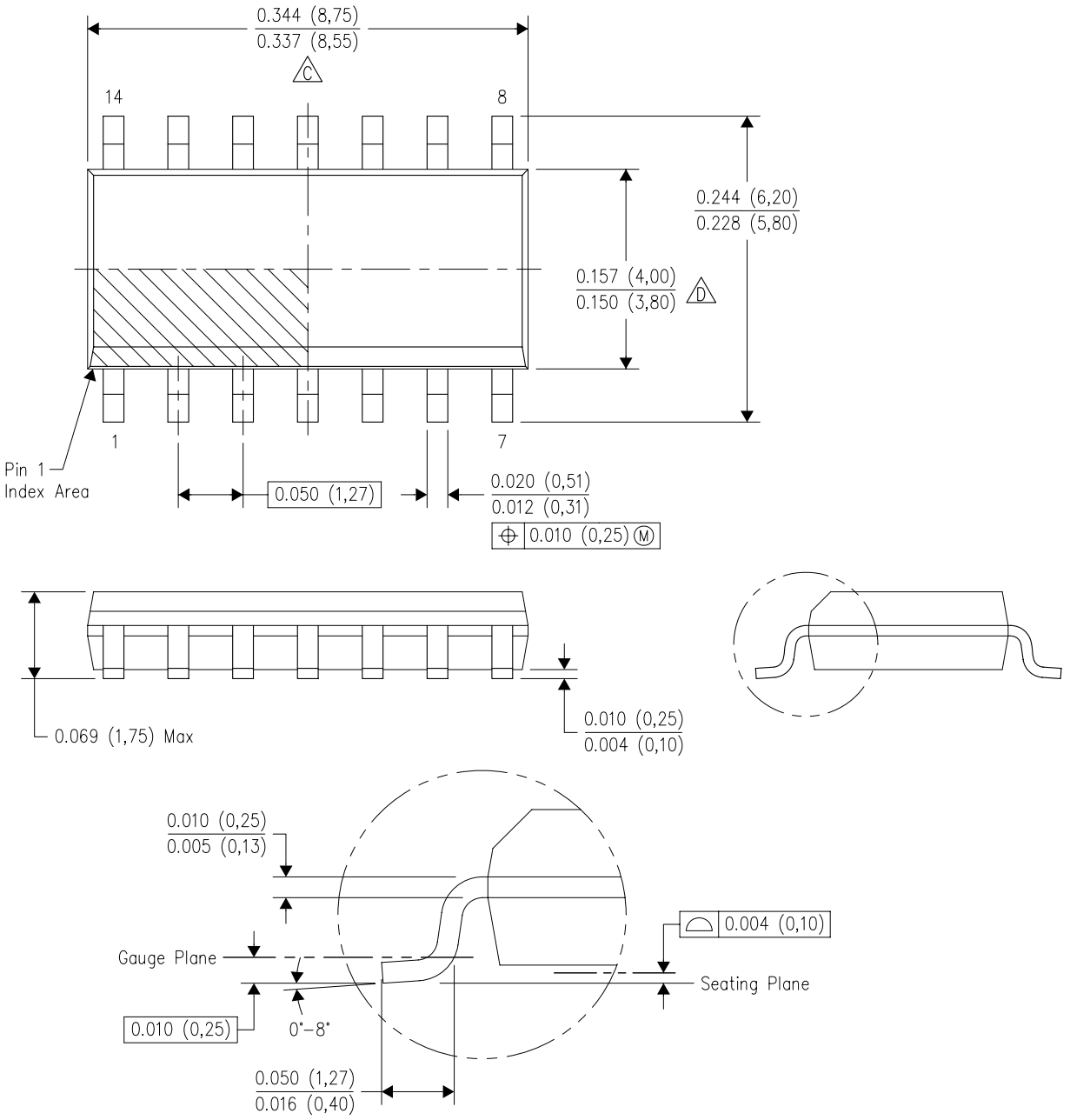
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

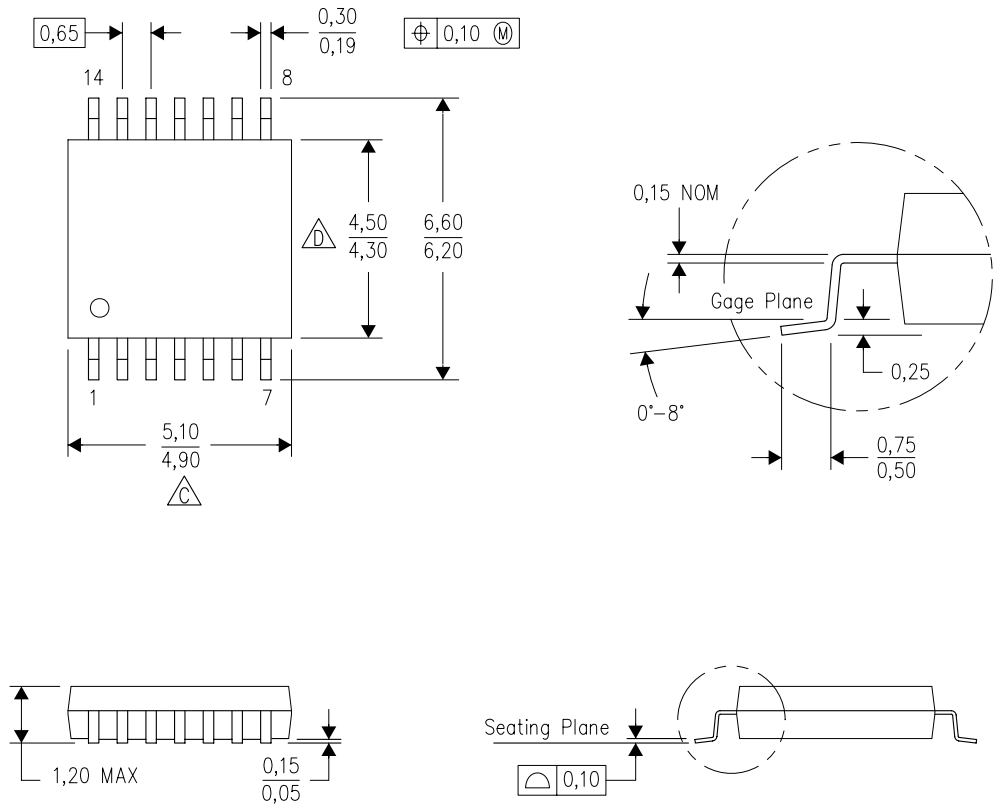
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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