

SN74LV4051A 8 通道模拟多路复用器和多路解复用器

1 特性

- 1.65V 至 5.5V V_{CC} 运行
- 所有端口上均支持以混合模式电压运行
- 高开关输出电压比
- 低开关间串扰
- 单独的开关控制
- 极低输入电流
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求
 - 2000V 人体放电模型 (A114-A)
 - 200V 机器放电模型 (A115-A)
 - 1000V 充电器件模型 (C101)

2 应用

- 电信
- 紧急呼叫
- 信息娱乐系统

3 说明

SN74LV4051A 8 通道 CMOS 模拟多路复用器和多路解复用器可在 1.65V 至 5.5V V_{CC} 电压下运行。

SN74LV4051A 器件能够处理模拟和数字信号。每个通道允许在任意方向传输振幅高达 5.5V (峰值) 的信号。

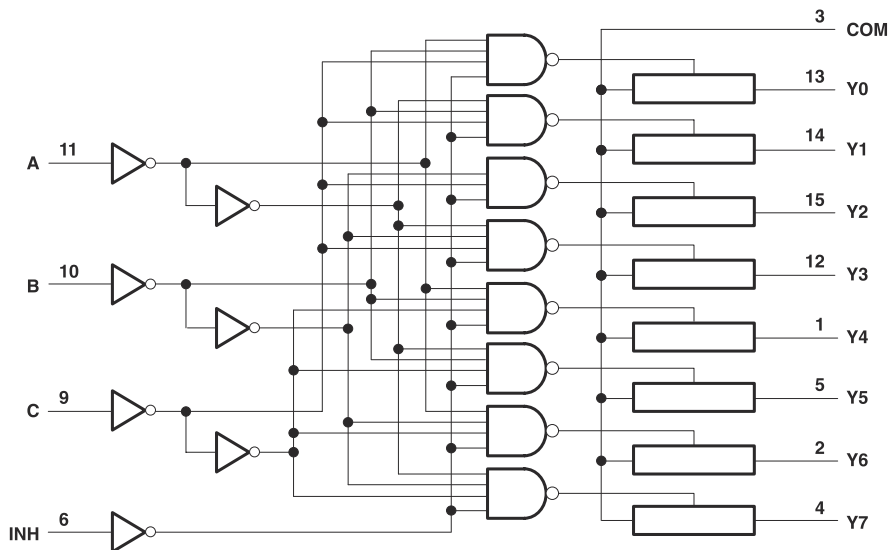
应用包括用于模数和数模转换系统的信号选通、斩波、调制/解调 (调制解调器) 以及信号多路复用。

封装信息

| 器件型号 | 封装 ⁽¹⁾ | 封装尺寸 ⁽²⁾ |
|-------------|-------------------|---------------------|
| SN74LV4051A | PW (TSSOP , 16) | 5mm × 6.4mm |
| | D (SOIC , 16) | 9.9mm × 6mm |
| | RGY (VQFN , 16) | 4mm × 3.5mm |

(1) 有关更多信息，请参阅节 11。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



逻辑图 (正逻辑)



Table of Contents

| | | | |
|---|-----------|--|-----------|
| 1 特性 | 1 | 7.2 Functional Block Diagram..... | 14 |
| 2 应用 | 1 | 7.3 Feature Description..... | 14 |
| 3 说明 | 1 | 7.4 Device Functional Modes..... | 14 |
| 4 Pin Configuration and Functions | 3 | 8 Application and Implementation | 15 |
| 5 Specifications | 4 | 8.1 Application Information..... | 15 |
| 5.1 Absolute Maximum Ratings..... | 4 | 8.2 Typical Application..... | 15 |
| 5.2 ESD Ratings..... | 4 | 8.3 Power Supply Recommendations..... | 16 |
| 5.3 Thermal Information: SN74LV4051A..... | 4 | 8.4 Layout..... | 16 |
| 5.4 Recommended Operating Conditions..... | 5 | 9 Device and Documentation Support | 18 |
| 5.5 Electrical Characteristics..... | 5 | 9.1 Documentation Support..... | 18 |
| 5.6 Timing Characteristics $V_{CC} = 2.5V \pm 0.2V$ | 7 | 9.2 接收文档更新通知..... | 18 |
| 5.7 Timing Characteristics $V_{CC} = 3.3V \pm 0.3V$ | 7 | 9.3 支持资源..... | 18 |
| 5.8 Timing Characteristics $V_{CC} = 5V \pm 0.5V$ | 8 | 9.4 Trademarks..... | 18 |
| 5.9 AC Characteristics..... | 8 | 9.5 静电放电警告..... | 18 |
| 5.10 Typical Characteristics..... | 10 | 9.6 术语表..... | 18 |
| 6 Parameter Measurement Information | 11 | 10 Revision History | 18 |
| 7 Detailed Description | 14 | 11 Mechanical, Packaging, and Orderable Information | 19 |
| 7.1 Overview..... | 14 | | |

4 Pin Configuration and Functions

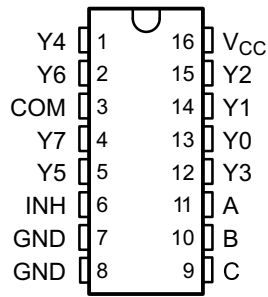


图 4-1. D, PW Package, 16-Pin SOIC, TSSOP (Top View)

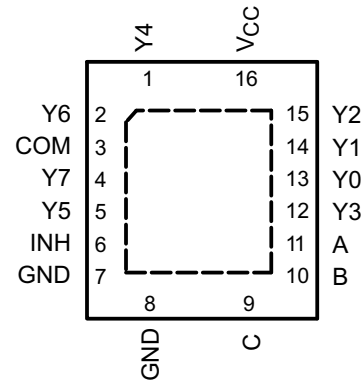


图 4-2. RGY Package 16-Pin VQFN With Exposed Thermal Pad (Top View)

表 4-1. Pin Functions

| PIN | | TYPE ⁽²⁾ | DESCRIPTION |
|-----------------|------|---------------------|---|
| NAME | NO. | | |
| A | 11 | I | Selector line A for outputs (see § 7.4 for specific information) |
| B | 10 | I | Selector line B for outputs (see § 7.4 for specific information) |
| C | 9 | I | Selector line C for outputs (see § 7.4 for specific information) |
| COM | 3 | O/I ⁽¹⁾ | Output/Input of mux |
| GND | 7, 8 | — | Ground |
| INH | 6 | I ⁽¹⁾ | Enables the outputs of the device. Logic low level with turn the outputs on, high level will turn them off. |
| Y0 | 13 | I/O ⁽¹⁾ | Input/Output to mux |
| Y1 | 14 | I/O ⁽¹⁾ | Input/Output to mux |
| Y2 | 15 | I/O ⁽¹⁾ | Input/Output to mux |
| Y3 | 12 | I/O ⁽¹⁾ | Input/Output to mux |
| Y4 | 1 | I/O ⁽¹⁾ | Input/Output of mux |
| Y5 | 5 | I/O ⁽¹⁾ | Input/Output to mux |
| Y6 | 2 | I/O ⁽¹⁾ | Input/Output to mux |
| Y7 | 4 | I/O ⁽¹⁾ | Input/Output to mux |
| V _{CC} | 16 | — | Device power |

- (1) These I/O descriptions represent the device when used as a multiplexer, when this device is operated as a demultiplexer pins Y0-Y7 may be considered outputs (O) and the COM pin may be considered inputs (I).
- (2) I = inputs, O = outputs

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾ ⁽³⁾

| | | MIN | MAX | UNIT |
|------------------|--|--|-----------------------|------|
| V _{CC} | Supply voltage | - 0.5 | 7.0 | V |
| V _I | Logic input voltage range | - 0.5 | 7.0 | V |
| V _{IO} | Switch I/O voltage range ⁽²⁾ ⁽³⁾ | - 0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | | mA |
| I _{IOK} | Switch IO diode clamp current | V _{IO} < 0 or V _{IO} > V _{CC} | 50 | mA |
| I _T | Switch continuous current | V _{IO} = 0 to V _{CC} | ±25 | mA |
| | Continuous current through V _{CC} or GND | | ±50 | mA |
| T _J | Junction temperature | | 150 | °C |
| T _{stg} | Storage temperature | - 65 | 150 | °C |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (3) This value is limited to 5.5V maximum

5.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | ±1000 | |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Thermal Information: SN74LV4051A

| THERMAL METRIC ⁽¹⁾ | | SN74LV4051A | SN74LV4051A | SN74LV4051A | UNIT |
|-------------------------------|--|-------------|-------------|-------------|------|
| | | D (SOIC) | PW (TSSOP) | RGY (VQFN) | |
| | | 16 PINS | 16 PINS | 16 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 115.2 | 140.2 | 89.4 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 75.0 | 72.6 | 89.7 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 76.6 | 98.7 | 65.4 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 31.3 | 13.4 | 25.0 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 75.7 | 97.3 | 65.2 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | 48.9 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | NOM | MAX | UNIT |
|-----------------|--|--------------------------------|-----------------------|-----------------------|------|
| V _{CC} | Supply voltage | 1 ⁽²⁾ | | 5.5 | V |
| V _{IH} | High-level input voltage, logic control inputs | V _{CC} = 1.65 | | 5.5 | V |
| | | V _{CC} = 2V | 1.5 | 5.5 | |
| | | V _{CC} = 2.3V to 2.7V | V _{CC} × 0.7 | 5.5 | |
| | | V _{CC} = 3V to 3.6V | V _{CC} × 0.7 | 5.5 | |
| | | V _{CC} = 4.5V to 5.5V | V _{CC} × 0.7 | 5.5 | |
| V _{IL} | Low-level input voltage, logic control inputs | V _{CC} = 1.65 | 0 | 0.4 | V |
| | | V _{CC} = 2V | 0 | 0.5 | |
| | | V _{CC} = 2.3V to 2.7V | 0 | V _{CC} × 0.3 | |
| | | V _{CC} = 3V to 3.6V | 0 | V _{CC} × 0.3 | |
| | | V _{CC} = 4.5V to 5.5V | 0 | V _{CC} × 0.3 | |
| V _I | Logic control input voltage | 0 | | 5.5 | V |
| V _{IO} | Switch input or output voltage | 0 | | V _{CC} | V |
| Δt/ΔV | Logic input transition rise or fall rate | V _{CC} = 2.3V to 2.7V | | 200 | ns/V |
| | | V _{CC} = 3V to 3.6V | | 100 | |
| | | V _{CC} = 4.5V to 5.5V | | 20 | |
| T _A | Ambient temperature | - 40 | | 125 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.
- (2) When using a V_{CC} of ≤1.2V, it is recommended to use these devices only for transmitting digital signals. When supply voltage is near 1.2V the analog switch ON resistance becomes very non-linear

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | Condition | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------|----------------------------|--|-----------------|-------|-----|-----|------|
| Γ _{ON} | ON-state switch resistance | I _T = 2mA, V _I = V _{CC} or GND, V _{INH} = V _{IL} | 25°C | 1.65V | 60 | 150 | Ω |
| Γ _{ON} | ON-state switch resistance | I _T = 2mA, V _I = V _{CC} or GND, V _{INH} = V _{IL} | - 40°C to 85°C | 1.65V | | 225 | Ω |
| Γ _{ON} | ON-state switch resistance | I _T = 2mA, V _I = V _{CC} or GND, V _{INH} = V _{IL} | - 40°C to 125°C | 1.65V | | 225 | Ω |
| Γ _{ON} | ON-state switch resistance | I _T = 2mA, V _I = V _{CC} or GND, V _{INH} = V _{IL} | 25°C | 2.3V | 38 | 180 | Ω |
| | | | - 40°C to 85°C | | 225 | | |
| | | | - 40°C to 125°C | | 225 | | |
| | | | 25°C | 3V | 30 | 150 | Ω |
| | | | - 40°C to 85°C | | 190 | | |
| | | | - 40°C to 125°C | | 190 | | |
| | | | 25°C | 4.5V | 22 | 75 | Ω |
| | | | - 40°C to 85°C | | 100 | | |
| | | | - 40°C to 125°C | | 100 | | |
| Γ _{ON(p)} | Peak ON-state resistance | I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL} | 25°C | 1.65V | 220 | 600 | Ω |

5.5 Electrical Characteristics (续)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | Condition | T _A | V _{CC} | MIN | TYP | MAX | UNIT | | | |
|------------------------------------|--|--|-----------------|-----------------|-----------------|------|------|------|-----|-----|---|
| r _{ON(p)} | Peak ON-state resistance | I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL} | - 40°C to 85°C | 1.65V | | | 700 | Ω | | | |
| r _{ON(p)} | Peak ON-state resistance | I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL} | - 40°C to 125°C | 1.65V | | | 700 | Ω | | | |
| r _{ON(p)} | Peak ON-state resistance | I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL} | 25°C | 2.3V | | 113 | 500 | Ω | | | |
| | | | - 40°C to 85°C | | | 600 | | | | | |
| | | | - 40°C to 125°C | | | 600 | | | | | |
| | | | | | | 25°C | 3V | | 54 | 180 | Ω |
| | | | | | - 40°C to 85°C | | | 225 | | | |
| | | | | | - 40°C to 125°C | | | 225 | | | |
| | | | | | | 25°C | 4.5V | | 31 | 100 | Ω |
| | | | | | - 40°C to 85°C | | | 125 | | | |
| | | | | | - 40°C to 125°C | | | 125 | | | |
| Δr _{ON} | Difference in ON-state resistance between switches | I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL} | 25°C | 1.65V | | 3 | 40 | Ω | | | |
| Δr _{ON} | Difference in ON-state resistance between switches | I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL} | - 40°C to 85°C | 1.65V | | | 50 | Ω | | | |
| Δr _{ON} | Difference in ON-state resistance between switches | I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL} | - 40°C to 85°C | 1.65V | | | 50 | Ω | | | |
| Δr _{ON} | Difference in ON-state resistance between switches | I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL} | 25°C | 2.3V | | 2.1 | 30 | Ω | | | |
| | | | - 40°C to 85°C | | | 40 | | | | | |
| | | | - 40°C to 125°C | | | 40 | | | | | |
| | | | | | | 25°C | 3V | | 1.4 | 20 | Ω |
| | | | | | - 40°C to 85°C | | | 30 | | | |
| | | | | | - 40°C to 125°C | | | 30 | | | |
| | | | | | | 25°C | 4.5V | | 1.3 | 15 | Ω |
| | | | | | - 40°C to 85°C | | | 20 | | | |
| | | | | | - 40°C to 125°C | | | 20 | | | |
| I _{IH} I _{IL} | Control input current | V _I = 5.5V or GND | 25°C | 0 to 5.5V | | | 0.1 | μA | | | |
| | | | - 40°C to 85°C | | | 1 | | | | | |
| | | | - 40°C to 125°C | | | 2 | | | | | |
| I _{S(off)} | OFF-state switch leakage current | V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH} | 25°C | 5.5V | | | 0.1 | μA | | | |
| | | | - 40°C to 85°C | | | 1 | | | | | |
| | | | - 40°C to 125°C | | | 2 | | | | | |
| I _{S(on)} | ON-state switch leakage current | V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 6-3) | 25°C | 5.5V | | | 0.1 | μA | | | |
| | | | - 40°C to 85°C | | | 1 | | | | | |
| | | | - 40°C to 125°C | | | 2 | | | | | |
| I _{CC} | Supply current | V _I = V _{CC} or GND V _{INH} = 0V | 25°C | 5.5V | | 0.01 | μA | | | | |
| | | | - 40°C to 85°C | | | 20 | | | | | |
| | | | - 40°C to 125°C | | | 40 | | | | | |

5.5 Electrical Characteristics (续)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | Condition | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|--------------------------------|----------------------------------|----------------|-----------------|-----|-----|-----|------|
| C _{IC} | Control input capacitance | f = 10MHz | 25°C | 3.3V | | 2 | | pF |
| C _{OS} | Switch terminal capacitance | f = 10MHz | 25°C | 3.3V | | 5 | | pF |
| C _{IS} | Common terminal capacitance | f = 10MHz | 25°C | 3.3V | | 23 | | pF |
| C _{OS(on)} | Common terminal ON-capacitance | f = 10MHz | 25°C | 3.3V | | 23 | | pF |
| C _F | Feedthrough capacitance | f = 10MHz | 25°C | 3.3V | | 0.5 | | pF |
| C _{PD} | Power dissipation capacitance | C _L = 50pF, f = 10MHz | 25°C | 3.3V | | 6 | | pF |

5.6 Timing Characteristics V_{CC} = 2.5V ± 0.2V

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | CONDITIONS | T _A | MIN | TYP | MAX | UNIT |
|--------------------------------------|------------------------|--------------|-------------|-----------------------|----------------|-----|------|-----|------|
| t _{PLH} t _{PHL} | Propagation delay time | COM or Yn | Yn or COM | C _L = 15pF | 25°C | | 1.9 | 10 | ns |
| | | | | | -40°C to 85°C | | | 16 | |
| | | | | | -40°C to 125°C | | | 18 | |
| t _{PZH} t _{PZL} | Enable delay time | INH | COM or Yn | C _L = 15pF | 25°C | | 6.6 | 18 | ns |
| | | | | | -40°C to 85°C | | | 23 | |
| | | | | | -40°C to 125°C | | | 25 | |
| t _{PHZ} t _{PLZ} | Disable delay time | INH | COM or Yn | C _L = 15pF | 25°C | | 7.4 | 18 | ns |
| | | | | | -40°C to 85°C | | | 23 | |
| | | | | | -40°C to 125°C | | | 25 | |
| t _{PLH} t _{PHL} | Propagation delay time | COM or Yn | Yn or COM | C _L = 50pF | 25°C | | 3.8 | 12 | ns |
| | | | | | -40°C to 85°C | | | 18 | |
| | | | | | -40°C to 125°C | | | 20 | |
| t _{PZH} t _{PZL} | Enable delay time | INH | COM or Yn | C _L = 50pF | 25°C | | 7.8 | 28 | ns |
| | | | | | -40°C to 85°C | | | 35 | |
| | | | | | -40°C to 125°C | | | 35 | |
| t _{PHZ} t _{PLZ} | Disable delay time | INH | COM or Yn | C _L = 50pF | 25°C | | 11.5 | 28 | ns |
| | | | | | -40°C to 85°C | | | 35 | |
| | | | | | -40°C to 125°C | | | 35 | |

5.7 Timing Characteristics V_{CC} = 3.3V ± 0.3V

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | CONDITIONS | T _A | MIN | TYP | MAX | UNIT |
|--------------------------------------|------------------------|--------------|-------------|-----------------------|----------------|-----|-----|-----|------|
| t _{PLH} t _{PHL} | Propagation delay time | COM or Yn | Yn or COM | C _L = 15pF | 25°C | | 1.2 | 6 | ns |
| | | | | | -40°C to 85°C | | | 10 | |
| | | | | | -40°C to 125°C | | | 12 | |
| t _{PZH} t _{PZL} | Enable delay time | INH | COM or Yn | C _L = 15pF | 25°C | | 4.7 | 12 | ns |
| | | | | | -40°C to 85°C | | | 15 | |
| | | | | | -40°C to 125°C | | | 18 | |

5.7 Timing Characteristics $V_{CC} = 3.3V \pm 0.3V$ (续)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | CONDITIONS | T_A | MIN | TYP | MAX | UNIT |
|------------------------|------------------------|--------------|-------------|--------------|----------------|-----|-----|-----|------|
| t_{PHZ} t_{PLZ} | Disable delay time | INH | COM or Yn | $C_L = 15pF$ | 25°C | | 5.7 | 12 | ns |
| | | | | | -40°C to 85°C | | | 15 | |
| | | | | | -40°C to 125°C | | | 18 | |
| t_{PLH} t_{PHL} | Propagation delay time | COM or Yn | Yn or COM | $C_L = 50pF$ | 25°C | | 2.5 | 9 | ns |
| | | | | | -40°C to 85°C | | | 12 | |
| | | | | | -40°C to 125°C | | | 14 | |
| t_{PZH} t_{PZL} | Enable delay time | INH | COM or Yn | $C_L = 50pF$ | 25°C | | 5.5 | 20 | ns |
| | | | | | -40°C to 85°C | | | 25 | |
| | | | | | -40°C to 125°C | | | 25 | |
| t_{PHZ} t_{PLZ} | Disable delay time | INH | COM or Yn | $C_L = 50pF$ | 25°C | | 8.8 | 20 | ns |
| | | | | | -40°C to 85°C | | | 25 | |
| | | | | | -40°C to 125°C | | | 25 | |

5.8 Timing Characteristics $V_{CC} = 5V \pm 0.5V$

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | CONDITIONS | T_A | MIN | TYP | MAX | UNIT |
|------------------------|------------------------|--------------|-------------|--------------|----------------|-----|-----|-----|------|
| t_{PLH} t_{PHL} | Propagation delay time | COM or Yn | Yn or COM | $C_L = 15pF$ | 25°C | | 0.6 | 4 | ns |
| | | | | | -40°C to 85°C | | | 7 | |
| | | | | | -40°C to 125°C | | | 10 | |
| t_{PZH} t_{PZL} | Enable delay time | INH | COM or Yn | $C_L = 15pF$ | 25°C | | 3.5 | 8 | ns |
| | | | | | -40°C to 85°C | | | 10 | |
| | | | | | -40°C to 125°C | | | 12 | |
| t_{PHZ} t_{PLZ} | Disable delay time | INH | COM or Yn | $C_L = 15pF$ | 25°C | | 4.4 | 10 | ns |
| | | | | | -40°C to 85°C | | | 11 | |
| | | | | | -40°C to 125°C | | | 12 | |
| t_{PLH} t_{PHL} | Propagation delay time | COM or Yn | Yn or COM | $C_L = 50pF$ | 25°C | | 1.5 | 6 | ns |
| | | | | | -40°C to 85°C | | | 8 | |
| | | | | | -40°C to 125°C | | | 10 | |
| t_{PZH} t_{PZL} | Enable delay time | INH | COM or Yn | $C_L = 50pF$ | 25°C | | 4 | 14 | ns |
| | | | | | -40°C to 85°C | | | 18 | |
| | | | | | -40°C to 125°C | | | 18 | |
| t_{PHZ} t_{PLZ} | Disable delay time | INH | COM or Yn | $C_L = 50pF$ | 25°C | | 6.2 | 14 | ns |
| | | | | | -40°C to 85°C | | | 18 | |
| | | | | | -40°C to 125°C | | | 18 | |

5.9 AC Characteristics

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | Device | CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|--------------|-------------|------------|---|-----------------|-----|-----|------|
| Frequency response (switch on) | COM or Yn | Yn or COM | SN74LV4051 | $C_L = 50pF$, $R_L = 600\Omega$, $F_{in} = 1MHz$ (sine wave) (see Figure 6-6) (1) | $V_{CC} = 2.3V$ | | 20 | MHz |
| | | | | | $V_{CC} = 3V$ | | 25 | |
| | | | | | $V_{CC} = 4.5V$ | | 35 | |

5.9 AC Characteristics (续)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | Device | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--------------|-------------|--------|---|--|-----|-----|------|
| Charge Injection (control input to signal output) | INH | COM or Yn | | $C_L = 50\text{pF}$, $R_L = 600\ \Omega$, $F_{in} = 1\text{MHz}$ (sine wave) (see Figure 6-8) | $V_{CC} = 2.3\text{V}$ | 20 | | mV |
| | | | | | $V_{CC} = 3\text{V}$ | 35 | | |
| | | | | | $V_{CC} = 4.5\text{V}$ | 60 | | |
| Feedthrough attenuation (switch off) | COM or Yn | Yn or COM | | $C_L = 50\text{pF}$, $R_L = 600\ \Omega$, $F_{in} = 1\text{MHz}$ (sine wave) (see Figure 6-9) (2) | $V_{CC} = 2.3\text{V}$ | -45 | | dB |
| | | | | | $V_{CC} = 3\text{V}$ | -45 | | |
| | | | | | $V_{CC} = 4.5\text{V}$ | -45 | | |
| Crosstalk (between any switches) | COM or Yn | Yn or COM | | $C_L = 50\text{pF}$, $R_L = 600\ \Omega$, $F_{in} = 1\text{MHz}$ (sine wave) (see Figure 6-7) (2) | $V_{CC} = 2.3\text{V}$ | -45 | | dB |
| | | | | | $V_{CC} = 3\text{V}$ | -45 | | |
| | | | | | $V_{CC} = 4.5\text{V}$ | -45 | | |
| Sine-wave distortion | COM or Yn | Yn or COM | | $C_L = 50\text{pF}$, $R_L = 10\text{k}\ \Omega$, $F_{in} = 1\text{kHz}$ (sine wave) (see Figure 6-9) | $V_I = 2V_{p-p}$ $V_{CC} = 2.3\text{V}$ | 0.1 | | % |
| | | | | | $V_I = 2.5V_{p-p}$ $V_{CC} = 3\text{V}$ | 0.1 | | |
| | | | | | $V_I = 4V_{p-p}$ $V_{CC} = 4.5\text{V}$ | 0.1 | | |

5.10 Typical Characteristics

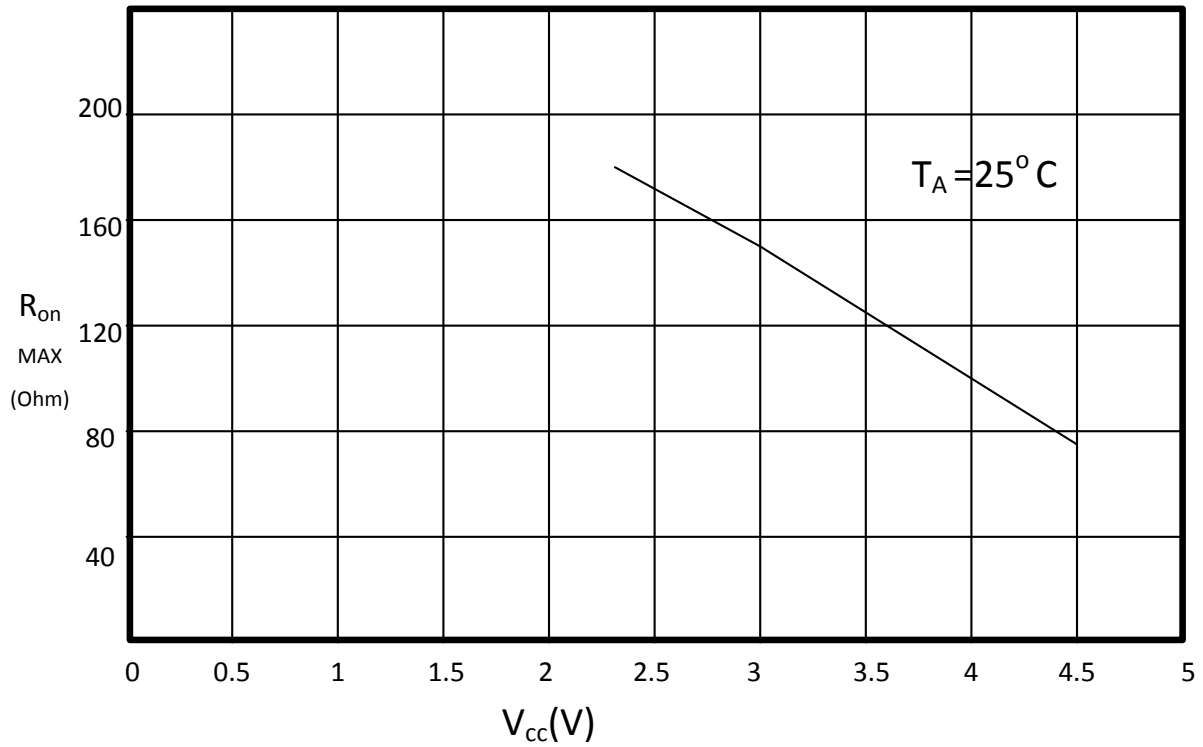


图 5-1. Plot at 25°C for V_{CC} vs Max R_{ON}

6 Parameter Measurement Information

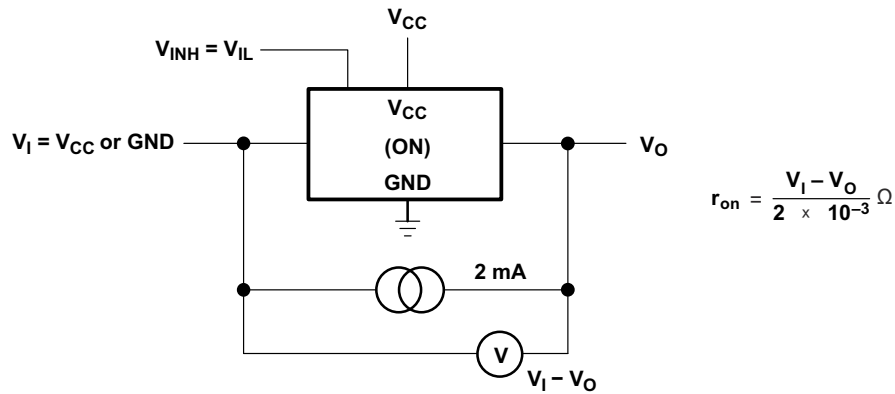
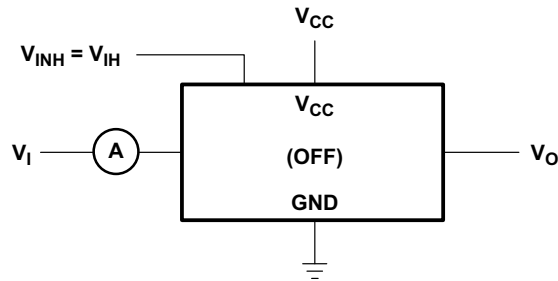


图 6-1. On-State Resistance Test Circuit



Condition 1: V_I = 0, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = 0

图 6-2. Off-State Switch Leakage-Current Test Circuit

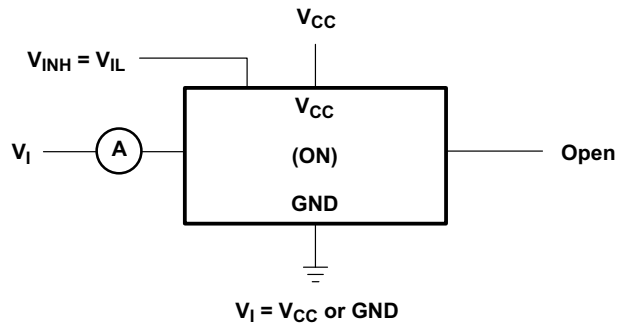


图 6-3. On-State Switch Leakage-Current Test Circuit

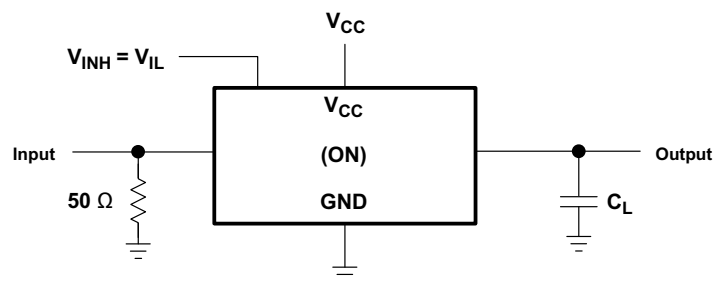


图 6-4. Propagation Delay Time, Signal Input to Signal Output

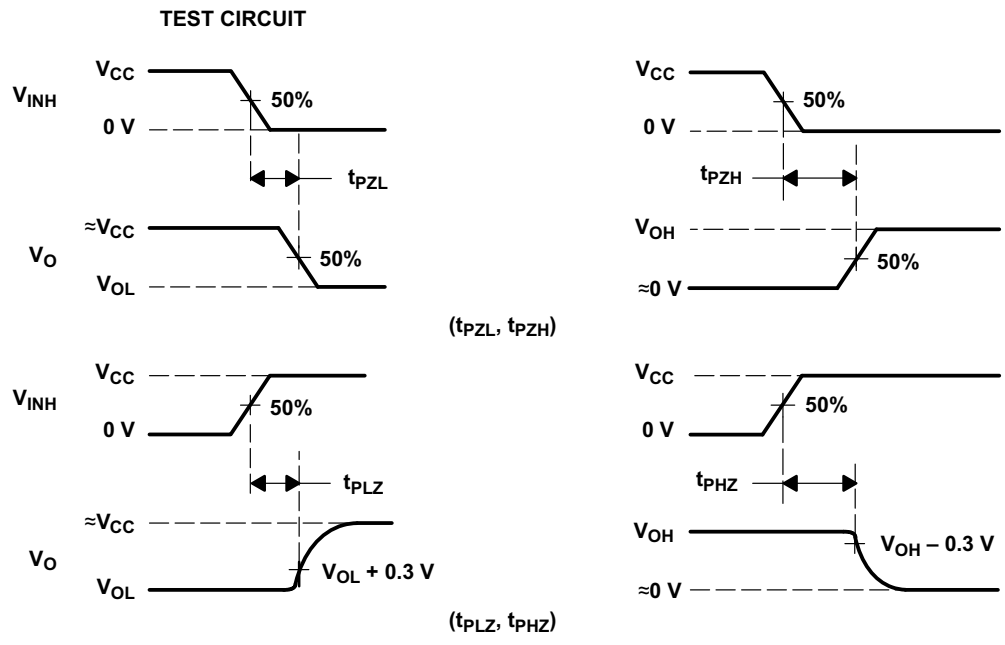
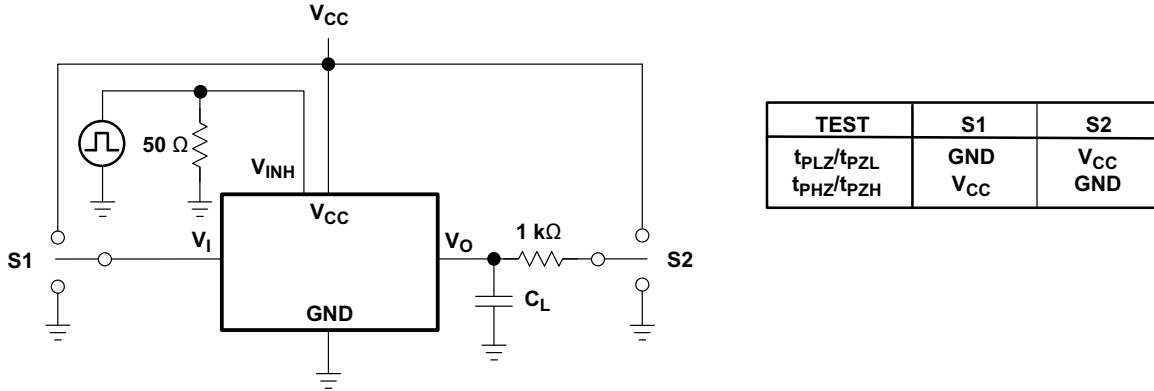
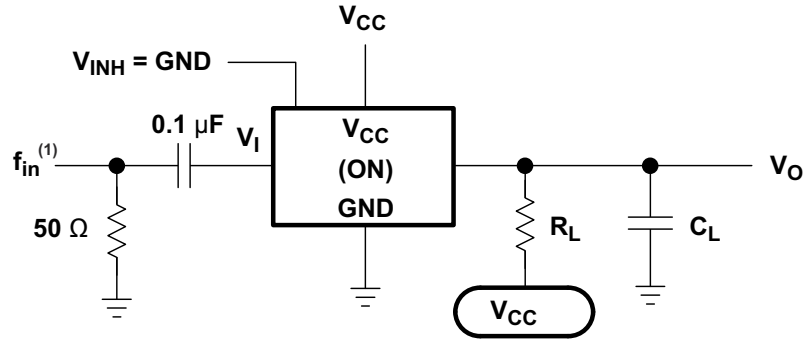


图 6-5. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output



A. f_{in} is a sine wave.

图 6-6. Frequency Response (Switch On)

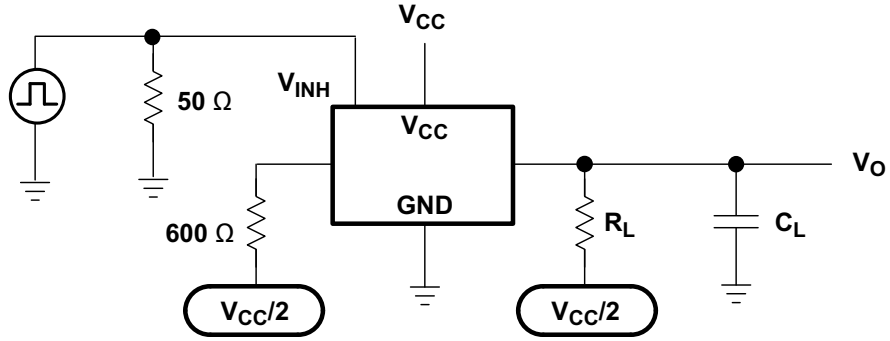


图 6-7. Crosstalk (Control Input, Switch Output)

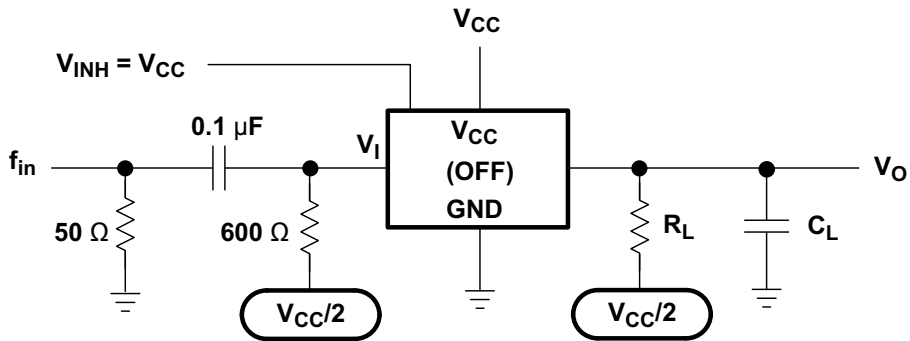


图 6-8. Feedthrough Attenuation (Switch Off)

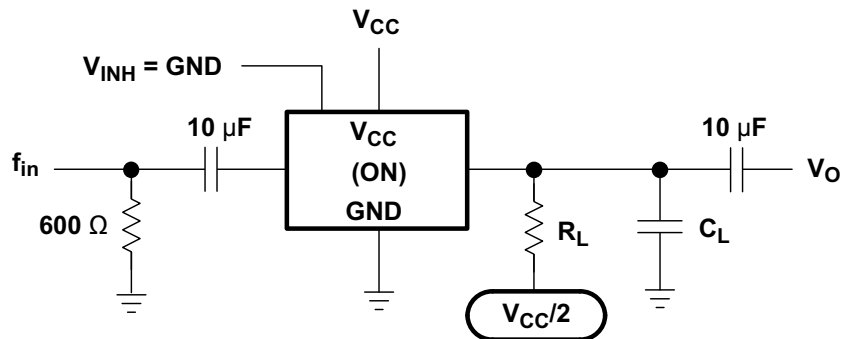


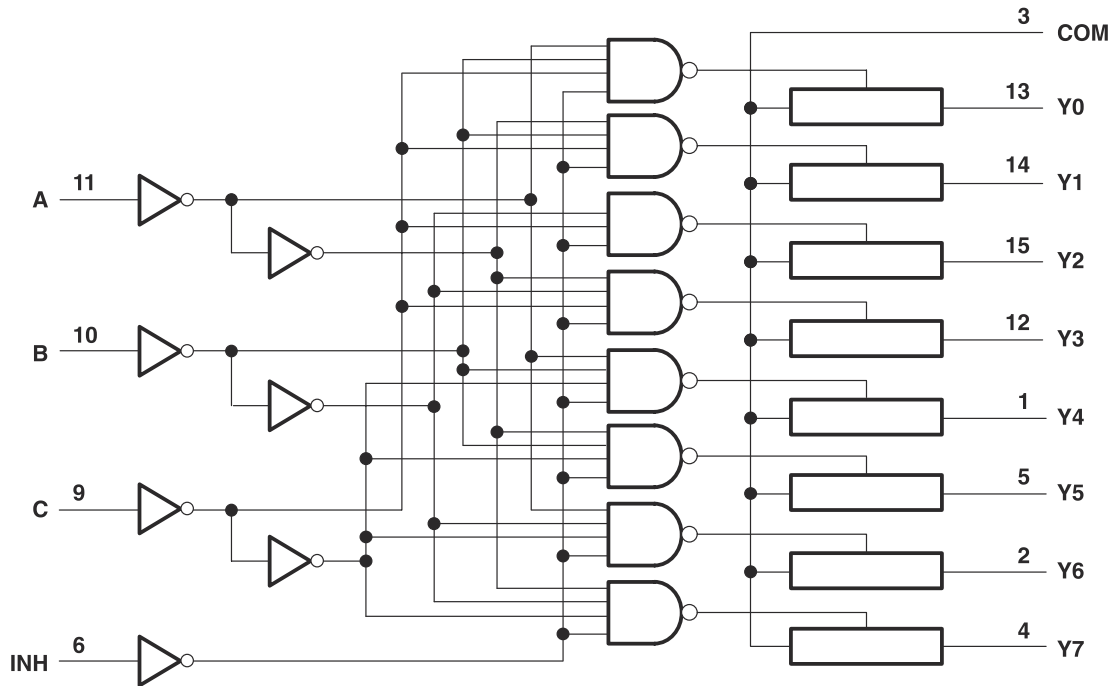
图 6-9. Sine-Wave Distortion

7 Detailed Description

7.1 Overview

The SN74LV4051A device is an 8-channel analog multiplexer. A multiplexer is used when several signals must share the same device or resource. This device allows for the selection of one of these signals at a time for analysis or propagation.

7.2 Functional Block Diagram



7.3 Feature Description

The SN74LV4051A device contains one 8-channel multiplexer for use in a variety of applications and can also be configured as demultiplexer by using the COM pin as an input and the Yn pins as outputs. This device is qualified to operate in the temperature range -40°C to +85°C (maximum depends on package type).

7.4 Device Functional Modes

表 7-1. Function Table

| INPUTS | | | | ON CHANNEL |
|--------|---|---|---|------------|
| INH | C | B | A | |
| L | L | L | L | Y0 |
| L | L | L | H | Y1 |
| L | L | H | L | Y2 |
| L | L | H | H | Y3 |
| L | H | L | L | Y4 |
| L | H | L | H | Y5 |
| L | H | H | L | Y6 |
| L | H | H | H | Y7 |
| H | X | X | X | None |

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

A multiplexer is used in applications where multiple signals share a resource. In [图 8-1](#), several different sensors are connected to the analog-to-digital converter (ADC) of a microcontroller unit (MCU).

8.2 Typical Application

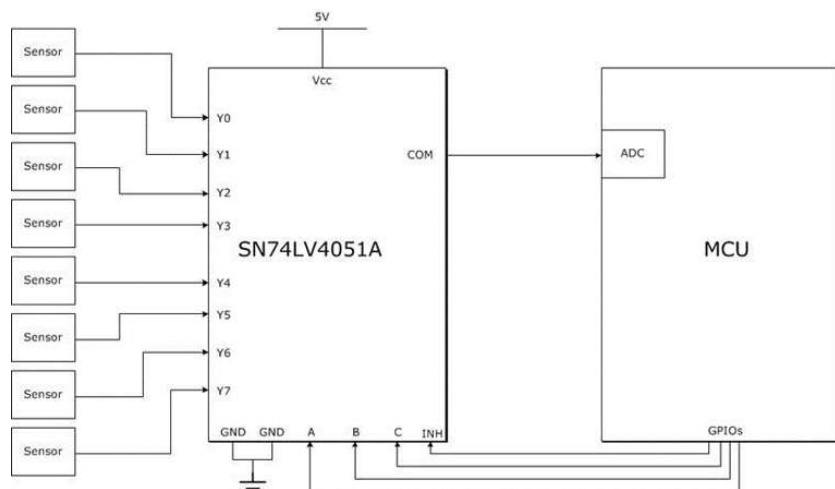


图 8-1. Example of Multiplexer Use With Analog Sensors and the ADC of an MCU

8.2.1 Design Requirements

Designing with the SN74LV4051A device requires a stable input voltage between 2V (see [节 5.4](#) for details) and 5.5V. Another important design consideration are the characteristics of the signal being multiplexed—ensure no important information is lost due to timing or incompatibility with this device.

8.2.2 Detailed Design Procedure

Processing eight different analog signals normally requires eight separate ADCs, but [图 8-1](#) shows how to achieve this using only one ADC and four GPIOs (general-purpose input/outputs).

8.2.3 Application Curve

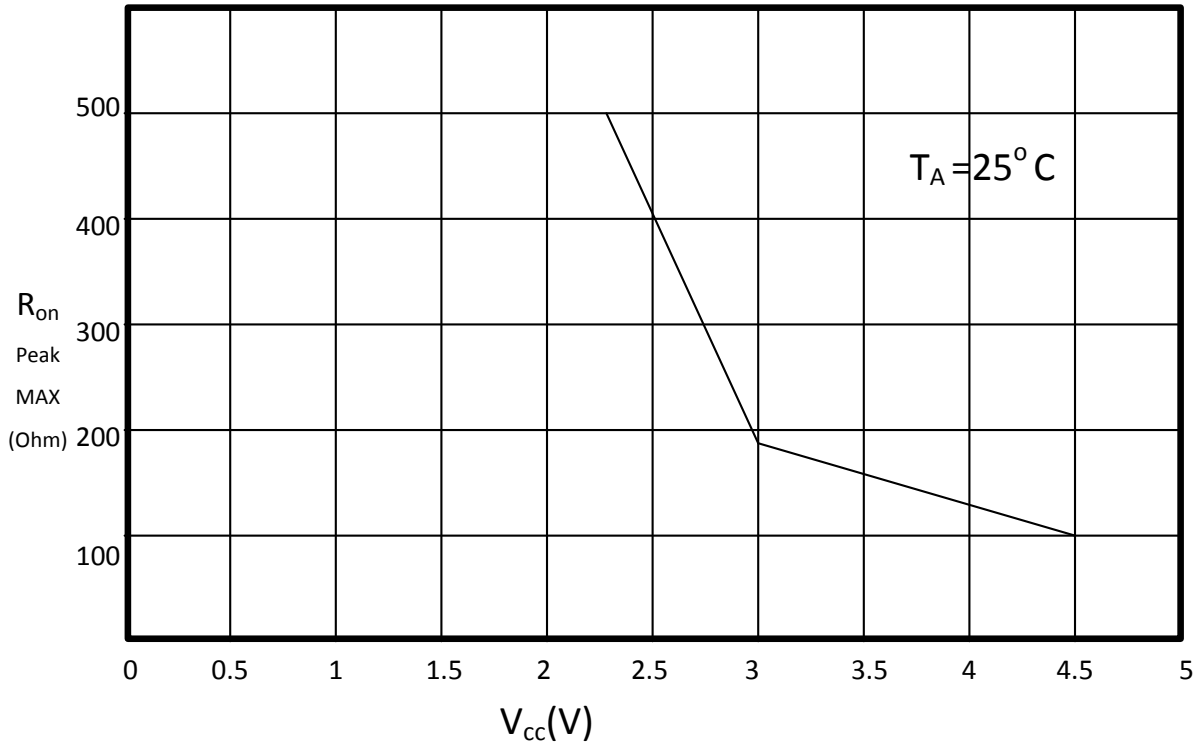


图 8-2. Plot at 25°C for V_{CC} vs Max R_{ON(peak)}

8.3 Power Supply Recommendations

Most systems have a common 3.3V or 5V rail that can supply the V_{CC} pin of this device. If this rail is not available, a switched-mode power supply (SMPS) or a low dropout regulator (LDO) can supply this device from a higher-voltage rail.

8.4 Layout

8.4.1 Layout Guidelines

TI recommends keeping the signal lines as short and straight as possible (see 图 8-3). Incorporation of microstrip or stripline techniques are also recommended when signal lines are more than 1" long. These traces must be designed with a characteristic impedance of either 50Ω or 75Ω as required by the application. *Do not* place this device too close to high-voltage switching components because they may cause interference.

8.4.2 Layout Example

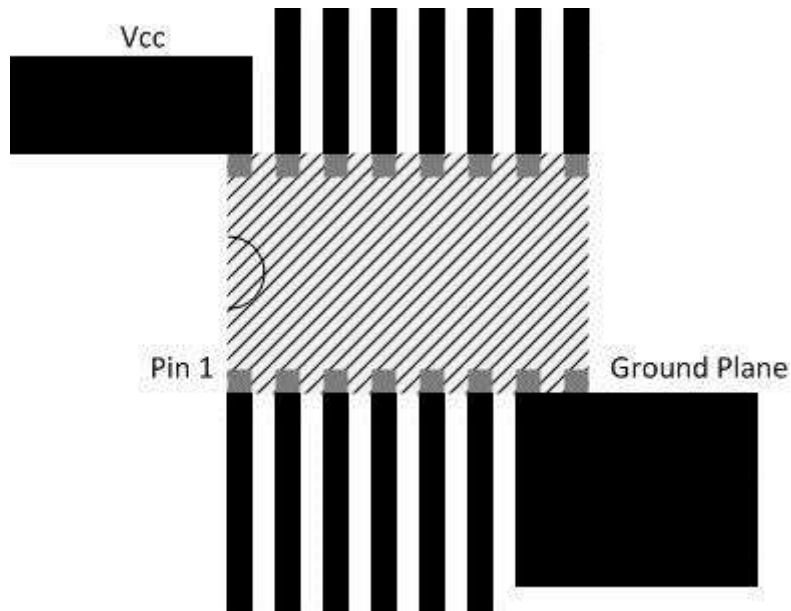


图 8-3. Layout Schematic

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)

9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision I (September 2015) to Revision J (June 2024) | Page |
|---|------|
| • 通篇更新了表格、图和交叉参考的编号格式..... | 1 |
| • Added new VIH and VIL Specifications at 1.65V Vcc..... | 5 |
| • Increased max ambient temperature max to 125C..... | 5 |
| • Added Ron, Ron Peak, and Delta Ron Specifications at 1.65V Vcc..... | 5 |
| • Added Ron, Ron Peak, and Delta Ron Specifications at 125C..... | 5 |
| • Added Timing Specifications at 125C..... | 7 |

| Changes from Revision H (April 2005) to Revision I (September 2015) | Page |
|---|------|
| • 添加了 器件信息表 、 引脚功能表 、 ESD 等级表 、 热性能信息表 、 详细说明部分 、 应用和实施部分 、 电源相关建议部分 、 布局部分 、 器件和文档支持部分 ，以及 机械 、 封装和可订购信息部分 | 1 |
| • 删除了数据表中的 SN54LV4051A 器件型号..... | 1 |
| • 删除了 订购信息表 | 1 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN74LV4051ADBR | NRND | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LW051A | |
| SN74LV4051ADGVR | NRND | TVSOP | DGV | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LW051A | |
| SN74LV4051ADGVRG4 | NRND | TVSOP | DGV | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LW051A | |
| SN74LV4051ADR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | LV4051A | Samples |
| SN74LV4051AN | NRND | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74LV4051AN | |
| SN74LV4051ANS | NRND | SO | NS | 16 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV4051A | |
| SN74LV4051ANSR | NRND | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV4051A | |
| SN74LV4051APWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | LW051A | Samples |
| SN74LV4051ARGYR | ACTIVE | VQFN | RGY | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LW051A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV4051A :

- Automotive : [SN74LV4051A-Q1](#)
- Enhanced Product : [SN74LV4051A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV4051ADBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LV4051ADGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV4051ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV4051ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV4051APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV4051APWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV4051APWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV4051ARGYR | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV4051ADBR | SSOP | DB | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV4051ADGVR | TVSOP | DGV | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV4051ADR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LV4051ANSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV4051APWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV4051APWRG4 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV4051APWT | TSSOP | PW | 16 | 250 | 356.0 | 356.0 | 35.0 |
| SN74LV4051ARGYR | VQFN | RGY | 16 | 3000 | 367.0 | 367.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LV4051AD | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74LV4051AN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LV4051AN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LV4051ANS | NS | SOP | 16 | 50 | 530 | 10.5 | 4000 | 4.1 |
| SN74LV4051APW | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| SN74LV4051APWG4 | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB0016A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

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