

## SN74LV4052A 双路 4 通道模拟多路复用器和多路解复用器

### 1 特性

- 1.65V 至 5.5V  $V_{CC}$  运行
- 快速开关
- 高开关输出电压比
- 低开关间串扰
- 极低输入电流
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求：
  - 2000V 人体放电模型 (A114-A)
  - 1000V 充电器件模型 (C101)

### 2 应用

- 电信
- 信息娱乐系统
- 信号选通和隔离
- 家用电器
- 可编程逻辑电路
- 调制和解调

### 3 说明

SNx4LV4052A 器件是可在 1.65V 至 5.5V  $V_{CC}$  电压下运行的双路 4 通道 CMOS 模拟多路复用器和多路解复用器。

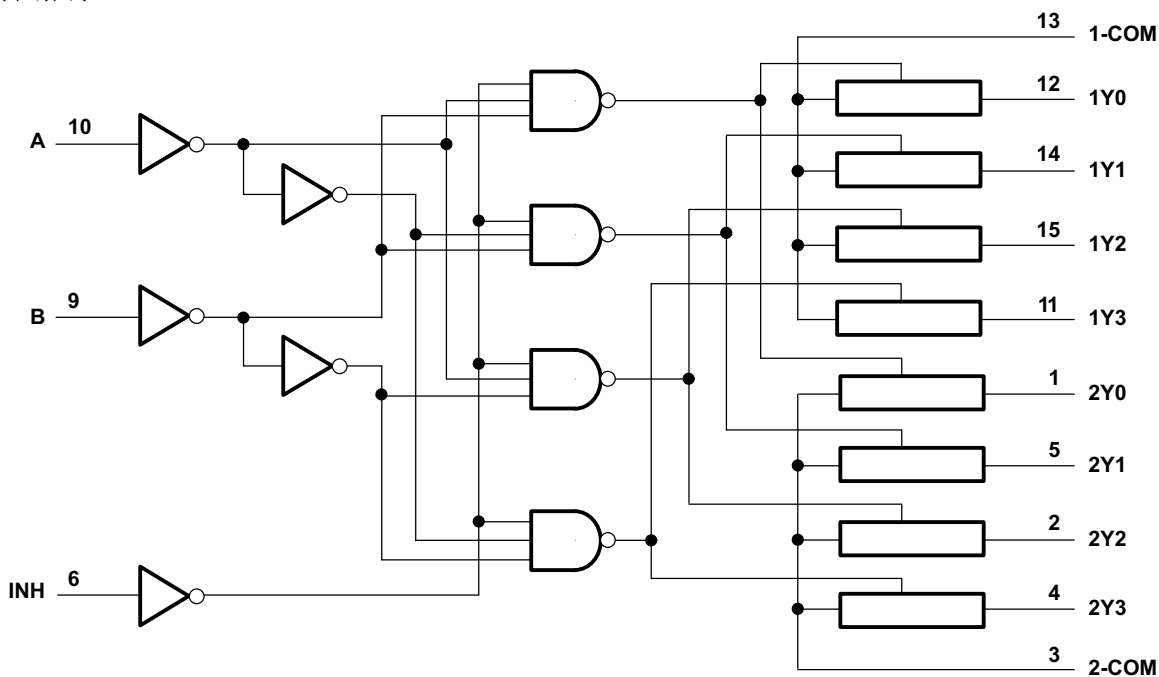
SNx4LV4052A 器件能够处理模拟和数字信号。每个通道允许在任意方向传输振幅高达 5.5V (峰值) 的信号。

#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
SNx4LV4052A	D (SOIC, 16)	9.9mm × 6mm
	PW (TSSOP, 16)	5mm × 6.4mm
	RGY (VQFN, 16)	4mm × 3.5mm

(1) 有关更多信息，请参阅节 11。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



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逻辑图 (正逻辑)



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## 4 Pin Configuration and Functions

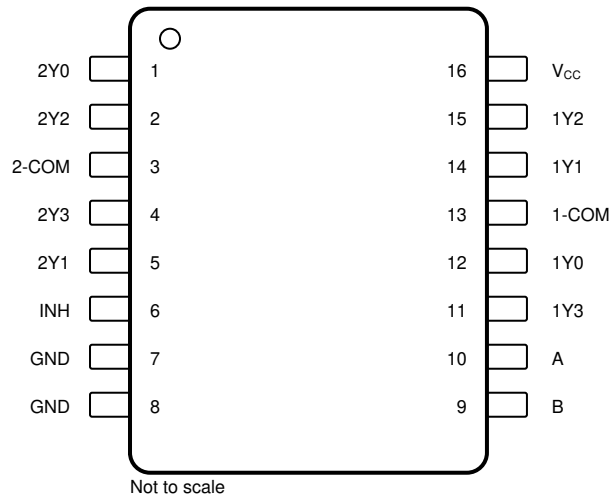


图 4-1. D or PW Packages, 16-Pin SOIC or TSSOP (Top View)

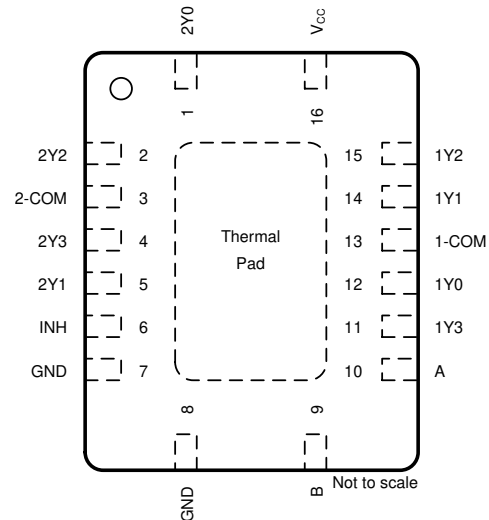


图 4-2. RGY Package, 16-Pin VQFN With Thermal Pad (Top View)

表 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
2Y0	1	I/O	Port 2 channel 0
2Y2	2	I/O	Port 2 channel 2
2-COM	3	I/O	Port 2 common channel
2Y3	4	I/O	Port 2 channel 3
2Y1	5	I/O	Port 2 channel 1
INH	6	I	Inhibit input
GND	7	—	Device ground
GND	8	—	Device ground
B	9	I	Logic input selector B
A	10	I	Logic input selector A
1Y3	11	I/O	Port 1 channel 3
1Y0	12	I/O	Port 1 channel 0
1-COM	13	I/O	Port 1 common channel
1Y1	14	I/O	Port 1 channel 1
1Y2	15	I/O	Port 1 channel 2
V <sub>CC</sub>	16	—	Device power

(1) I = input, O = output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (3)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	- 0.5	7.0	V
$V_I$	Logic input voltage range	- 0.5	7.0	V
$V_{IO}$	Switch I/O voltage range <sup>(2) (3)</sup>	- 0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		mA
$I_{IOK}$	Switch IO diode clamp current	$V_{IO} < 0$ or $V_{IO} > V_{CC}$	50	mA
$I_T$	Switch continuous current	$V_{IO} = 0$ to $V_{CC}$	$\pm 25$	mA
	Continuous current through $V_{CC}$ or GND		$\pm 50$	mA
$T_J$	Junction temperature		150	°C
$T_{stg}$	Storage temperature	- 65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (3) This value is limited to 5.5V maximum

### 5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	All pins	$\pm 4000$
		Charged device model (CDM), per AEC Q100-011	All pins	$\pm 1500$

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Thermal Information: SN74LV4052A

THERMAL METRIC <sup>(1)</sup>		SN74LV4052A	SN74LV4052A	SN74LV4052A	UNIT
		D (SOIC)	PW (TSSOP)	RGY (VQFN)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.2	140.2	89.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.0	72.6	89.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.6	98.7	65.4	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	31.3	13.4	25.0	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	75.7	97.3	65.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	48.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1 <sup>(2)</sup>		5.5	V
V <sub>IH</sub>	High-level input voltage, logic control inputs	V <sub>CC</sub> = 1.65		5.5	V
		V <sub>CC</sub> = 2V	1.5	5.5	
		V <sub>CC</sub> = 2.3V to 2.7V	V <sub>CC</sub> × 0.7	5.5	
		V <sub>CC</sub> = 3V to 3.6V	V <sub>CC</sub> × 0.7	5.5	
		V <sub>CC</sub> = 4.5V to 5.5V	V <sub>CC</sub> × 0.7	5.5	
V <sub>IL</sub>	Low-level input voltage, logic control inputs	V <sub>CC</sub> = 1.65	0	0.4	V
		V <sub>CC</sub> = 2V	0	0.5	
		V <sub>CC</sub> = 2.3V to 2.7V	0	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 3V to 3.6V	0	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 4.5V to 5.5V	0	V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Logic control input voltage	0		5.5	V
V <sub>IO</sub>	Switch input or output voltage	0		V <sub>CC</sub>	V
Δt/ΔV	Logic input transition rise or fall rate	V <sub>CC</sub> = 2.3V to 2.7V		200	ns/V
		V <sub>CC</sub> = 3V to 3.6V		100	
		V <sub>CC</sub> = 4.5V to 5.5V		20	
T <sub>A</sub>	Ambient temperature	- 40		125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND for proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.
- (2) When using a V<sub>CC</sub> of ≤1.2V, it is recommended to use these devices only for transmitting digital signals. When supply voltage is near 1.2V the analog switch ON resistance becomes very non-linear

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	Condition	T <sub>A</sub>	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
Γ <sub>ON</sub>	ON-state switch resistance	I <sub>T</sub> = 2mA, V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>INH</sub> = V <sub>IL</sub>	25°C	1.65V	60	150	Ω
Γ <sub>ON</sub>	ON-state switch resistance	I <sub>T</sub> = 2mA, V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>INH</sub> = V <sub>IL</sub>	- 40°C to 85°C	1.65V		225	Ω
Γ <sub>ON</sub>	ON-state switch resistance	I <sub>T</sub> = 2mA, V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>INH</sub> = V <sub>IL</sub>	- 40°C to 125°C	1.65V		225	Ω
Γ <sub>ON</sub>	ON-state switch resistance	I <sub>T</sub> = 2mA, V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>INH</sub> = V <sub>IL</sub>	25°C	2.3V	38	180	Ω
			- 40°C to 85°C		225		
			- 40°C to 125°C		225		
			25°C	3V	30	150	Ω
			- 40°C to 85°C		190		
			- 40°C to 125°C		190		
			25°C	4.5V	22	75	Ω
			- 40°C to 85°C		100		
			- 40°C to 125°C		100		
Γ <sub>ON(p)</sub>	Peak ON-state resistance	I <sub>T</sub> = 2mA, V <sub>I</sub> = GND to V <sub>CC</sub> , V <sub>INH</sub> = V <sub>IL</sub>	25°C	1.65V	220	600	Ω

## 5.5 Electrical Characteristics (续)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T <sub>A</sub>	V <sub>CC</sub>	MIN	TYP	MAX	UNIT			
r <sub>ON(p)</sub>	Peak ON-state resistance	I <sub>T</sub> = 2mA, V <sub>I</sub> = GND to V <sub>CC</sub> , V <sub>INH</sub> = V <sub>IL</sub>	- 40°C to 85°C	1.65V			700	Ω			
r <sub>ON(p)</sub>	Peak ON-state resistance	I <sub>T</sub> = 2mA, V <sub>I</sub> = GND to V <sub>CC</sub> , V <sub>INH</sub> = V <sub>IL</sub>	- 40°C to 125°C	1.65V			700	Ω			
r <sub>ON(p)</sub>	Peak ON-state resistance	I <sub>T</sub> = 2mA, V <sub>I</sub> = GND to V <sub>CC</sub> , V <sub>INH</sub> = V <sub>IL</sub>	25°C	2.3V		113	500	Ω			
			- 40°C to 85°C			600					
			- 40°C to 125°C			600					
						25°C	3V		54	180	Ω
					- 40°C to 85°C			225			
					- 40°C to 125°C			225			
						25°C	4.5V		31	100	Ω
					- 40°C to 85°C			125			
					- 40°C to 125°C			125			
Δr <sub>ON</sub>	Difference in ON-state resistance between switches	I <sub>T</sub> = 2mA, V <sub>I</sub> = GND to V <sub>CC</sub> , V <sub>INH</sub> = V <sub>IL</sub>	25°C	1.65V		3	40	Ω			
Δr <sub>ON</sub>	Difference in ON-state resistance between switches	I <sub>T</sub> = 2mA, V <sub>I</sub> = GND to V <sub>CC</sub> , V <sub>INH</sub> = V <sub>IL</sub>	- 40°C to 85°C	1.65V			50	Ω			
Δr <sub>ON</sub>	Difference in ON-state resistance between switches	I <sub>T</sub> = 2mA, V <sub>I</sub> = GND to V <sub>CC</sub> , V <sub>INH</sub> = V <sub>IL</sub>	- 40°C to 85°C	1.65V			50	Ω			
Δr <sub>ON</sub>	Difference in ON-state resistance between switches	I <sub>T</sub> = 2mA, V <sub>I</sub> = GND to V <sub>CC</sub> , V <sub>INH</sub> = V <sub>IL</sub>	25°C	2.3V		2.1	30	Ω			
			- 40°C to 85°C			40					
			- 40°C to 125°C			40					
						25°C	3V		1.4	20	Ω
					- 40°C to 85°C			30			
					- 40°C to 125°C			30			
						25°C	4.5V		1.3	15	Ω
					- 40°C to 85°C			20			
					- 40°C to 125°C			20			
I <sub>IH</sub> I <sub>IL</sub>	Control input current	V <sub>I</sub> = 5.5V or GND	25°C	0 to 5.5V			0.1	μA			
			- 40°C to 85°C			1					
			- 40°C to 125°C			2					
I <sub>S(off)</sub>	OFF-state switch leakage current	V <sub>I</sub> = V <sub>CC</sub> and V <sub>O</sub> = GND, or V <sub>I</sub> = GND and V <sub>O</sub> = V <sub>CC</sub> , V <sub>INH</sub> = V <sub>IH</sub>	25°C	5.5V			0.1	μA			
			- 40°C to 85°C			1					
			- 40°C to 125°C			2					
I <sub>S(on)</sub>	ON-state switch leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>INH</sub> = V <sub>IL</sub> (see Figure 6-3)	25°C	5.5V			0.1	μA			
			- 40°C to 85°C			1					
			- 40°C to 125°C			2					
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND V <sub>INH</sub> = 0V	25°C	5.5V		0.01	μA				
			- 40°C to 85°C			20					
			- 40°C to 125°C			40					

## 5.5 Electrical Characteristics (续)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T <sub>A</sub>	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
C <sub>IC</sub>	Control input capacitance	f = 10MHz	25°C	3.3V		2		pF
C <sub>OS</sub>	Switch terminal capacitance	f = 10MHz	25°C	3.3V		5		pF
C <sub>IS</sub>	Common terminal capacitance	f = 10MHz	25°C	3.3V		23		pF
C <sub>OS(on)</sub>	Common terminal ON-capacitance	f = 10MHz	25°C	3.3V		23		pF
C <sub>F</sub>	Feedthrough capacitance	f = 10MHz	25°C	3.3V		0.5		pF
C <sub>PD</sub>	Power dissipation capacitance	C <sub>L</sub> = 50pF, f = 10MHz	25°C	3.3V		6		pF

## 5.6 Timing Characteristics V<sub>CC</sub> = 2.5V ± 0.2V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	COM or Yn	Yn or COM	C <sub>L</sub> = 15pF	25°C		1.9	10	ns
					-40°C to 85°C			16	
					-40°C to 125°C			18	
t <sub>PZH</sub> t <sub>PZL</sub>	Enable delay time	INH	COM or Yn	C <sub>L</sub> = 15pF	25°C		6.6	18	ns
					-40°C to 85°C			23	
					-40°C to 125°C			25	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable delay time	INH	COM or Yn	C <sub>L</sub> = 15pF	25°C		7.4	18	ns
					-40°C to 85°C			23	
					-40°C to 125°C			25	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	COM or Yn	Yn or COM	C <sub>L</sub> = 50pF	25°C		3.8	12	ns
					-40°C to 85°C			18	
					-40°C to 125°C			20	
t <sub>PZH</sub> t <sub>PZL</sub>	Enable delay time	INH	COM or Yn	C <sub>L</sub> = 50pF	25°C		7.8	28	ns
					-40°C to 85°C			35	
					-40°C to 125°C			35	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable delay time	INH	COM or Yn	C <sub>L</sub> = 50pF	25°C		11.5	28	ns
					-40°C to 85°C			35	
					-40°C to 125°C			35	

## 5.7 Timing Characteristics V<sub>CC</sub> = 3.3V ± 0.3V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	COM or Yn	Yn or COM	C <sub>L</sub> = 15pF	25°C		1.2	6	ns
					-40°C to 85°C			10	
					-40°C to 125°C			12	
t <sub>PZH</sub> t <sub>PZL</sub>	Enable delay time	INH	COM or Yn	C <sub>L</sub> = 15pF	25°C		4.7	12	ns
					-40°C to 85°C			15	
					-40°C to 125°C			18	

### 5.7 Timing Characteristics $V_{CC} = 3.3V \pm 0.3V$ (续)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$t_{PHZ}$ $t_{PLZ}$	Disable delay time	INH	COM or Yn	$C_L = 15pF$	25°C		5.7	12	ns
					-40°C to 85°C			15	
					-40°C to 125°C			18	
$t_{PLH}$ $t_{PHL}$	Propagation delay time	COM or Yn	Yn or COM	$C_L = 50pF$	25°C		2.5	9	ns
					-40°C to 85°C			12	
					-40°C to 125°C			14	
$t_{PZH}$ $t_{PZL}$	Enable delay time	INH	COM or Yn	$C_L = 50pF$	25°C		5.5	20	ns
					-40°C to 85°C			25	
					-40°C to 125°C			25	
$t_{PHZ}$ $t_{PLZ}$	Disable delay time	INH	COM or Yn	$C_L = 50pF$	25°C		8.8	20	ns
					-40°C to 85°C			25	
					-40°C to 125°C			25	

### 5.8 Timing Characteristics $V_{CC} = 5V \pm 0.5V$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay time	COM or Yn	Yn or COM	$C_L = 15pF$	25°C		0.6	4	ns
					-40°C to 85°C			7	
					-40°C to 125°C			10	
$t_{PZH}$ $t_{PZL}$	Enable delay time	INH	COM or Yn	$C_L = 15pF$	25°C		3.5	8	ns
					-40°C to 85°C			10	
					-40°C to 125°C			12	
$t_{PHZ}$ $t_{PLZ}$	Disable delay time	INH	COM or Yn	$C_L = 15pF$	25°C		4.4	10	ns
					-40°C to 85°C			11	
					-40°C to 125°C			12	
$t_{PLH}$ $t_{PHL}$	Propagation delay time	COM or Yn	Yn or COM	$C_L = 50pF$	25°C		1.5	6	ns
					-40°C to 85°C			8	
					-40°C to 125°C			10	
$t_{PZH}$ $t_{PZL}$	Enable delay time	INH	COM or Yn	$C_L = 50pF$	25°C		4	14	ns
					-40°C to 85°C			18	
					-40°C to 125°C			18	
$t_{PHZ}$ $t_{PLZ}$	Disable delay time	INH	COM or Yn	$C_L = 50pF$	25°C		6.2	14	ns
					-40°C to 85°C			18	
					-40°C to 125°C			18	

### 5.9 AC Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	SN74LV4052	$C_L = 50pF$ , $R_L = 600\Omega$ , $F_{in} = 1MHz$ (sine wave) see Figure 6-6) (1)	$V_{CC} = 2.3V$		30	MHz
					$V_{CC} = 3V$		35	
					$V_{CC} = 4.5V$		50	



### 5.9 AC Characteristics (续)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS	MIN	TYP	MAX	UNIT
Charge Injection (control input to signal output)	INH	COM or Yn		C <sub>L</sub> = 50pF, R <sub>L</sub> = 600 Ω, F <sub>in</sub> = 1MHz (sine wave) (see Figure 6-8)	V <sub>CC</sub> = 2.3V	20		mV
					V <sub>CC</sub> = 3V	35		
					V <sub>CC</sub> = 4.5V	60		
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM		C <sub>L</sub> = 50pF, R <sub>L</sub> = 600 Ω, F <sub>in</sub> = 1MHz (sine wave) (see Figure 6-9) (2)	V <sub>CC</sub> = 2.3V	-45		dB
					V <sub>CC</sub> = 3V	-45		
					V <sub>CC</sub> = 4.5V	-45		
Crosstalk (between any switches)	COM or Yn	Yn or COM		C <sub>L</sub> = 50pF, R <sub>L</sub> = 600 Ω, F <sub>in</sub> = 1MHz (sine wave) (see Figure 6-7) (2)	V <sub>CC</sub> = 2.3V	-45		dB
					V <sub>CC</sub> = 3V	-45		
					V <sub>CC</sub> = 4.5V	-45		
Sine-wave distortion	COM or Yn	Yn or COM		C <sub>L</sub> = 50pF, R <sub>L</sub> = 10k Ω, F <sub>in</sub> = 1kHz (sine wave) (see Figure 6-9)	V <sub>I</sub> = 2V <sub>p-p</sub> V <sub>CC</sub> = 2.3V	0.1		%
					V <sub>I</sub> = 2.5V <sub>p-p</sub> V <sub>CC</sub> = 3V	0.1		
					V <sub>I</sub> = 4V <sub>p-p</sub> V <sub>CC</sub> = 4.5V	0.1		

### 5.10 Typical Characteristics

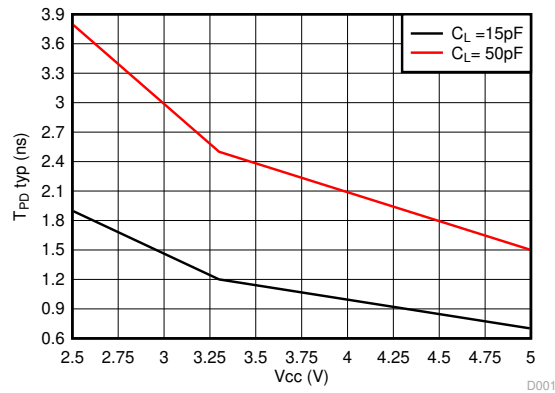


图 5-1. Typical Propagation Delay vs V<sub>CC</sub>

## 6 Parameter Measurement Information

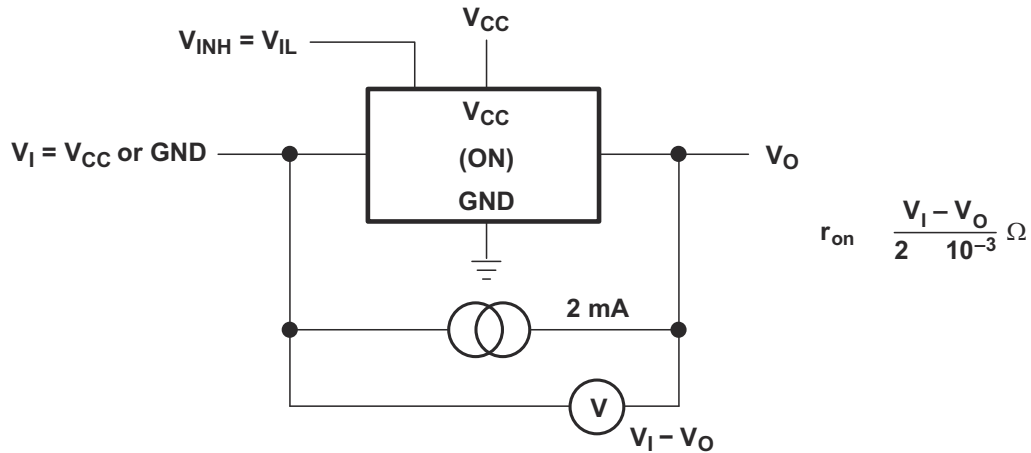


图 6-1. ON-State Resistance Test Circuit

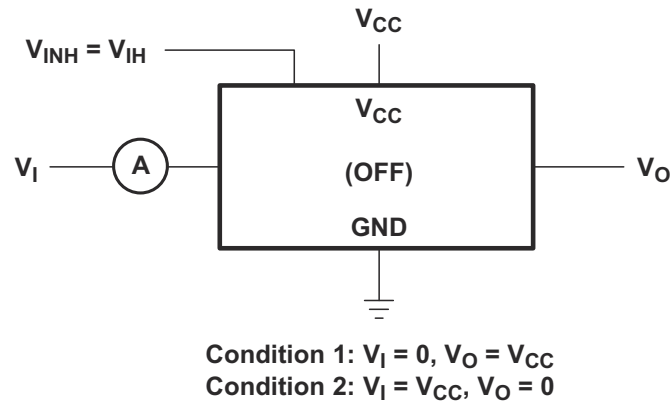


图 6-2. OFF-State Switch Leakage-Current Test Circuit

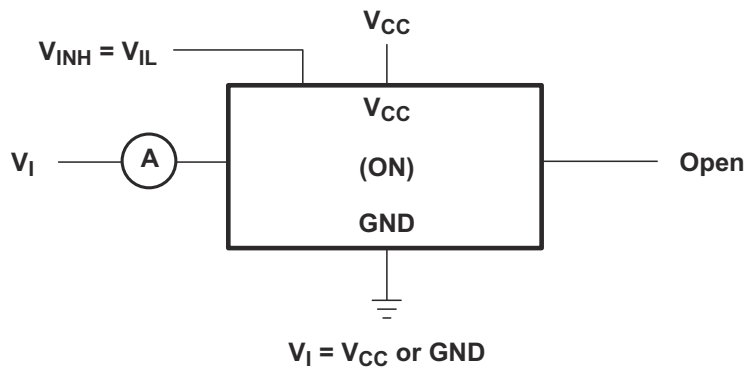


图 6-3. ON-State Switch Leakage-Current Test Circuit

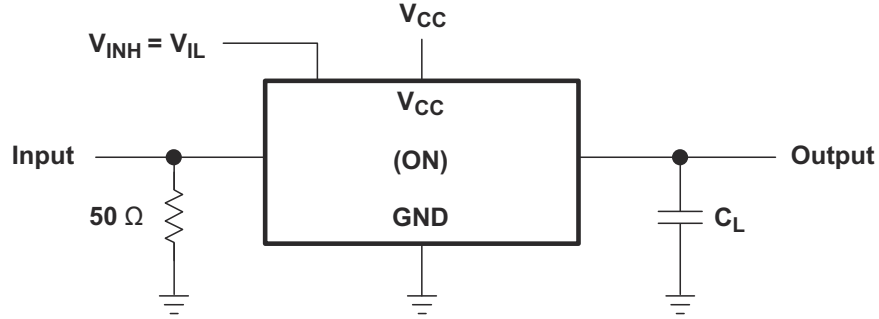


图 6-4. Propagation Delay Time, Signal Input to Signal Output

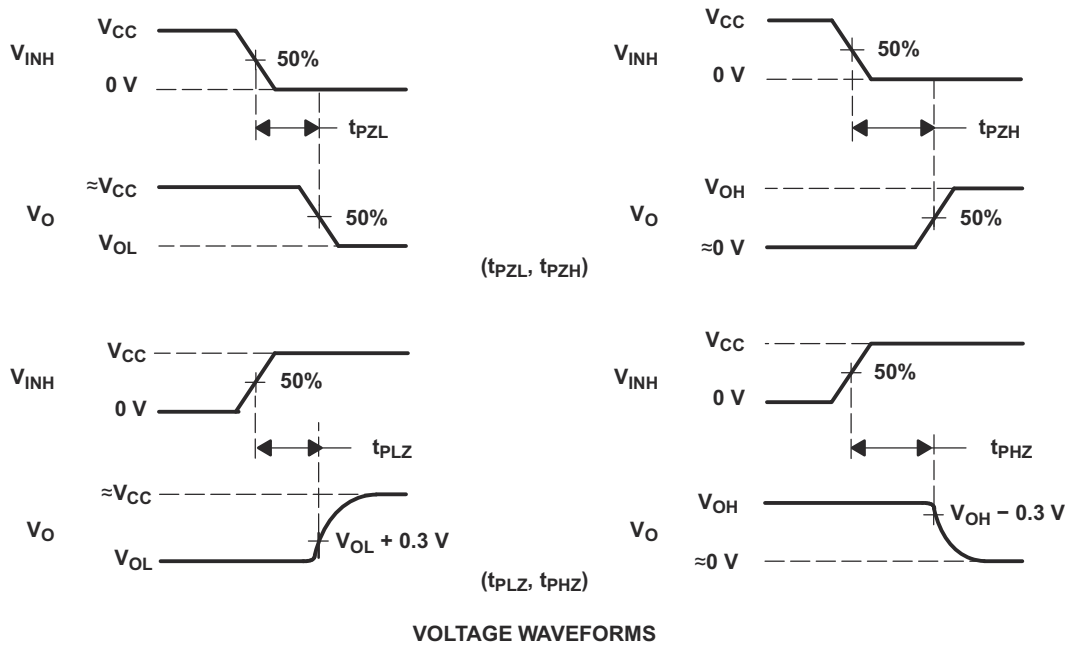
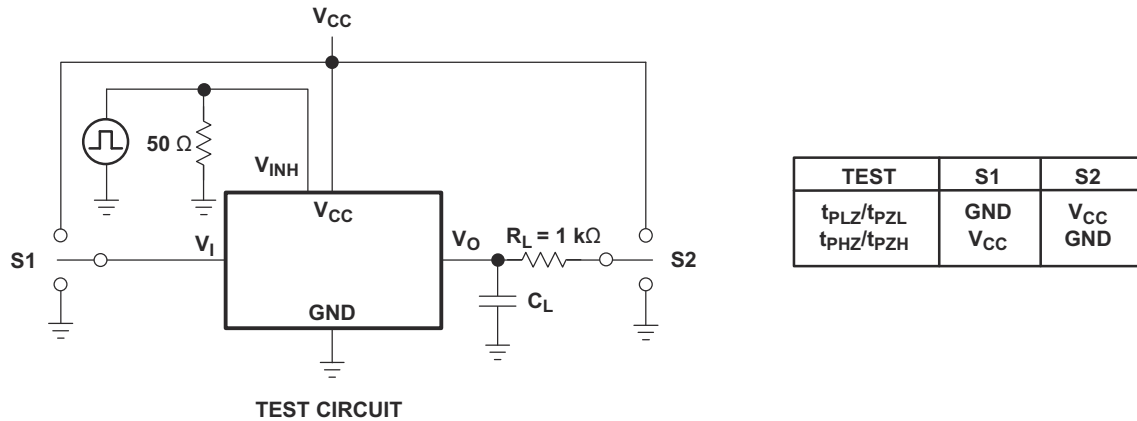
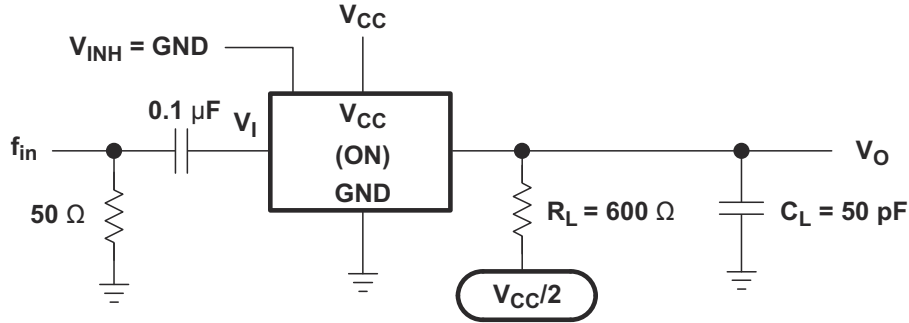


图 6-5. Switching Time ( $t_{PZL}$ ,  $t_{PLZ}$ ,  $t_{PHZ}$ ,  $t_{PHZ}$ ), Control to Signal Output



NOTE A:  $f_{in}$  is a sine wave.

图 6-6. Frequency Response (Switch ON)

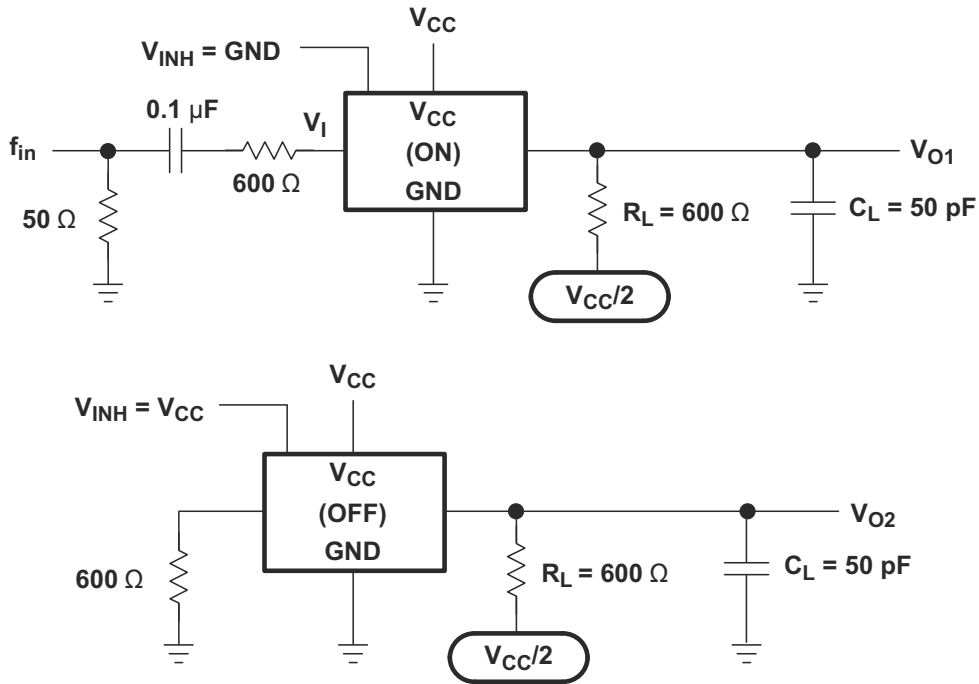


图 6-7. Crosstalk Between Any Two Switches

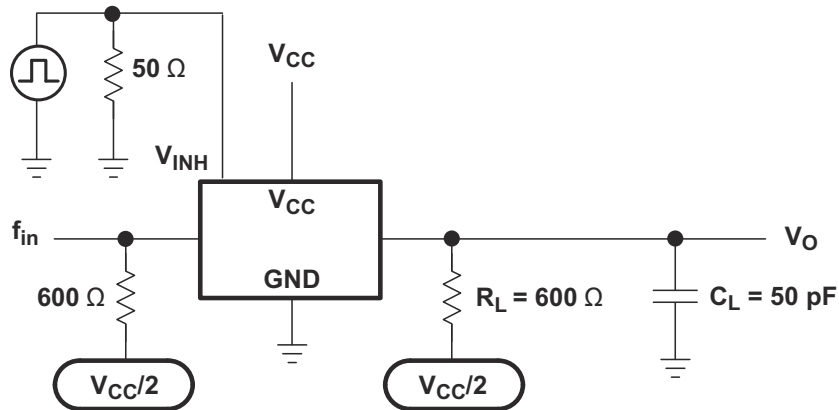


图 6-8. Crosstalk Between Control Input and Switch Output

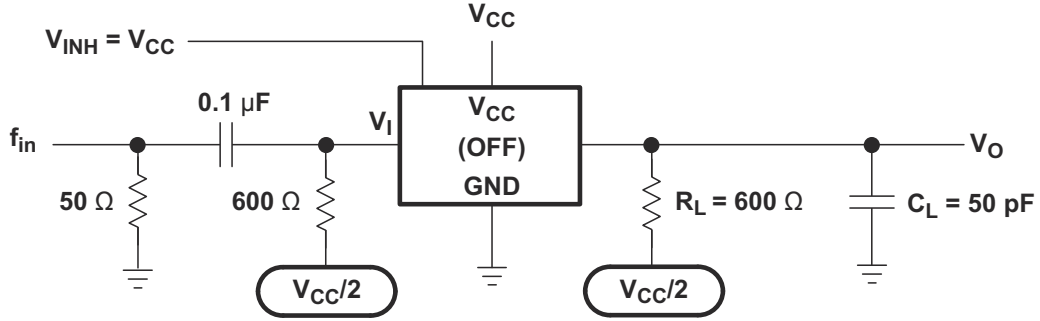


图 6-9. Feedthrough Attenuation (Switch OFF)

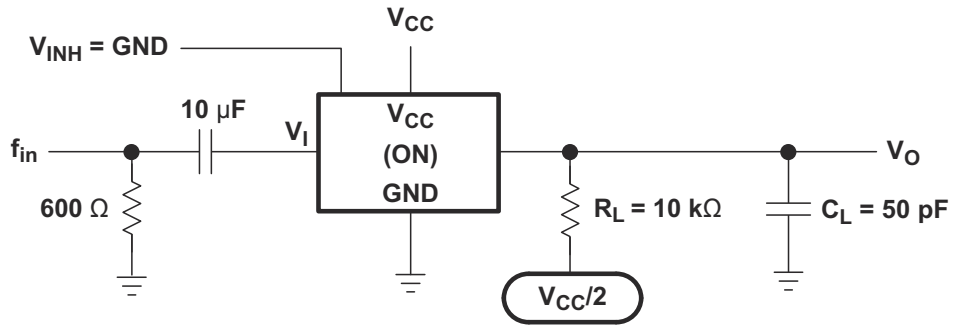


图 6-10. Sine-Wave Distortion

## 7 Detailed Description

### 7.1 Overview

The SNx4LV4052A device is a dual, 4-channel CMOS analog multiplexer and demultiplexer that is designed for 2V to 5.5V  $V_{CC}$  operation. It has low input current consumption at the digital input pins and low crosstalk between switches. The active low Inhibit (INH) tri-state all the channels when high and when low, depending on the A and B inputs, one of the four independent input/outputs (nY0 - nY3) connects to the COM channel. The SNx4LV4052A is available in multiple package options including TSSOP (PW) and QFN (RGY).

### 7.2 Functional Block Diagram

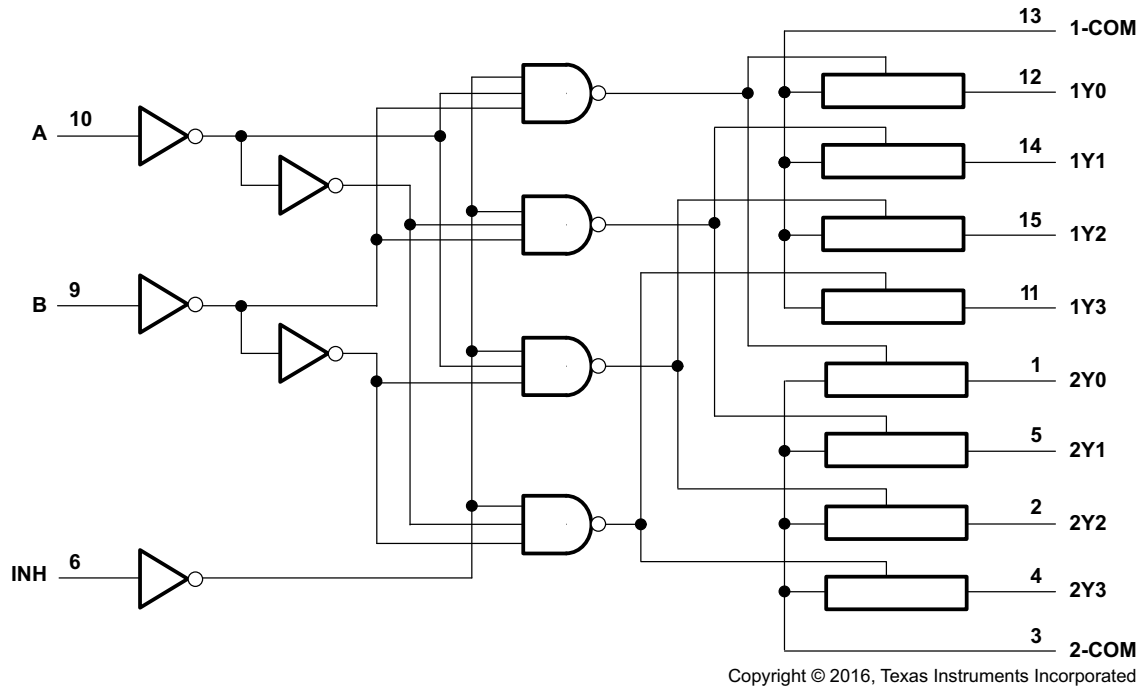


图 7-1. Logic Diagram (Positive Logic)

### 7.3 Feature Description

- The SNx4LV4052A operates from 2V to 5.5V  $V_{CC}$  with extremely low input current consumption at the CMOS input pins of A, B and INH.
- The SNx4LV4052A enables fast switching with low crosstalk between the switches. 5.5V peak level bidirectional transmission allowed with the either analog or digital signals.

### 7.4 Device Functional Modes

表 7-1 lists the functional modes of SNx4LV4052A.

表 7-1. Function Table

INPUTS			ON CHANNELS
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

## 8 Application and Implementation

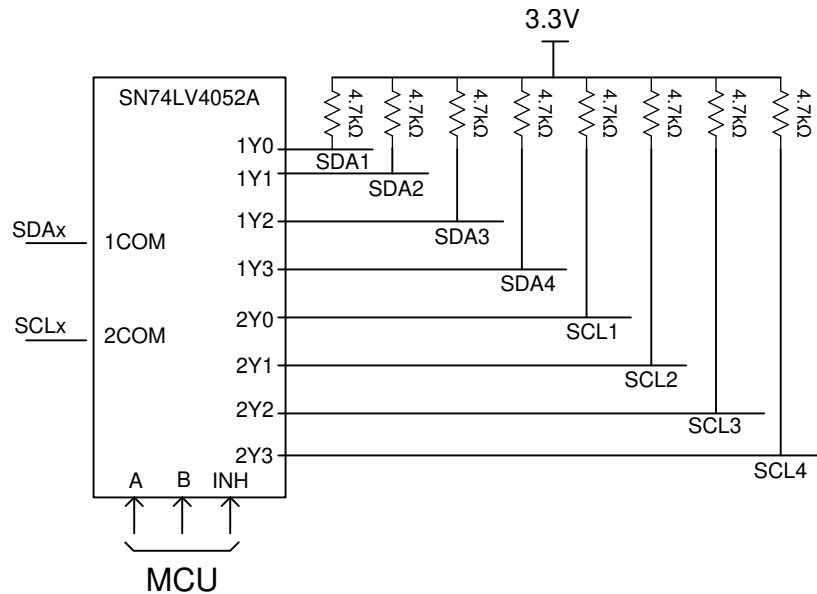
### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

Typical applications for the SNx4LV4052A include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

### 8.2 Typical Application



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图 8-1. Typical I<sup>2</sup>C Multiplexing Application

#### 8.2.1 Design Requirements

Designing with the SNx4LV4052A device requires a stable input voltage between 2V and 5.5V (see *Recommended Operating Conditions* for details). Another important design consideration are the characteristics of the signal being multiplexed—ensure no important information is lost due to timing or incompatibility with this device.

#### 8.2.2 Detailed Design Procedure

The SNx4LV4052A dual 1- to 4-channel multiplexer is an excellent choice for I<sup>2</sup>C selection. The I<sup>2</sup>C data and clock lines are selected using A,B select lines from the MCU. The pullup resistors are selected based on the capability of the driver. Low pullup resistor results in faster rise time; however, it generates additional current during the low state into the driver. See the *Recommended Operating Conditions* for the input transition rates ( $V_{IH}$  and  $V_{IL}$ ) of the CMOS inputs.

### 8.2.3 Application Curve

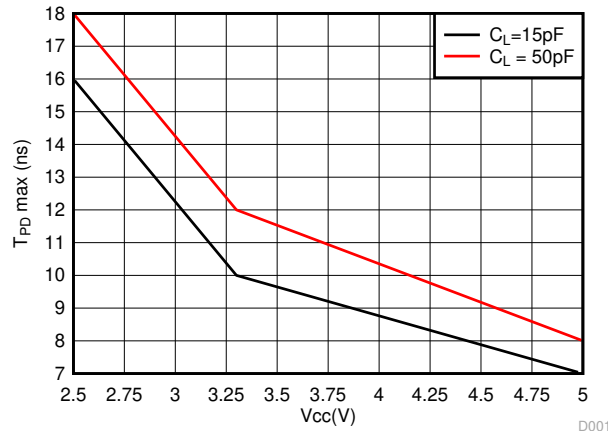


图 8-2. Maximum Propagation Delay vs V<sub>CC</sub>

### 8.3 Power Supply Recommendations

Most systems have a common 3.3V or 5V rail that can supply the V<sub>CC</sub> pin of this device. If this rail is not available, a switched-mode power supply (SMPS) or a low dropout regulator (LDO) can supply this device from a higher-voltage rail.

See the *Recommended Operating Conditions* for operating voltage range for this device. Having bypass capacitors of 0.1μF is highly recommended.

### 8.4 Layout

#### 8.4.1 Layout Guidelines

TI recommends keeping the signal lines as short and as straight as possible (see 图 8-3). Incorporation of microstrip or stripline techniques are also recommended when signal lines are more than 1 in. long. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω as required by the application.

Do not place this device too close to high-voltage switching components because they may cause interference. Not all PCB traces can be straight and therefore some traces must turn corners. 图 8-4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.



### 8.4.2 Layout Example

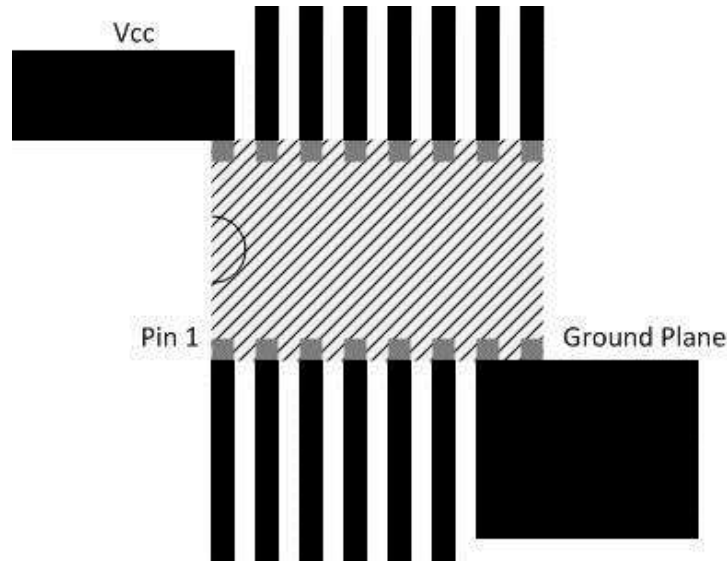


图 8-3. Layout Schematic

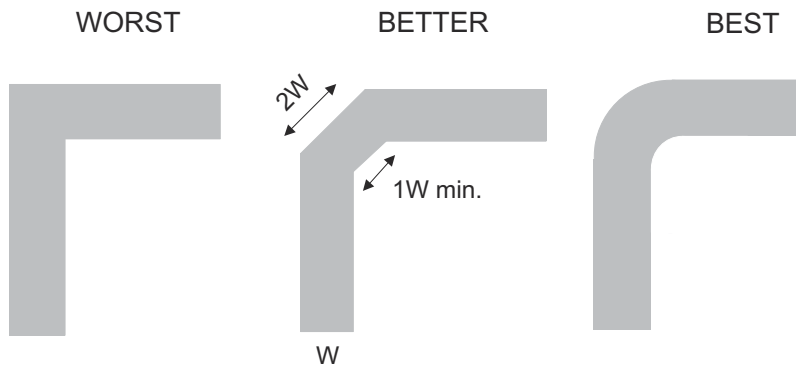


图 8-4. Trace Example

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

### 9.4 Trademarks

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### 9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision K (November 2016) to Revision L (June 2024)	Page
• 通篇更新了表格、图和交叉参考的编号格式.....	1
• Added new VIH and VIL Specifications at 1.65V Vcc.....	5
• Increased max ambient temperature max to 125C.....	5
• Added Ron, Ron Peak, and Delta Ron Specifications at 1.65V Vcc.....	5
• Added Ron, Ron Peak, and Delta Ron Specifications at 125C.....	5
• Added Timing Specifications at 125C.....	7

Changes from Revision J (October 2012) to Revision K (November 2016)	Page
• 添加了 ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• 删除了订购信息表，请参阅数据表末尾的封装选项附录.....	1
• 从数据表中删除了 SN54LV4052A.....	1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4052ADBR	NRND	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	
SN74LV4052ADBRE4	NRND	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	
SN74LV4052ADGVR	NRND	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	
SN74LV4052ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	LV4052A	Samples
SN74LV4052AN	NRND	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4052AN	
SN74LV4052ANSR	NRND	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4052A	
SN74LV4052APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052ARGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LW052A	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV4052A :**

- Automotive : [SN74LV4052A-Q1](#)
- Enhanced Product : [SN74LV4052A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

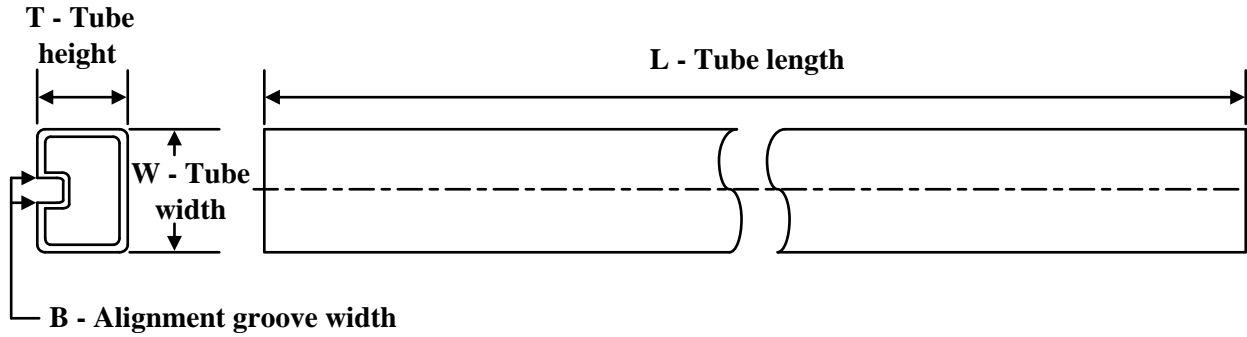

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4052ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV4052ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4052ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4052ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV4052APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4052ADBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74LV4052ADGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74LV4052ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LV4052ANSR	SO	NS	16	2000	356.0	356.0	35.0
SN74LV4052APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV4052APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV4052APWT	TSSOP	PW	16	250	356.0	356.0	35.0
SN74LV4052ARGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LV4052AD	D	SOIC	16	40	507	8	3940	4.32
SN74LV4052AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4052AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LV4052APW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LV4052APWE4	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LV4052APWG4	PW	TSSOP	16	90	530	10.2	3600	3.5



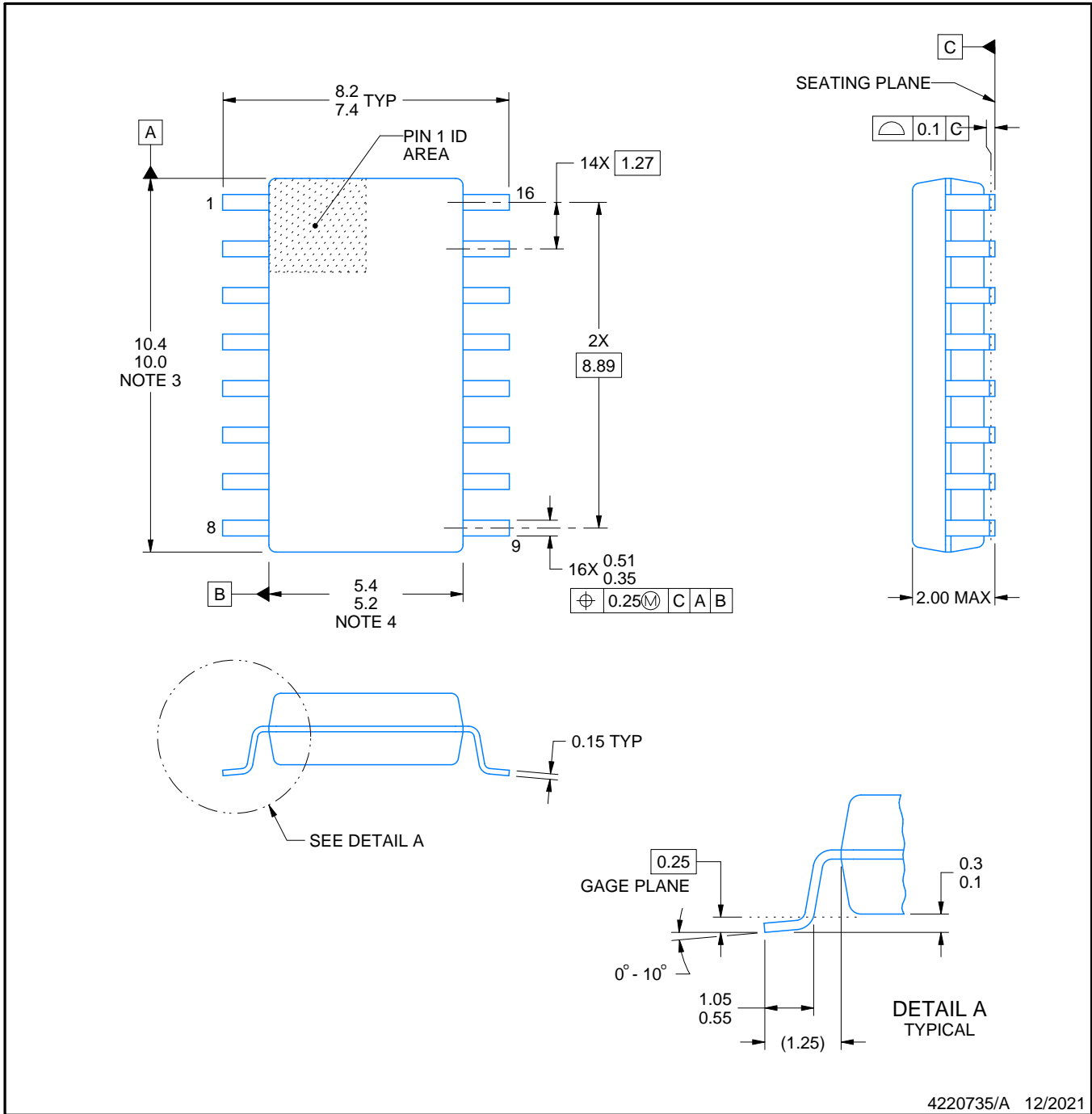


# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

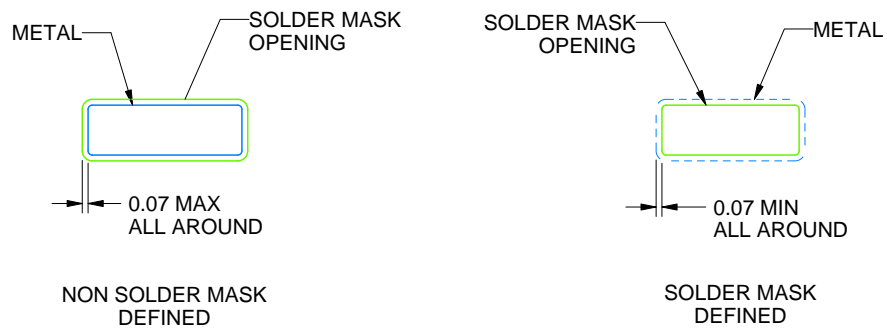
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

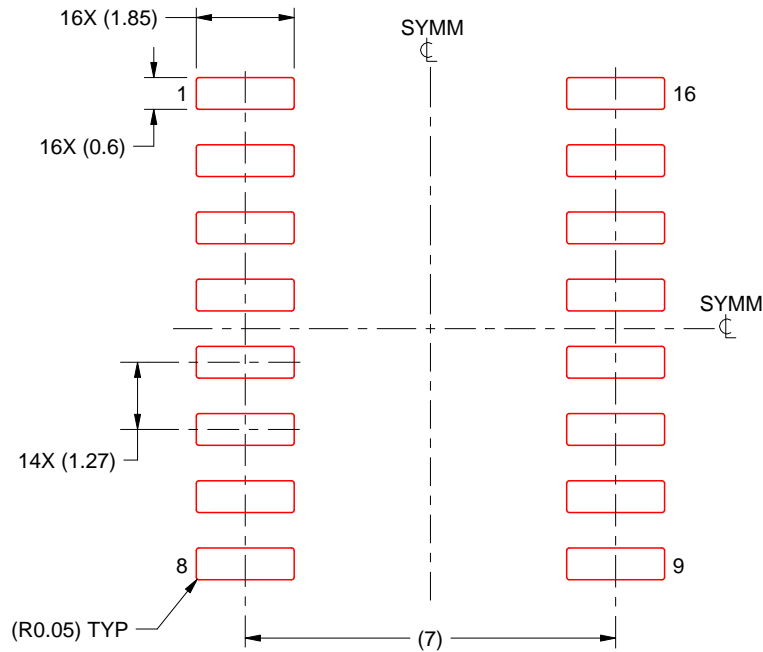
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



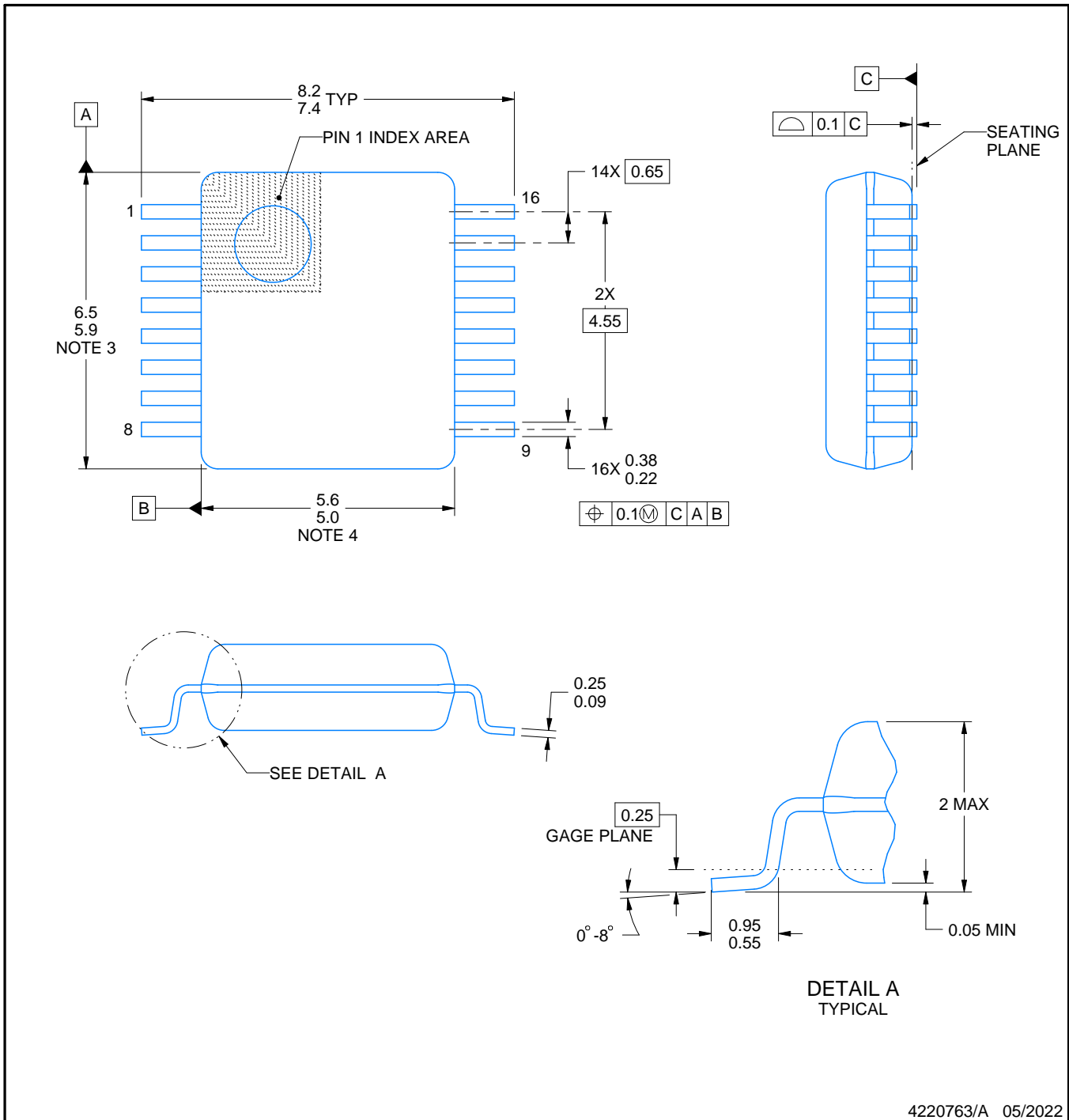
# DB0016A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

**NOTES:**

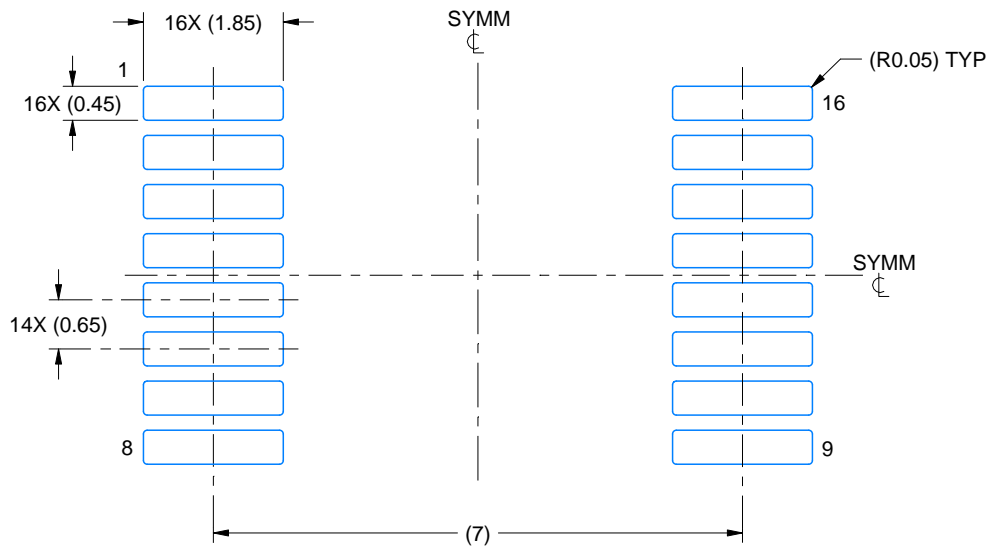
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

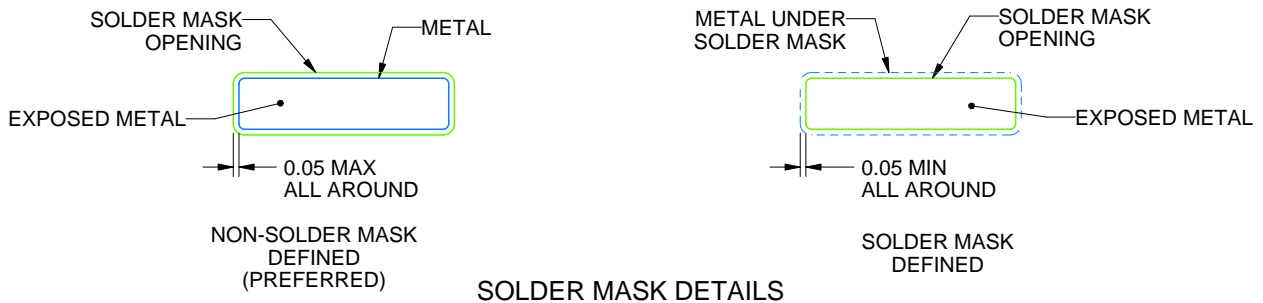
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

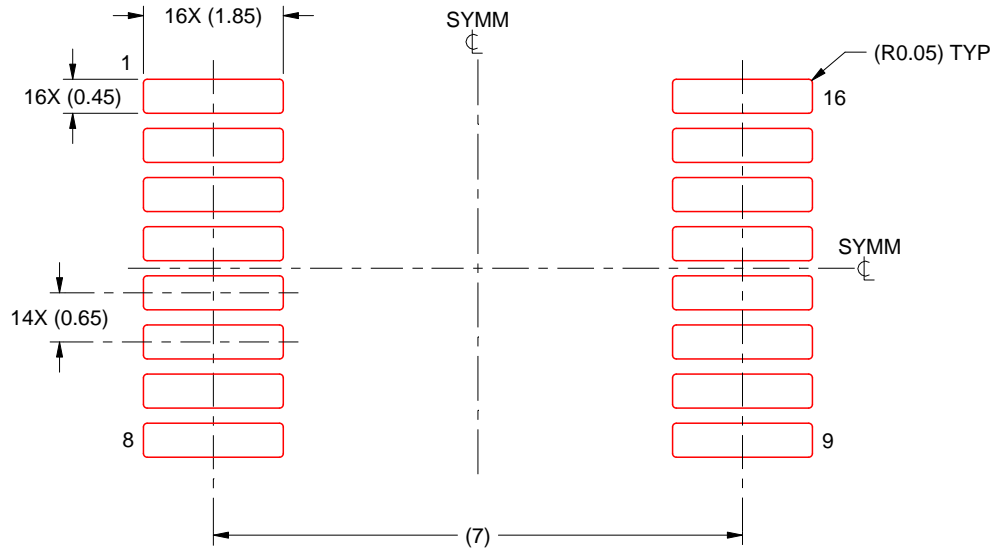
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

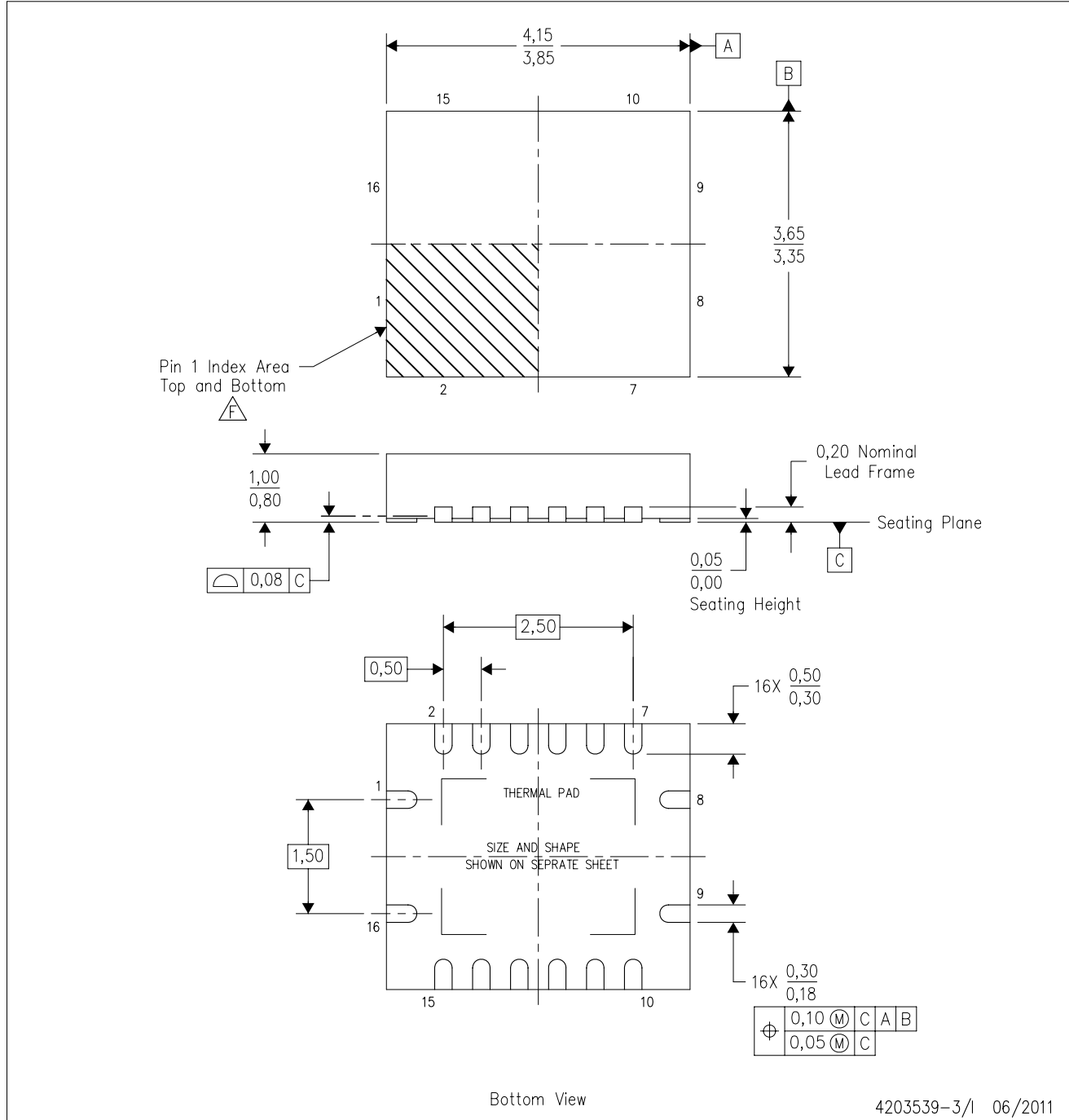
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/1 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

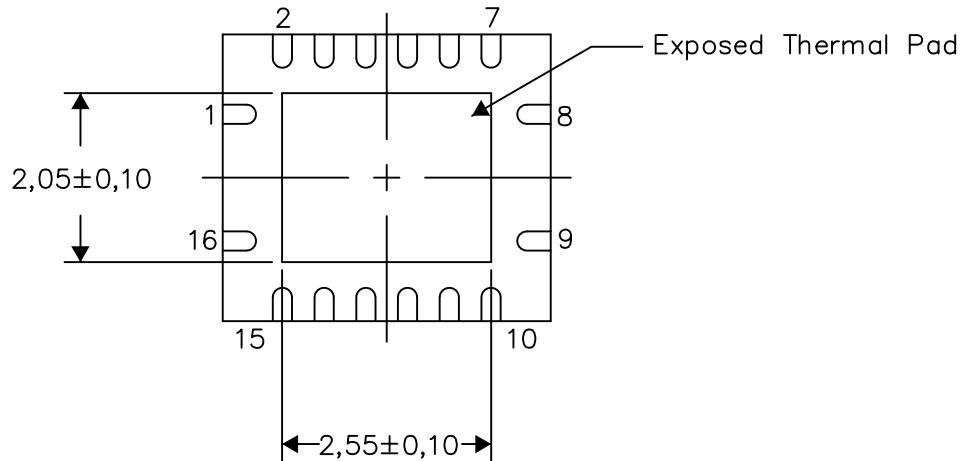
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

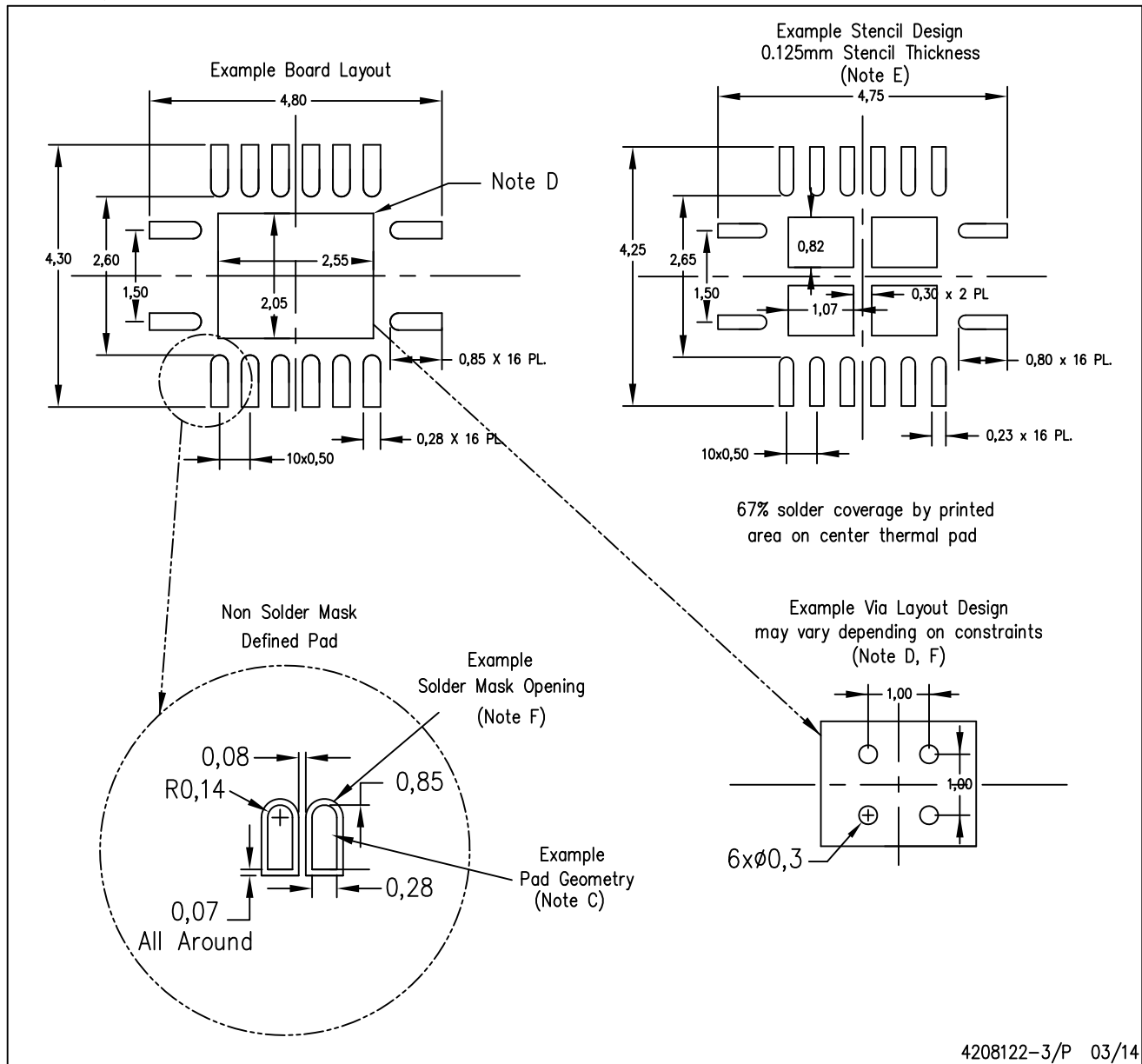
4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters



RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## 重要声明和免责声明

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