SN74LVC126A 具有三态输出的四路总线缓冲门

1 特性

- 可在 1.65V 至 3.6V 范围内工作
- 额定温度范围为 –40°C 至 +125°C
- 输入电压高达 5.5V
- 3.3V 时，t_{pd} 最大值为 4.7ns
- V_{OLP}（输出接地反弹）典型值 <0.8V（V_{CC} = 3.3V、T_A = 25°C）
- V_{OHV}（输出 V_{OH} 下冲）典型值 >2V（V_{CC} = 3.3V、T_A = 25°C）
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- AV 接收器
- 音频接口盒：便携
- 蓝光播放器和家庭影院
- MP3 播放器或录像机
- 个人数字助理 (PDA)
- 电源：电信电源、服务器电源和交流/直流电源（单控制器、模拟和数字）
- 固态硬盘 (SSD)：客户端和企业级
- 电视：LCD 电视、数字电视和高清电视 (HDTV)
- 平板电脑：企业级
- 视频分析：服务器
- 无线耳机、键盘和鼠标

3 说明

SN74LVC126A 器件是一款四通道总线缓冲门，旨在于 1.65V 至 3.6V V_{CC} 范围内运行。

SN74LVC126A 器件具有独立的线路驱动器，以及三态输出。当每个输出的相关输出使能 (OE) 输入为低电平时，输出被禁用。

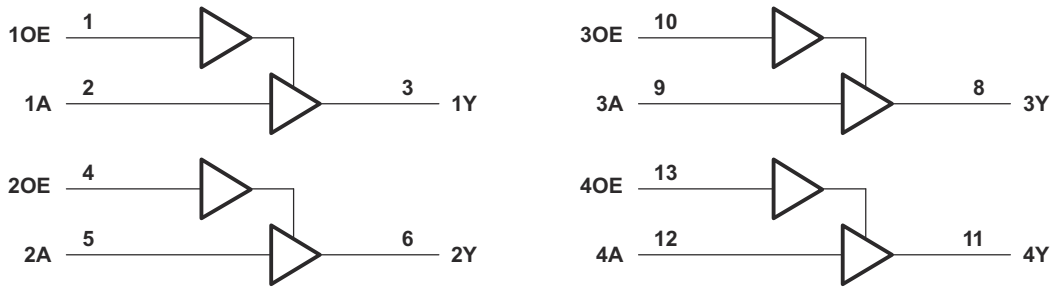
为了确保上电或下电期间的高阻抗状态，OE 必须通过一个下拉电阻器接至 GND；此电阻器的最小阻值由驱动器的拉电流能力决定。

输入可以由 3.3V 或 5V 器件驱动。此功能允许在 3.3V 和 5V 的混合系统环境中将该器件用作转换器。

封装信息

器件型号	封装 (1)	封装尺寸(2)	本体尺寸(3)
SN74LVC126A	BQA（WQFN，14）	3mm × 2.5mm	3mm × 2.5mm
	D（SOIC，14）	8.65mm x 6mm	8.65mm × 3.91mm
	DB（SSOP，14）	6.2mm x 7.8mm	6.20mm × 5.30mm
	DGV（TVSOP，14）	3.60mm × 6.4mm	3.60mm × 4.40mm
	NS（SOP，14）	10.2mm x 7.8mm	10.20mm × 5.30mm
	PW（TSSOP，14）	5mm x 6.4mm	5.00mm × 4.40mm
	RGY（VQFN，14）	3.50mm × 3.50mm	3.50mm × 3.50mm

(1) 如需了解更多信息，请参阅机械、封装和可订购信息。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。



简化版原理图

内容

4 引脚配置和功能

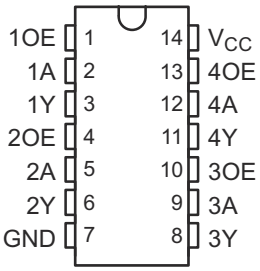


图 4-1. SN74LVC126A D、DB、DGV、NS 或 PW 封装；14 引脚 SOIC、SSOP、TVSOP、SOP 或 TSSOP（顶视图）

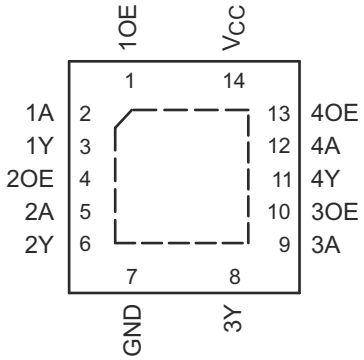


图 4-2. SN74LVC126A BQA 或 RGY 封装；14 引脚 WQFN 或 VQFN（顶视图）

表 4-1. 引脚功能

引脚		I/O[1]	说明
编号	名称		
1	1OE	I	输出使能 1
2	1A	I	栅极 1 输入
3	1Y	O	栅极 1 输出
4	2OE	I	输出使能 2
5	2A	I	栅极 2 输入
6	2Y	O	栅极 2 输出
7	GND	—	接地引脚
8	3Y	O	栅极 3 输出
9	3A	I	栅极 3 输入
10	3OE	I	输出使能 3
11	4Y	O	栅极 4 输出
12	4A	I	栅极 4 输入
13	4OE	I	输出使能 4
14	V_{CC}	—	电源引脚
散热焊盘		—	将 GND 引脚连接到裸露的散热焊盘以确保正确操作。使用多个过孔将散热焊盘连接到任何内部 PCB 接地平面，以获得良好的热性能。

(1) I = 输入、O = 输出、P = 电源、FB = 反馈、GND = 地、 N/A = 不适用

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压		-0.5	6.5	V
V_I (2)	输入电压		-0.5	6.5	V
V_O (2) (3)	输出电压		-0.5	V_{CC} + 0.5	V
I_{IK}	输入钳位电流	V_I < 0		-50	mA
I_{OK}	输出钳位电流	V_O < 0		-50	mA
I_O	持续输出电流			±50	mA
	通过 V_{CC} 或 GND 的持续电流			±100	mA
P_{tot}	功率耗散	T_A = -40°C 至 +125°C(4) (5)		500	mW
T_J	最大结温			150	°C
T_{stg}	贮存温度		-65	150	°C

(1) 应力超出*绝对最大额定值*下所列的值可能会对器件造成永久损坏。这些列出的值仅仅是应力等级，并不表示器件在这些条件下以及在*建议运行条件*以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，则可能会超过输入和输出负电压额定值。
(3) V_{CC} 的值在*建议运行条件*中提供。
(4) 对于 D 封装：在 70°C 以上时，P_{tot} 值以 8mW/K 的幅度线性降额。
(5) 对于 DB、NS 和 PW 封装：在 60°C 以上时，P_{tot} 值以 5.5mW/K 的幅度线性降额。

5.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准(1)	±2000	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101(2)	±1500	

(1) JEDEC 文档 JEP155 指出：500V HBM 能够在标准 ESD 控制流程下安全生产。该等级在 D (SOIC) 封装上进行了测试。
(2) JEDEC 文档 JEP157 指出：250V CDM 能够在标准 ESD 控制流程下安全生产。该等级在 D (SOIC) 封装上进行了测试。

5.3 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	标称值	最大值	单位
V_{CC}	电源电压	运行	1.65		3.6	V
		仅数据保留	1.5			
V_{IH}	高电平输入电压	V_{CC} = 1.65V 至 1.95V	0.65 × V_{CC}			V
		V_{CC} = 2.3V 至 2.7V	1.7			
		V_{CC} = 2.7V 至 3.6V	2			
V_{IL}	低电平输入电压	V_{CC} = 1.65V 至 1.95V			0.35 × V_{CC}	V
		V_{CC} = 2.3V 至 2.7V			0.7	
		V_{CC} = 2.7V 至 3.6V			0.8	
V_I	输入电压		0		5.5	V
V_O	输出电压		0		V_{CC}	V
I_{OH}	高电平输出电流	V_{CC} = 1.65V			-4	mA
		V_{CC} = 2.3V			-8	
		V_{CC} = 2.7V			-12	
		V_{CC} = 3V			-24	

5.3 建议运行条件（续）

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	标称值	最大值	单位
I_{OL}	低电平输出电流	V_{CC} = 1.65V			4	mA
		V_{CC} = 2.3V			8	
		V_{CC} = 2.7V			12	
		V_{CC} = 3V			24	
$\Delta t/\Delta v$	输入转换上升或下降速率				10	ns/V
T_A	自然通风条件下的工作温度范围		-40		125	°C

(1) 器件所有的未使用输入必须保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告 *CMOS 输入缓慢或悬空的影响* 。

5.4 热性能信息

热指标(1)		SN74LVC126A							单位
		BQA (WQFN)	D (SOIC)	DB (SSOP)	DGV (TVSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	
$R_{\theta JA}$	结至环境热阻	102.3(3)	127.8(2)	112.2(2)	140.9(2)	123.8(2)	150.8(2)	92.1(3)	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	96.8	81.9	64.2	59.9	51.7	78.3	91.8	°C/W
$R_{\theta JB}$	结至电路板热阻	70.9	84.4	59.6	70.2	52.7	93.8	66.7	°C/W
ψ_{JT}	结至顶部特征参数	16.6	39.6	28.3	9.1	20.7	38.2	20	°C/W
ψ_{JB}	结至电路板特征参数	70.9	83.9	59.1	69.5	52.3	93.2	66.5	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	50.1	不适用	不适用	不适用	不适用	不适用	50.1	°C/W

(1) 有关新旧热指标的更多信息，请参阅 *半导体和 IC 封装热指标* 应用报告。
(2) 封装热阻抗根据 JESD 51-7 计算。
(3) 封装热阻抗根据 JESD 51-5 计算。

5.5 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件			最小值	典型值	最大值	单位
V_{OH}	I_{OH} = –100μA，V_{CC} = 1.65V 至 3.6V		T_A = 25°C	V_{CC} – 0.2			V
			T_A = -40°C 至 +125°C	V_{CC} – 0.3			
	I_{OH} = –4 mA，V_{CC} = 1.65 V		T_A = 25°C	1.29			
			T_A = -40°C 至 +85°C	1.2			
			T_A = -40°C 至 +125°C	1.05			
	I_{OH} = –8mA，V_{CC} = 2.3V		T_A = 25°C	1.9			
			T_A = –40°C 至 +85°C	1.7			
			T_A = -40°C 至 +125°C	1.55			
	I_{OH} = -12mA	V_{CC} = 2.7V	T_A = 25°C	2.2			
			T_A = -40°C 至 +125°C	2.05			
		V_{CC} = 3V	T_A = 25°C	2.4			
			T_A = -40°C 至 +125°C	2.25			
	I_{OH} = –24 mA，V_{CC} = 3 V		T_A = 25°C	2.3			
			T_A = -40°C 至 +85°C	2.2			
			T_A = -40°C 至 +125°C	2			

5.5 电气特性（续）

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数		测试条件			最小值	典型值	最大值	单位
V_{OL}		I_{OL} = 100μA，V_{CC} = 1.65V 至 3.6V		T_A = 25°C			0.1	V
				T_A = -40°C 至 +85°C			0.2	
				T_A = -40°C 至 +125°C			0.3	
		I_{OL} = 4mA，V_{CC} = 1.65V		T_A = 25°C			0.24	
				T_A = -40°C 至 +85°C			0.45	
				T_A = -40°C 至 +125°C			0.6	
		I_{OL} = 8mA，V_{CC} = 2.3V		T_A = 25°C			0.3	
				T_A = -40°C 至 +85°C			0.7	
				T_A = -40°C 至 +125°C			0.75	
		I_{OL} = 12mA，V_{CC} = 2.7V		T_A = 25°C			0.4	
				T_A = -40°C 至 +125°C			0.6	
		I_{OL} = 24mA，V_{CC} = 3V		T_A = 25°C			0.55	
				T_A = -40°C 至 +125°C			0.8	
I_I		V_I = 5.5V 或 GND，V_{CC} = 3.6V		T_A = 25°C			±1	μA
				T_A = -40°C 至 +85°C			±5	
				T_A = -40°C 至 +125°C			±20	
I_{OZ}		V_O = V_{CC} 或 GND，V_{CC} = 3.6V		T_A = 25°C			±1	μA
				T_A = -40°C 至 +85°C			±10	
				T_A = -40°C 至 +125°C			±20	
I_{CC}		V_I = V_{CCI} 或 GND，I_O = 0，V_{CCI} = 3.6V		T_A = 25°C			1	μA
				T_A = -40°C 至 +85°C			10	
				T_A = -40°C 至 +125°C			40	
ΔI_{CC}		一个输入电压为 V_{CC} – 0.6V，另一个输入电压为 V_{CC} 或 GND，V_{CC} = 2.7V 至 3.6V		T_A = 25°C			500	μA
				T_A = -40°C 至 +125°C			5000	
C_i		V_I = V_{CC} 或 GND，V_{CC} = 3.3V				4.5		pF
C_o		V_O = V_{CC} 或 GND，V_{CC} = 3.3V				7		pF
C_{pd}	每个栅极的功率耗散电容	f = 10 MHz，T_A = 25°C	输出已启用	V_{CC} = 1.8V		20		pF
				V_{CC} = 2.5V		21		
				V_{CC} = 3.3V		22		
			输出已禁用	V_{CC} = 1.8V		2		
				V_{CC} = 2.5V		3		
				V_{CC} = 3.3V		4		

5.6 开关特性

在自然通风条件下的建议工作温度范围内测得（除非另有说明；请参阅 *参数测量信息*）

参数	测试条件			最小值	典型值	最大值	单位
t_{pd}	从 A（输入）到 Y（输出）	V_{CC} = 1.8V ± 0.15V	T_A = 25°C	1	4.2	9.3	ns
			T_A = -40°C 至 +85°C			9.8	
			T_A = -40°C 至 +125°C			11.3	
		V_{CC} = 2.5V ± 0.2V	T_A = 25°C	1	2.7	6.7	
			T_A = -40°C 至 +85°C			7.2	
			T_A = -40°C 至 +125°C			9.3	
		V_{CC} = 2.7V	T_A = 25°C	1	2.9	5	
			T_A = -40°C 至 +85°C			5.2	
			T_A = -40°C 至 +125°C			6.5	
		V_{CC} = 3.3V ± 0.3V	T_A = 25°C	1	2.5	4.5	
			T_A = -40°C 至 +85°C			4.7	
			T_A = -40°C 至 +125°C			6	
t_{en}	从 OE（输入）到 Y（输出）	V_{CC} = 1.8V ± 0.15V	T_A = 25°C	1	4.8	9.5	ns
			T_A = -40°C 至 +85°C			10	
			T_A = -40°C 至 +125°C			11.5	
		V_{CC} = 2.5V ± 0.2V	T_A = 25°C	1	2.8	7.8	
			T_A = -40°C 至 +85°C			8.3	
			T_A = -40°C 至 +125°C			10.4	
		V_{CC} = 2.7V	T_A = 25°C	1	3.1	6.1	
			T_A = -40°C 至 +85°C			6.3	
			T_A = -40°C 至 +125°C			8	
		V_{CC} = 3.3V ± 0.3V	T_A = 25°C	1	2.5	5.5	
			T_A = -40°C 至 +85°C			5.7	
			T_A = -40°C 至 +125°C			7.5	

5.6 开关特性（续）

在自然通风条件下的建议工作温度范围内测得（除非另有说明；请参阅 *参数测量信息*）

参数	测试条件			最小值	典型值	最大值	单位
t_{dis}	从 OE（输入）到 Y（输出）	V_{CC} = 1.8V ± 0.15V	T_A = 25°C	1	4.4	12.1	ns
			T_A = -40°C 至 +85°C			12.6	
			T_A = -40°C 至 +125°C			14.1	
		V_{CC} = 2.5V ± 0.2V	T_A = 25°C	1	2.7	8.2	
			T_A = -40°C 至 +85°C			8.7	
			T_A = -40°C 至 +125°C			10.8	
		V_{CC} = 2.7V	T_A = 25°C	1	2.7	6.5	
			T_A = -40°C 至 +85°C			6.7	
			T_A = -40°C 至 +125°C			8.5	
		V_{CC} = 3.3V ± 0.3V	T_A = 25°C	1.3	2.3	5.8	
			T_A = -40°C 至 +85°C			6	
			T_A = -40°C 至 +125°C			7.5	
$t_{sk(o)}$	V_{CC} = 3.3V ± 0.3V		T_A = -40°C 至 +85°C			1	ns
			T_A = -40°C 至 +125°C			1.5	

5.7 典型特性

T_A = 25°C

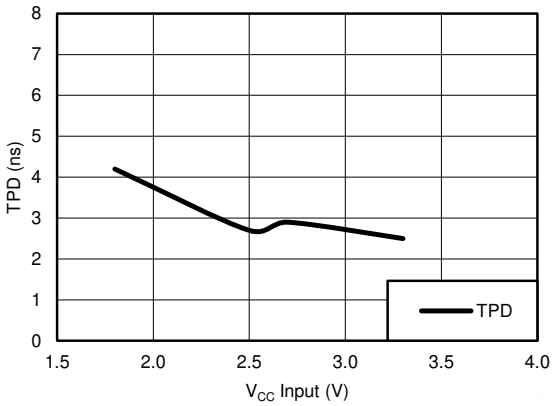


图 5-1. TPD 与 V_{CC} 之间的关系

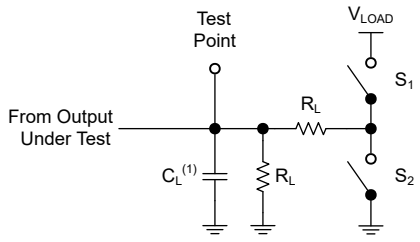
6 参数测量信息

对于下表中列出的示例，波形之间的相位关系是任意选择的。所有输入脉冲均由具有以下特性的发生器提供：PRR ≤ 1MHz，Z_O = 50Ω，t_t ≤ 2.5ns。

输出单独测量，每次测量一个输入转换。

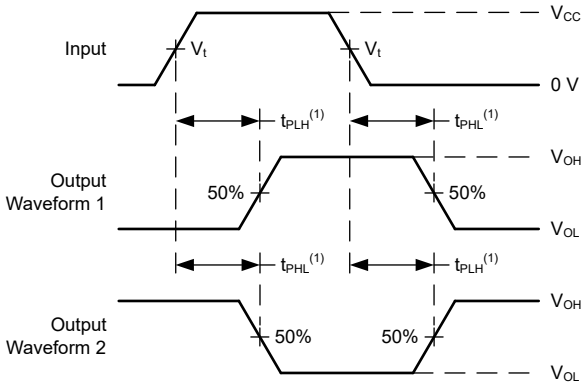
测试	S1	S2	R_L	C_L	Δ V	V_{LOAD}
t_{PLH}、t_{PHL}	断开	断开	500 Ω	50pF	—	—
t_{PLZ}、t_{PZL}	闭合	断开	500 Ω	50pF	0.3V	2×V_{CC}
t_{PHZ}，t_{PZH}	断开	闭合	500 Ω	50pF	0.3V	—

V_{CC}	V_t	R_L	C_L	Δ V	V_{LOAD}
1.8V ± 0.15V	V_{CC}/2	1k Ω	30pF	0.15V	2×V_{CC}
2.5V ± 0.2V	V_{CC}/2	500 Ω	30pF	0.15V	2×V_{CC}
2.7V	1.5V	500 Ω	50pF	0.3V	6V
3.3V ± 0.3V	1.5V	500 Ω	50pF	0.3V	6V



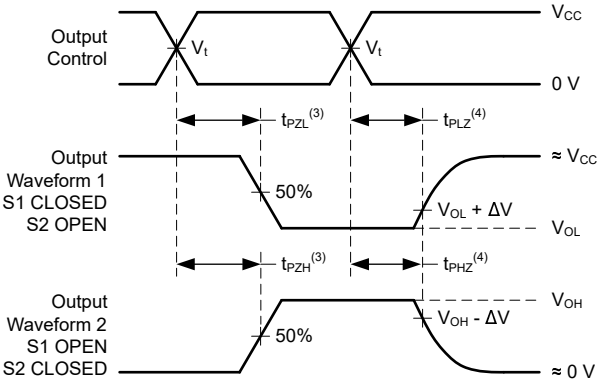
(1) C_L 包括探头和测试夹具电容。

图 6-1. 三态输出的负载电路



(1) t_{PLH} 和 t_{PHL} 之间的较大者与 t_{pd} 相同。

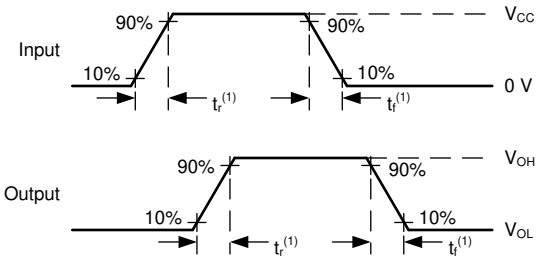
图 6-2. 电压波形传播延迟



(1) t_{PZL} 和 t_{PZH} 之间的较大者与 t_{en} 相同。

(2) t_{PLZ} 和 t_{PHZ} 之间的较大者与 t_{dis} 相同。

图 6-3. 电压波形传播延迟



(1) t_r 和 t_f 之间的较大值与 t_t 相同。

图 6-4. 电压波形，输入和输出转换时间

7 详细说明

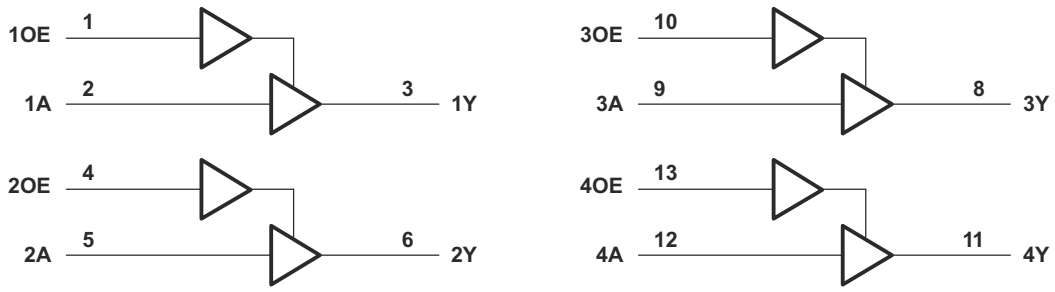
7.1 概述

SN74LVC126A 四通道缓冲器旨在于 1.65V 至 3.6V V_{CC} 范围内运行，并具有三态输出。

SN74LVC126A 器件以正逻辑执行布尔函数 Y = A。

输入可以由 3.3V 或 5V 器件驱动。此功能允许在 3.3V 或 5V 的混合系统环境中将这些器件用作降压转换器。

7.2 功能方框图



7.3 特性说明

SN74LVC126A 器件具有四个提供三态输出的独立缓冲器，旨在于 1.65V 至 3.6V 的 V_{CC} 范围内运行。当输出使能 (OE) 输入为低电平时，相应输出被禁用并进入高阻抗状态。该器件还具有高容差输入，允许在混合电压系统中进行电压转换。宽工作温度范围支持该器件用于任何应用，包括恶劣或极端环境。

7.4 器件功能模式

SN74LVC126A 的三态输出可通过输出使能 (OE) 引脚来禁用。为了确保在上电和下电期间处于高阻抗状态，OE 引脚必须通过下拉电阻器连接至 GND。该电阻的最小阻值取决于驱动器的拉电流能力。

表 7-1. 功能表
(每个缓冲器)

输入		输出
OE	A	Y
H	H	H
H	L	L
L	X	高阻态

8 应用和实施

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户应负责确定各元件是否适用于其应用。客户应验证并测试其设计是否能够实现，以确保系统功能。

8.1 应用信息

SN74LVC126A 器件是一款高驱动能力 CMOS 器件，可用于实现多种缓冲器类型的功能。该器件可以在 3V 下产生 24mA 驱动电流，因此非常适合驱动多个输入，也适合用于高达 100MHz 的高速应用。输入和输出可承受 5.5V 电压，因此该器件可转换至最高 5.5V 或最低 V_{CC} 电压。

8.2 典型应用

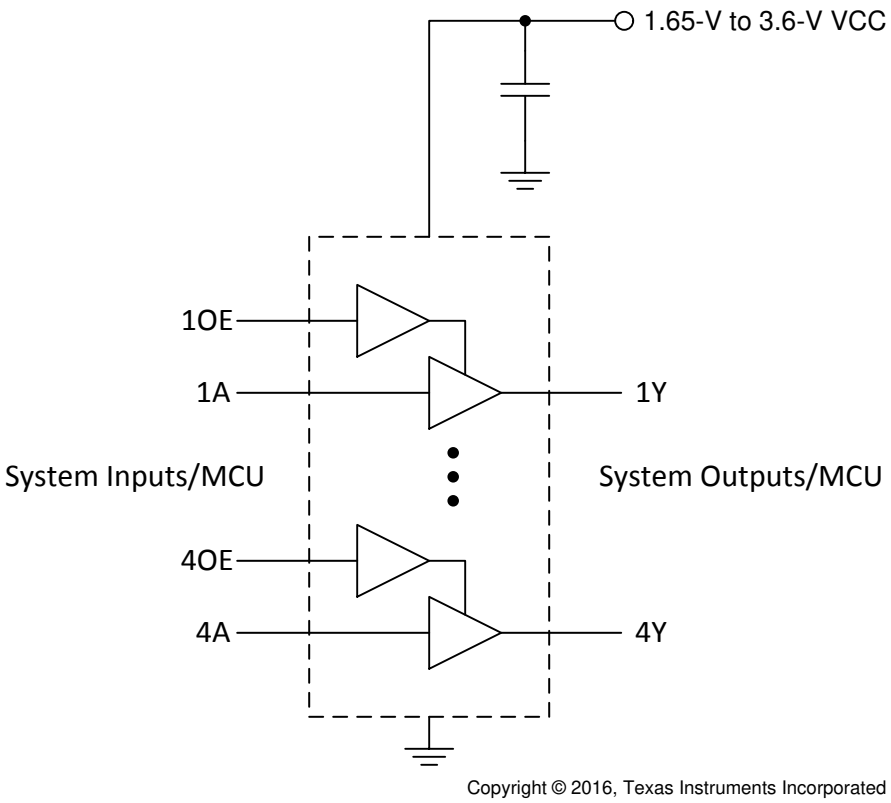


图 8-1. 典型缓冲器应用和电源电压

8.2.1 设计要求

此器件采用 CMOS 技术并具有平衡输出驱动。注意避免总线争用，因为它可以驱动超过最大限值的电流。高驱动也会在轻负载时产生快速边沿，因此应考虑布线和负载条件以防止振铃。

8.2.2 详细设计过程

1. 建议的输入条件
   - 上升时间和下降时间规格：请参阅 *建议运行条件* 中的 ($\Delta t/\Delta V$)。
   - 指定的高电平和低电平：请参阅 *建议工作条件* 中的 (V_{IH} 和 V_{IL})。
   - 输入具有过压容限，因此在任何有效 V_{CC} 下高达 5.5 V。
2. 建议的输出条件
   - 负载电流不得超过 25mA (每个输出) 和 50mA 总电流 (器件级)。
   - 输出不得拉至高于 5.5V。

8.2.3 应用曲线

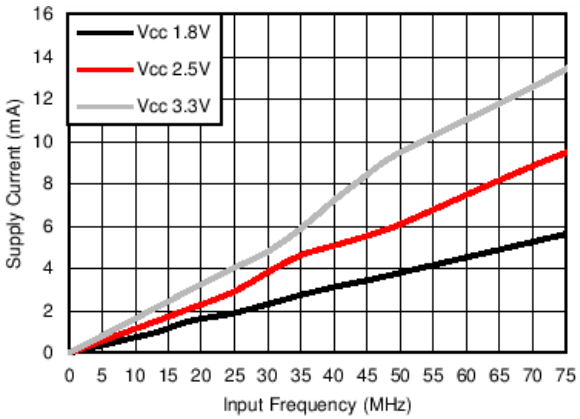


图 8-2. 电源电流与输入频率间的关系

8.3 电源相关建议

电源可以是 *建议运行条件* 中最小和最大电源电压额定值之间的任何电压。

每个 V_{CC} 引脚必须具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 0.1μF；如果有多个 V_{CC} 引脚，则建议每个电源引脚使用 0.01μF 或 0.022μF。可以并联多个旁路电容器以抑制不同的噪声频率。0.1μF 和 1μF 通常并联使用。为了获得更佳效果，旁路电容器必须尽可能靠近电源引脚安装。

8.4 布局

8.4.1 布局指南

当使用多位逻辑器件时，输入不得悬空。

在许多情况下，数字逻辑器件的功能或部分功能未被使用 (例如，当仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个时)。此类输入引脚不得悬空，因为外部连接处的未定义电压会导致未定义的运行状态。图 8-3 指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须连接至一个高或低偏置以防止悬空。必须应用于任何特定未使用输入的逻辑电平取决于器件的功能。通常，它们会连接到 GND 或 V_{CC}，具体取决于哪种更合理或更方便。使输出悬空通常是可以接受的，除非该器件是收发器。

8.4.2 布局示例

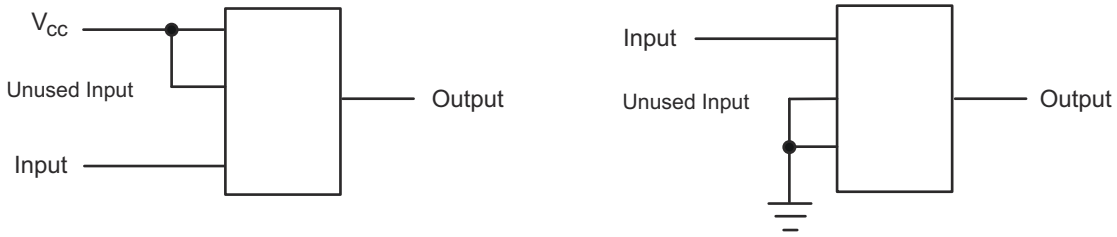


图 8-3. 布局图

9 器件和文档支持

9.1 文档支持

9.1.1 相关文档

请参阅以下相关文档：

TI 应用报告 *CMOS 输入缓慢或悬空的影响* (SCBA004)

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision T (May 2024) to Revision U (July 2024)	Page
• 更新了 R θ JA 值：D = 98.4 更新至 127.8，NS = 93.9 更新至 123.8，PW = 127.7 更新至 150.8，RGY = 35 更新至 92.1；更新了 D、NS、PW 和 RGY 封装的 R θ JC(top)、R θ JB、ΨJT、ΨJB 和 R θ JC(bot)，所有值均以 °C/W 为单位	5

Changes from Revision S (February 2017) to Revision T (May 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 向*封装信息* 表、*引脚配置和功能* 部分以及*热性能信息* 表中添加了 BQA 封装	1
• 向*封装信息* 表中添加了封装尺寸	1

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC126ABQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A	Samples
SN74LVC126AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126ADRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126ADT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A	Samples
SN74LVC126APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126APWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126APWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A	Samples
SN74LVC126ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC126A	Samples
SN74LVC126ARGYRG4	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC126A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LVC126A :

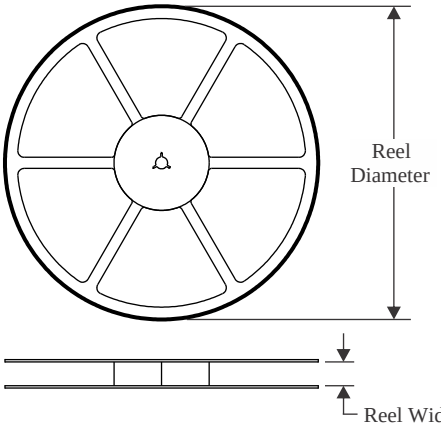
- Automotive : SN74LVC126A-Q1

NOTE: Qualified Version Definitions:

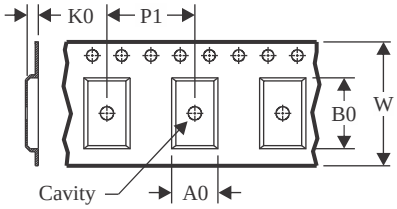
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

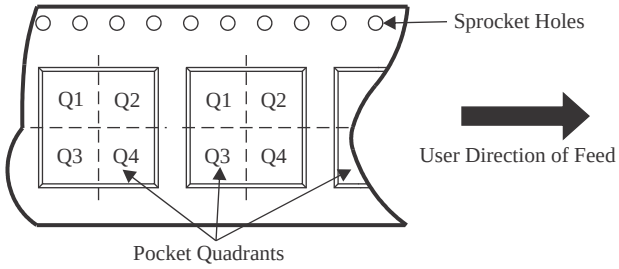


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

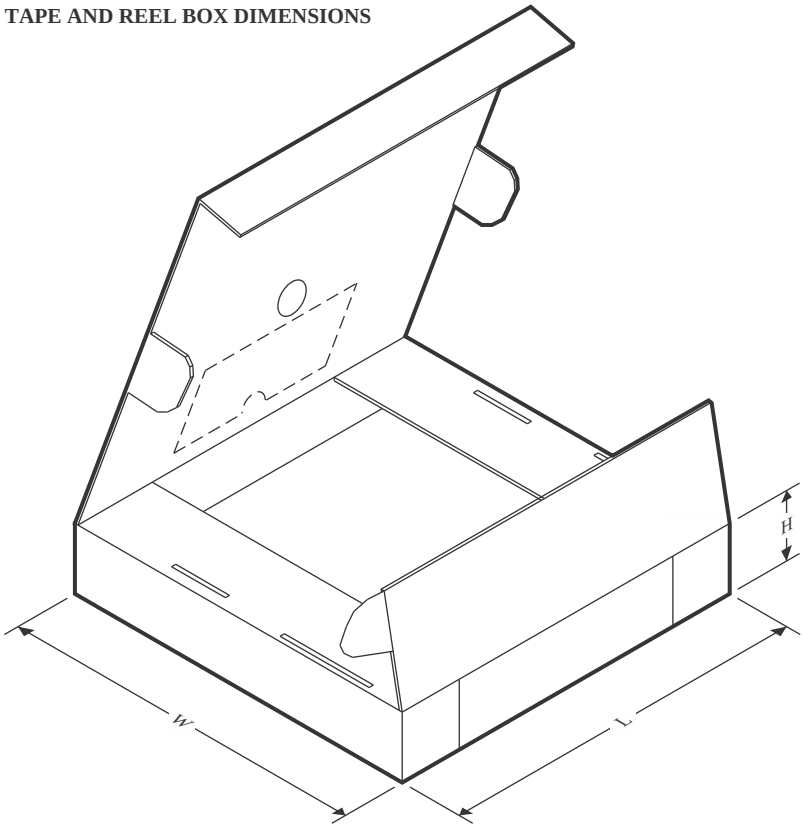
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC126ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC126ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC126ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC126ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC126ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC126ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC126APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC126APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC126ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

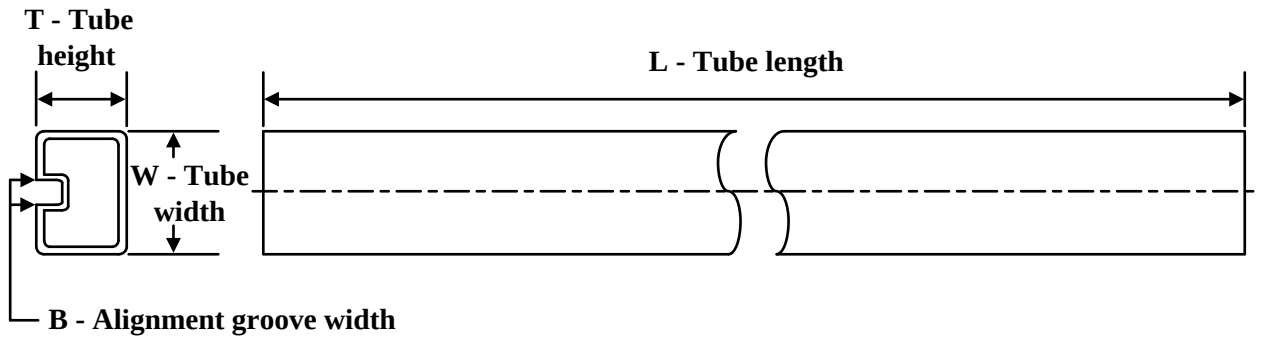
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

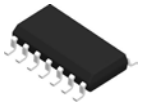
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC126ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC126ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LVC126ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LVC126ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LVC126ADT	SOIC	D	14	250	210.0	185.0	35.0
SN74LVC126ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LVC126APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC126APWT	TSSOP	PW	14	250	356.0	356.0	35.0
SN74LVC126ARGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVC126AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC126APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC126APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5

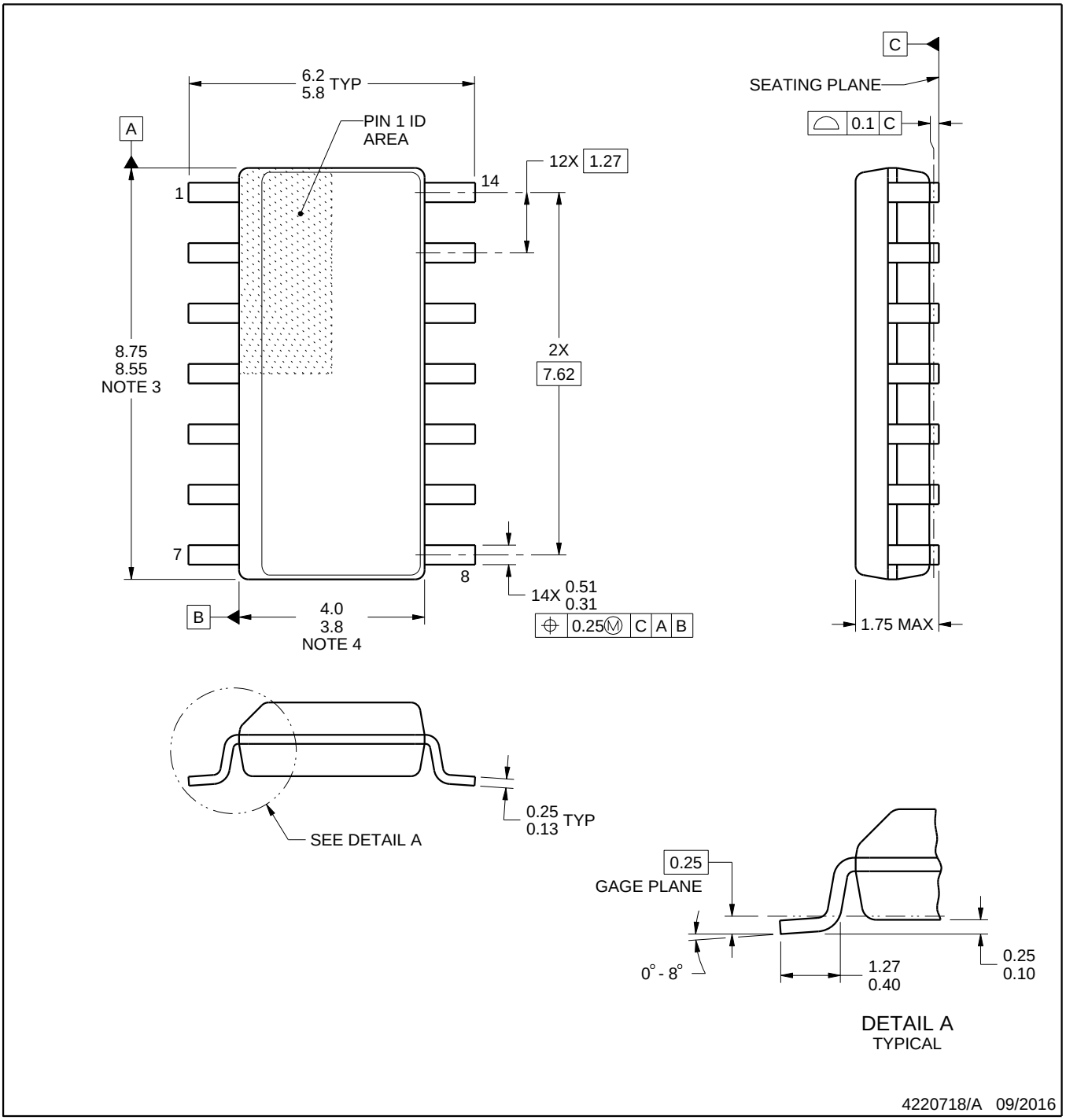


PACKAGE OUTLINE

D0014A

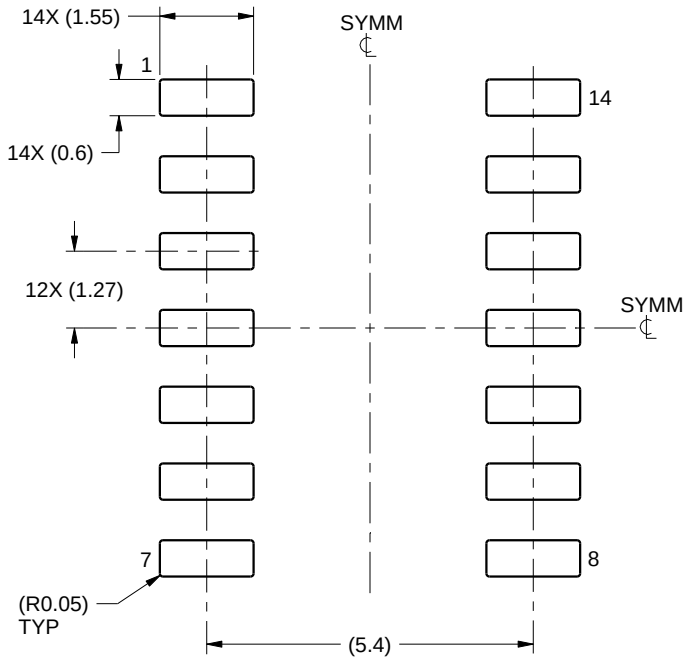
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

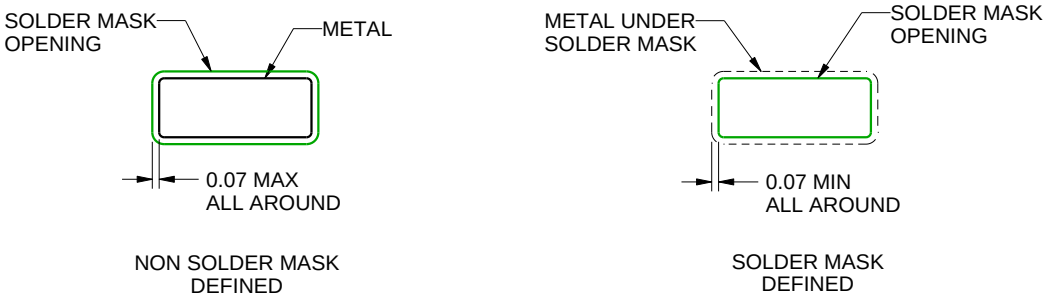


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

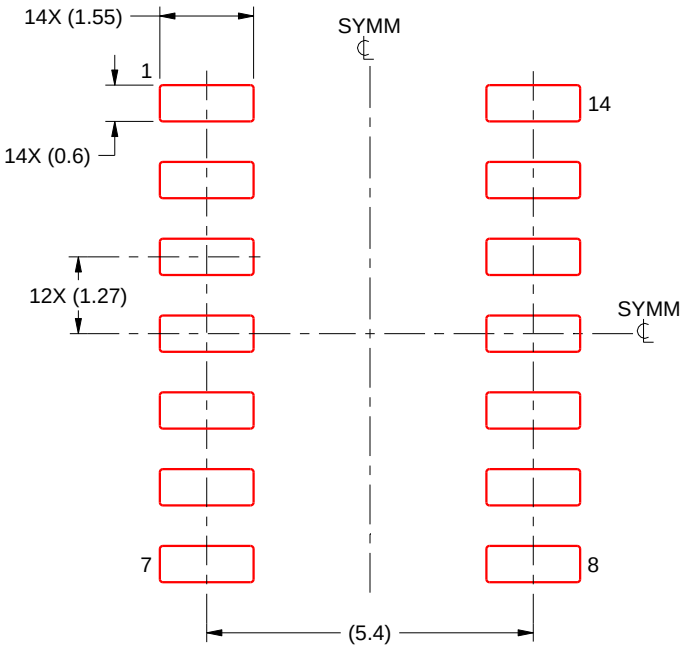
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



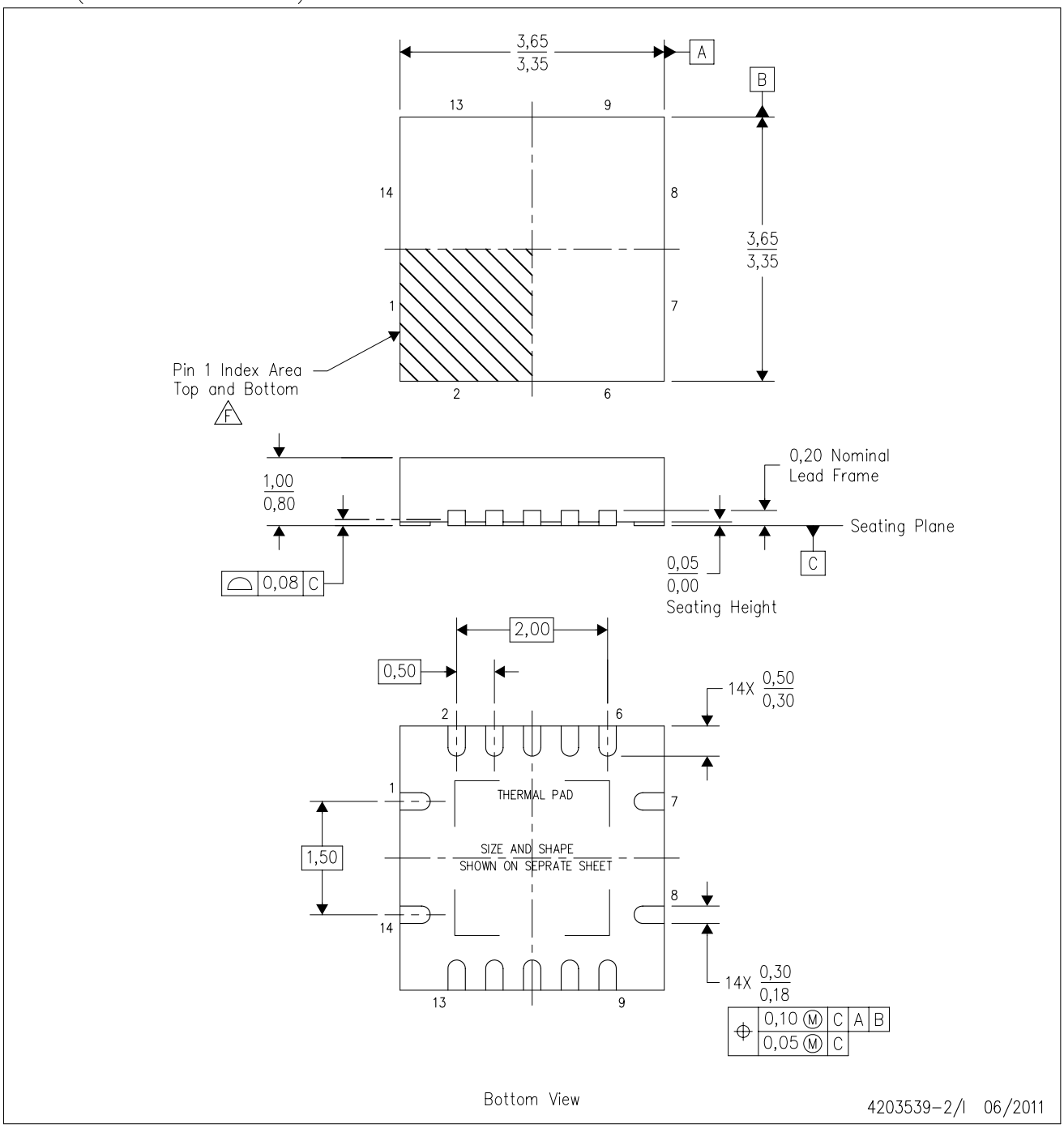
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

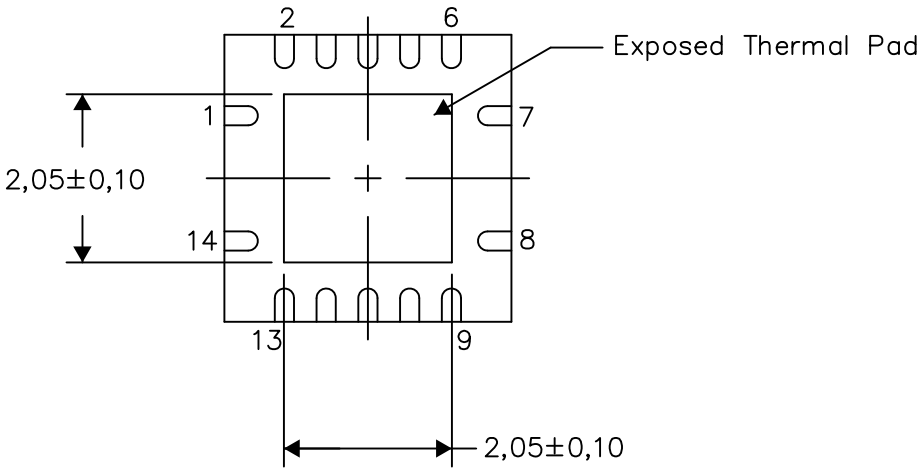
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



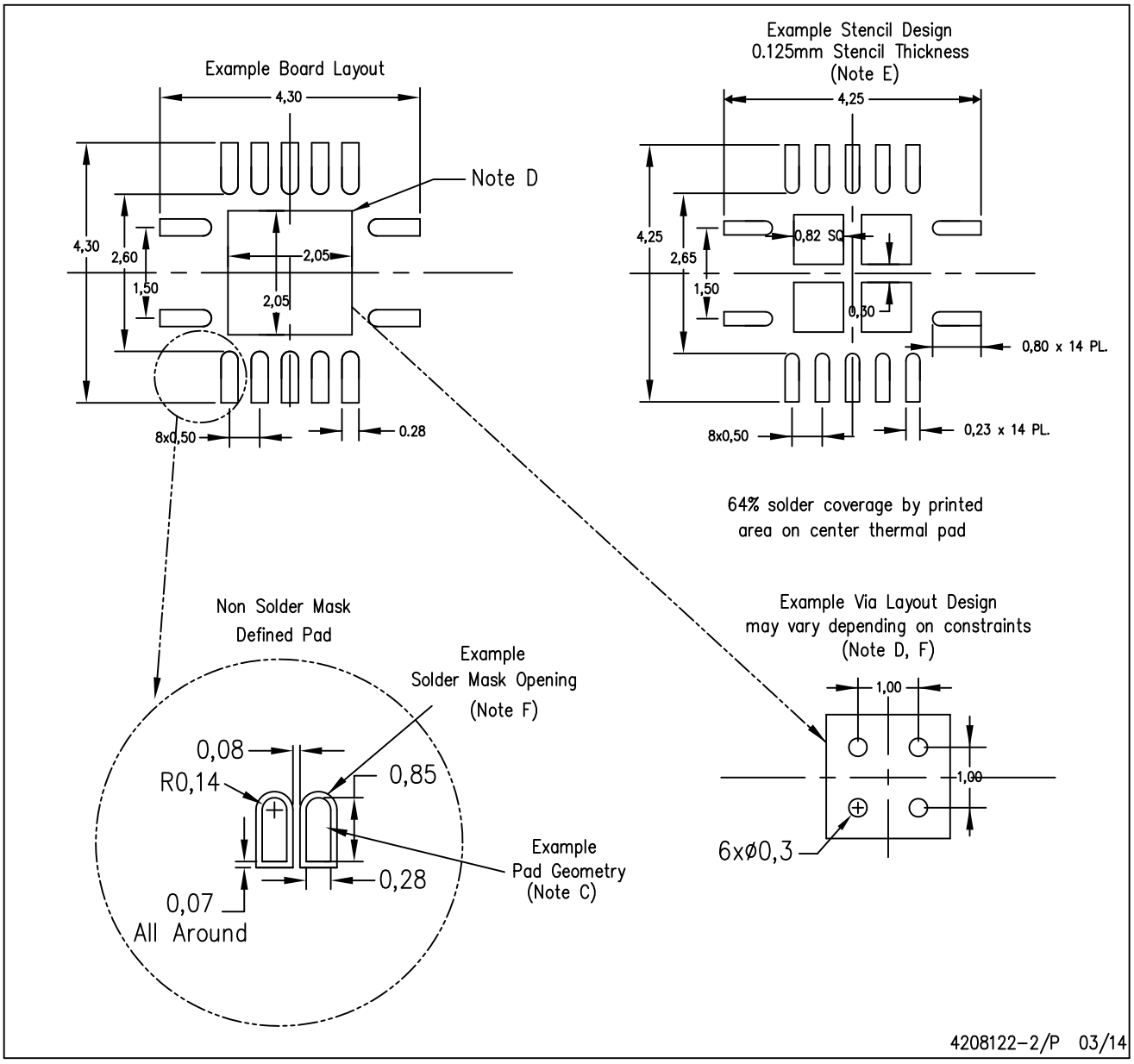
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

GENERIC PACKAGE VIEW

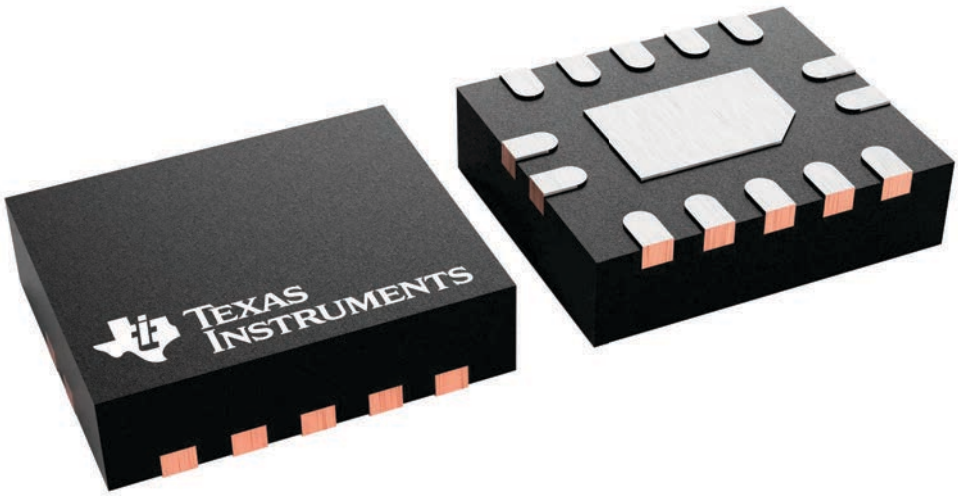
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

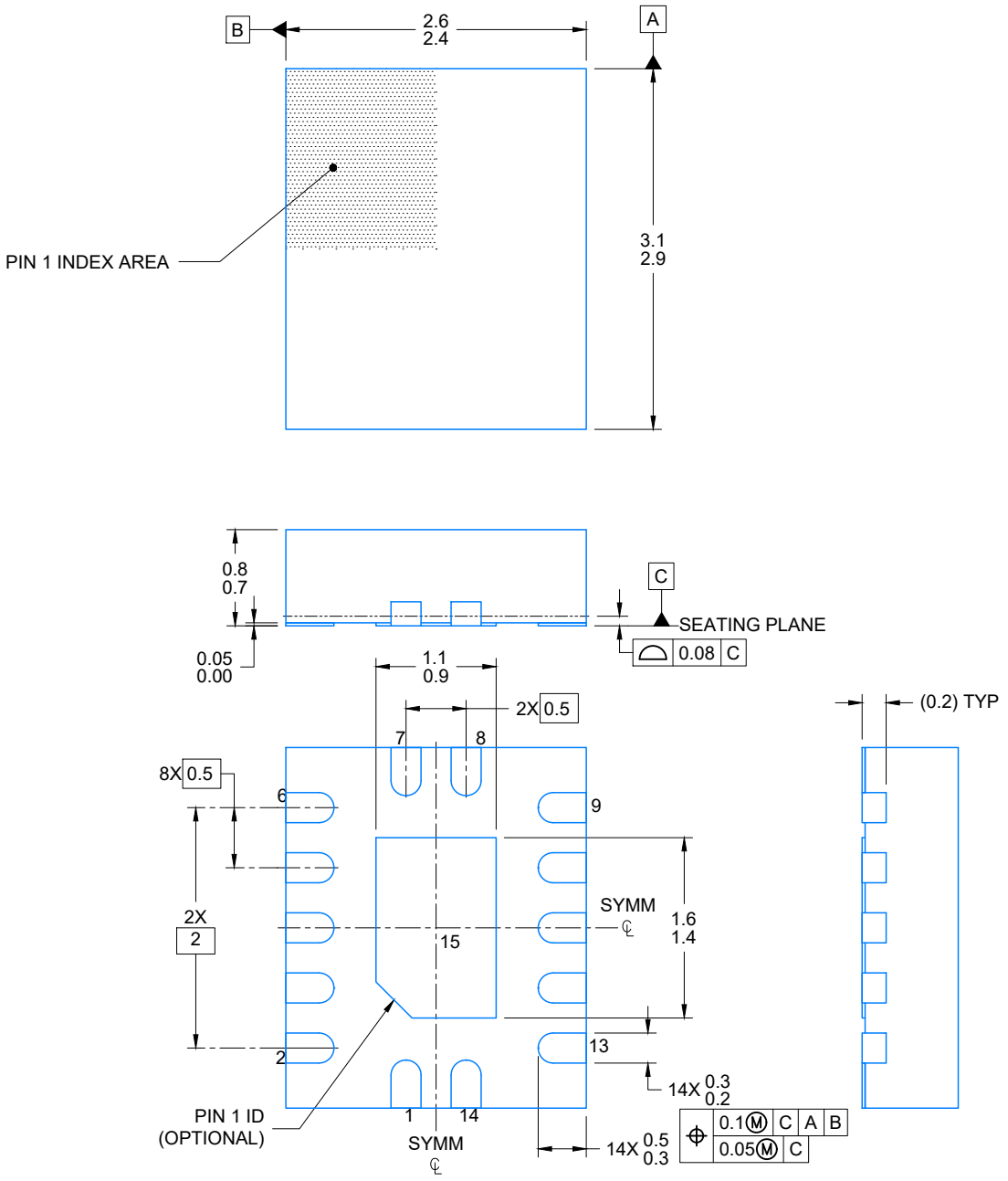


PACKAGE OUTLINE

BQA0014A

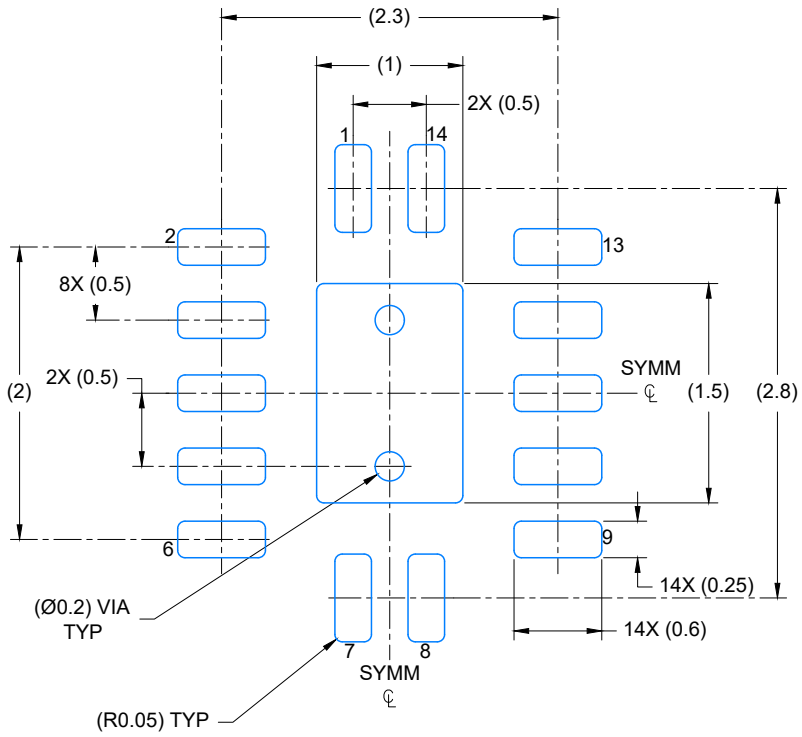
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

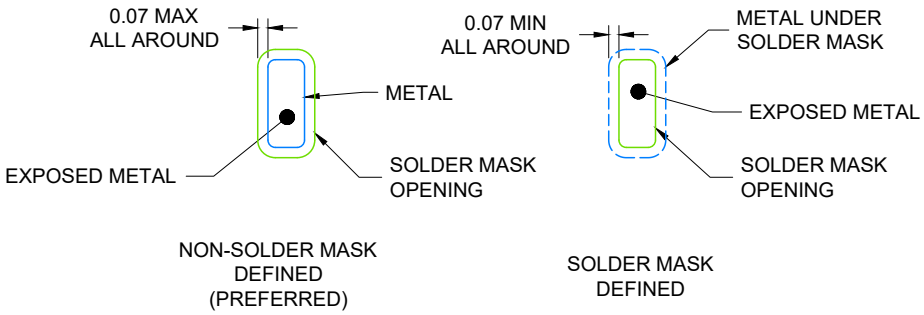


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



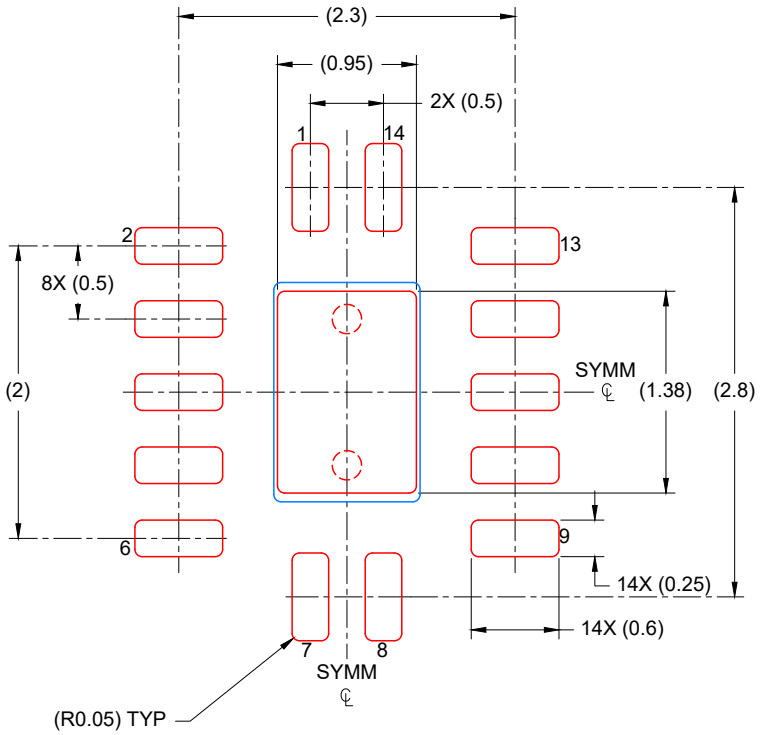
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

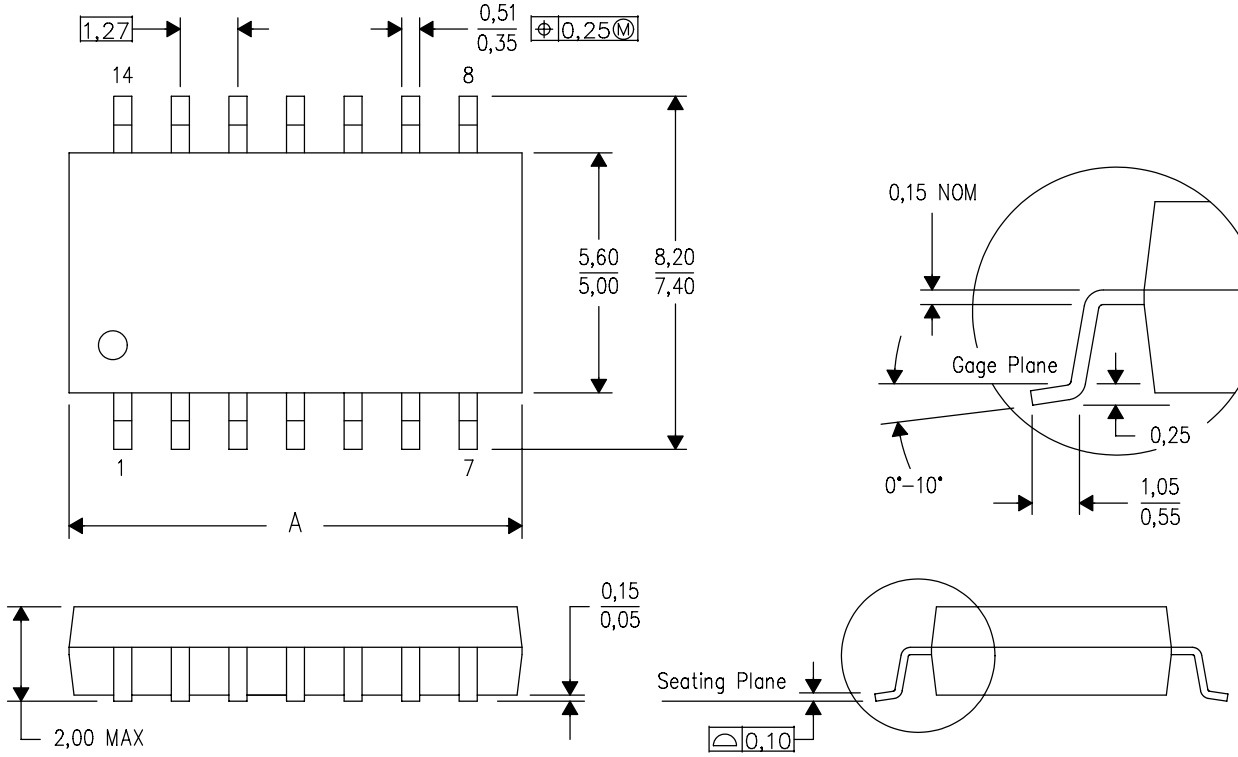
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

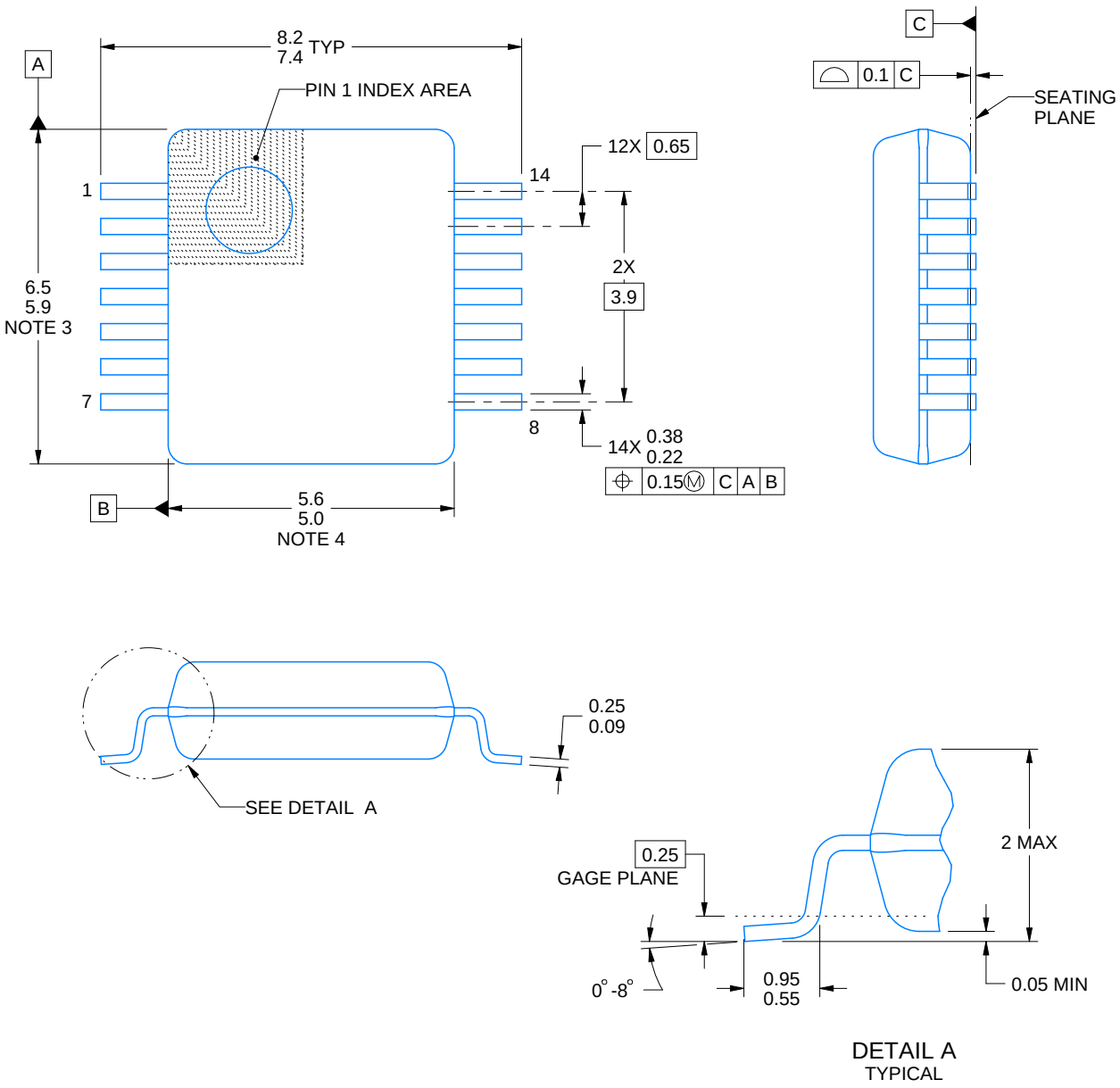
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

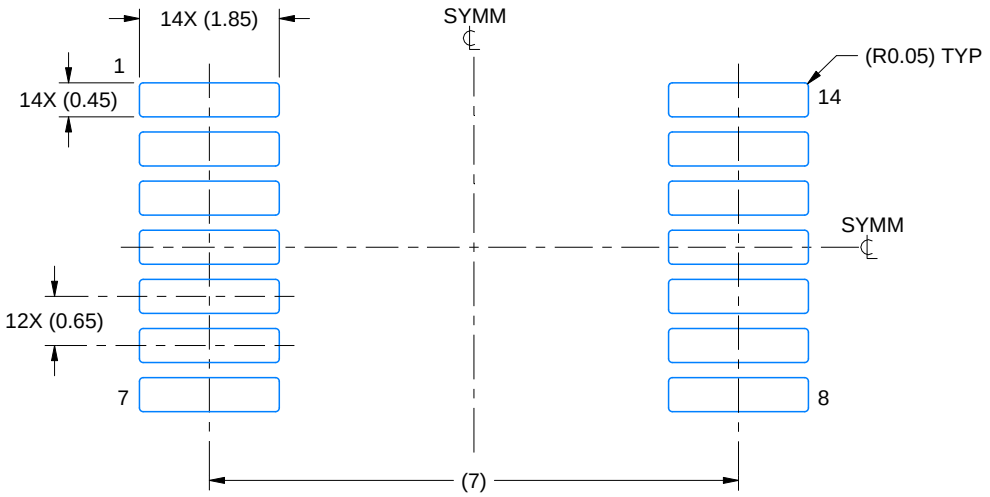
SMALL OUTLINE PACKAGE



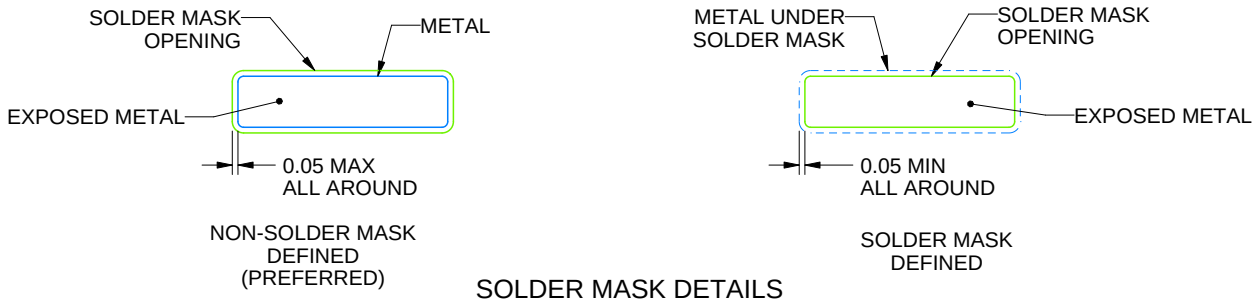
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

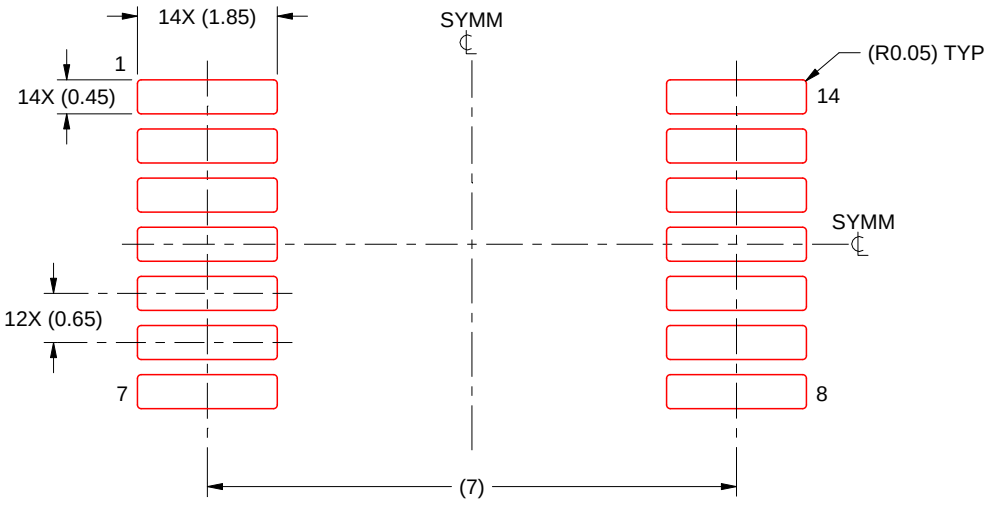


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

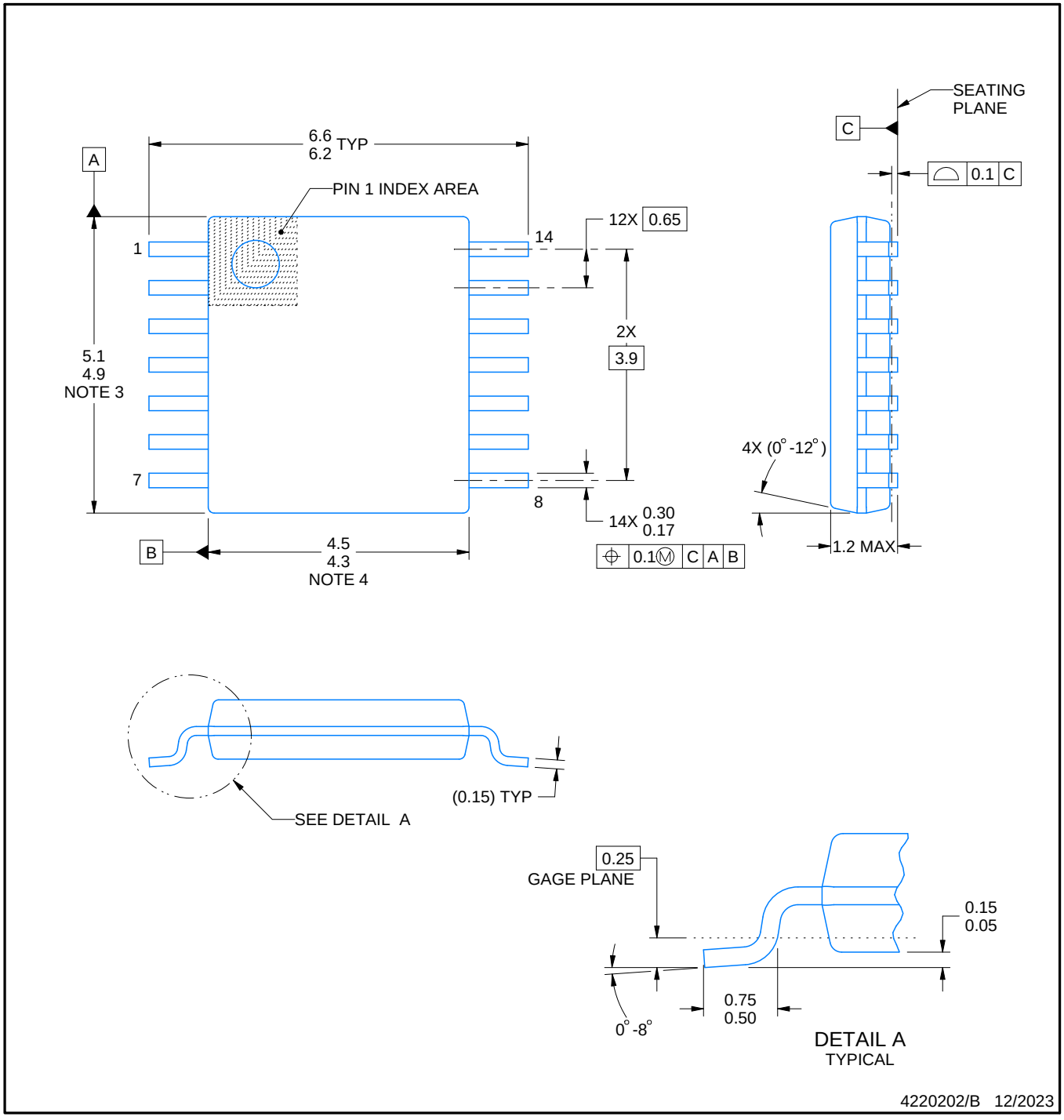
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

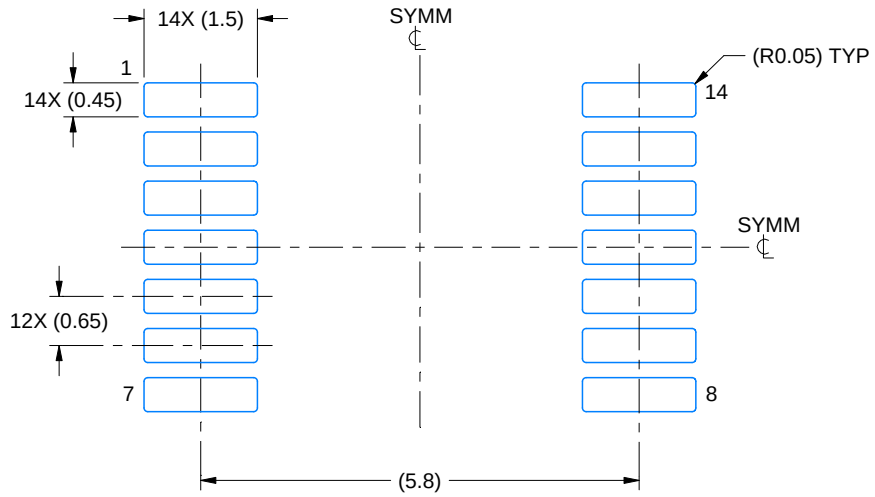
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

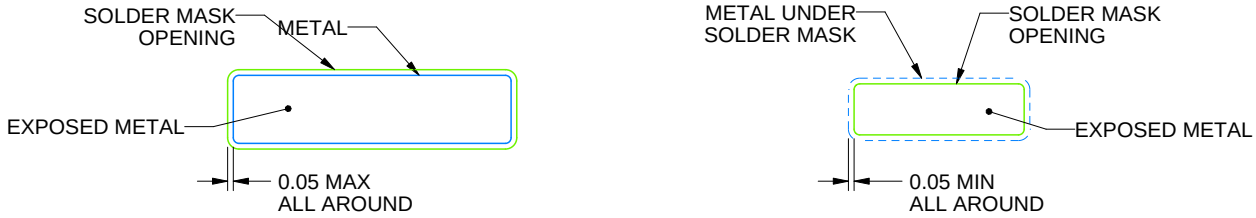


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

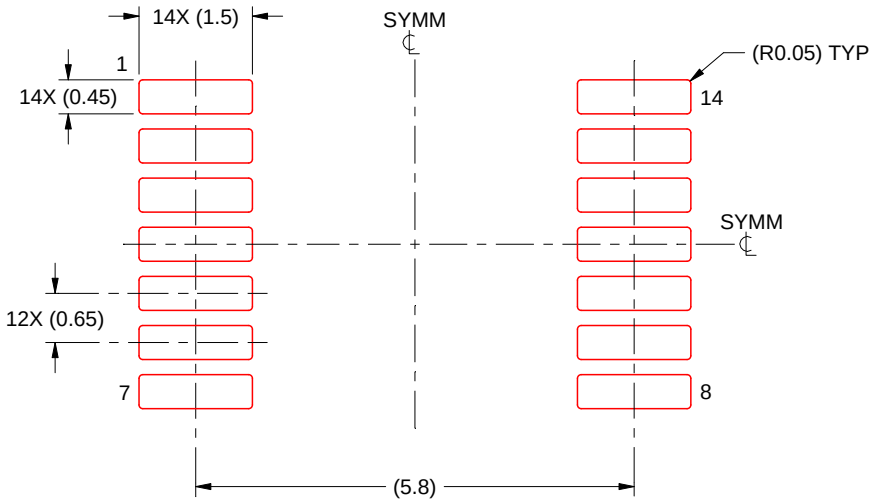


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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