SN74LVC1G3157 单极双投模拟开关

1 特性

- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 1000V 充电器件模型 (C101)
- 1.65V 至 5.5V V_{CC} 运行
- 可在 125°C 的温度下运行
- 指定的先断后合开关
- 轨到轨信号处理
- 室温下的典型工作频率为 340MHz
- 高速，典型值为 0.5ns（V_{CC} = 3V，C_L = 50pF）
- 低导通状态电阻，典型值约为 6Ω (V_{CC} = 4.5V)
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- 可穿戴设备和移动设备
- 便携式计算
- 物联网（IoT）
- 音频信号路由
- 远程无线电单元
- 便携式医疗设备
- 监控
- 家庭自动化
- I2C/SPI/UART 总线多路复用
- 无线充电

3 说明

该单通道单极双投 (SPDT) 模拟开关的设计工作电压范围为 1.65V 至 5.5V V_{CC}。

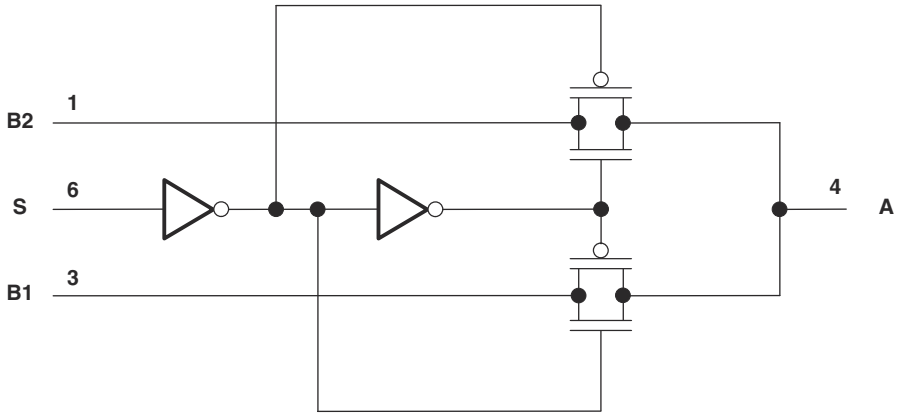
SN74LVC1G3157 器件能够同时处理模拟和数字信号。SN74LVC1G3157 器件允许在任意方向传输振幅高达 V_{CC}（峰值）的信号。

应用包括用于模数和数模转换系统的信号选通、斩波、调制/解调（调制解调器）以及信号多路复用。

封装信息

器件型号	封装 (1)	本体尺寸（标称值）
SN74LVC1G3157	SOT-23 (DBV) (6)	2.90mm × 1.60mm
	SC70 (DCK) (6)	2.00mm × 1.25mm
	SOT (DRL) (6)	1.60mm × 1.20mm
	SON (DRY) (6)	1.45mm × 1.00mm
	DSBGA (YZP) (6)	1.41mm × 0.91mm
	SON (DSF) (6)	1.00mm × 1.00mm
	X2SON (DTB) (6)	0.80mm × 1.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 引脚配置和功能

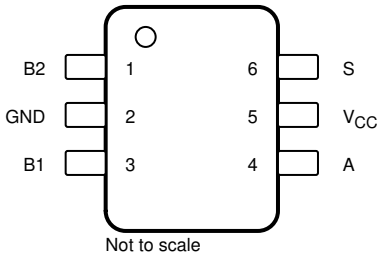

图 4-1. DBV 封装，6 引脚 SOT-23（顶视图）

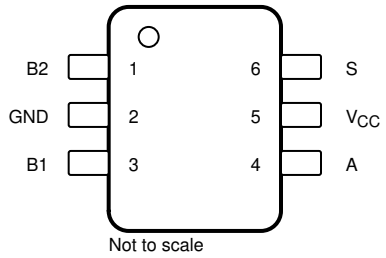

图 4-2. DCK 封装、6 引脚 SC70（顶视图）

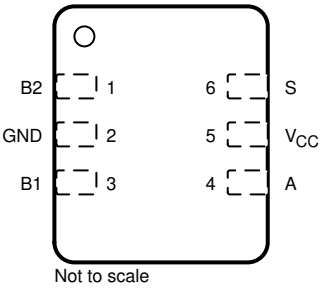

图 4-3. DRY 封装、6 引脚 SON（顶视图）

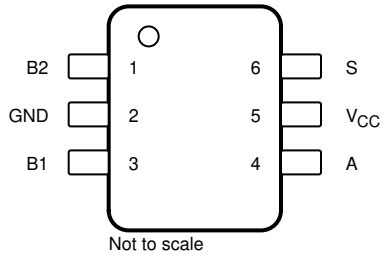

图 4-4. DRL 封装、6 引脚 SOT（顶视图）

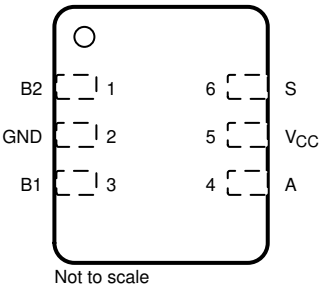

图 4-5. DSF 封装、6 引脚 SON（顶视图）

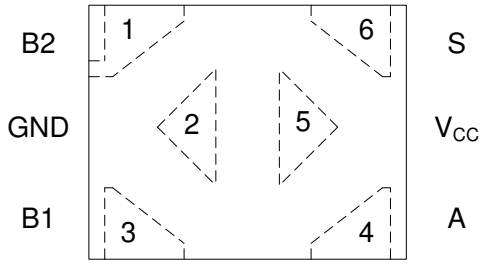

图 4-6. DTB 封装、6 引脚 X2SON（顶视图）

表 4-1. 引脚功能

引脚		类型(1)	说明
名称	SOT-23、SC70、SON、X2SON 或 SOT		
B2	1	I/O	开关 I/O。将 S 设置为高电平以启用。
GND	2	P	接地
B1	3	I/O	开关 I/O。将 S 设置为低电平以启用。
A	4	I/O	普通端子
V_{CC}	5	P	电源
S	6	I	选择

(1) I = 输入；O = 输出；P = 电源

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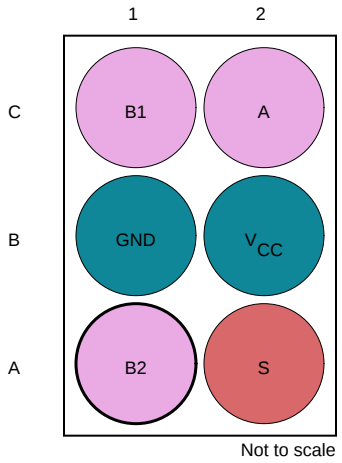

图 4-7. YZP 封装 、6 引脚 DSBGA （底视图）

图例	
输入	输入或输出
电源	

表 4-2. 引脚功能

引脚		类型(1)	说明
编号	名称		
A1	B2	I/O	开关 I/O。将 S 设置为高电平以启用。
A2	S	I	选择
B1	GND	P	接地
B2	V_{CC}	P	电源
C1	B1	I/O	开关 I/O。将 S 设置为低电平以启用。
C2	A	I/O	普通端子

(1) I = 输入；O = 输出；P = 电源

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5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

		最小值	最大值	单位
V_{CC}	（YZP、DSF、DTB、DRY、DRL）电源电压(2)	-0.5	6.5	V
V_{CC}	（DBV、DCK）电源电压(2)	-0.5	6	V
V_{IN}	（YZP、DSF、DTB、DRY、DRL）控制输入电压(2) (3)	-0.5	6.5	V
V_{IN}	（DBV、DCK）控制输入电压(2) (3)	-0.5	6	V
$V_{I/O}$	开关 I/O 电压(2) (3) (4) (5)	-0.5	V_{CC} + 0.5V	V
I_{IK}	控制输入钳位电流 V_{IN} < 0	-50		mA
$I_{I/OK}$	I/O 端口二极管电流 $V_{I/O}$ < 0 或 $V_{I/O}$ > V_{CC}	-50	50	mA
$I_{I/O}$	导通状态开关电流(6) $V_{I/O}$ = 0 至 V_{CC}	-128	128	mA
	通过 V_{CC} 或 GND 的持续电流	-100	100	mA
T_J	结温		150	C
T_{stg}	贮存温度	-65	150	C

(1) 应力超出“绝对最大额定值”下列出的值可能会对器件造成永久损坏。这些列出的值只是应力额定值，并不意味着器件能够在该等条件下以及在除建议工作条件以外的任何其他条件下正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 除非另有说明，否则所有电压均以地为基准。
(3) 如果遵守输入和输出电流额定值，则允许超出输入负压和输出电压额定值。
(4) 该值被限制为最大 5.5V。
(5) V_I、V_O、V_A 和 V_{Bn} 用于表示 $V_{I/O}$ 的特定条件。
(6) I_I、I_O、I_A 和 I_{Bn} 用于表示 $I_{I/O}$ 的特定条件。

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5.2 热性能信息

热指标		SN74LVC1G3157						单位
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (SON)	DTB (X2SON)	YZP (DSBGA)	
		6 引脚	6 引脚	6 引脚	6 引脚	6 引脚	6 引脚	
$R_{\theta JA}$	结至环境热阻	258.2	286.4	244.1	284.2	324.5	129.4	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	182.8	224.6	112.5	138.6	150.5	1.9	°C/W
$R_{\theta JB}$	结至电路板热阻	142.8	143.7	109.9	170.9	239.0	40.0	°C/W
Ψ_{JT}	结至顶部特征参数	118.4	124.5	9.3	13.7	17.2	0.6	°C/W
Ψ_{JB}	结至电路板特征参数	142.2	142.8	109.3	167.9	238.3	40.2	°C/W

5.3 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准(1)	±2000	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101(2)	±1000	V

(1) JEDEC 文档 JEP155 指出：500V HBM 支持在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 能够在标准 ESD 控制流程下安全生产。

5.4 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	标称值	最大值	单位
V_{CC}	电源电压		1.65		5.5	V
$V_{I/O}$	开关输入或输出电压（V_{CC} 的最大值）		0		V_{CC}	V
V_{IN}	控制输入电压		0		5.5	V
V_{IH}	高电平输入电压，控制输入	V_{CC} = 1.65V 至 1.95V	V_{CC} * 0.75			V
		V_{CC} = 2.3V 至 5.5V	V_{CC} * 0.7			V
V_{IL}	低电平输入电压，控制输入	V_{CC} = 1.65V 至 1.95V			V_{CC} * 0.25	V
		V_{CC} = 2.3V 至 5.5V			V_{CC} * 0.3	V
$\Delta t/\Delta v$	输入转换上升或下降速率	V_{CC} = 1.8 ± 0.15V			20	ns/V
		V_{CC} = 2.5 ± 0.2V			20	
		V_{CC} = 3.3V ± 0.3V			10	
		V_{CC} = 5V ± 0.5V			10	
T_A	自然通风条件下的工作温度范围	BGA 封装 (YZP)	-40		85	°C
		所有其他封装（DBV、DCK、DRL、DRY、DSF）	-40		125	

(1) 器件所有的未使用输入必须保持在 VCC 或 GND 以确保器件正常运行。请参阅 TI 应用报告 CMOS 输入缓慢或悬空的影响 (SCBA004)

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5.5 电气特性

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

参数		测试条件				最小值	典型值	最大值	单位
SN74LVC1G3157									
		V_{CC} V	$V_{I/O}$ V	I_O mA	T_A				
r_{ON}	导通状态开关电阻(2)	1.65	V_I = 0V	I_O = 4mA	25°C		11		Ω
					-40°C 至 +85°C			20	
					-40°C 至 +125°C			20	
			V_I = 1.65	I_O = -4mA	25°C		15		
					-40°C 至 +85°C			50	
					-40°C 至 +125°C			50	
		2.3	V_I = 0V	I_O = 8mA	25°C		8		
					-40°C 至 +85°C			12	
					-40°C 至 +125°C			12	
			V_I = 2.3V	I_O = -8mA	25°C		11		
					-40°C 至 +85°C			30	
					-40°C 至 +125°C			30	
		3	V_I = 0V	I_O = 24mA	25°C		7		
					-40°C 至 +85°C			9	
					-40°C 至 +125°C			9	
			V_I = 3V	I_O = -24mA	25°C		9		
					-40°C 至 +85°C			20	
					-40°C 至 +125°C			20	
		4.5	V_I = 0V	I_O = 30mA	25°C		6		
					-40°C 至 +85°C			7	
					-40°C 至 +125°C			7	
			V_I = 2.4V	I_O = 30mA	25°C		7		
					-40°C 至 +85°C			12	
					-40°C 至 +125°C			12	
			V_I = 4.5V	I_O = -30mA	25°C		7		
					-40°C 至 +85°C			15	
					-40°C 至 +125°C			15	
r_{range}	（YZP、DSF、DTB、DRY、DRL）信号范围内的导通状态开关电阻(2) (3)	1.65	0 ≤ V_{Bn} ≤ V_{CC}	I_A = -4mA	25°C		140		Ω
					-40°C 至 +85°C			140	
					-40°C 至 +125°C			140	
		2.3		I_A = -8mA	25°C		45		
					-40°C 至 +85°C			45	
					-40°C 至 +125°C			45	
		3		I_A = -24mA	25°C		18		
					-40°C 至 +85°C			18	
					-40°C 至 +125°C			18	
		4.5		I_A = -30mA	25°C		10		
					-40°C 至 +85°C			10	
					-40°C 至 +125°C			10	

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在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

参数		测试条件				最小值	典型值	最大值	单位
r_{range}	（DBV、DCK）信号范围内的导通状态开关电阻(2) (3)	1.65	0 ≤ V_{Bn} ≤ V_{CC}	I_A = -4mA	25°C			200	Ω
					-40°C 至 +85°C			200	
					-40°C 至 +125°C			200	
		2.3		I_A = -8mA	25°C			65	
					-40°C 至 +85°C			65	
					-40°C 至 +125°C			65	
		3		I_A = -24mA	25°C			25	
					-40°C 至 +85°C			25	
					-40°C 至 +125°C			25	
		4.5		I_A = -30mA	25°C			15	
					-40°C 至 +85°C			15	
					-40°C 至 +125°C			15	
Δr_{ON}	任何两个通道之间的最大导通电阻 (2) (4) (5)	1.65	V_{Bn} = 1.15V	I_A = -4mA	25°C		0.5		Ω
					-40°C 至 +85°C		0.5		
					-40°C 至 +125°C		0.5		
		2.3	V_{Bn} = 1.6V	I_A = -8mA	25°C		0.1		
					-40°C 至 +85°C		0.1		
					-40°C 至 +125°C		0.3		
		3	V_{Bn} = 2.1V	I_A = -24mA	25°C		0.1		
					-40°C 至 +85°C		0.1		
					-40°C 至 +125°C		0.3		
		4.5	V_{Bn} = 3.15V	I_A = -30mA	25°C		0.1		
					-40°C 至 +85°C		0.1		
					-40°C 至 +125°C		0.2		
$r_{on(flat)}$	导通电组平坦度(2) (4) (6)	1.65	0 ≤ V_{Bn} ≤ V_{CC}	I_A = -4mA	25°C		110		Ω
					-40°C 至 +85°C		110		
					-40°C 至 +125°C		110		
		2.3		I_A = -8mA	25°C		26		
					-40°C 至 +85°C		26		
					-40°C 至 +125°C		40		
		3		I_A = -24mA	25°C		9		
					-40°C 至 +85°C		9		
					-40°C 至 +125°C		10		
		4.5		I_A = -30mA	25°C		4		
					-40°C 至 +85°C		4		
					-40°C 至 +125°C		5		
I_{off} (7)	关断漏电流	1.65 至 5.5	0 ≤ V_I , V_O ≤ V_{CC}		25°C		±0.05	±0.1	μA
					-40°C 至 +85°C			±1	
					-40°C 至 +125°C			±1	
$I_{S(on)}$	导通状态开关漏电流	5.5	V_I = V_{CC} 或 GND，V_O = 开路		25°C			±0.1	μA
					-40°C 至 +85°C			±1	
					-40°C 至 +125°C			±1	

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在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

参数		测试条件			最小值	典型值	最大值	单位
I_{IN}	控制输入电流	0 至 5.5	0 ≤ V_{IN} ≤ V_{CC}	25°C		±0.05	±0.1	μA
				-40°C 至 +85°C			±1	
				-40°C 至 +125°C			±1	
I_{CC}	电源电流	5.5	S = V_{CC} 或 GND	25°C			1	μA
				-40°C 至 +85°C			10	
				-40°C 至 +125°C			35	
ΔI_{CC}	静态器件电流，I_{DD} 最大值	5.5	S = V_{CC} - 0.6V	25°C			500	μA
				-40°C 至 +85°C			500	
				-40°C 至 +125°C			500	
C_I	控制输入电容	5	S (VDD/2)	25°C		2.7		pF
				-40°C 至 +85°C		2.7		
				-40°C 至 +125°C		2.7		
$C_{io(off)}$	开关输入/输出电容	5	Bn (VDD/2)	25°C		5.2		pF
				-40°C 至 +85°C		5.2		
				-40°C 至 +125°C		5.2		
$C_{io(on)}$	开关输入/输出电容	5	Bn (VDD/2)	25°C		17.3		pF
				-40°C 至 +85°C		17.3		
				-40°C 至 +125°C		17.3		
			A (VDD/2)	25°C		17.3		
				-40°C 至 +85°C		17.3		
				-40°C 至 +125°C		17.3		

(1) T_A = 25C
(2) 在通过开关的指示电流下由 I/O 引脚之间的电压降测量。通态电阻由两个（A 或 B）端口上的较低电压决定。
(3) 根据设计确定
(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$，在相同的 V_{CC}、温度或电压电平下测得
(5) 此参数已表征，但未经生产测试。
(6) 平坦度定义为在指定条件范围内导通状态电阻的最大值和最小值之间的差异。
(7) I_{off} 与 $I_{S(off)}$ 相同（关断状态开关漏电流）。

5.6 开关特性 85C（DBV、DCK）

T_A = -40 至 +85℃

参数		从（输入）	至（输出）	V_{CC}	最小值	标称值	最大值	单位
t_{pd}	R_L = 250 Ω，C_L = 50pF，V_{load} = V_{CC}	A 或 Bn	Bn 或 A	1.8V ± 0.15V			2	ns
				2.5V ± 0.2V			1.2	
				3.3V ± 0.3V			0.8	
				5V ± 0.5V			0.3	
t_{en}	R_L = 250 Ω，C_L = 50pF，V_{load} = V_{CC}	S	Bn	1.8V ± 0.15V	5		24	ns
				2.5V ± 0.2V	3.5		14	
				3.3V ± 0.3V	2.5		7.6	
				5V ± 0.5V	1.7		5.7	
t_{dis}	R_L = 250 Ω，C_L = 50pF，V_{load} = V_{CC}，$V_▲$ = 0.3V			1.8V ± 0.15V	3		13	
				2.5V ± 0.2V	2		7.5	
				3.3V ± 0.3V	1.5		6	
				5V ± 0.5V	0.8		5	

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T_A = -40 至 +85℃

参数		从（输入）	至（输出）	V_{CC}	最小值	标称值	最大值	单位
T_{B-M}	先断后合时间			1.8V ± 0.15V	0.5			ns
				2.5V ± 0.2V	0.5			
				3.3V ± 0.3V	0.5			
				5V ± 0.5V	0.5			

5.7 开关特性 125C（DBV、DCK）

T_A = -40 至 +125℃

参数		从（输入）	至（输出）	V_{CC}	最小值	标称值	最大值	单位
t_{pd}	R_L = 250Ω，C_L = 50pF，V_{load} = V_{CC}	A 或 Bn	Bn 或 A	1.8V ± 0.15V			2	ns
				2.5V ± 0.2V			1.2	
				3.3V ± 0.3V			0.8	
				5V ± 0.5V			0.5	
t_{en}	R_L = 250Ω，C_L = 50pF，V_{load} = V_{CC}	S	Bn	1.8V ± 0.15V	1		24.5	ns
				2.5V ± 0.2V	1		14.5	
				3.3V ± 0.3V	2.5		8	
				5V ± 0.5V	1.7		7	
t_{dis}	R_L = 250Ω，C_L = 50pF，V_{load} = V_{CC}，$V_▲$ = 0.3V			1.8V ± 0.15V	2.5		13.5	
				2.5V ± 0.2V	2		8	
				3.3V ± 0.3V	1.5		6.5	
				5V ± 0.5V	0.8		5	
T_{B-M}	先断后合时间			1.8V ± 0.15V	0.5			ns
				2.5V ± 0.2V	0.5			
				3.3V ± 0.3V	0.5			
				5V ± 0.5V	0.5			

5.8 开关特性 85C（YZP、DSF、DTB、DRY、DRL）

T_A = -40 至 +85℃

参数		从（输入）	至（输出）	V_{CC}	最小值	标称值	最大值	单位
t_{pd}	R_L = 500Ω，C_L = 50pF，V_{load} = V_{CC}	A 或 Bn	Bn 或 A	1.8V ± 0.15V			2	ns
				2.5V ± 0.2V			1.2	
				3.3V ± 0.3V			0.8	
				5V ± 0.5V			0.3	
t_{en}	R_L = 500Ω，C_L = 50pF，V_{load} = V_{CC}	S	Bn	1.8V ± 0.15V	7		24	ns
				2.5V ± 0.2V	3.5		14	
				3.3V ± 0.3V	2.5		7.6	
				5V ± 0.5V	1.7		5.7	
t_{dis}	R_L = 500Ω、C_L = 50pF、V_{load} = V_{CC}、$V_△$ = 0.3V			1.8V ± 0.15V	3		13	
				2.5V ± 0.2V	2		7.5	
				3.3V ± 0.3V	1.5		5.3	
				5V ± 0.5V	0.8		3.8	

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T_A = -40 至 +85℃

参数		从（输入）	至（输出）	V_{CC}	最小值	标称值	最大值	单位
T_{B-M}	先断后合时间			1.8V ± 0.15V	0.5			ns
				2.5V ± 0.2V	0.5			
				3.3V ± 0.3V	0.5			
				5V ± 0.5V	0.5			

5.9 开关特性 125C（YZP、DSF、DTB、DRY、DRL）

T_A = -40 至 +125℃

参数		从（输入）	至（输出）	V_{CC}	最小值	标称值	最大值	单位
t_{pd}	R_L = 500Ω，C_L = 50pF，V_{load} = V_{CC}	A 或 Bn	Bn 或 A	1.8V ± 0.15V			2	ns
				2.5V ± 0.2V			1.2	
				3.3V ± 0.3V			0.8	
				5V ± 0.5V			0.5	
t_{en}	R_L = 500Ω，C_L = 50pF，V_{load} = V_{CC}	S	Bn	1.8V ± 0.15V	1		24.5	ns
				2.5V ± 0.2V	1		14.5	
				3.3V ± 0.3V	2.5		8	
				5V ± 0.5V	1.7		6	
t_{dis}	R_L = 500Ω、C_L = 50pF、V_{load} = V_{CC}、$V_{Δ}$ = 0.3V			1.8V ± 0.15V	2.5		13.5	
				2.5V ± 0.2V	2		8	
				3.3V ± 0.3V	1.5		5.5	
				5V ± 0.5V	0.8		4	
T_{B-M}	先断后合时间			1.8V ± 0.15V	0.5			ns
				2.5V ± 0.2V	0.5			
				3.3V ± 0.3V	0.5			
				5V ± 0.5V	0.5			

5.10 模拟通道规格

在自然通风条件下的工作温度范围内测得（除非另有说明）

参数	从（输入）	至（输出）	测试条件	v_{cc}	最小值	标称值	最大值	单位
频率响应（开关导通）(1)	A 或 Bn	Bn 或 A	R_L = 50Ω，f_{in} = 正弦波	1.65V		340		MHz
				2.3V		340		
				3V		340		
				4.5V		340		
串扰（开关间）(2)	B1 或 B2	B2 或 B1	R_L = 50Ω，f_{in} = 10MHz（正弦波）	1.65V		-54		dB
				2.3V		-54		
				3V		-54		
				4.5V		-54		
馈通衰减（开关关闭）(2)	A 或 Bn	Bn 或 A	C_L = 5pF，R_L = 50Ω，f_{in} = 10MHz（正弦波）	1.65V		-57		dB
				2.3V		-57		
				3V		-57		
				4.5V		-57		
电荷注入	S (Vs = VDD/2)	A	C_L = 0.1nF，R_L = 1MΩ	3.3V		3		pC
				5V		7		

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在自然通风条件下的工作温度范围内测得（除非另有说明）

参数	从（输入）	至（输出）	测试条件	v_{cc}	最小值	标称值	最大值	单位
总谐波失真（YZP、DSF、DTB、DRY、DRL）	A 或 Bn	Bn 或 A	V_I = 1.4V_{p-p}，Vbias = Vcc/2，R_L = 10kΩ，f_{in} = 600Hz 至 20kHz（正弦波）	1.65V		0.1		%
总谐波失真（DBV、DCK）	A 或 Bn	Bn 或 A	V_I = 1.4V_{p-p}，Vbias = Vcc/2，R_L = 10kΩ，f_{in} = 600Hz 至 20kHz（正弦波）	1.65V		0.5		%
总谐波失真	A 或 Bn	Bn 或 A	V_I = 2.0V_{p-p}，Vbias = Vcc/2，R_L = 10kΩ，f_{in} = 600Hz 至 20kHz（正弦波）	2.3V		0.025		%
				3V		0.015		
				4.5V		0.01		

(1) 将 fin 设置为 0dBm 并提供 0.4V 的偏压。增大 fin 频率，直到增益低于插入损耗 3dB。
(2) 将 fin 设置为 0dBm 并提供 0.4V 的偏压。

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6 参数测量信息

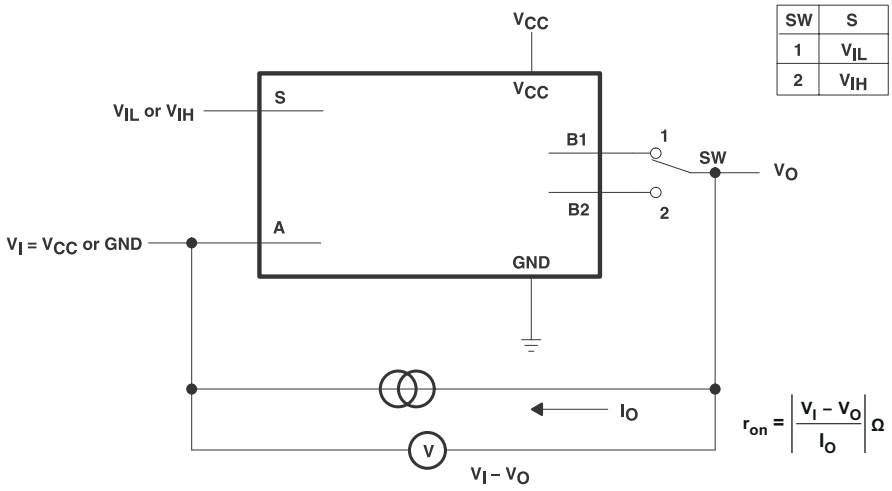
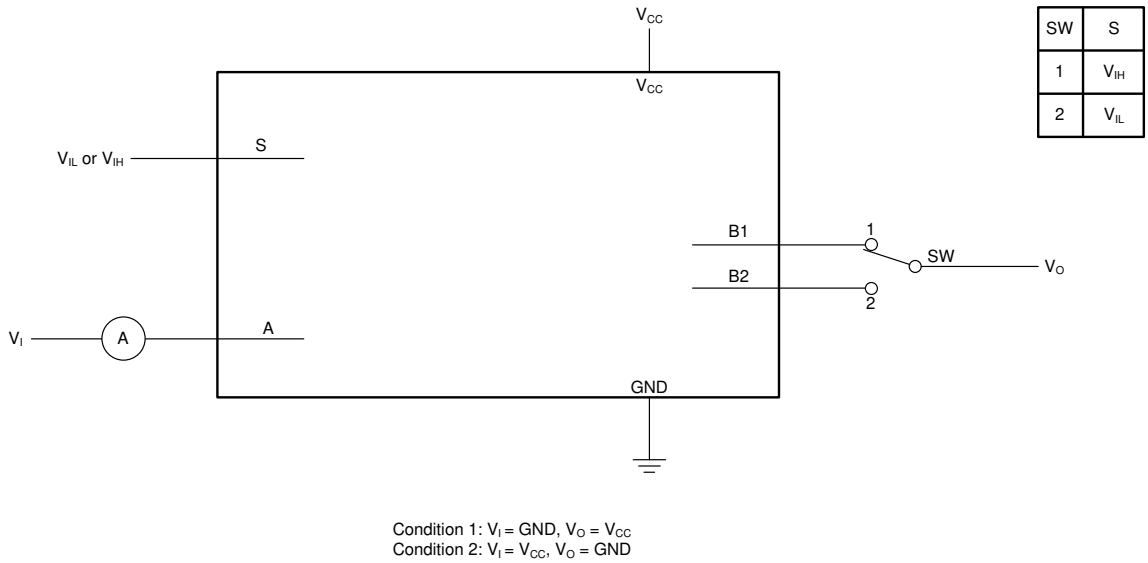


图 6-1. 导通电阻测试电路



Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

图 6-2. 关断状态开关漏电流测试电路

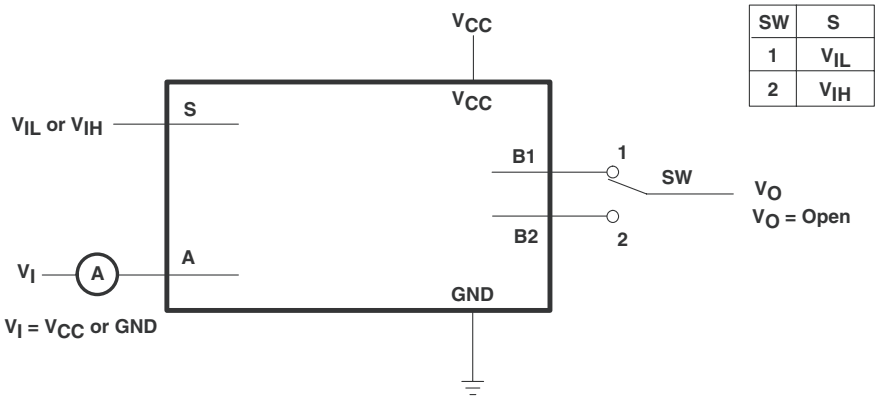
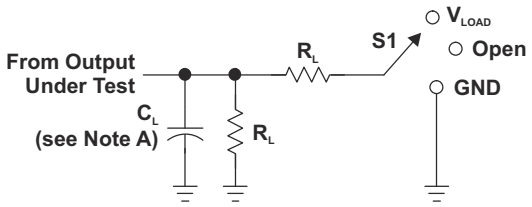


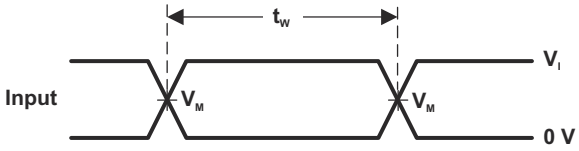
图 6-3. 导通状态开关漏电流测试电路



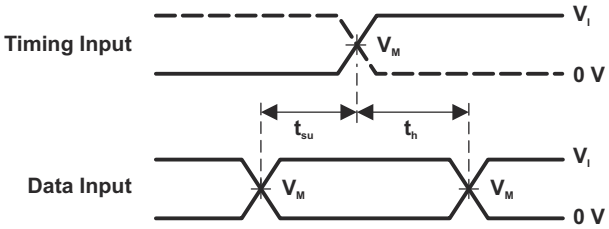
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

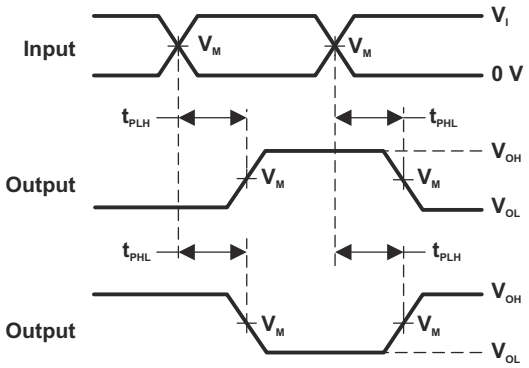
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



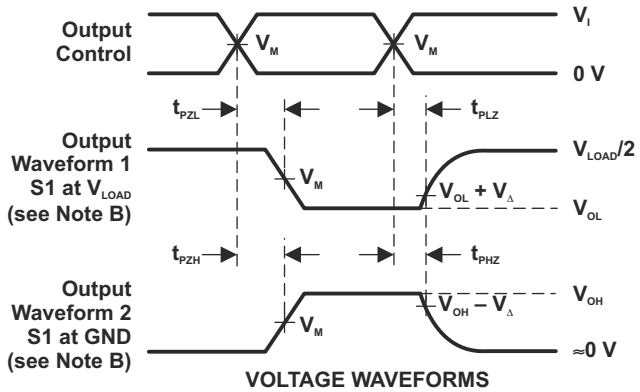
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

图 6-4. 负载电路和电压波形

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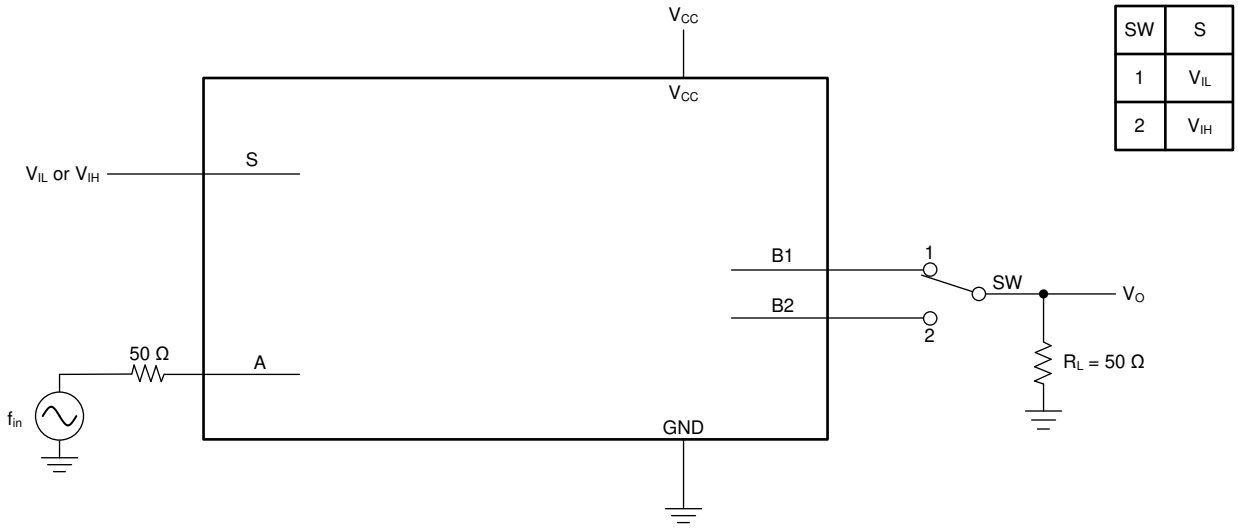

图 6-5. 频率响应（开关导通）

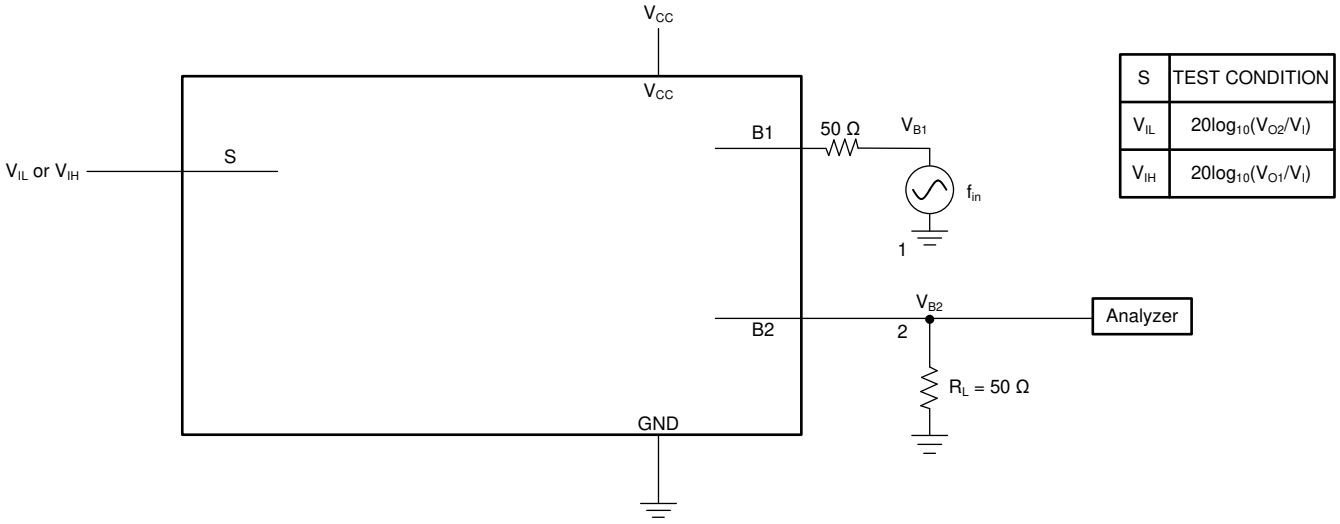

图 6-6. 串扰（开关间）

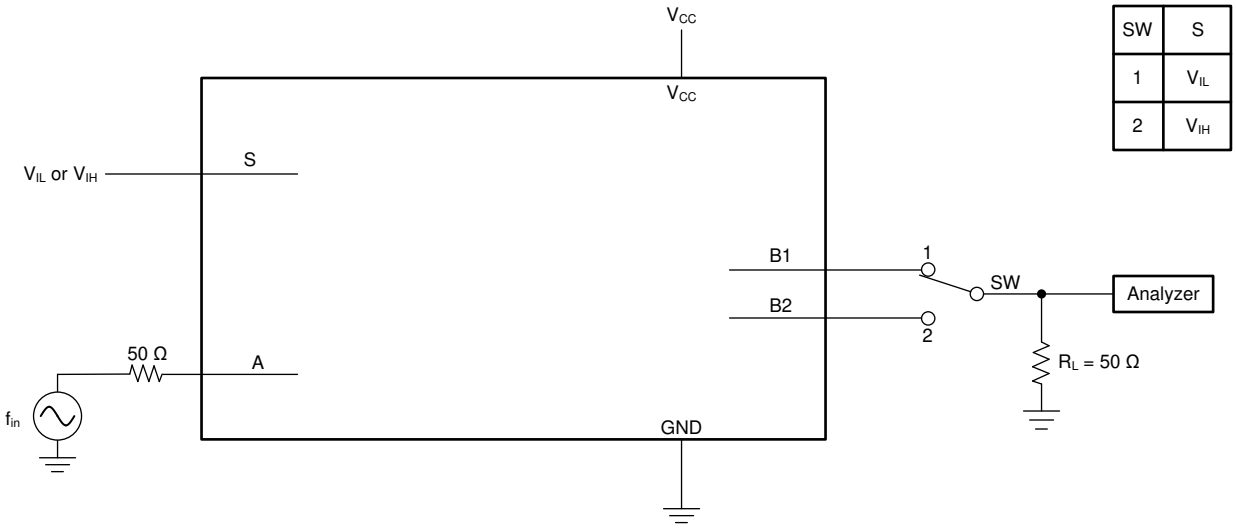

图 6-7. 馈通

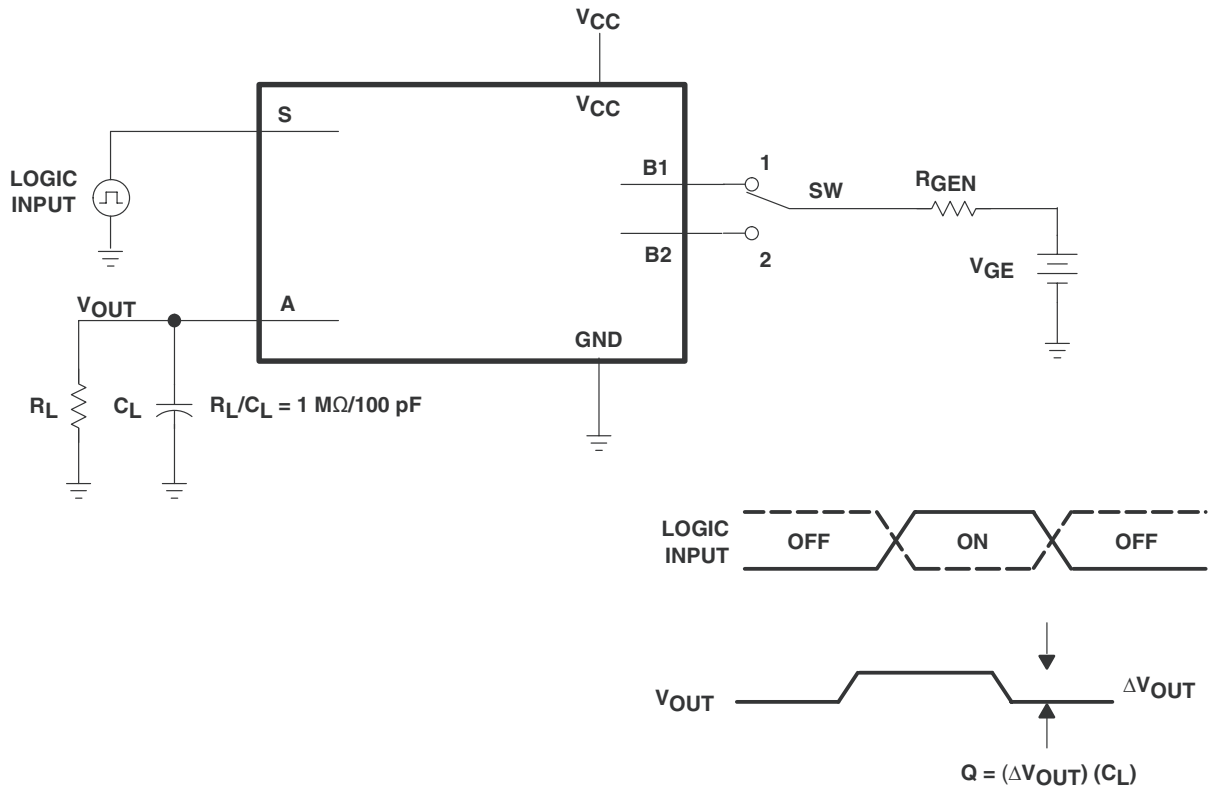

图 6-8. 电荷注入测试

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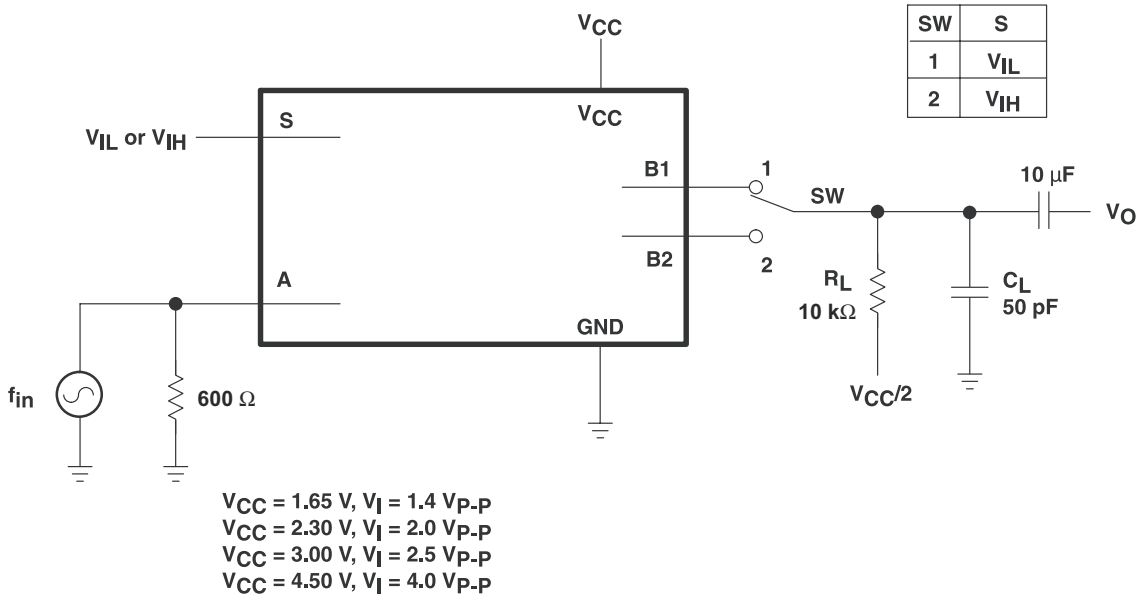

图 6-9. 总谐波失真

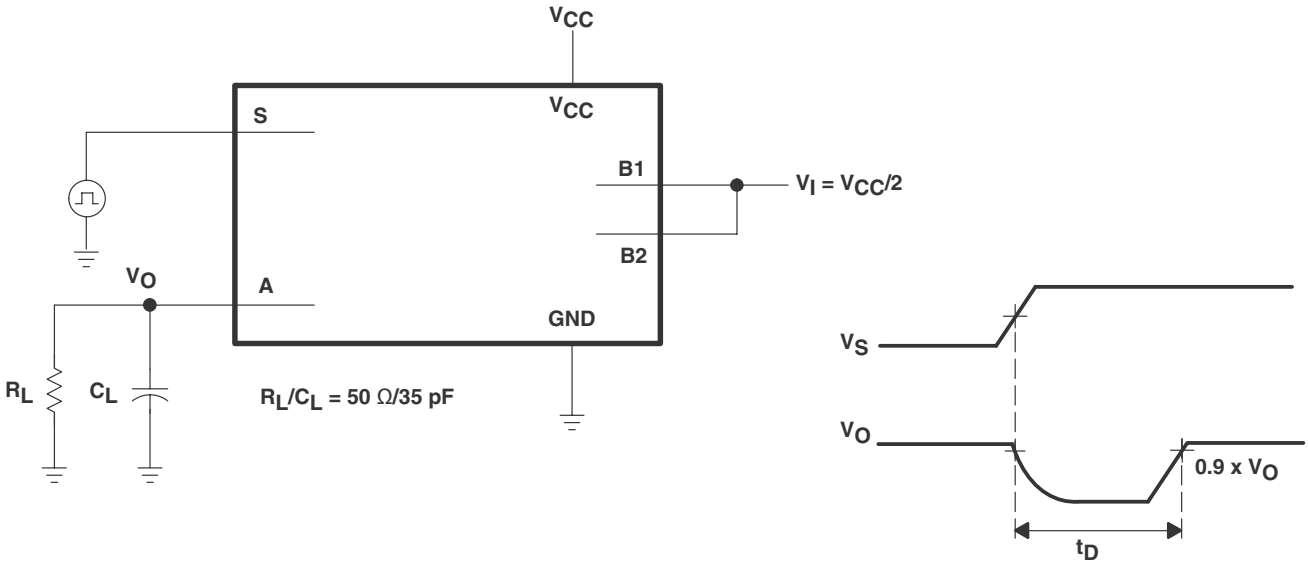

图 6-10. 先断后合内部时序

7 详细说明

7.1 概述

SN74LVC1G3157 器件是一种单极双投 (SPDT) 模拟开关，设计工作电压范围为 1.65V 至 5.5V V_{CC}。SN74LVC1G3157 器件能够处理模拟和数字信号。该器件允许在任意方向传输振幅高达 V_{CC}（峰值）的信号。

7.2 功能方框图

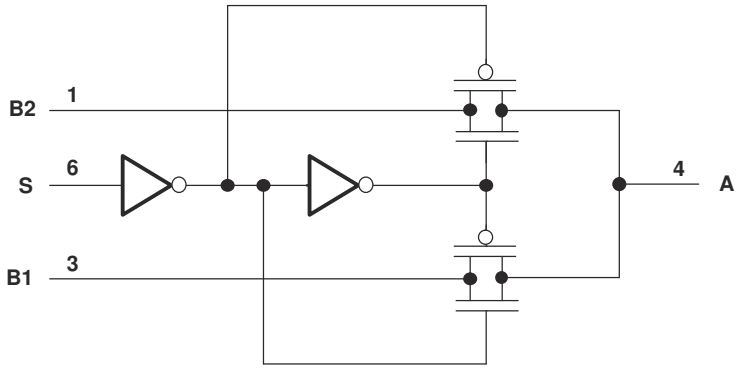

图 7-1. 逻辑图（正逻辑）

7.3 特性说明

由 1.65V 至 5.5V 电源供电使该器件能在由不同逻辑电平组成的许多不同系统中运行，从而实现轨到轨信号切换。根据控制输入激活 B1 通道或 B2 通道。如果控制输入为低电平，则选择 B1 通道。如果控制输入为高电平，则选择 B2 通道。

7.4 器件功能模式

表 7-1 列出了选择其中一个控制输入时的导通通道。

表 7-1. 功能表

控制 输入	导通 通道
L	B1
H	B2

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8 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 应用信息

SN74LVC1G3157 SPDT 模拟开关足够灵活，可用于各种电路，例如模拟音频路由、加电监视器、内存共享等。有关应用的详细信息，请参阅 SN74LVC1G3157 和 SN74LVC2G53 SPDT 模拟开关。

8.2 典型应用

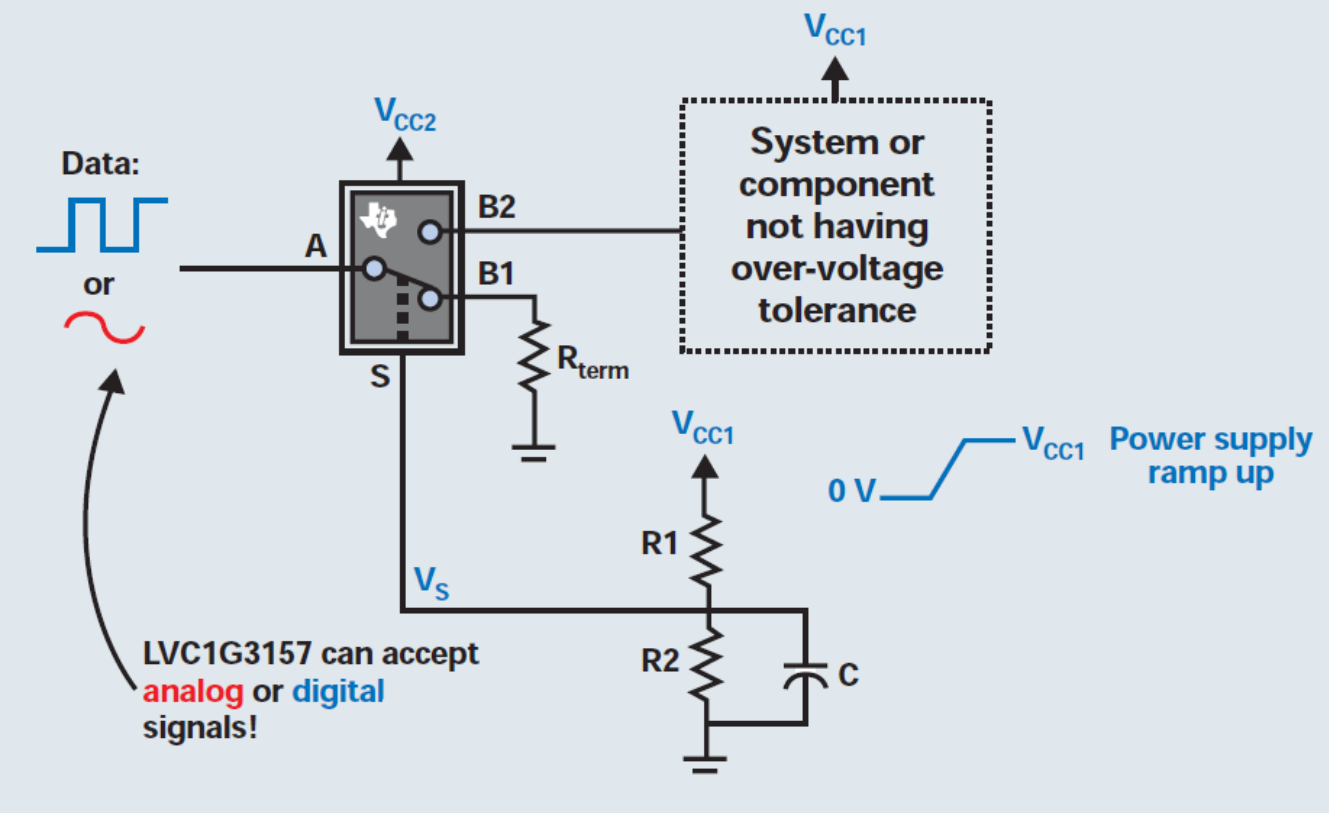

图 8-1. 典型应用原理图

8.2.1 设计要求

输入可以是模拟输入或数字输入，但 TI 建议在施加任何信号之前等待 V_{CC} 上升到 *节 5.4* 中的电平。应根据信号类型和规格使用适当的终端电阻器。选择引脚不应悬空；上拉或下拉时使用可由 GPIO 过驱动的电阻器。

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8.2.2 详细设计过程

使用此电路创意，系统设计人员可以确保组件或子系统电源在允许信号施加到其输入之前斜升。这对于没有过压耐受输入的集成电路很有用。基本思路是在 VCC1 电源轨上使用电阻分压器，该分压器正在斜升。电阻分压器的 RC 时间常数进一步延迟了 SPDT 总线开关选择引脚上的电压斜坡。通过仔细选择 R1、R2 和 C 的值，可以确保 VCC1 在从 A 到 B2 的路径建立之前达到其标称值，从而防止在器件/系统上电之前 I/O 上出现信号通电。为了确保实现所需的极低延迟，设计人员应使用方程式 1 来计算从接地转换 (0V) 到电源电压 (VCC1/2) 一半所需的时间。

$$\text{Set}\left(\frac{R2}{R1+R2}\times V_{CC1} > V_{IH}\right)\text{of the select pin} \tag{1}$$

选择 Rs 和 C 以获得所需的延迟。当 V_S 变为高电平时，信号将被传递。

8.2.3 应用曲线

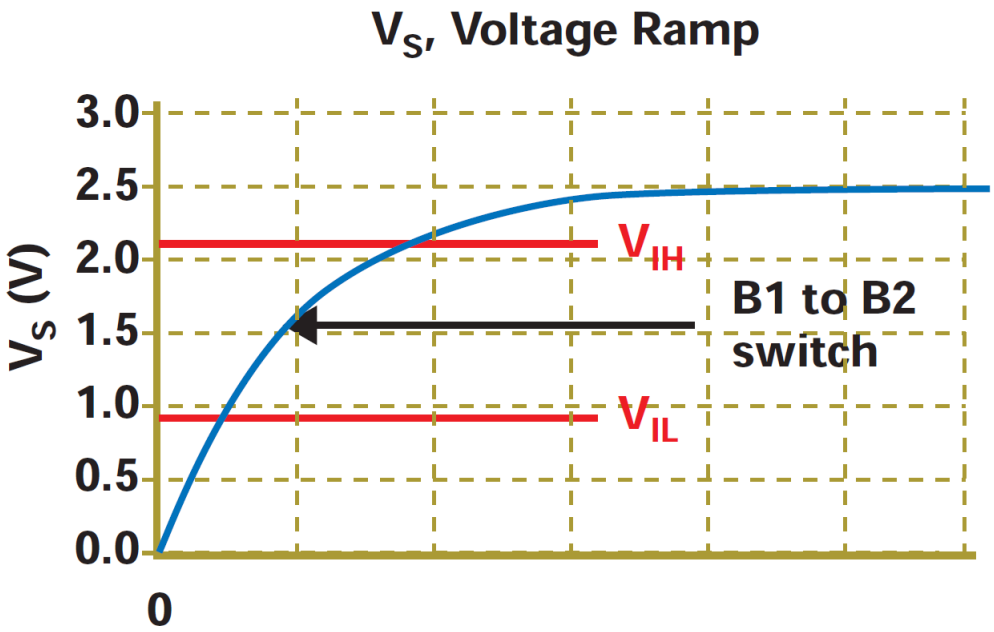

图 8-2. V_S 电压斜坡

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9 电源相关建议

大多数系统有一个常见的 3.3V 或 5V 电源轨，可为该器件的 V_{CC} 引脚供电。如果这不可用，则可以使用开关模式电源 (SMPS) 或线性压差稳压器 (LDO) 从另一个电压轨为该器件供电。

10 布局

10.1 布局指南

TI 建议使信号线路尽可能短。TI 还建议在信号线长度大于 1 英寸时采用微带线或带状线技术。根据应用的要求，这些布线的特征阻抗必须设计为 50Ω 或 75Ω。不要将此器件放置在离高压开关元件太近的地方，因为它们可能会干扰器件。

10.2 布局示例

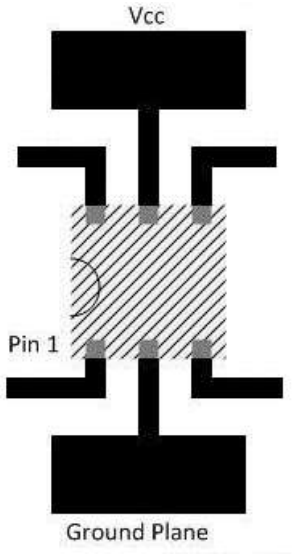

图 10-1. 推荐布局示例

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*慢速或浮点 CMOS 输入的影响*
- 德州仪器 (TI)，*SN74LVC1G3157 和 SN74LVC2G53 SPDT 模拟开关*

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

11.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision N (May 2025) to Revision O (June 2025)	Page
• 将相关 DBV 和 DCK 规格与其他封装分离	5

Changes from Revision M (August 2022) to Revision N (May 2025)	Page
• 绝对最大电源电压已更改	5
• 更新了 DBV 和 DCK 的热参数	6
• 更新了 r_{range}	7
• 更新了 85°C 1.8V 和 125°C 5V 条件下的启用时序	9
• 更新了 85°C 5V 和 125°C 3.3V、5V 条件下的禁用时序	9
• 更新了 THD 测试条件和 1.65V 规格	11

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Changes from Revision L (May 2017) to Revision M (August 2022) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式.....1
- 更新了 *引脚配置和功能* 部分.....3
- 更新了 *详细设计过程* 部分中的公式.....20

Changes from Revision K (January 2017) to Revision L (May 2017) **Page**

- 删除了 *特性* 中的“用于模拟和数字应用”.....1
- 删除了 *特性* 中的“高度线性”.....1
- 将 *说明* 中的第一句从“该单极双投 (SPDT)...”更改为：“该单通道单极双投 (SPDT)...”.....1
- 向 *器件信息* 添加了 X2SON (DTB) 封装.....1
- 向 *引脚配置和功能* 添加了 X2SON (DTB 封装.....3
- 更改了图 6-2，从 SW1 = V_{IL} 更新为 SW1 = V_{IH}，从 SW2 = V_{IH} 更新为：SW2 = V_{IL}.....13
- 更改了图 6-5.....13
- 在图 6-6 中的 B1 上添加了一个串联 50Ω 电阻器.....13
- 更改了图 6-7.....13

Changes from Revision J (June 2016) to Revision K (January 2017) **Page**

- 向 *应用* 部分添加了新的应用.....1

Changes from Revision I (June 2015) to Revision J (June 2016) **Page**

- 删除了 *特性* 中的 200V 机器模型 (A115-A).....1
- 将 *特性* 从“室温下的典型工作频率为 300MHz”更改为“室温下的典型工作频率为 340MHz”.....1
- 更新了 *器件信息* 表.....1
- 更新了所有封装的引脚排列图.....3
- 添加了 *接收文档更新通知* 部分.....22

Changes from Revision H (May 2012) to Revision I (June 2015) **Page**

- 添加了 *器件信息* 表、*引脚配置和功能* 部分、*ESD 等级* 表、*特性说明* 部分、*器件功能模式* 部分、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分.....1
- 更新了 *特性*.....1

Changes from Revision G (September 2011) to Revision H (May 2012) **Page**

- 使用正确的引脚标签更改了 YZP。.....3

13 机械、封装和可订购信息

下述页面包含机械、封装和订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVC1G3157DBVR1G4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC55
74LVC1G3157DBVR1G4.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC55
74LVC1G3157DBVR1G4.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC55
74LVC1G3157DBVRG4	Obsolete	Production	SOT-23 (DBV) | 6	-	-	Call TI	Call TI	-40 to 85	(CC5F, CC5R)
74LVC1G3157DRLRG4	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C57
74LVC1G3157DRLRG4.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C57
74LVC1G3157DSFRG4	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
74LVC1G3157DSFRG4.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(3HRH, CC55, CC5F, CC5K, CC5R) CC5S
SN74LVC1G3157DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(3HRH, CC55, CC5F, CC5K, CC5R) CC5S
SN74LVC1G3157DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(3HRH, CC55, CC5F, CC5K, CC5R) CC5S
SN74LVC1G3157DCK3	Obsolete	Production	SC70 (DCK) | 6	-	-	Call TI	Call TI	-40 to 125	C5Z
SN74LVC1G3157DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(3HSH, C55, C5F, C 5J, C5R)
SN74LVC1G3157DCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(3HSH, C55, C5F, C 5J, C5R)
SN74LVC1G3157DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(3HSH, C55, C5F, C 5J, C5R)
SN74LVC1G3157DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(C57, C5R)
SN74LVC1G3157DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C57, C5R)
SN74LVC1G3157DRLR.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C57, C5R)
SN74LVC1G3157DRY2	Obsolete	Production	SON (DRY) | 6	-	-	Call TI	Call TI	-40 to 125	C5
SN74LVC1G3157DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DRYR.A	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G3157DSFR	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DSFR.A	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DSFR.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DTBR	Active	Production	X2SON (DTB) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7X
SN74LVC1G3157DTBR.B	Active	Production	X2SON (DTB) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7X
SN74LVC1G3157YZPR	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C5N
SN74LVC1G3157YZPR.B	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C5N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G3157 :

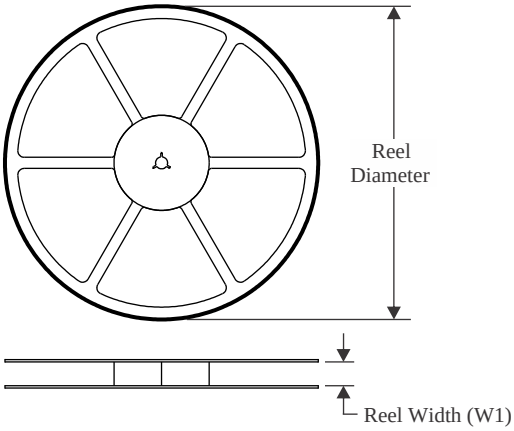
- Automotive : SN74LVC1G3157-Q1

NOTE: Qualified Version Definitions:

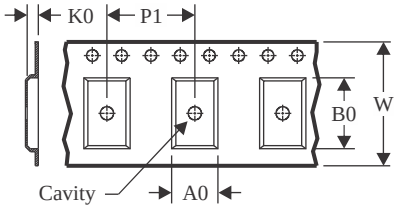
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

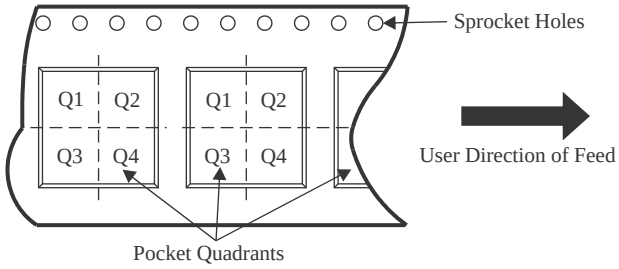


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

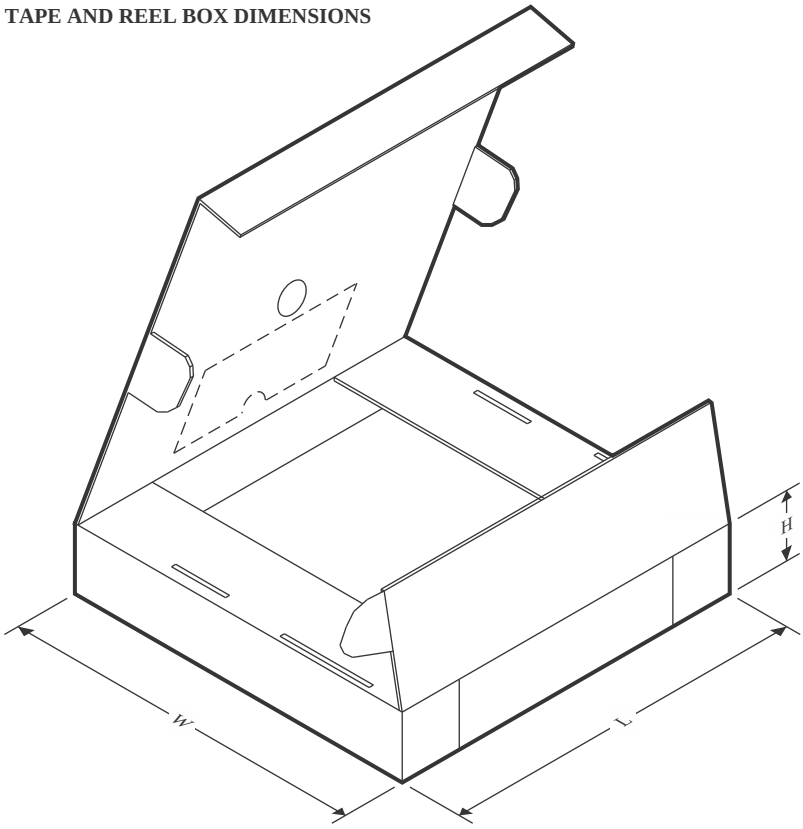
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G3157DBVR1G4	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
74LVC1G3157DRLRG4	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
74LVC1G3157DSFRG4	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G3157DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G3157DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC1G3157DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1G3157DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G3157DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G3157DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G3157DTBR	X2SON	DTB	6	3000	180.0	9.5	0.94	1.13	0.41	2.0	8.0	Q2
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

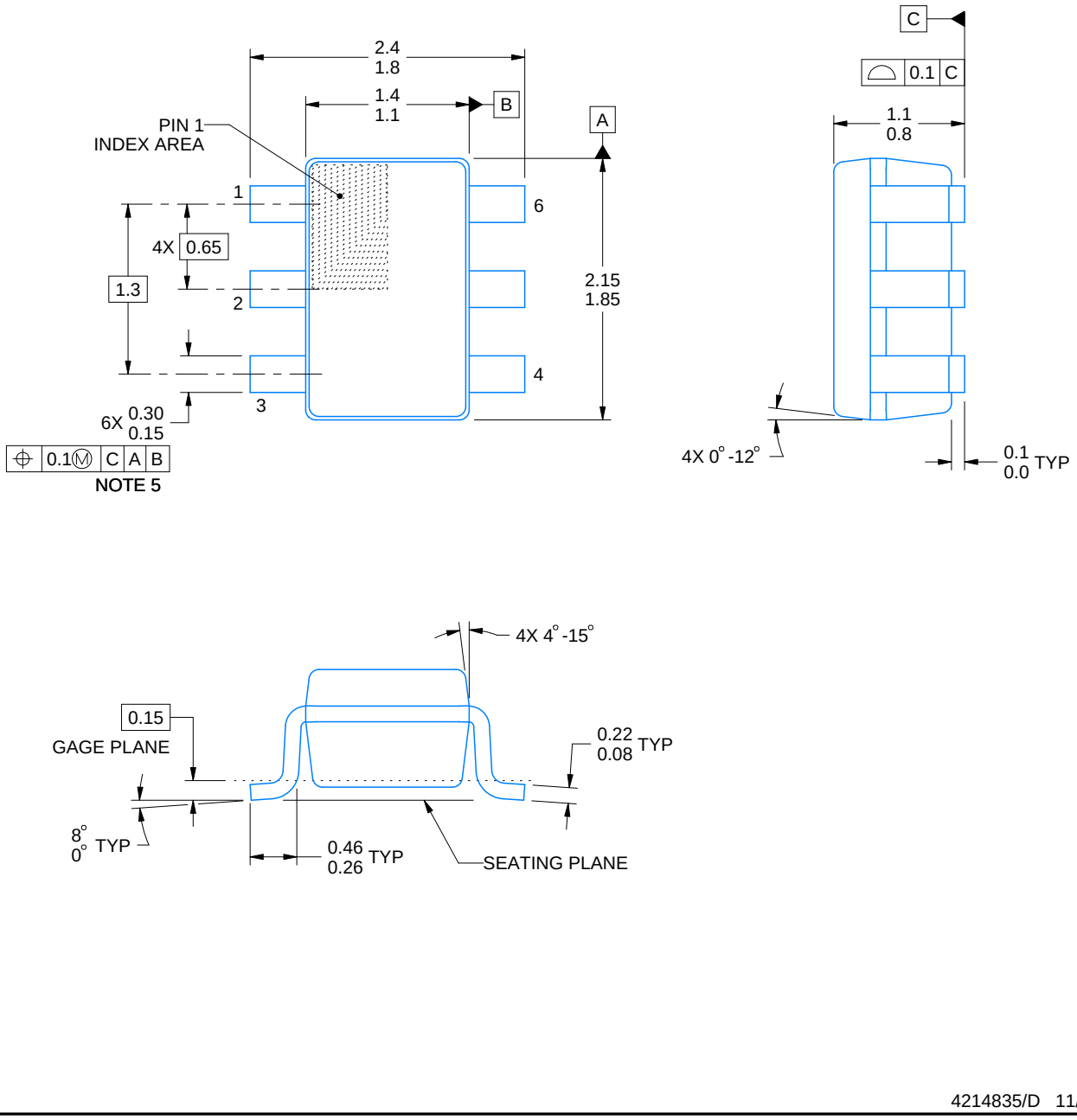
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G3157DBVR1G4	SOT-23	DBV	6	3000	210.0	185.0	35.0
74LVC1G3157DRLRG4	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
74LVC1G3157DSFRG4	SON	DSF	6	5000	210.0	185.0	35.0
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1G3157DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G3157DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74LVC1G3157DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	189.0	185.0	36.0
SN74LVC1G3157DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74LVC1G3157DTBR	X2SON	DTB	6	3000	189.0	185.0	36.0
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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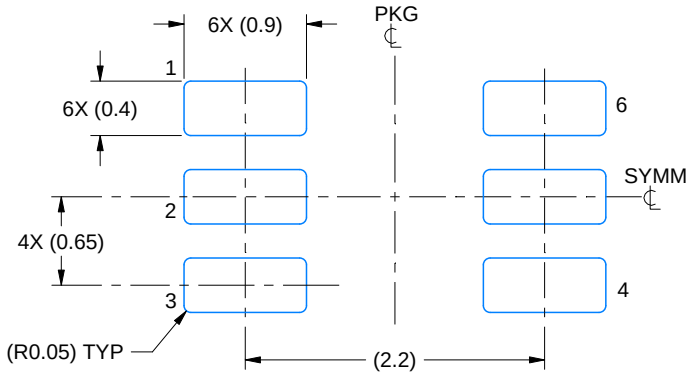
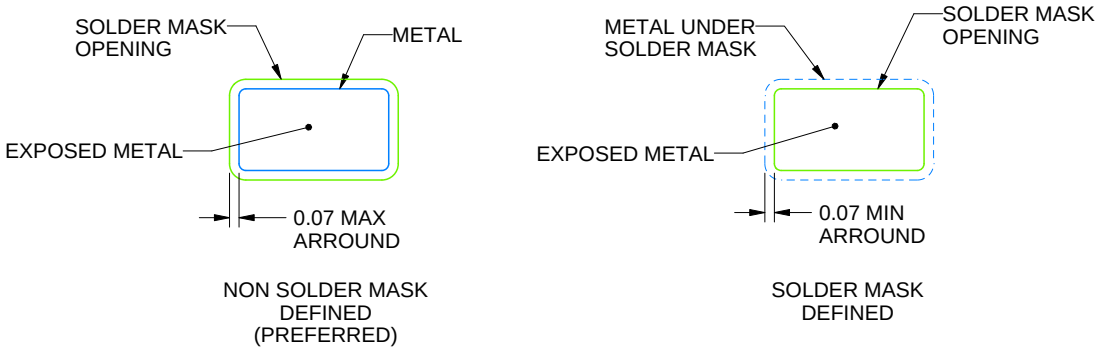
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

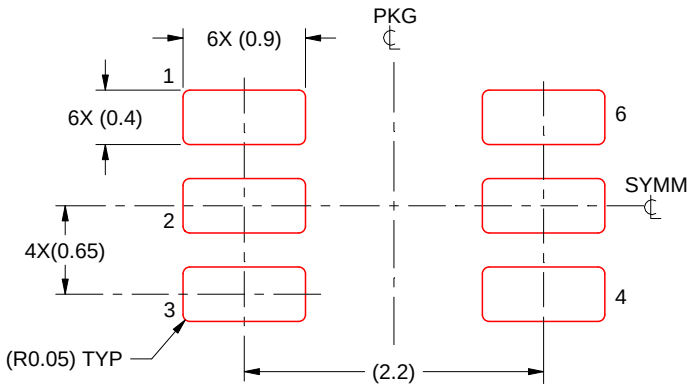


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

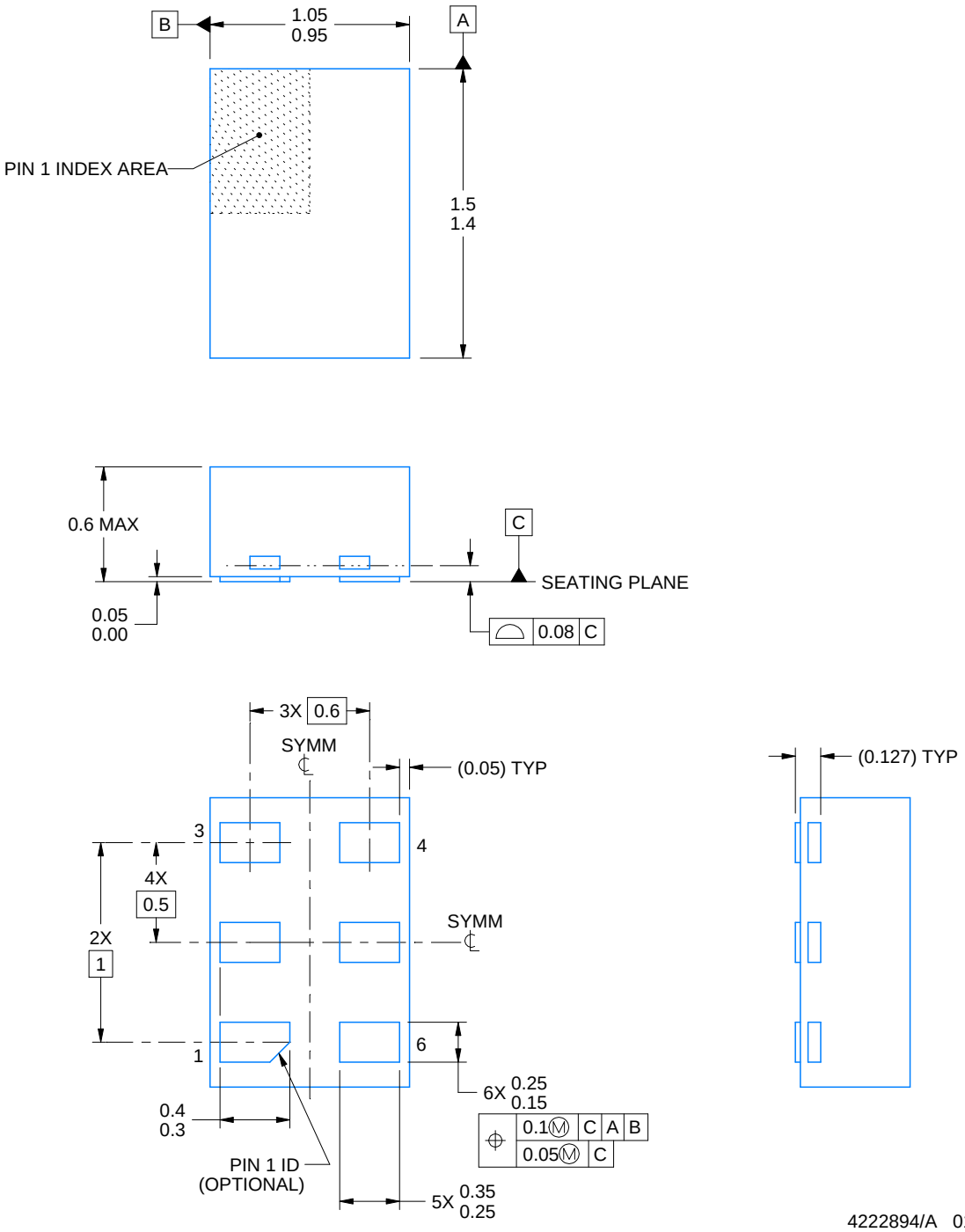
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRY0006A

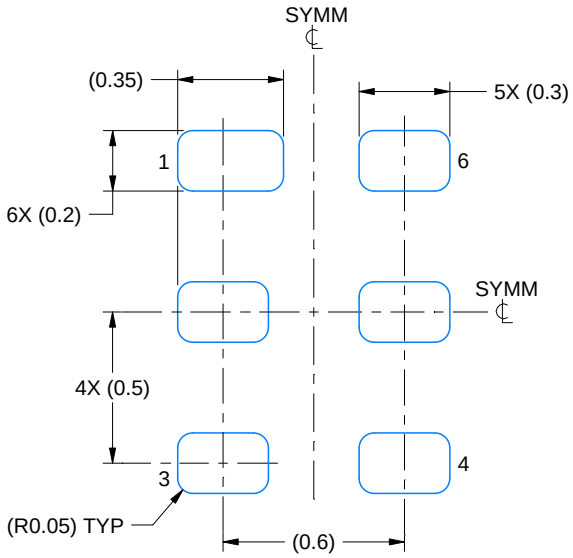
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

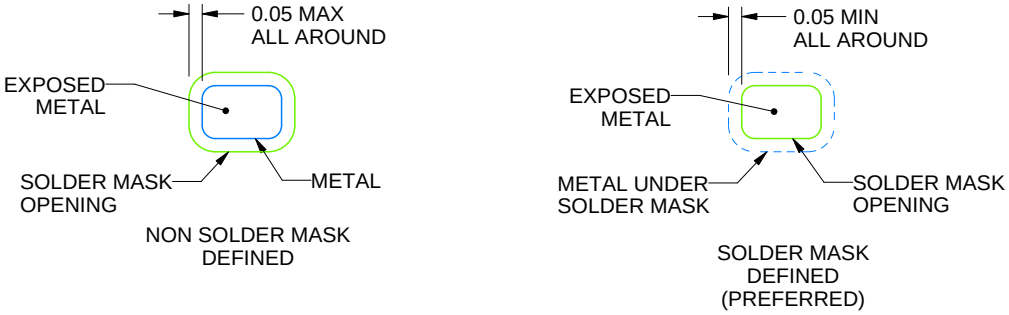


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

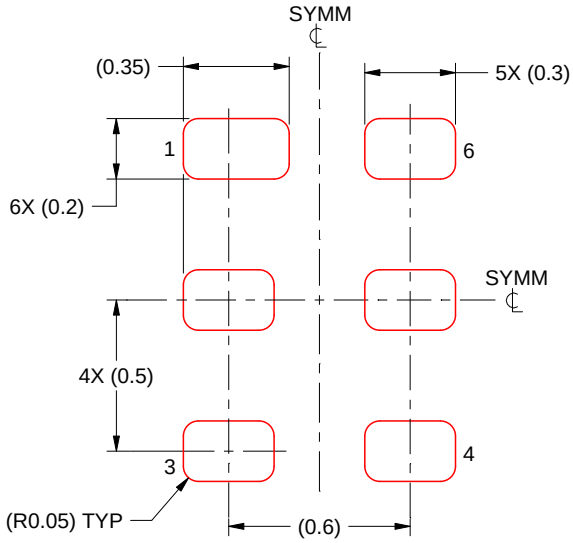
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

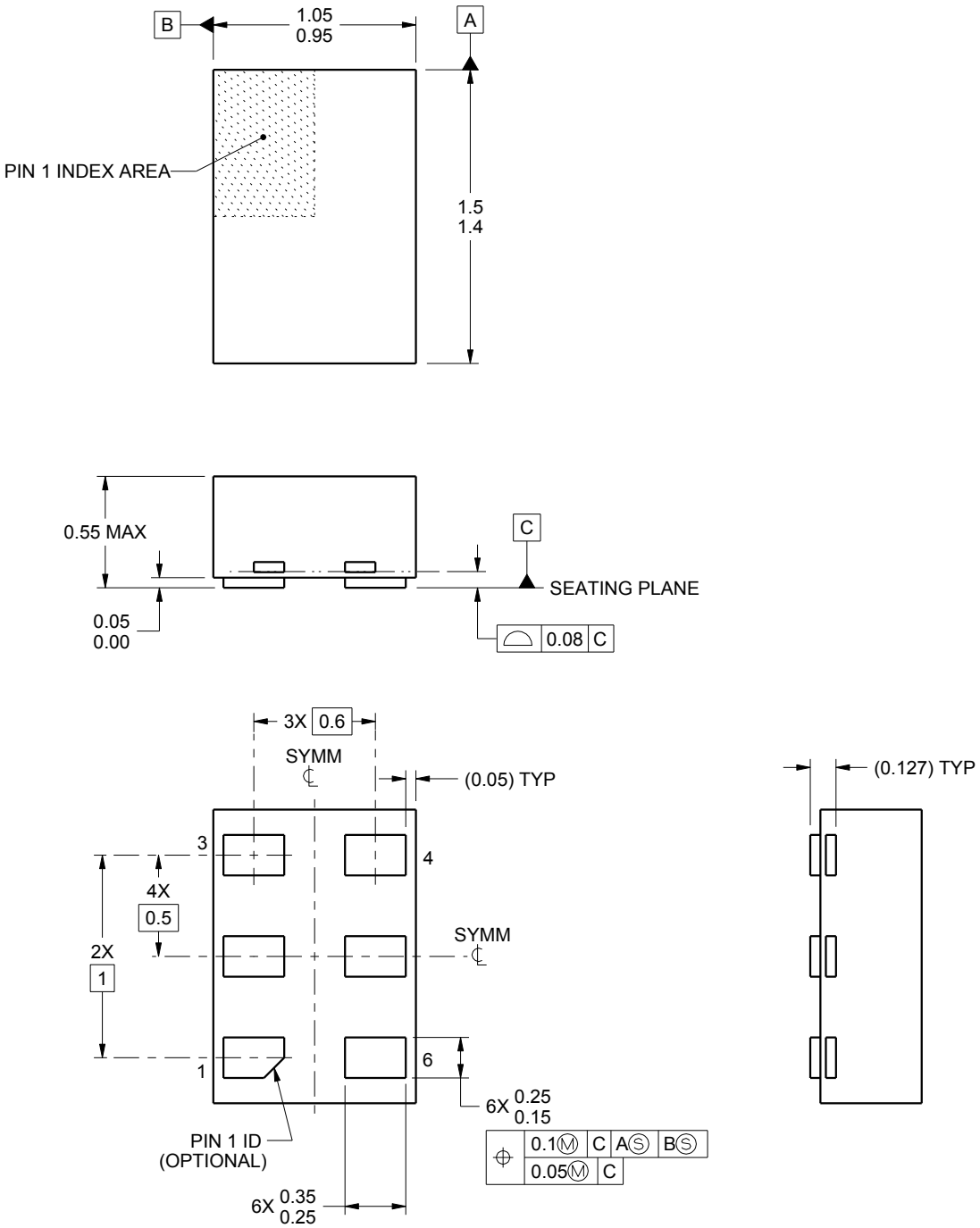
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DRY0006B

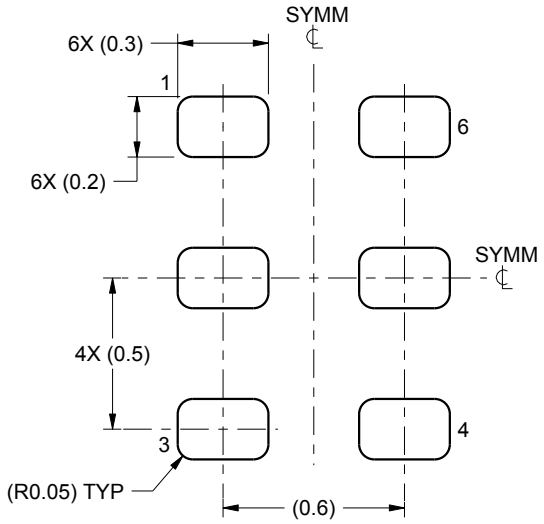
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

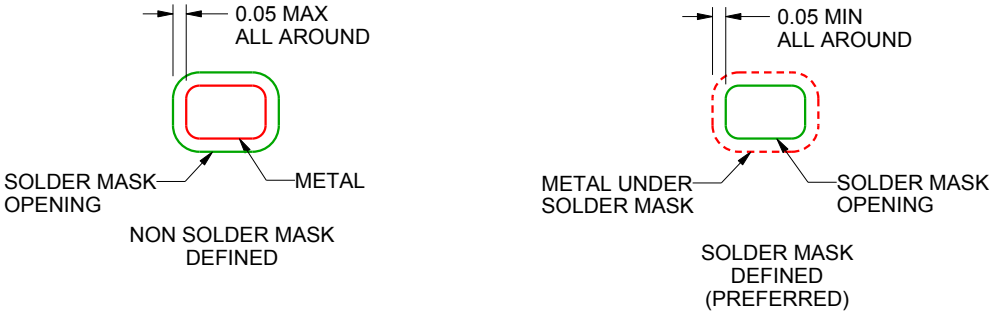


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X

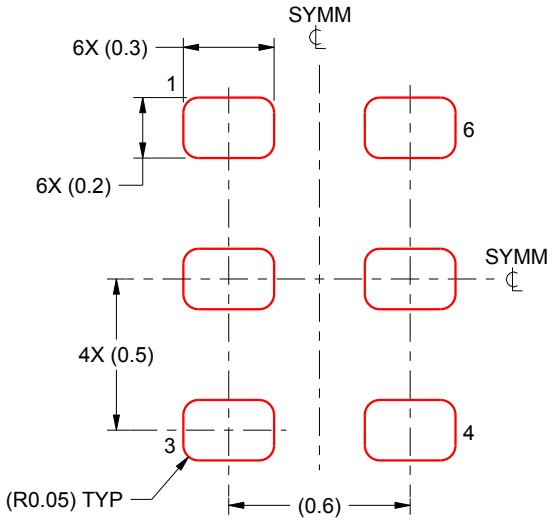


SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

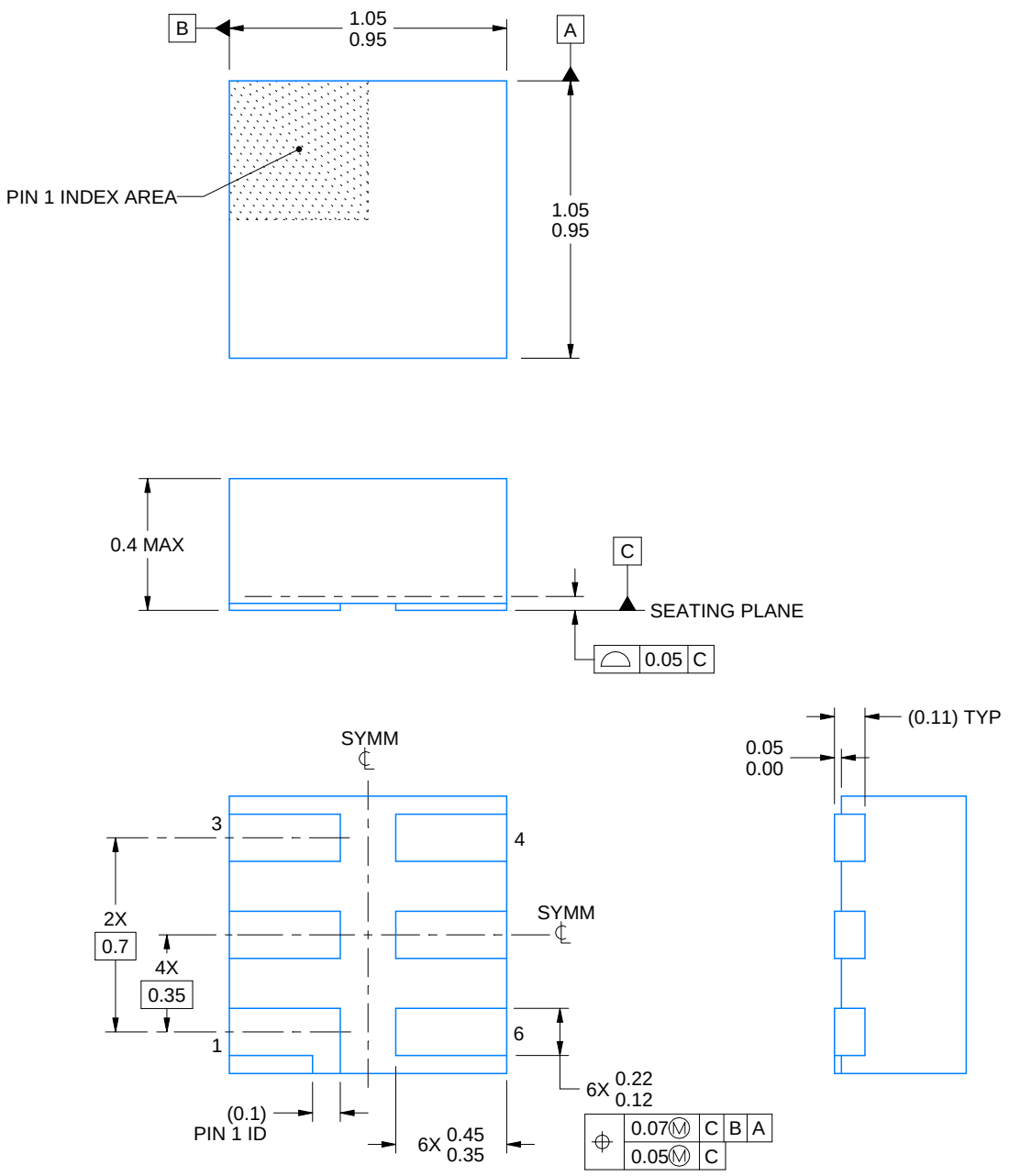
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

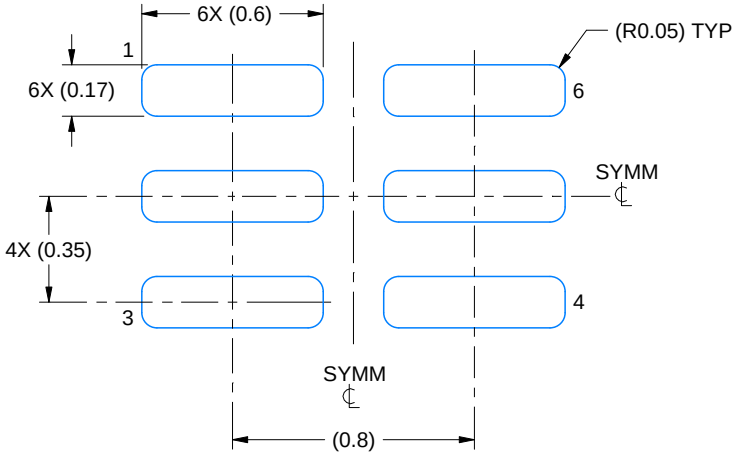
PLASTIC SMALL OUTLINE - NO LEAD



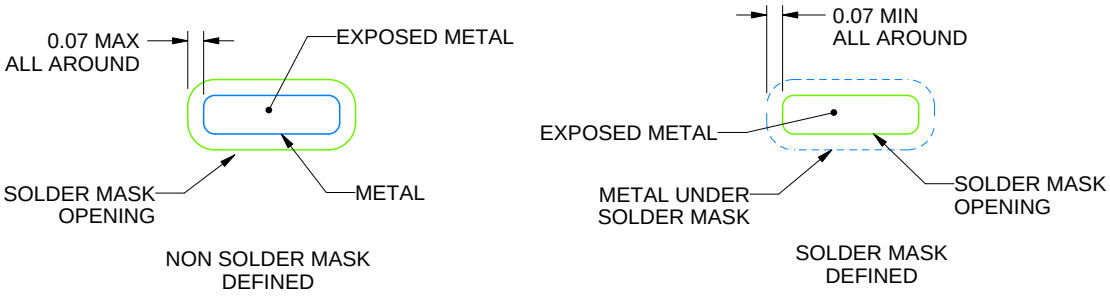
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

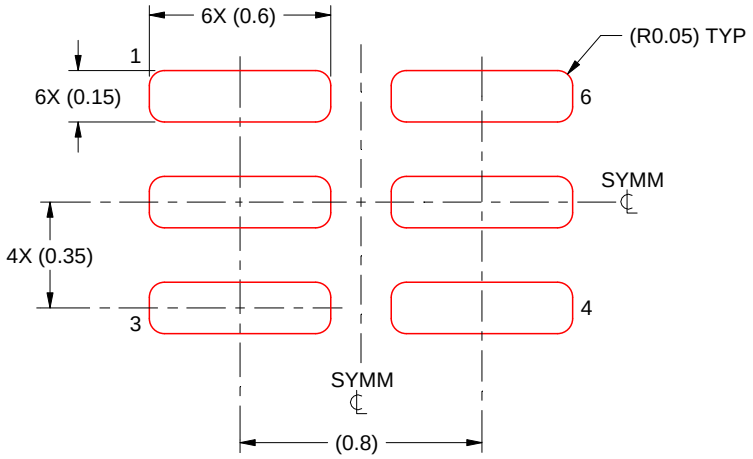
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

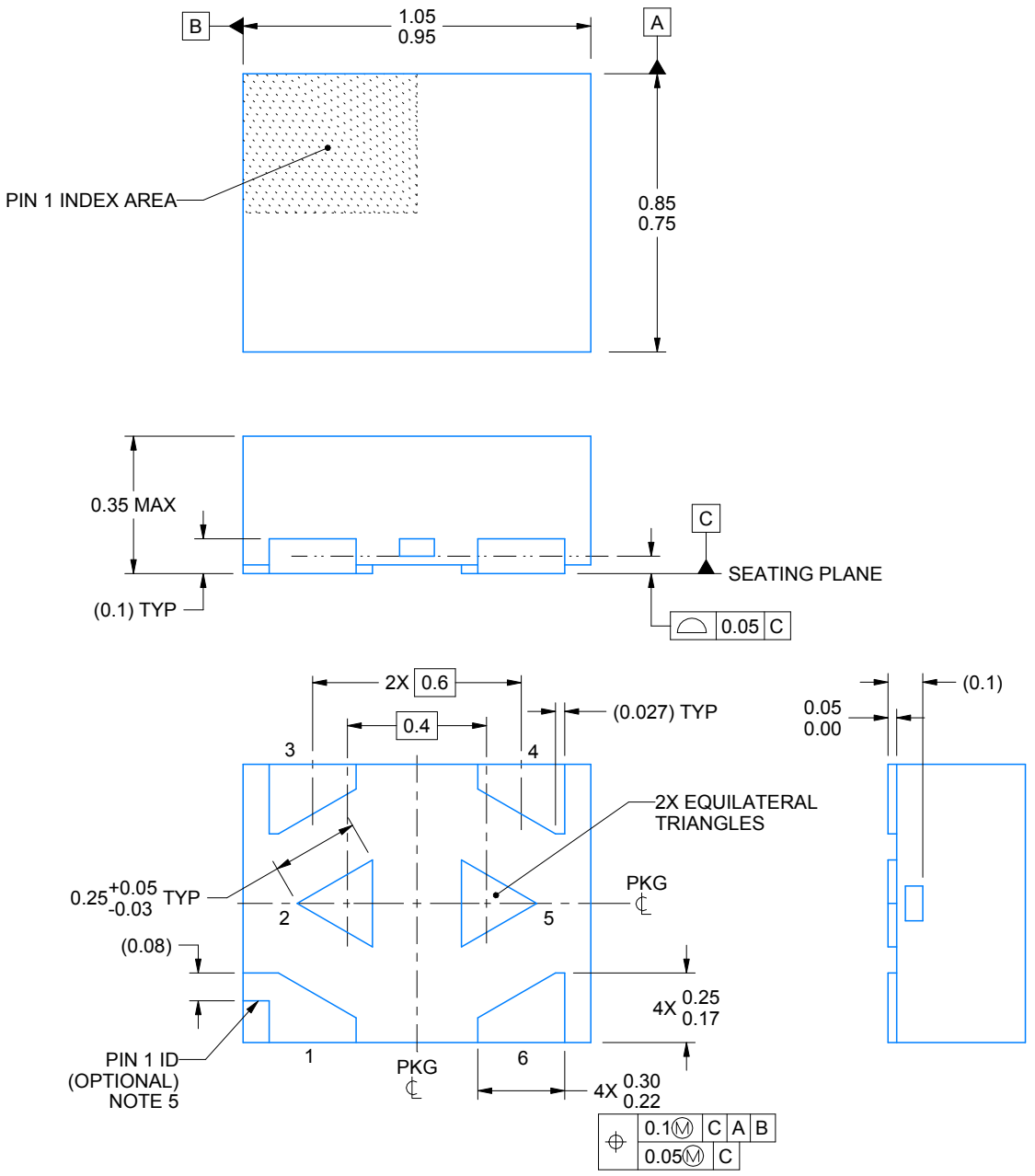
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DTB0006A

PACKAGE OUTLINE

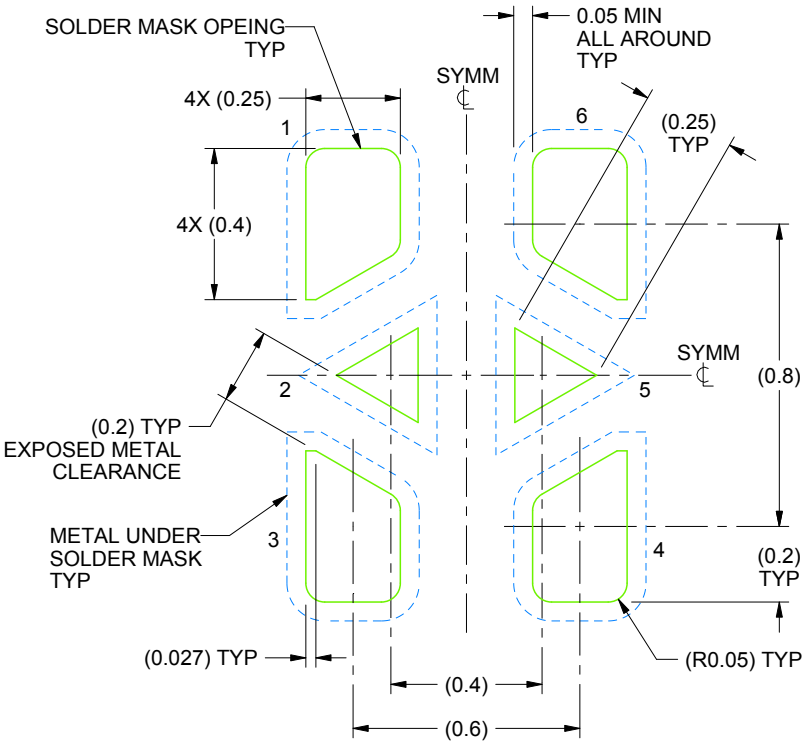
X2SON - 0.35 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

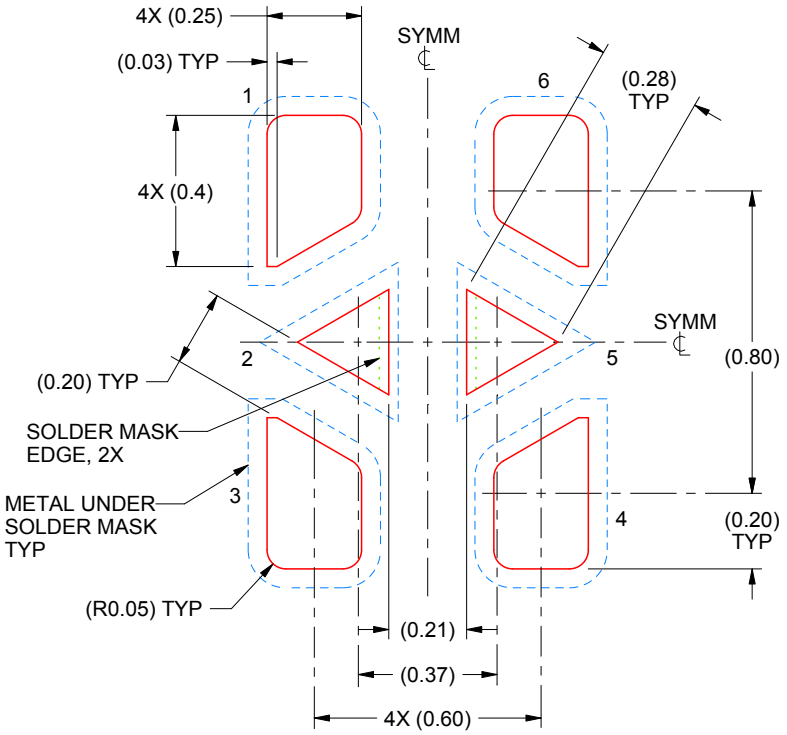


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4223406/C 02/2019

NOTES: (continued)

6. This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.07 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

4223406/C 02/2019

NOTES: (continued)

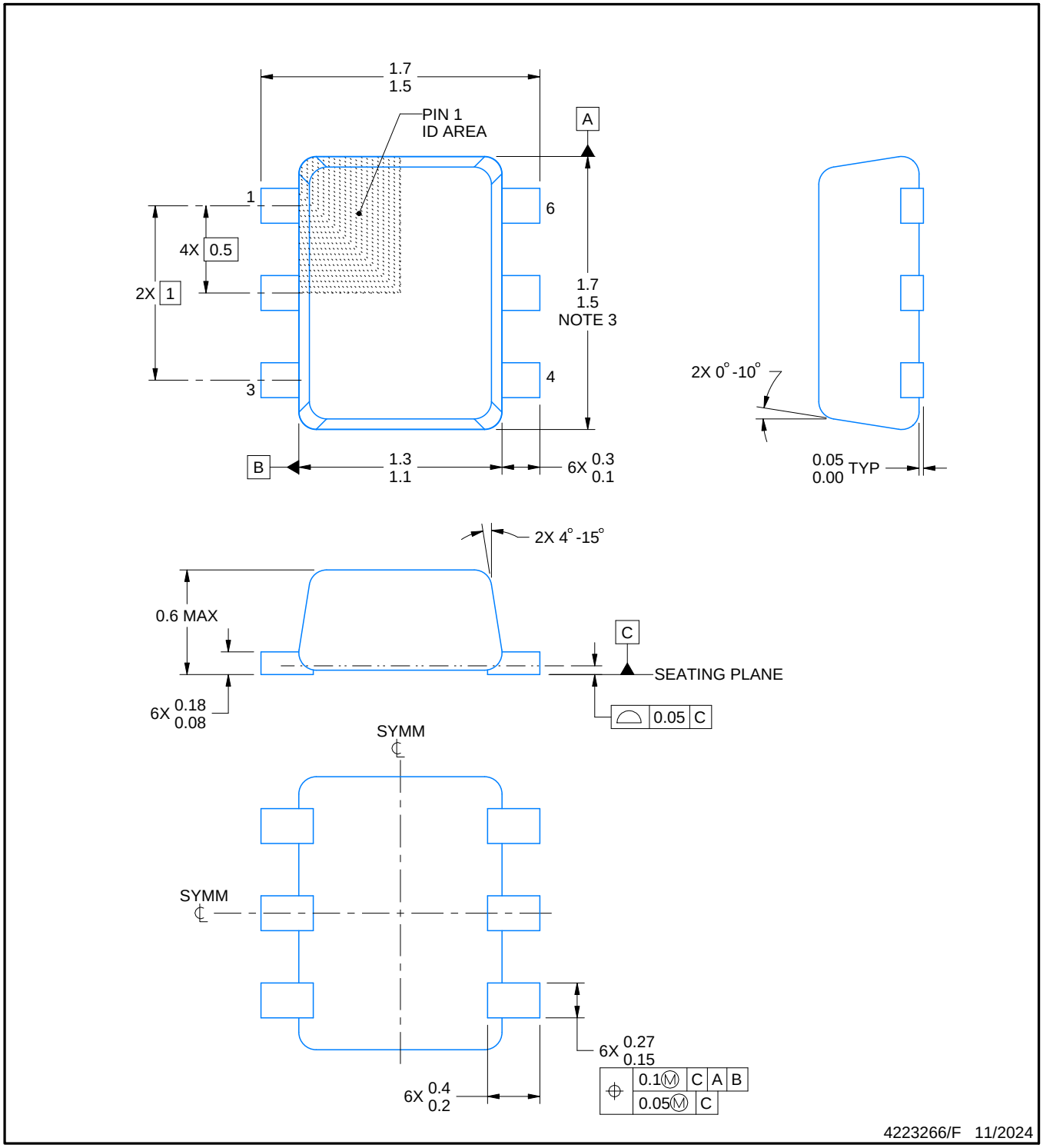
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

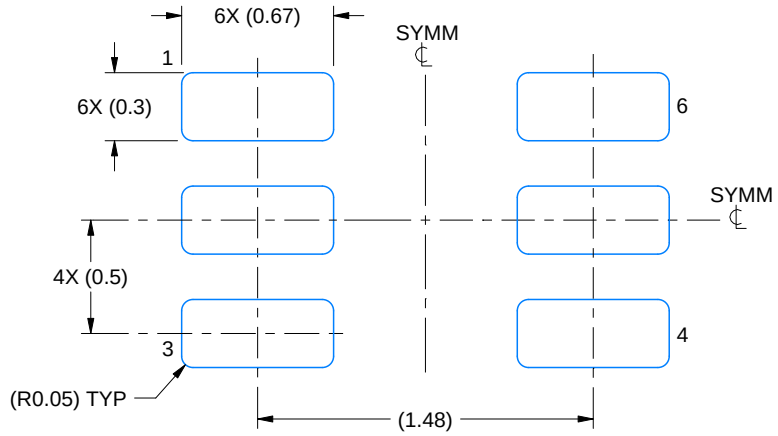
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

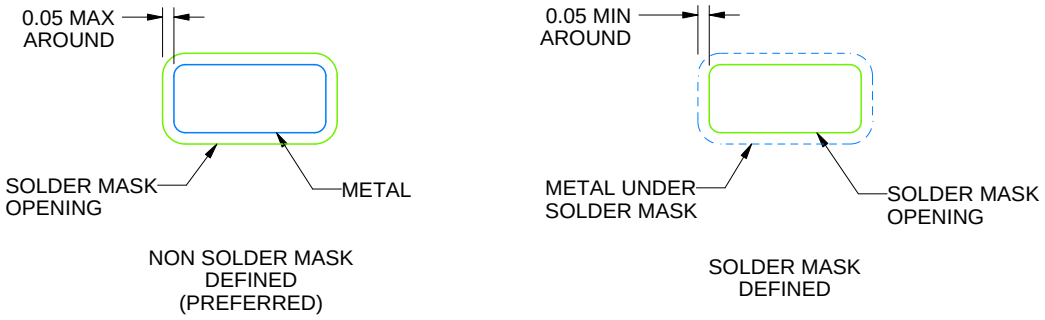
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

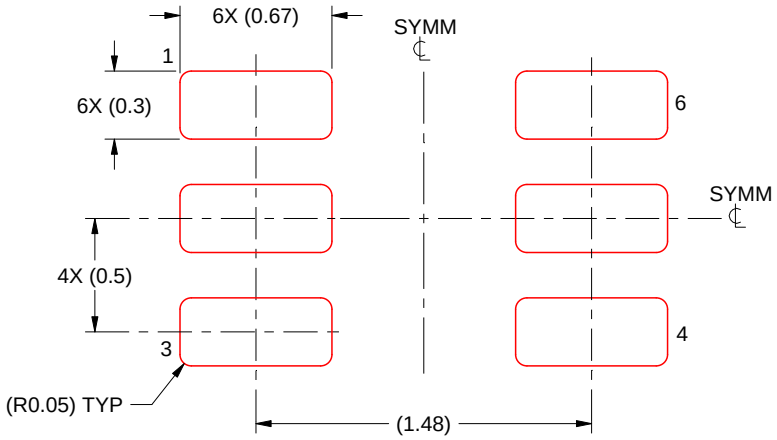
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

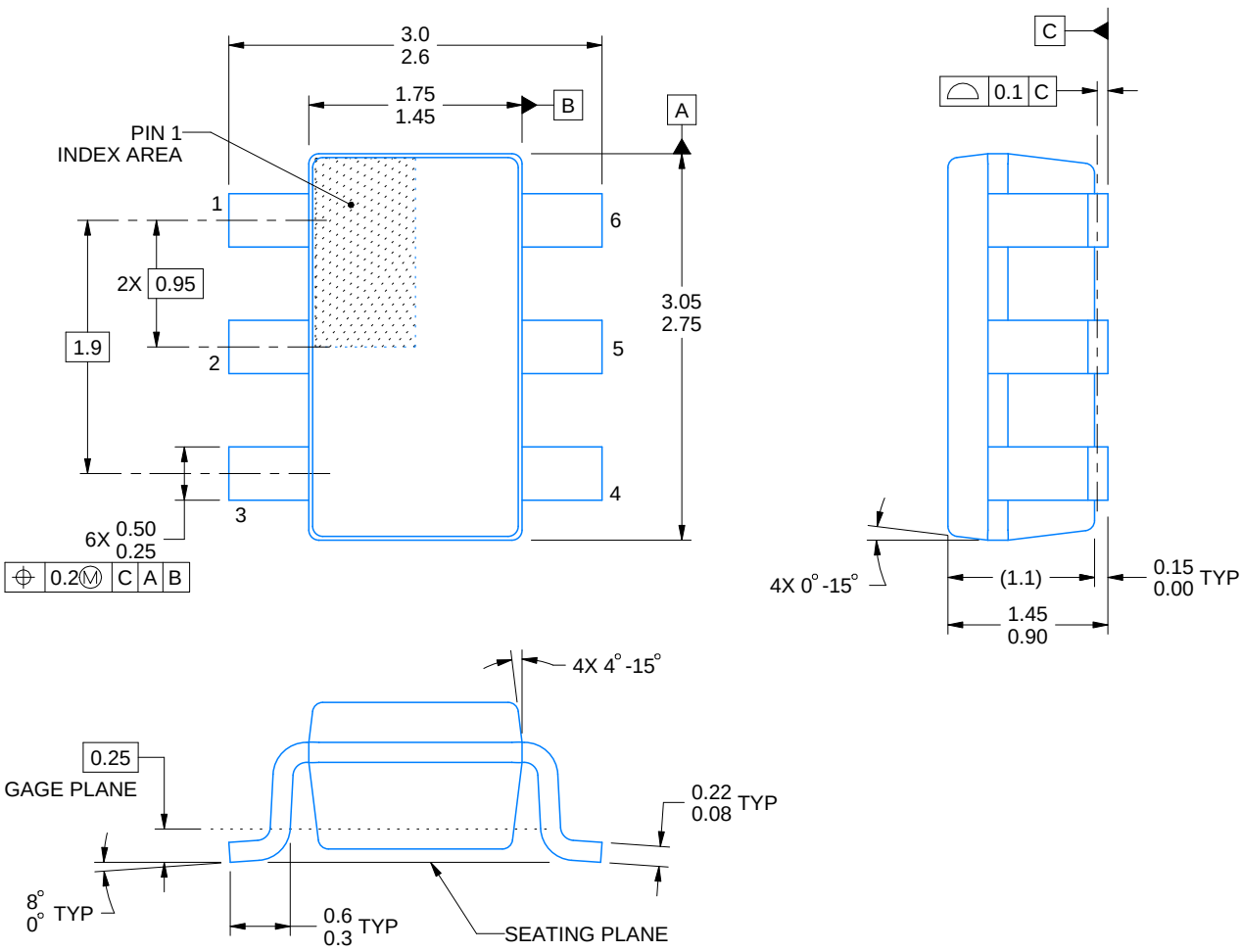
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

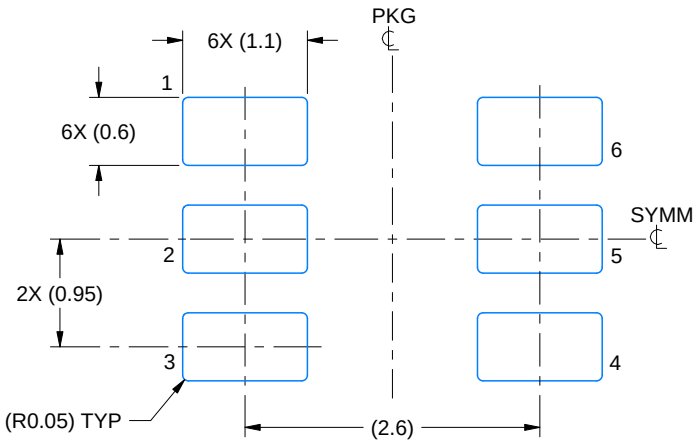
SMALL OUTLINE TRANSISTOR



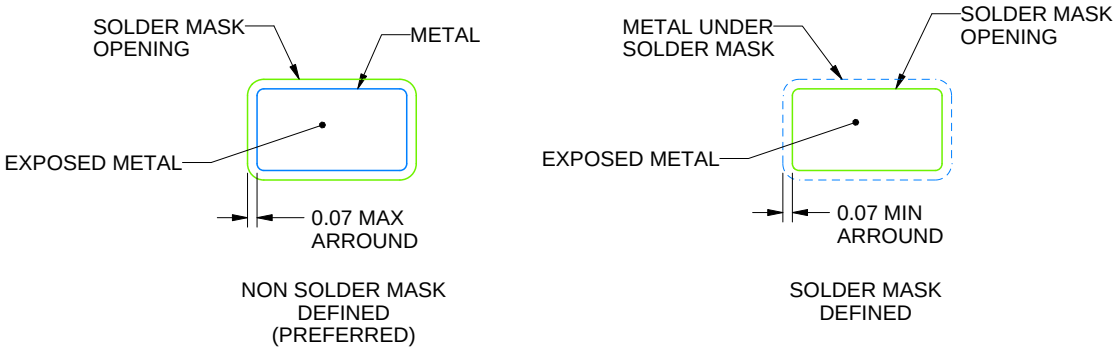
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

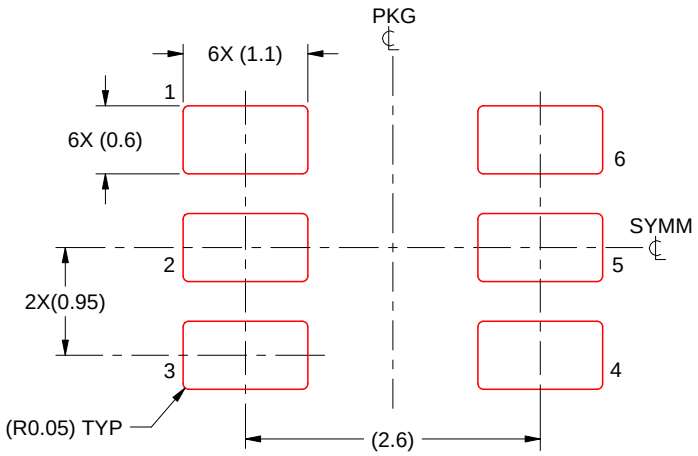


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

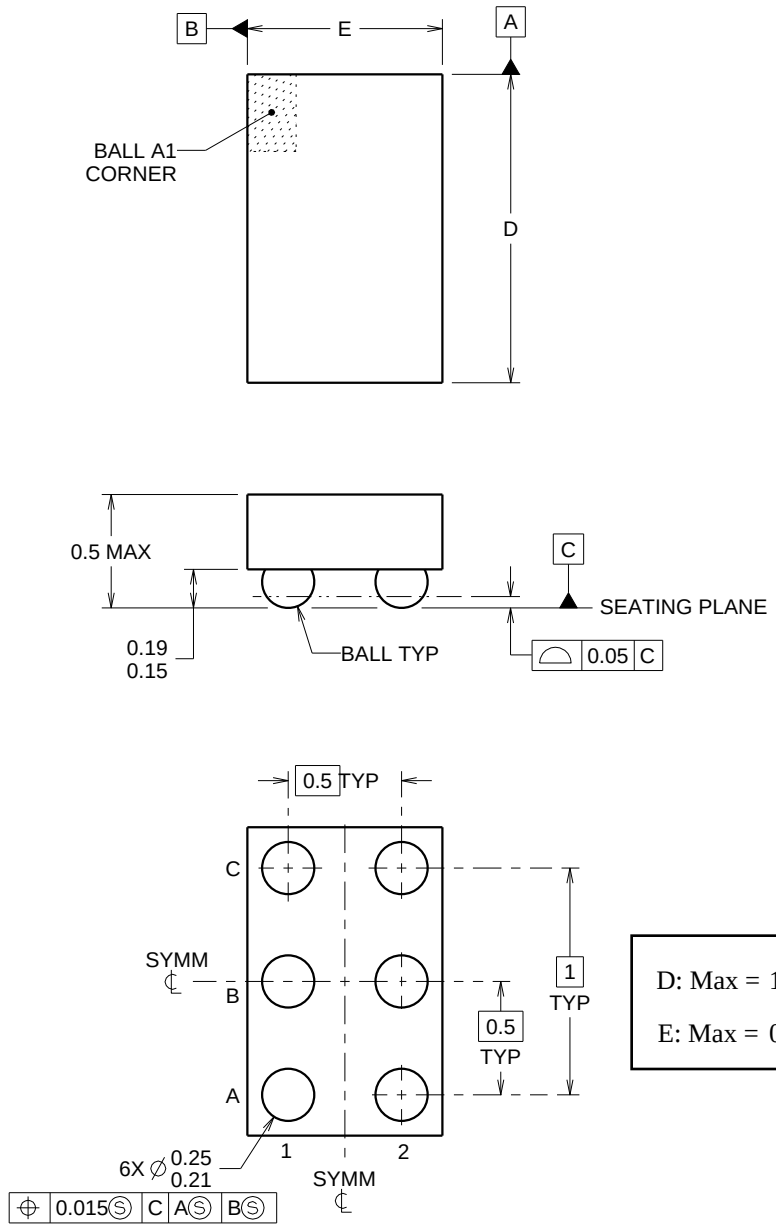
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.357 mm

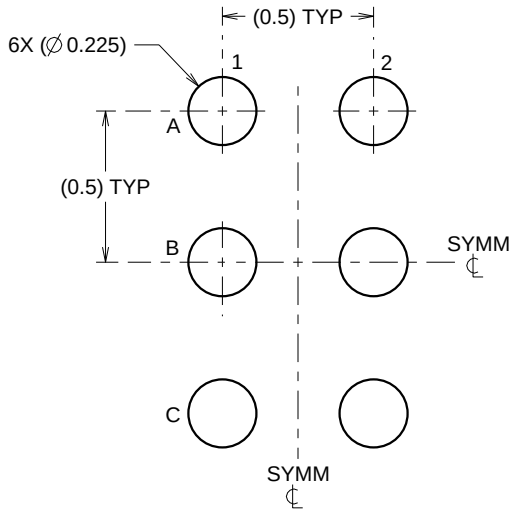
E: Max = 0.918 mm, Min =0.857 mm

4219524/A 06/2014

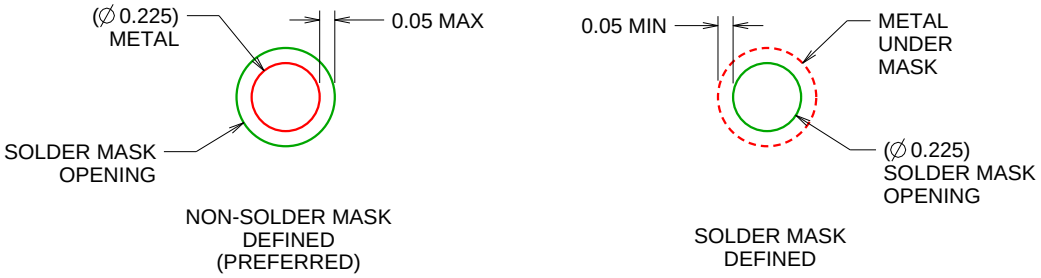
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

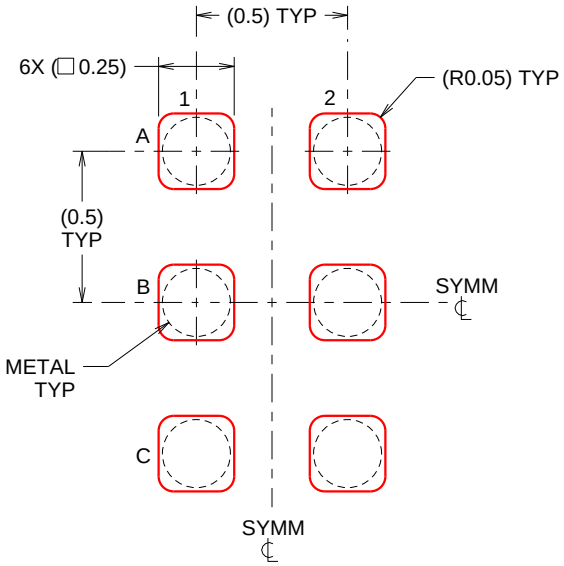
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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最后更新日期：2025 年 10 月