

SNx4LVC32A 四通道双输入正或门

1 特性

- 工作电压范围为 1.65V 至 3.6V
- 额定温度范围为 -40°C 至 $+85^{\circ}\text{C}$ 、 -40°C 至 $+125^{\circ}\text{C}$ 以及 -55°C 至 $+125^{\circ}\text{C}$
- 输入电压高达 5.5V
- 3.3V 时, t_{pd} 最大值为 3.8ns
- V_{OLP} (输出接地反弹) 典型值小于 0.8V ($V_{CC} = 3.3\text{V}$ 、 $T_A = 25^{\circ}\text{C}$ 时)
- V_{OHV} (输出 V_{OH} 下冲) 典型值大于 2V ($V_{CC} = 3.3\text{V}$ 、 $T_A = 25^{\circ}\text{C}$ 时)
- 闩锁性能超过 250mA, 符合 JESD 17 规范
- 对于符合 MIL-PRF-38535 标准的产品, 所有参数均经过测试, 除非另外注明。对于所有其他产品, 生产流程不一定包含对所有参数的测试。
- ESD 保护性能超过 JESD 22 规范要求
 - 2000V 人体放电模型
 - 1000V 充电器件模型

2 应用

- AV 接收器
- 音频接口盒: 便携
- 蓝光播放器与家庭影院
- MP3 播放器或录像机
- 个人数字助理 (PDA)
- 电源: 电信/服务器 交流/直流电源: 一个 控制器: 模拟和数字
- 固态硬盘 (SSD): 客户端和企业级
- 电视: LCD 电视、数字电视和高清电视 (HDTV)
- 平板电脑: 企业级
- 视频分析: 服务器
- 无线耳机、键盘和鼠标

3 说明

SN54LVC32A 四通道双输入正或门旨在 2.7V 至 3.6V V_{CC} 下运行, SN74LVC32A 四通道双输入正或门旨在 1.65V 至 3.6V V_{CC} 下运行。

SNx4LVC32A 器件以正逻辑执行布尔函数 $Y = A + B$ 或 $Y = \overline{A} \cdot \overline{B}$ 。

输入可以由 3.3V 或 5V 器件驱动。此功能允许在 3.3V/5V 的混合系统环境中将此类器件用作转换器。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
SNx4LVC32A	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.91mm
	DB (SSOP, 14)	6.2mm × 7.8mm	6.20mm × 5.30mm
	NS (SOP, 14)	10.2mm × 7.8mm	10.30mm × 5.30mm
	PW (TSSOP, 14)	5mm × 6.4mm	5.00mm × 4.40mm
	RGY (VQFN, 14)	3.50mm × 3.50mm	3.50mm × 3.50mm
	FK (LCCC, 20)	8.9mm × 8.9mm	8.9mm × 8.9mm
	J (CDIP, 14)	19.55mm × 7.9mm	19.55mm × 6.7mm
W (CFP, 14)	9.21mm × 9mm	9.21mm × 6.28mm	

- (1) 有关更多信息, 请参阅第 11 节。
- (2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。
- (3) 本体尺寸 (长 × 宽) 为标称值, 不包括引脚。

简化原理图

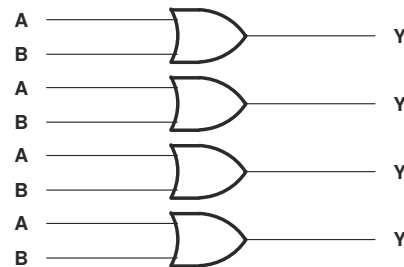


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4 Pin Configuration and Functions

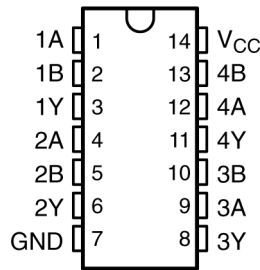


图 4-1. SN54LVC32A J 或 W 封装, 14-引脚 (顶视图)

SN74LVC32A D, DB, NS, 或 PW 封装, 14-引脚
CDIP, CFP, SOIC, SSOP, SOP, TSSOP (顶视图)

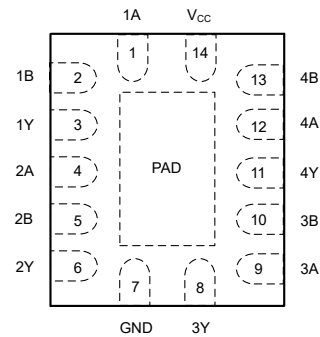


图 4-2. SN74LVC32A RGY 或 BQA 封装, 14-引脚 VQFN 或 WQFN (顶视图)

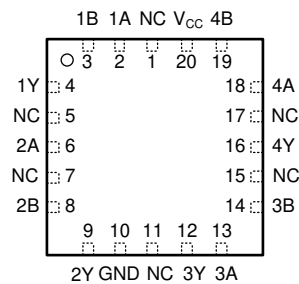


图 4-3. SN54LVC32A FK 封装, 20-引脚 LCCC (顶视图)

表 4-1. Pin Functions

NAME	PIN				TYPE	DESCRIPTION
	SN74LVC32A		SN54LVC32A			
	D, DB, NS, PW	BQA, RGY	J, W	FK		
1A	1	1	1	2	I	Gate 1 input
1B	2	2	2	3	I	Gate 1 input
1Y	3	3	3	4	O	Gate 1 output
2A	4	4	4	6	I	Gate 2 input
2B	5	5	5	8	I	Gate 2 input
2Y	6	6	6	9	O	Gate 2 output
GND	7	7	7	10	—	Ground Pin
3Y	8	8	8	12	O	Gate 3 output
3A	9	9	9	13	I	Gate 3 input
3B	10	10	10	14	I	Gate 3 input
4Y	11	11	11	16	O	Gate 4 output
4A	12	12	12	18	I	Gate 4 input
4B	13	13	13	19	I	Gate 4 input
V _{CC}	14	14	14	20	—	Power Pin
NC	—	—	—	1, 5, 7, 11, 15, 17	—	No Connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	6.5	V
V _I	Input voltage ⁽²⁾		-0.5	6.5	V
V _O	Output voltage ^{(2) (3)}		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND			±100	mA
P _{tot}	Power dissipation	T _A = -40°C to +125°C ^{(4) (5)}		500	mW
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* tables.
- (4) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
- (5) For the DB, DGV, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions, SN54LVC32A

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN54LVC32A		UNIT
		–55 to +125°C		
		MIN	MAX	
V _{CC}	Supply voltage	Operating		V
		Data retention only		
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		V
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2.7 V		mA
		V _{CC} = 3 V		
I _{OL}	Low-level output current	V _{CC} = 2.7 V		mA
		V _{CC} = 3 V		
Δt/Δv	Input transition rise and fall rate	7		ns/V

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

5.4 Recommended Operating Conditions, SN74LVC32A

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN74LVC32A						UNIT
		T _A = 25°C		–40 to +85°C		–40 to +125°C		
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	Operating		1.65		3.6		V
		Data retention only		1.5		1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.65 × V _{CC}		0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V		1.7		1.7		
		V _{CC} = 2.7 V to 3.6 V		2		2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V		0.7		0.7		
		V _{CC} = 2.7 V to 3.6 V		0.8		0.8		
V _I	Input voltage	0	5.5	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		–4		–4		mA
		V _{CC} = 2.3 V		–8		–8		
		V _{CC} = 2.7 V		–12		–12		
		V _{CC} = 3 V		–24		–24		
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4		4		mA
		V _{CC} = 2.3 V		8		8		
		V _{CC} = 2.7 V		12		12		
		V _{CC} = 3 V		24		24		
Δt/Δv	Input transition rise and fall rate	7		7		7		ns/V

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC32A						UNIT
	BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R _{θJA} Junction-to-ambient thermal resistance	102.3	127.8	140.4	123.8	150.8	92.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Electrical Characteristics, SN54LVC32A

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC32A		UNIT
			–55 to +125°C		
			MIN	MAX	
V _{OH}	I _{OH} = –100 μA	2.7 V to 3.6 V	V _{CC} – 0.2		V
	I _{OH} = –12 mA	2.7 V	2.2		
	I _{OH} = –24 mA	3 V	2.4		
V _{OL}	I _{OL} = 100 μA	2.7 V to 3.6 V	0.2		V
	I _{OL} = 12 mA	2.7 V	0.4		
	I _{OL} = 24 mA	3 V	0.55		
I _I	V _I = 5.5 V or GND	3.6 V	±5		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10		μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500		μA

5.7 Electrical Characteristics, SN74LVC32A

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LVC32A						UNIT	
			T _A = 25°C			–40 to +85°C		–40 to +125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
V _{OH}	I _{OH} = –100 μA	1.65 V to 3.6 V	V _{CC} – 0.2			V _{CC} – 0.2		V _{CC} – 0.3		V
	I _{OH} = –4 mA	1.65 V	1.29			1.2		1.05		
	I _{OH} = –8 mA	2.3 V	1.9			1.7		1.55		
	I _{OH} = –12 mA	2.7 V	2.2			2.2		2.05		
		3 V	2.4			2.4		2.25		
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V				0.1		0.2		V
	I _{OL} = 4 mA	1.65 V				0.24		0.45		
	I _{OL} = 8 mA	2.3 V				0.3		0.7		
	I _{OL} = 12 mA	2.7 V				0.4		0.4		
	I _{OL} = 24 mA	3 V				0.55		0.55		
I _I	V _I = 5.5 V or GND	3.6 V				±1		±5		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V				1		10		μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V				500		500		μA

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LVC32A						UNIT	
			T _A = 25°C			–40 to +85°C		–40 to +125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
C _i	V _I = V _{CC} or GND	3.3 V	5						pF	

5.8 Switching Characteristics, SN54LVC32A

over operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN54LVC32A		UNIT
				–55 to +125°C		
				MIN	MAX	
t _{pd}	A or B	Y	2.7V	4.4		ns
			3.3V ± 0.3V	1	3.8	

5.9 Switching Characteristics, SN74LVC32A

over operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN74LVC32A						UNIT	
				T _A = 25°C			–40 to +85°C		–40 to +125°C		
				MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{pd}	A or B	Y	1.8V ± 0.15V	1	4.2	8.2	1	8.7	1	10.2	ns
			2.5V ± 0.2V	1	2.6	4.9	1	5.4	1	6.9	
			2.7V	1	3	4.2	1	4.4	1	5.5	
			3.3V ± 0.3V	1	2.5	3.6	1	3.8	1	5	
t _{sk(o)}			3.3V ± 0.3V				1		1.5	ns	

5.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	f = 10 MHz	1.8V	7.5	pF
			2.5V	10.6	
			3.3V	12.5	

5.11 Typical Characteristics

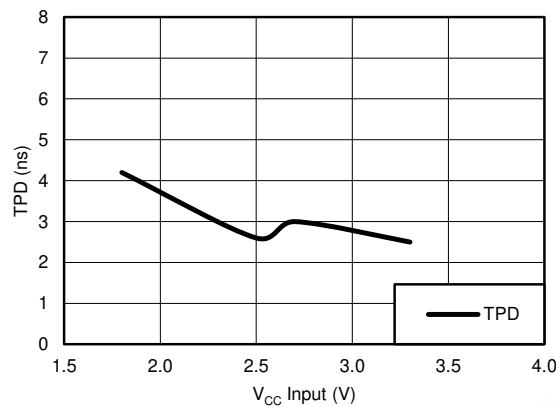
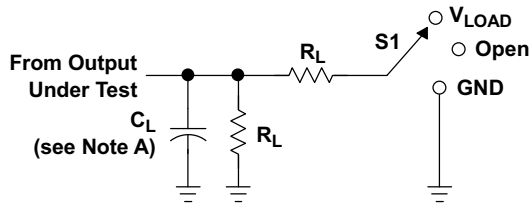


图 5-1. TPD vs V_{CC} (T_A = 25°C)

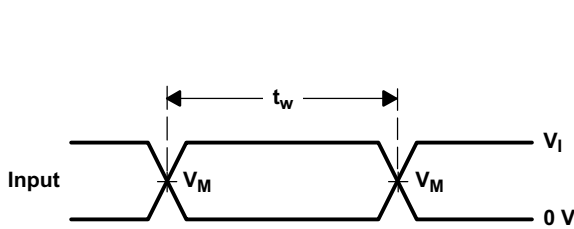
6 Parameter Measurement Information



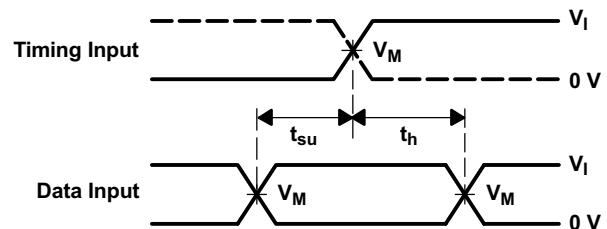
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

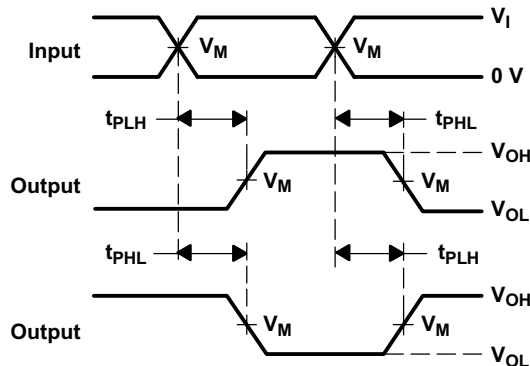
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



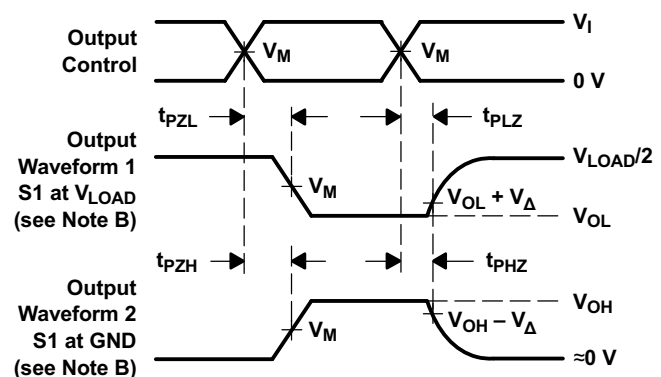
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN54LVC32A quadruple 2-input positive-OR gate is designed for 2-V to 3.6-V V_{CC} operation, and the SN74LVC32A quadruple 2-input positive-OR gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The SNx4LVC32A devices perform the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as down-translators in a mixed 3.3-V/5-V system environment.

7.2 Functional Block Diagram



Logic Diagram, Each Gate (Positive Logic)

7.3 Feature Description

- Wide operating voltage range
 - Operates from 1.65 V to 3.6 V
- Allows up or down voltage translation
 - Inputs accept voltages to 5.5 V

7.4 Device Functional Modes

表 7-1 lists the functional modes of SNx4LVC32A.

表 7-1. Function Table
(Each Gate)

INPUTS		OUTPUT Y
A	B	
H	X	H
X	H	H
L	L	L

Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

1 Application Information

SN74LVC32A device is a high-drive, CMOS device that can be used for a multitude of buffer-type functions. It can produce 24 mA of drive current at 3 V. Therefore, this device is ideal for driving multiple inputs and for high-speed applications up to 100 MHz. The inputs and outputs are 5.5-V tolerant allowing the device to translate down to V_{CC} .

2 Typical Application

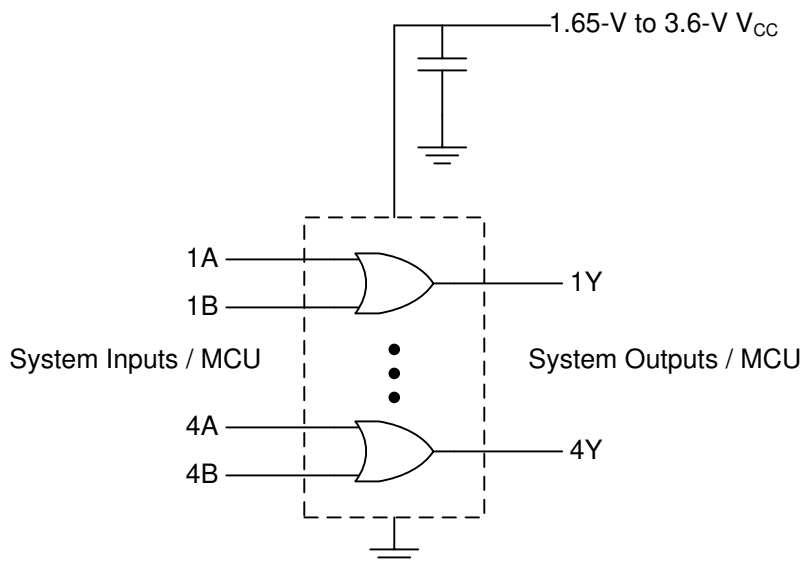


图 8-1. Typical OR Gate Application and Supply Voltage

2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

2.2 Detailed Design Procedure

- Recommended Input Conditions
 - Rise time and fall time specs: See $(\Delta t/\Delta V)$ in the [§ 5.4](#) table.
 - Specified high and low levels: See $(V_{IH}$ and $V_{IL})$ in the [§ 5.4](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommended Output Conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above 5.5 V.

2.3 Application Curve

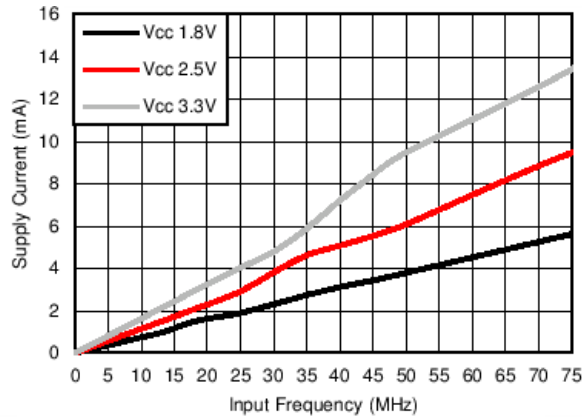


图 8-2. Supply Current vs Input Frequency

Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the 节 5.4 table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended; if there are multiple V_{CC} pins, then 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and a 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

3 Layout

3.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. 节 8.3.2 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

3.2 Layout Example

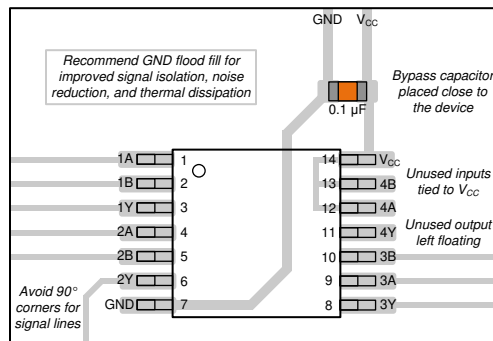


图 8-3. Layout Diagram

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC32A	Click here	Click here	Click here	Click here	Click here
SN74LVC32A	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

8.3.1 Community Resources

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision T (May 2024) to Revision U (July 2024)

Page

- Updated thermal values for D package from RθJA = 86 to 127.8, all values in °C/W6

Changes from Revision S (March 2024) to Revision T (May 2024)

Page

- Updated RθJA values: DB = 96 to 140.4, NS = 76 to 123.8, PW = 113 to 150.8, RGY = 47 to 92.1; Updated DB, NS, PW, and RGY packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W.....6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9761801Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761801Q2A SNJ54LVC32AFK	Samples
5962-9761801QCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761801QC A SNJ54LVC32AJ	Samples
5962-9761801QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761801QD A SNJ54LVC32AW	Samples
SN74LVC32ABQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC32A	Samples
SN74LVC32AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC32A	Samples
SN74LVC32ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	Samples
SN74LVC32ADBRG4	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	Samples
SN74LVC32ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC32A	Samples
SN74LVC32ADRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC32A	Samples
SN74LVC32ADT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC32A	Samples
SN74LVC32ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC32A	Samples
SN74LVC32APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	Samples
SN74LVC32APWE4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	Samples
SN74LVC32APWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	Samples
SN74LVC32APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LC32A	Samples
SN74LVC32APWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	Samples
SN74LVC32APWRG3	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LC32A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC32APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	Samples
SN74LVC32APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	Samples
SN74LVC32ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC32A	Samples
SNJ54LVC32AFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9761801Q2A SNJ54LVC 32AFK	Samples
SNJ54LVC32AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761801QC A SNJ54LVC32AJ	Samples
SNJ54LVC32AW	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761801QD A SNJ54LVC32AW	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVC32A, SN74LVC32A :

- Catalog : [SN74LVC32A](#)

- Automotive : [SN74LVC32A-Q1](#), [SN74LVC32A-Q1](#)

- Enhanced Product : [SN74LVC32A-EP](#), [SN74LVC32A-EP](#)

- Military : [SN54LVC32A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC32ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC32ADBDR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC32ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC32ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC32ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC32APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC32APWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC32APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC32APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC32ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC32ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC32ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LVC32ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LVC32ADT	SOIC	D	14	250	210.0	185.0	35.0
SN74LVC32ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LVC32APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC32APWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC32APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC32APWT	TSSOP	PW	14	250	356.0	356.0	35.0
SN74LVC32ARGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9761801Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9761801QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LVC32AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC32APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC32APWE4	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC32APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54LVC32AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LVC32AW	W	CFP	14	25	506.98	26.16	6220	NA



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

GENERIC PACKAGE VIEW

BQA 14

WQFN - 0.8 mm max height

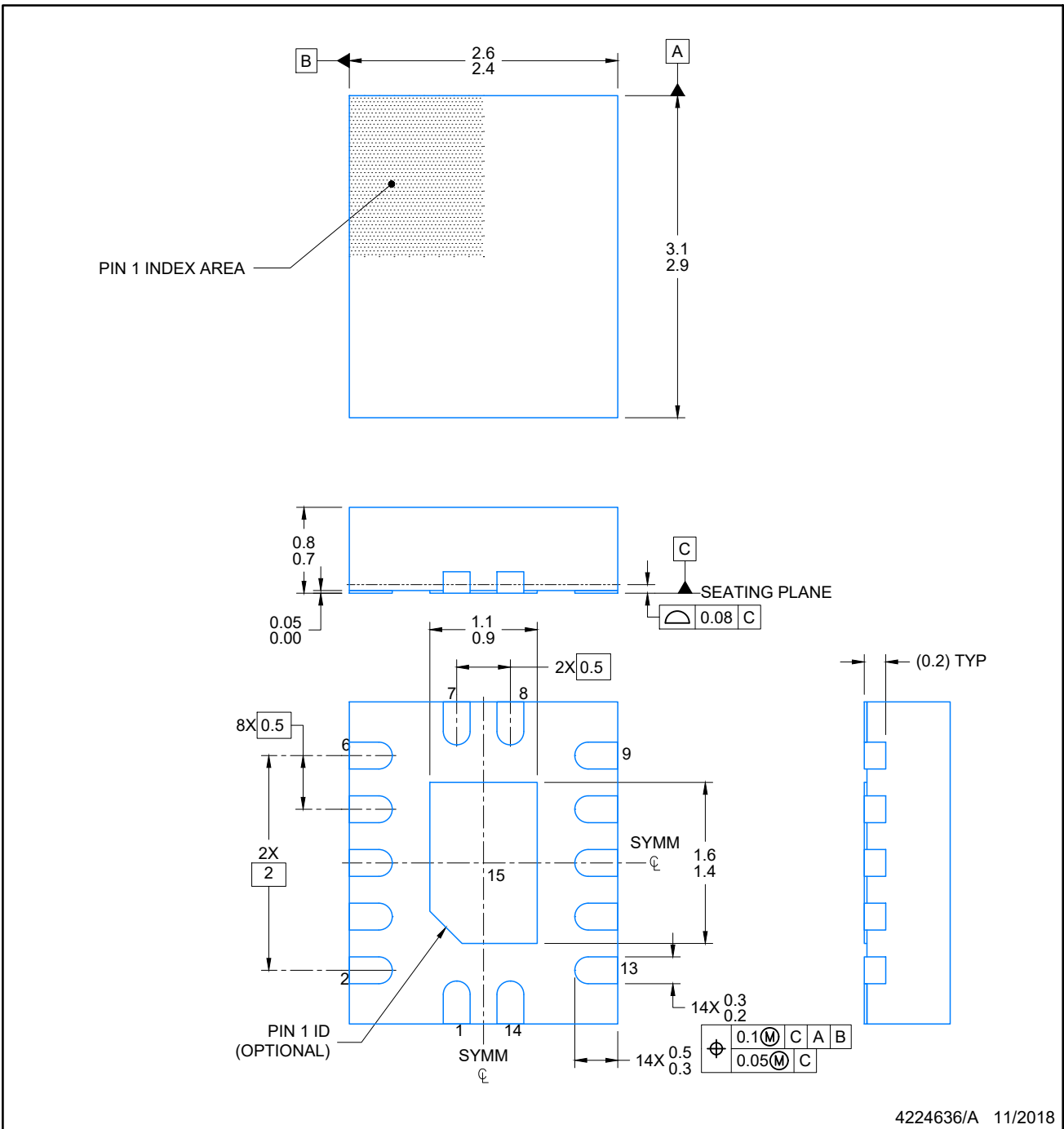
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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