SNx4LVC74A 具有清零和预设功能的双通道正边沿触发式 D 型触发器

1 特性

- 工作电压范围为 1.65V 至 3.6V
- 输入电压高达 5.5V
- 3.3V 时，t_{pd} 最大值为 5.2ns
- V_{OLP}（输出接地反弹）典型值 <0.8V（V_{CC} = 3.3V、T_A = 25°C）
- V_{OHV}（输出 V_{OH} 下冲）典型值 >2V（V_{CC} = 3.3V、T_A = 25°C）
- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 1000V 充电器件模型 (C101)

2 应用

- 服务器
- 医疗、保健与健身
- 电信基础设施
- 电视、机顶盒和音频
- 测试和测量
- 工业运输
- 无线基础设施
- 企业交换
- 电机驱动器
- 工厂自动化与控制

3 说明

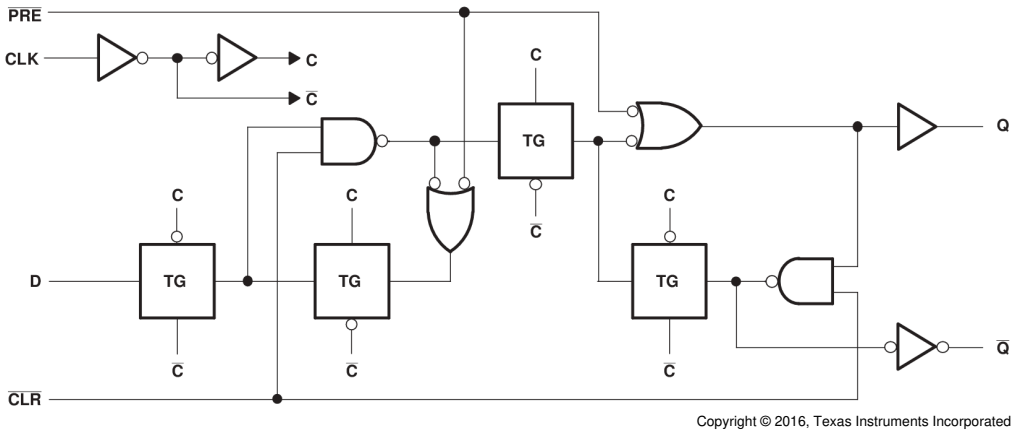
SNx4LVC74A 器件在一个器件中便捷地集成了两个正边沿触发式 D 型触发器。

SN54LVC74A 可在 2.7V 至 3.6V V_{CC} 下运行，SN74LVC74A 可在 1.65V 至 3.6V V_{CC} 下运行。

器件信息

器件型号	封装 (1)	封装尺寸(2)	本体尺寸(3)
SNx4LVC74A	BQA（WQFN，14）	3mm × 2.5mm	3mm × 2.5mm
	D（SOIC，14）	8.65mm x 6mm	8.65mm × 3.91mm
	DB（SSOP，14）	6.2mm x 7.8mm	6.20mm × 5.30mm
	NS（SOP，14）	10.2mm x 7.8mm	10.20mm × 5.30mm
	PW（TSSOP，14）	5mm x 6.4mm	5.00mm × 4.40mm
	RGY（VQFN，14）	3.50mm × 3.50mm	3.50mm × 3.50mm
	J（CDIP，14）	19.55mm x 7.9mm	19.56mm × 6.67mm
	W（CFP，14）	9.21mm x 9 mm	9.21mm × 5.97mm
	FK（LCCC，20）	8.9mm x 8.9mm	8.89mm × 8.89mm

(1) 如需了解更多信息，请参阅机械、封装和可订购信息。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 x 宽）为标称值，不包括引脚。



展示各触发器的逻辑图（正逻辑）

内容

4 引脚配置和功能

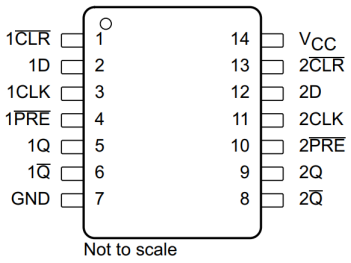


图 4-1. D、DB、J、PW、NS 或 W 封装 14 引脚 SOIC、SSOP、CDIP、TSSOP、SO 或 CFP（顶视图）

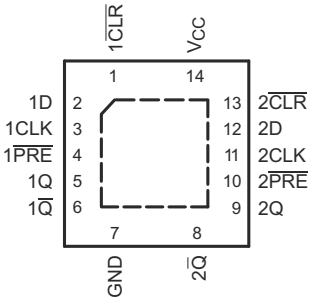


图 4-2. BQA 或 RGY 封装 14 引脚 WQFN 或 VQFN，带外露散热焊盘（顶视图）

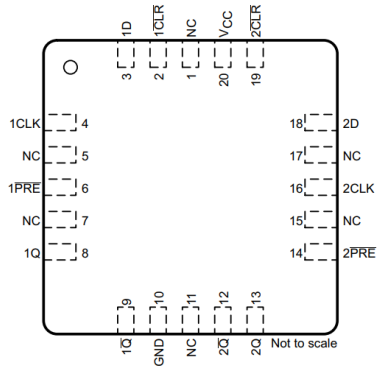


图 4-3. FK 封装 20 引脚 LCCC（顶视图）

表 4-1. 引脚功能

引脚			I/O	说明
名称	CDIP、CFP、PDIP、SO、SOIC、SSOP、TSSOP、VQFN	LCCC		
1CLK	3	4	I	通道 1 时钟输入
1 $\overline{CLR}$	1	2	I	通道 1 清零输入。拉低可将 Q 输出设置为低电平。
1D	2	3	I	通道 1 数据输入
1 $\overline{PRE}$	4	6	I	通道 1 预设输入。拉低可将 Q 输出设置为高电平。
1Q	5	8	O	通道 1 输出
1 $\overline{Q}$	6	9	O	通道 1 反相输出
2CLK	11	16	I	通道 2 时钟输入
2 $\overline{CLR}$	13	19	I	通道 2 清零输入。拉低可将 Q 输出设置为低电平。
2D	12	18	I	通道 2 数据输入
2 $\overline{PRE}$	10	14	I	通道 2 预设输入。拉低可将 Q 输出设置为高电平。
2Q	9	13	O	通道 2 输出
2 $\overline{Q}$	8	12	O	通道 2 反相输出
GND	7	10	—	地
NC	—	1、5、7、11、15、17	—	无连接
V_{CC}	14	20	—	电源

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

		最小值	最大值	单位
电源电压，V_{CC}		-0.5	6.5	V
输入电压，V_I (2)		-0.5	6.5	V
输出电压，V_O (2) (3)		-0.5	V_{CC} + 0.5	V
输入钳位电流，I_{IK}	V_I < 0		-50	mA
输出钳位电流，I_{OK}	V_O < 0		-50	mA
持续输出电流，I_O			±50	mA
通过 V_{CC} 或 GND 的持续电流			±100	mA
贮存温度，T_{stg}		-65	150	°C

(1) 应力超出*绝对最大额定值*下所列的值可能会对器件造成永久损坏。这些列出的值仅仅是应力等级，这并不表示器件在这些条件下以及在*建议运行条件*以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，则可能会超过输入和输出负电压额定值。
(3) V_{CC} 的值在*建议运行条件*表中提供。

5.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准(1)	±2000	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101(2)	±1000	

(1) JEDEC 文档 JEP155 指出：500V HBM 能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 能够在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

请参阅(1)

				最小值	最大值	单位
V_{CC}	电源电压	运行	SN54LVC74A	2	3.6	V
			SN74LVC74A	1.65	3.6	
		仅数据保留		1.5		
V_{IH}	高电平输入电压	V_{CC} = 1.65V 至 1.95V	SN74LVC74A	0.65 × V_{CC}		V
		V_{CC} = 2.3V 至 2.7V	SN74LVC74A	1.7		
		V_{CC} = 2.7V 至 3.6V		2		
V_{IL}	低电平输入电压	V_{CC} = 1.65V 至 1.95V	SN74LVC74A		0.35 × V_{CC}	V
		V_{CC} = 2.3V 至 2.7V	SN74LVC74A		0.7	
		V_{CC} = 2.7V 至 3.6V			0.8	
V_I	输入电压			0	5.5	V
V_O	输出电压			0	V_{CC}	V
I_{OH}	高电平输出电流	V_{CC} = 1.65V	SN74LVC74A		-4	mA
		V_{CC} = 2.3V	SN74LVC74A		-8	
		V_{CC} = 2.7V			-12	
		V_{CC} = 3V			-24	
I_{OL}	低电平输出电流	V_{CC} = 1.65V	SN74LVC74A		4	mA
		V_{CC} = 2.3V	SN74LVC74A		8	
		V_{CC} = 2.7V			12	
		V_{CC} = 3V			24	
$\Delta t/\Delta v$	输入转换上升或下降速率				10	ns/V

5.3 建议运行条件（续）

请参阅(1)

			最小值	最大值	单位
T_A	自然通风条件下的工作温度范围	SN54LVC74A	-55	125	°C
		SN74LVC74A	-40	125	

(1) 器件所有的未使用输入必须保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告*慢速或浮点 CMOS 输入的影响* (SCBA004)。

5.4 热性能信息：SN74LVC74A

热指标(1)		SN74LVC74A						单位
		BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	
		14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	
$R_{\theta JA}$	结至环境热阻	102.3	93.7	107.3	90.3	121.7	54.9	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	96.8	54.8	59.2	48.1	50.3	52.2	°C/W
$R_{\theta JB}$	结至电路板热阻	70.9	48	54.6	49.1	63.4	30.8	°C/W
ψ_{JT}	结至顶部特征参数	16.6	20.3	24.1	17.9	6.2	2.4	°C/W
ψ_{JB}	结至电路板特征参数	70.9	47.7	54.1	48.8	62.8	30.9	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	50.1	—	—	—	—	12.5	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告。

5.5 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数		测试条件		最小值	典型值	最大值	单位
V_{OH}	高电平输出电压	I_{OH} = -100μA	V_{CC} = 1.65V 至 3.6V 且 T_A = –55°C 至 125°C（仅限 SN54LVC74A）	V_{CC} – 0.2			V
			V_{CC} = 2.7V 至 3.6V 且 T_A = –40°C 至 125°C（仅限 SN74LVC74A）	V_{CC} – 0.2			
		I_{OH} = -4mA、V_{CC} = 1.65V 且 T_A = –40°C 至 125°C（仅限 SN74LVC74A）		1.2			
		I_{OH} = -8mA、V_{CC} = 2.3V 且 T_A = –40°C 至 125°C（仅限 SN74LVC74A）		1.7			
		I_{OH} = -12mA	V_{CC} = 2.7V	2.2			
			V_{CC} = 3V	2.4			
		I_{OH} = -24mA、V_{CC} = 3V		2.2			
V_{OL}	低电平输出电压	I_{OL} = 100μA	V_{CC} = 1.65V 至 3.6V 且 T_A = –40°C 至 125°C（仅限 SN74LVC74A）			0.2	V
			V_{CC} = 2.7V 至 3.6V 且 T_A = –55°C 至 125°C（仅限 SN54LVC74A）			0.2	
		I_{OL} = 4mA、V_{CC} = 1.65V 且 T_A = –40°C 至 125°C（仅限 SN74LVC74A）				0.45	
		I_{OL} = 8mA、V_{CC} = 2.3V 且 T_A = –40°C 至 125°C（仅限 SN74LVC74A）				0.7	
		I_{OL} = 12mA、V_{CC} = 2.7V				0.4	
		I_{OL} = 24mA、V_{CC} = 3V				0.55	
I_I	输入电流	V_I = 5.5V 或 GND、V_{cc} = 3.6V				±5	μA
I_{CC}	电源电流	V_I = V_{CC} 或 GND，I_O = 0，V_{CC} = 3.6V				10	μA
ΔI_{CC}	电源电流变化	一个输入电压为 V_{CC} – 0.6V，其他输入电压为 V_{CC} 或 GND，并且 V_{CC} = 2.7V 至 3.6V				500	μA

5.5 电气特性（续）

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数		测试条件	最小值	典型值	最大值	单位
C_i	输入电容	V_I = V_{CC} 或 GND、V_{CC} = 3.3V、T_A = 25°C		5		pF

5.6 时序要求：SN54LVC74A

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅参数测量信息）

				最小值	最大值	单位
f_{clock}	时钟频率	V_{CC} = 2.7V			83	MHz
		V_{CC} = 3.3V ± 0.3V			100	
t_w	脉冲持续时间	$\overline{PRE}$ 或 $\overline{CLR}$ 为低电平		3.3		ns
		CLK 高电平或低电平		3.3		
t_{su}	CLK ↑ 前的建立时间	数据	V_{CC} = 2.7V	3.4		ns
			V_{CC} = 3.3V ± 0.3V	3		
		$\overline{PRE}$ 或 $\overline{CLR}$ 处于非活动状态	V_{CC} = 2.7V	2.2		
			V_{CC} = 3.3V ± 0.3V	2		
t_h	保持时间，CLK ↑ 后的数据			1		ns

5.7 时序要求：SN74LVC74A

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅参数测量信息）

				最小值	最大值	单位
f_{clock}	时钟频率	V_{CC} = 1.8V 或 2.5V			83	MHz
t_w	脉冲持续时间	$\overline{PRE}$ 或 $\overline{CLR}$ 为低电平	V_{CC} = 1.8V ± 0.15V	4.1		ns
			V_{CC} = 2.5V ± 0.2V	3.3		
		CLK 高电平或低电平	V_{CC} = 1.8V ± 0.15V	4.1		
			V_{CC} = 2.5V ± 0.2V	3.3		
t_{su}	CLK ↑ 前的建立时间	数据	V_{CC} = 1.8V ± 0.15V	3.6		ns
			V_{CC} = 2.5V ± 0.2V	2.3		
		$\overline{PRE}$ 或 $\overline{CLR}$ 处于非活动状态	V_{CC} = 1.8V ± 0.15V	2.7		
			V_{CC} = 2.5V ± 0.2V	1.9		
t_h	保持时间，CLK ↑ 后的数据	V_{CC} = 1.8V 或 2.5V		1		ns

5.8 时序要求：SN74LVC74A，–40°C 至 125°C 以及 –40°C 至 85°C

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅参数测量信息）

					最小值	最大值	单位
f_{clock}	时钟频率	T_A = -40°C 至 125°C	V_{CC} = 2.7V			83	MHz
			V_{CC} = 3.3V ± 0.3V			100	
		T_A = -40°C 至 85°C 且 V_{CC} = 3.3V ± 0.3V				150	
t_w	脉冲持续时间	$\overline{PRE}$ 或 $\overline{CLR}$ 为低电平	V_{CC} = 2.7V 或 3.3V		3.3		ns
		CLK 高电平或低电平	V_{CC} = 2.7V 或 3.3V		3.3		
t_{su}	CLK ↑ 前的建立时间	数据	T_A = -40°C 至 125°C	V_{CC} = 2.7V	3.4		ns
				V_{CC} = 3.3V ± 0.3V	3		
			T_A = -40°C 至 85°C 且 V_{CC} = 3.3V ± 0.3V		3		
		$\overline{PRE}$ 或 $\overline{CLR}$ 处于非活动状态	T_A = -40°C 至 125°C	V_{CC} = 2.7V	2.2		
				V_{CC} = 3.3V ± 0.3V	2		
			T_A = -40°C 至 85°C 且 V_{CC} = 3.3V ± 0.3V		2		
t_h	保持时间，CLK ↑ 后的数据	V_{CC} = 2.7V 或 3.3V			1		ns

5.9 开关特性：SN54LVC74A

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅参数测量信息）

参数		从（输入）	到（输出）	测试条件	最小值	最大值	单位
f_{max}	最大时钟频率	—	—	V_{CC} = 2.7V	83		MHz
				V_{CC} = 3.3V ± 0.3V	100		
t_{pd}	传播（延迟）时间	CLK	Q 或 $\overline{Q}$	V_{CC} = 2.7V		6	ns
				V_{CC} = 2.7V	1	5.2	
		$\overline{PRE}$ 或 $\overline{CLR}$		V_{CC} = 3.3V ± 0.3V		6.4	
				V_{CC} = 3.3V ± 0.3V	1	5.4	

5.10 开关特性：SN74LVC74A

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅参数测量信息）

参数		从（输入）	到（输出）	测试条件	最小值	最大值	单位
f_{max}	最大时钟频率	—	—		83		MHz
t_{pd}	传播（延迟）时间	CLK $\overline{PRE}$	Q 或 $\overline{Q}$	V_{CC} = 1.8V ± 0.15V	1	7.1	ns
				V_{CC} = 2.5V ± 0.2V	1	4.4	
		或 $\overline{CLR}$		V_{CC} = 1.8V ± 0.15V	1	6.9	
				V_{CC} = 2.5V ± 0.2V	1	4.6	

5.11 开关特性：SN74LVC74A，–40°C 至 125°C 以及 –40°C 至 85°C

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅参数测量信息）

参数		从（输入）	到（输出）	测试条件		最小值	最大值	单位
f_{max}	最大时钟频率	—	—	T_A = -40°C 至 125°C	V_{CC} = 2.7V	83		MHz
					V_{CC} = 3.3V ± 0.3V	100		
				T_A = -40°C 至 85°C 且 V_{CC} = 3.3V ± 0.3V		150		
t_{pd}	传播（延迟）时间	CLK	Q 或 $\overline{Q}$	T_A = -40°C 至 125°C	V_{CC} = 2.7V	1	6	ns
					V_{CC} = 3.3V ± 0.3V		5.2	
				T_A = -40°C 至 85°C 且 V_{CC} = 3.3V ± 0.3V		1	5.2	
		$\overline{PRE}$ 或 $\overline{CLR}$		T_A = -40°C 至 125°C	V_{CC} = 2.7V	1	6.4	
					V_{CC} = 3.3V ± 0.3V		5.4	
				T_A = -40°C 至 85°C 且 V_{CC} = 3.3V ± 0.3V		1	5.4	
$t_{sk(o)}$	偏斜（时间），输出	—	—	T_A = -40°C 至 85°C 且 V_{CC} = 3.3V ± 0.3V			1	ns

5.12 工作特性

T_A = 25°C

参数		测试条件		典型值	单位
C_{pd}	每个触发器的功率耗散电容	f = 10MHz	V_{CC} = 1.8V	24	pF
			V_{CC} = 2.5V	24	
			V_{CC} = 3.3V	26	

5.13 典型特性

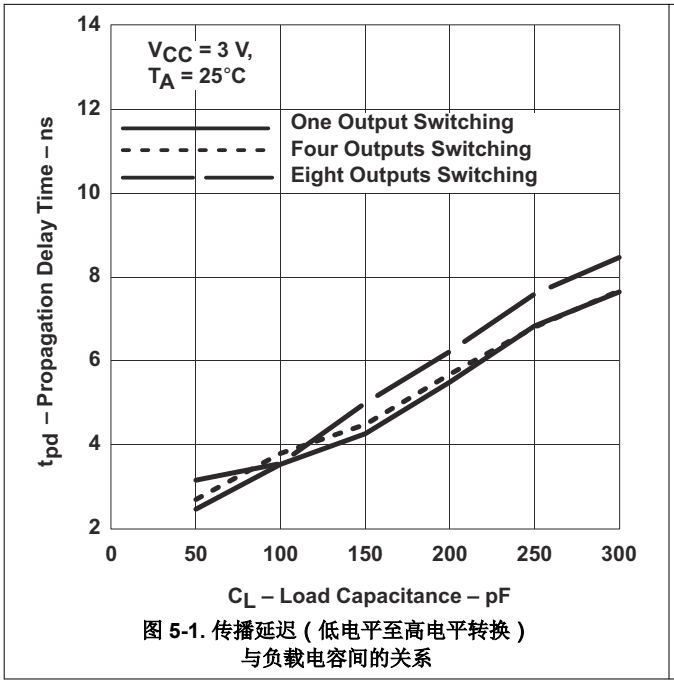


图 5-1. 传播延迟（低电平至高电平转换）与负载电容间的关系

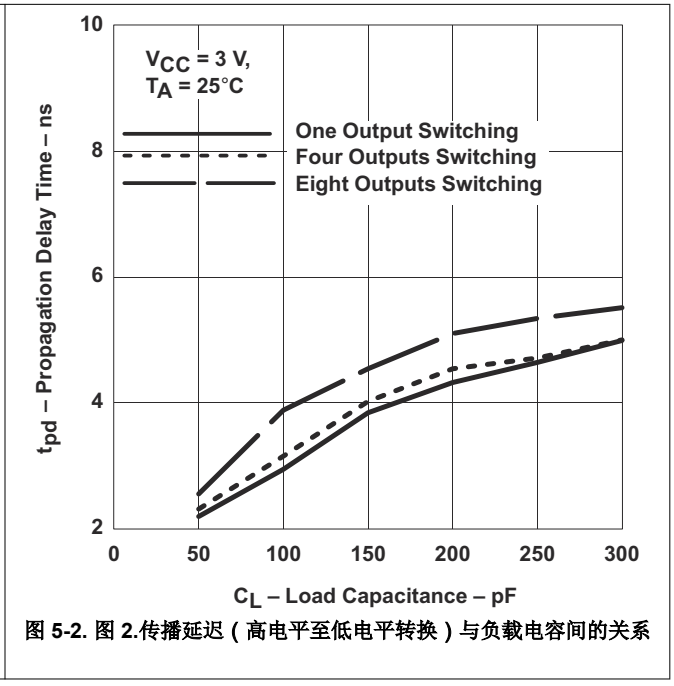


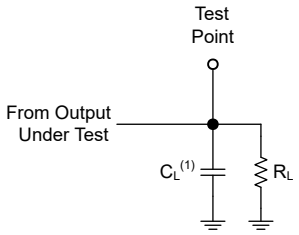
图 5-2. 图 2.传播延迟（高电平至低电平转换）与负载电容间的关系

6 参数测量信息

对于下表中列出的示例，波形之间的相位关系是任意选择的。所有输入脉冲均由具有以下特性的发生器提供：PRR ≤ 1MHz，Z_O = 50Ω，t_t ≤ 2.5ns。

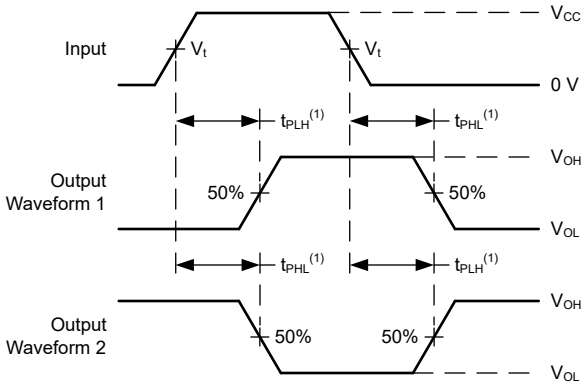
输出单独测量，每次测量一个输入转换。

V_{CC}	V_t	R_L	C_L	Δ V
1.8V ± 0.15V	V_{CC}/2	1kΩ	30pF	0.15V
2.5V ± 0.2V	V_{CC}/2	500Ω	30pF	0.15V
2.7V	1.5V	500Ω	50pF	0.3V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V



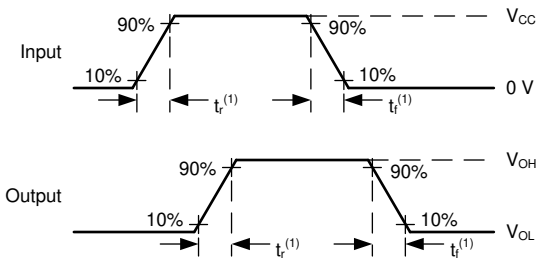
(1) C_L 包括探头和测试夹具电容。

图 6-1. 推挽输出的负载电路



(1) t_{PLH} 和 t_{PHL} 之间的较大者与 t_{pd} 相同。

图 6-2. 电压波形传播延迟



(1) t_r 和 t_f 之间的较大值与 t_t 相同。

图 6-3. 电压波形，输入和输出转换时间

7 详细说明

7.1 概述

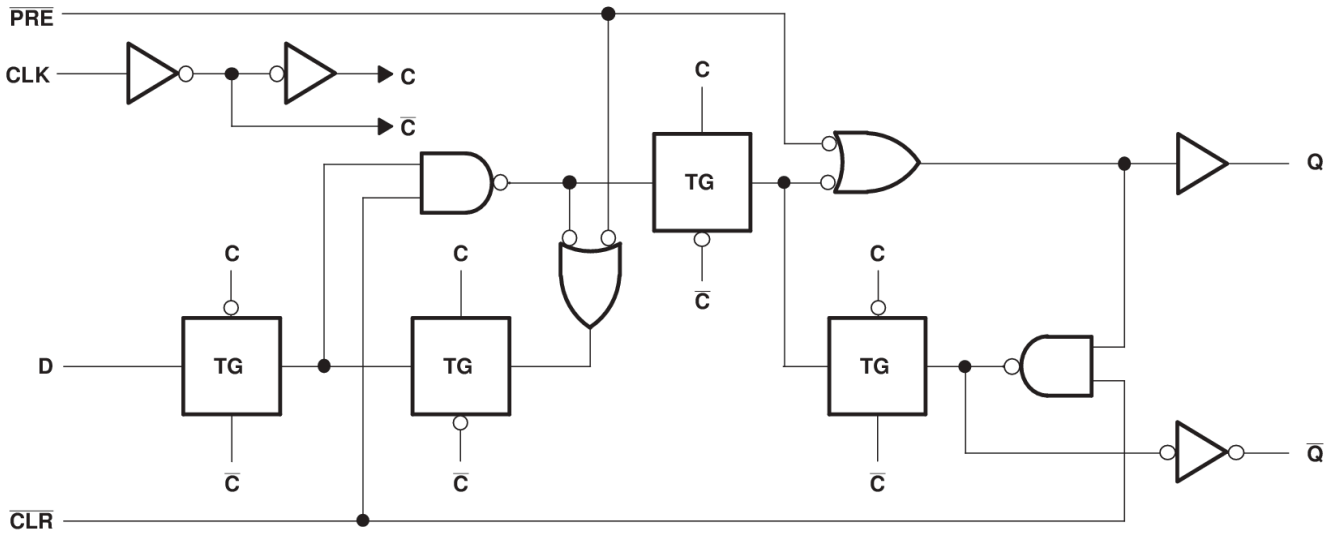
SNx4LVC74A 器件具有两个独立的正边沿触发式 D 型触发器。集成的预设 ($\overline{PRE}$) 和清零 ($\overline{CLR}$) 功能允许在运行期间进行轻松设置和控制。

SN54LVC74A 器件的额定工作温度范围为 -55°C 至 125°C，SN74LVC74A 器件的额定工作温度范围为 -40°C 至 125°C。

预设 ($\overline{PRE}$) 或清零 ($\overline{CLR}$) 输入端的低电平会设置或复位输出，不受其他输入端的电平的影响。当 $\overline{PRE}$ 和 $\overline{CLR}$ 处于非活动状态（高电平）时，数据 (D) 输入处满足设置时间要求的数据将传输到时钟脉冲正向缘上的输出处。时钟触发出现在一个特定电压电平上，并且不与时钟脉冲的上升时间直接相关。经过保持时间间隔后，可以更改 D 输入端的数据而不影响输出端的电平。

数据 I/O 和控制输入具有过压容限。此功能允许在混合电压环境中将此类器件用于降压转换。

7.2 功能方框图



7.3 特性说明

预设 ($\overline{PRE}$) 或清零 ($\overline{CLR}$) 输入端的低电平会设置或复位输出，不受其他输入端的电平的影响。当 $\overline{PRE}$ 和 $\overline{CLR}$ 处于非活动状态（高电平）时，数据 (D) 输入处满足设置时间要求的数据将传输到时钟脉冲正向缘上的输出处。时钟触发出现在一个特定电压电平上，并且不与时钟脉冲的上升时间直接相关。经过保持时间间隔后，可以更改 D 输入端的数据而不影响输出端的电平。

7.4 器件功能模式

表 7-1 描述了 SNx4LVC74A 的功能以及 $\overline{PRE}$、$\overline{CLR}$、CLK 和 D 输入之间的相互作用。

表 7-1. 功能表

输入				输出	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H(1)	H(1)
H	H	↑	H	H	L
H	H	↑	L	L	H

表 7-1. 功能表（续）

输入				输出	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
H	H	L	X	Q_0	$\overline{Q}_0$

(1) 该配置不稳定；也就是说，当 $\overline{PRE}$ 或 $\overline{CLR}$ 恢复到其非活动（高）电平时，该配置不会持续存在。

8 应用和实施

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户应负责确定各元件是否适用于其应用。客户应验证并测试其设计是否能够实现，以确保系统功能。

8.1 应用信息

SN74LVC74A 的一个常见应用是分频器。通过将 $\overline{Q}$ 输出连接到 D 输入，Q 输出在传入的时钟信号的每个正边沿上切换状态。由于需要两个正边沿或两个时钟脉冲才能在输出端完成一个完整脉冲（一个脉冲从低电平切换到高电平，另一个脉冲从高电平切换到低电平），因此传入的时钟频率实际上进行了二分频。

8.2 典型应用

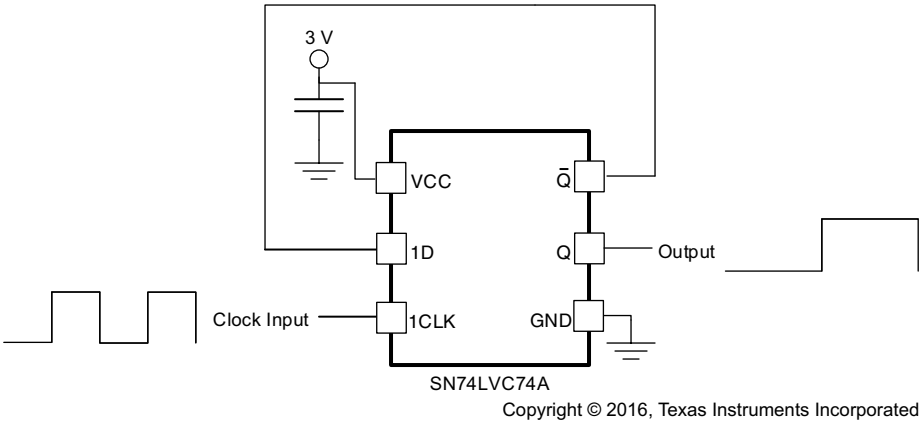


图 8-1. 分频器

8.2.1 设计要求

此器件采用 CMOS 技术并具有平衡输出驱动。避免总线争用，因为它可以驱动超过最大限制的电流。高驱动也会在轻负载时产生快速边沿，因此请考虑布线和负载条件以防止振铃。

8.2.2 详细设计过程

1. 建议的输入条件：
   - 有关上升时间和下降时间规格，请参阅*建议运行条件*中的 ($\Delta t/\Delta V$)。
   - 有关指定的高电平和低电平，请参阅*建议运行条件*中的（V_{IH} 和 V_{IL}）。
   - 输入可耐受过压，允许它们在任何有效 V_{CC} 下高达*建议运行条件*中的（V_I 最大值）。
2. 建议的输出条件上限：
   - 每路输出的负载电流不能超过（I_O 最大值），且不能超过该器件的总电流（通过 V_{CC} 或 GND 的持续电流）。这些限值可在*绝对最大额定值*中找到。
   - 输出不应被拉至高于 V_{CC}。

8.2.3 应用曲线

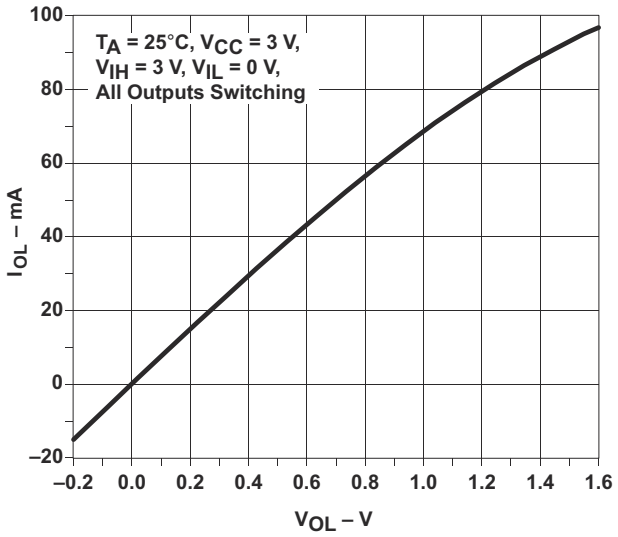


图 8-2. 输出驱动电流 (I_{OL})
与低电平输出电压 (V_{OL}) 间的关系

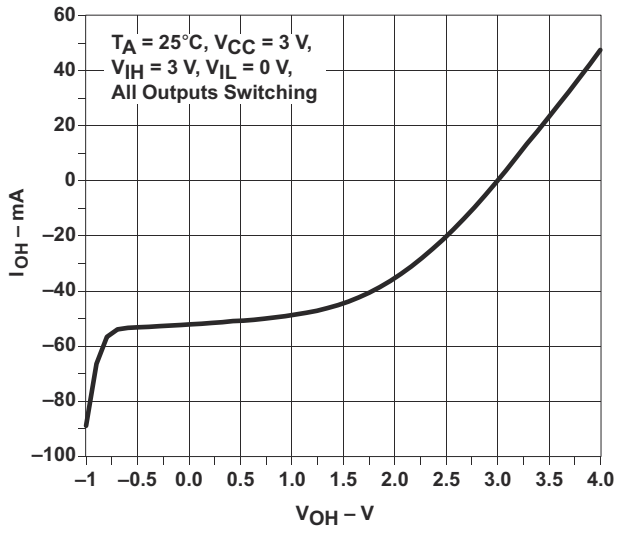


图 8-3. 输出驱动电流 (I_{OH})
与高电平输出电压 (V_{OH}) 间的关系

8.3 电源相关建议

电源可以是*建议运行条件* 中最小和最大电源电压额定值之间的任何电压。

每个 V_{CC} 端子都必须具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 0.1μF 电容器。如果有多个 V_{CC} 端子，则建议为每个电源端子使用 0.01 μ F 或 0.022 μ F 电容器。允许并联多个旁路电容器以抑制不同的噪声频率。为抑制不同的噪声频率，可以并联多个旁路电容器。为了获得最佳效果，旁路电容器必须尽可能靠近电源端子安装。

8.4 布局

8.4.1 布局指南

当使用多位逻辑器件时，输入不得悬空。在许多情况下，数字逻辑器件的功能或部分功能未被使用。例如，在仅使用三输入与门的 2 个输入，或仅使用 4 个缓冲门中的 3 个时。此类输入引脚不得悬空，因为外部连接处的未定义电压会导致未定义的运行状态。

图 8-4 指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须连接至一个高或低偏置以防止悬空。必须应用于任何特定未使用输入的逻辑电平取决于器件的功能。通常，它们会连接到 GND 或 V_{CC}，具体取决于哪种更合理或更方便。

8.4.2 布局示例

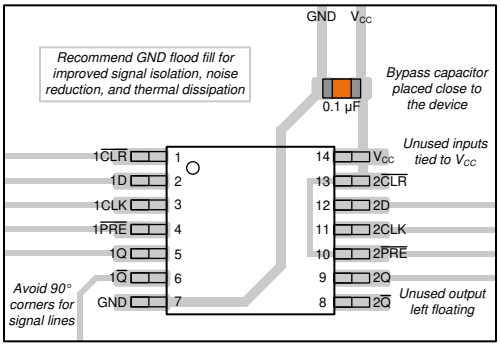


图 8-4. 布局图

9 器件和文档支持

9.1 文档支持

9.1.1 相关文档

请参阅以下相关文档：

慢速或浮点 CMOS 输入的影响 (SCBA004)

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision U (January 2017) to Revision V (May 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 向*器件信息* 表、*引脚配置和功能* 部分以及*热性能信息* 表中添加了 BQA 封装	1
• 向*器件信息* 表中添加了封装尺寸	1

Changes from Revision T (July 2013) to Revision U (January 2017)	Page
• 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• 将封装热阻 $R_{\theta JA}$ 值（位于*热性能信息：SN74LVC74A* 中）从 86 更改为 93.7 (D)、从 96 更改为 107.3 (DB)、从 76 更改为 90.3 (NS)、从 113 更改为 121.7 (PW) 以及从 47 更改为 54.9 (RGY)	5

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9761601Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761601Q2A SNJ54LVC 74AFK	Samples
5962-9761601QCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761601QC A SNJ54LVC74AJ	Samples
5962-9761601QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761601QD A SNJ54LVC74AW	Samples
5962-9761601VDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761601VD A SNV54LVC74AW	Samples
SN74LVC74ABQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples
SN74LVC74AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples
SN74LVC74ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74ADBRG4	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples
SN74LVC74ADRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples
SN74LVC74ADT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples
SN74LVC74ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC74A	Samples
SN74LVC74APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74APWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74APWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC74APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74APWTG4	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC74A	Samples
SN74LVC74ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC74A	Samples
SNJ54LVC74AFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761601Q2A SNJ54LVC 74AFK	Samples
SNJ54LVC74AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761601QC A SNJ54LVC74AJ	Samples
SNJ54LVC74AW	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761601QD A SNJ54LVC74AW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54LVC74A, SN54LVC74A-SP, SN74LVC74A :

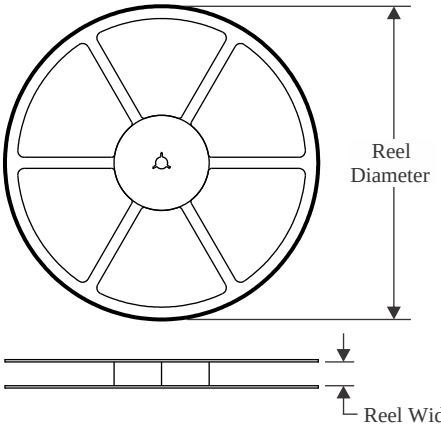
- Catalog : SN74LVC74A, SN54LVC74A
- Automotive : SN74LVC74A-Q1, SN74LVC74A-Q1
- Enhanced Product : SN74LVC74A-EP, SN74LVC74A-EP
- Military : SN54LVC74A
- Space : SN54LVC74A-SP

NOTE: Qualified Version Definitions:

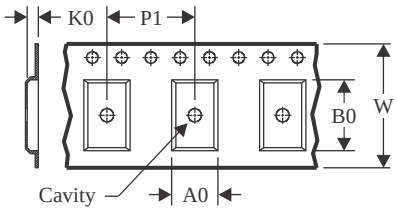
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

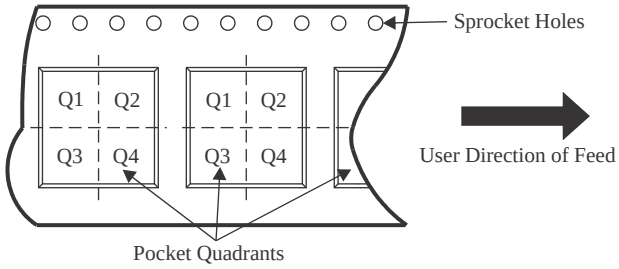


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

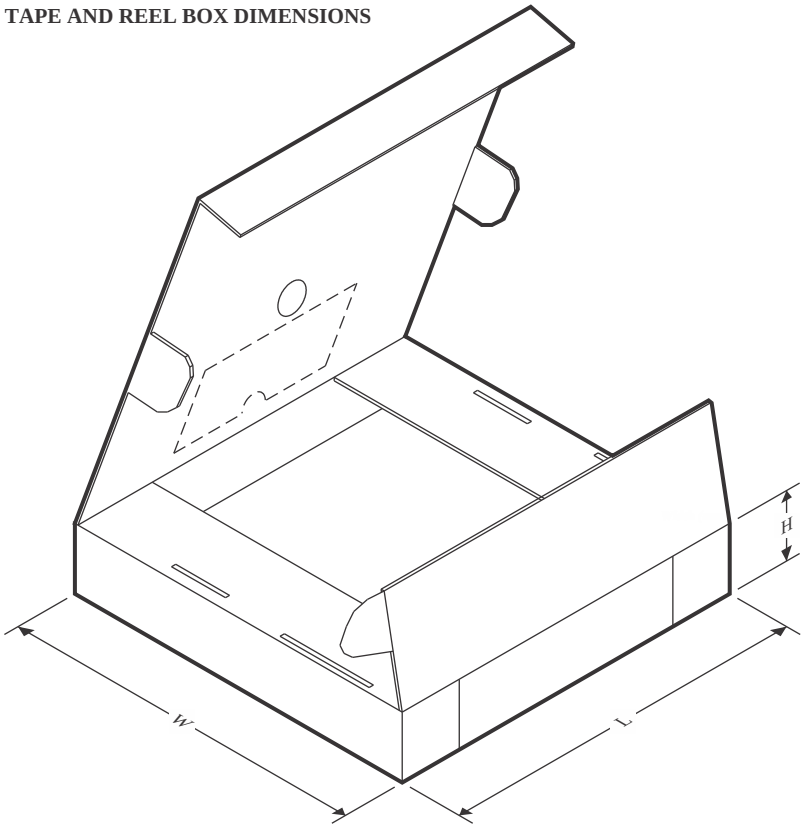
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC74ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC74ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC74ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC74ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC74ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC74APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC74ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

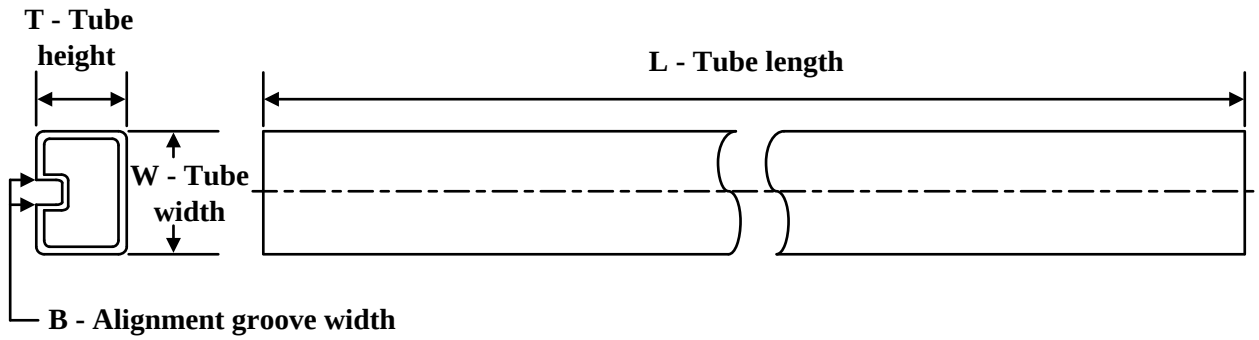
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

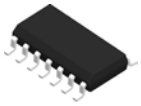
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC74ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC74ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LVC74ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LVC74ADT	SOIC	D	14	250	210.0	185.0	35.0
SN74LVC74ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LVC74APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC74APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC74APWT	TSSOP	PW	14	250	356.0	356.0	35.0
SN74LVC74ARGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9761601Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9761601VDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LVC74AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC74APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC74APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54LVC74AFK	FK	LCCC	20	55	506.98	12.06	2030	NA

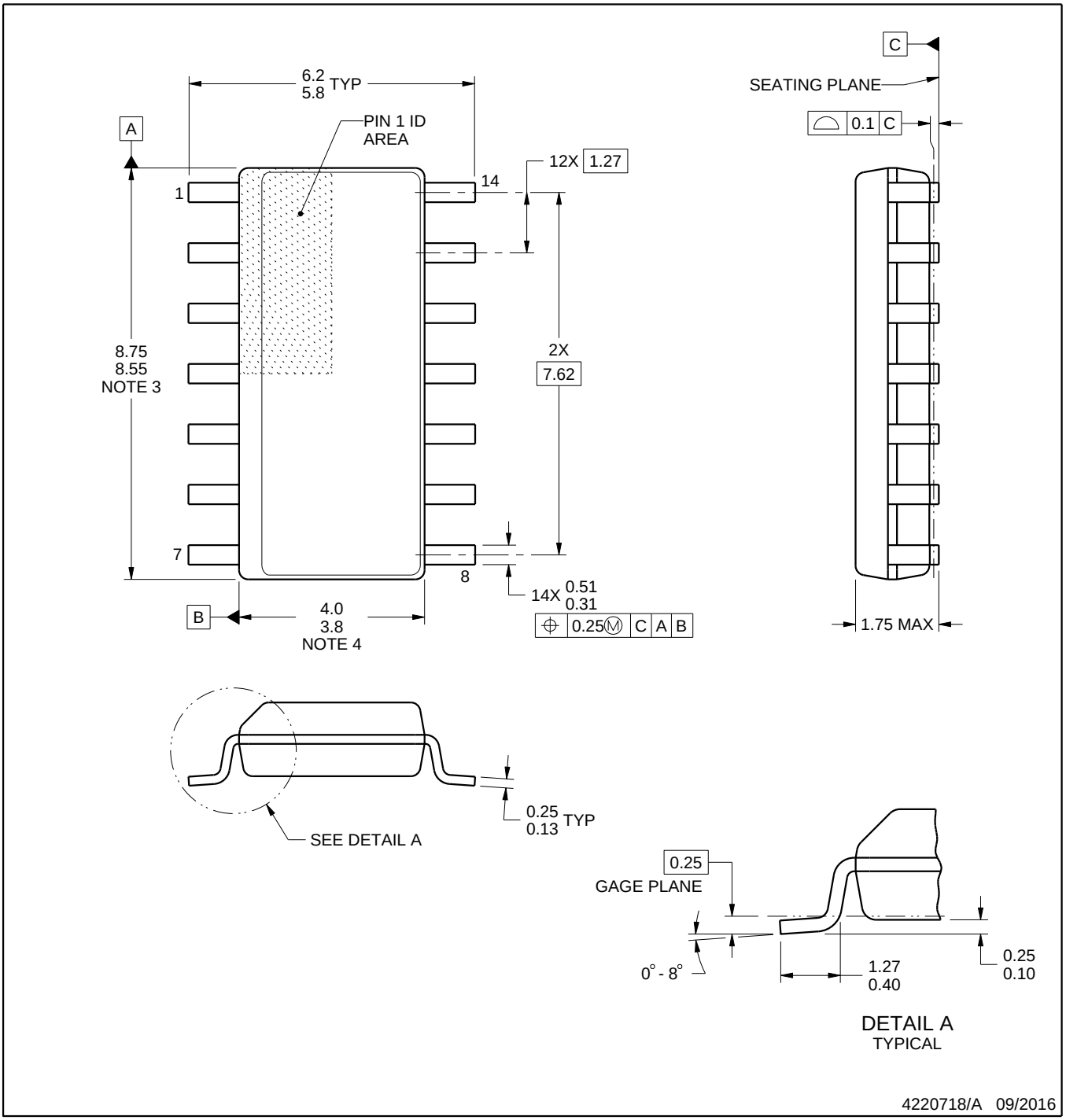


PACKAGE OUTLINE

D0014A

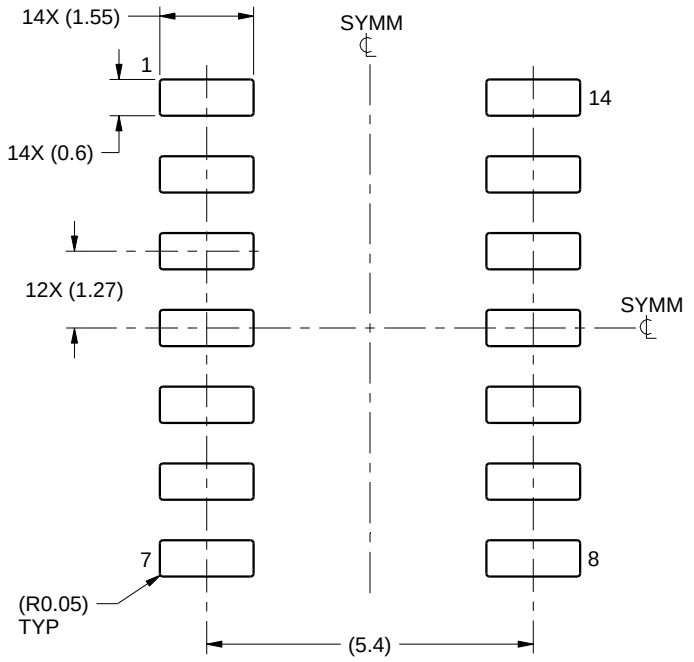
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

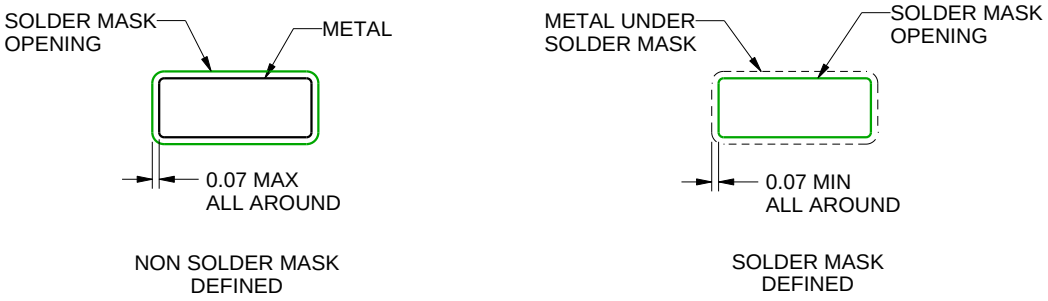


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

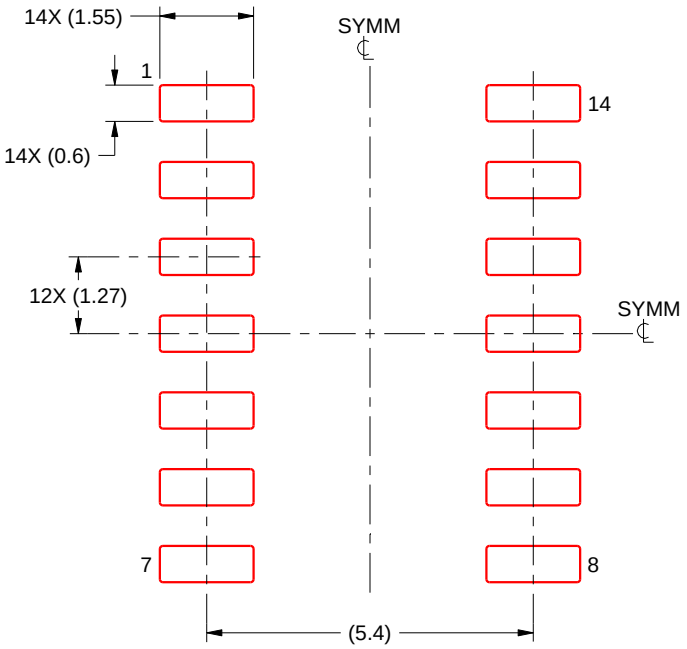
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



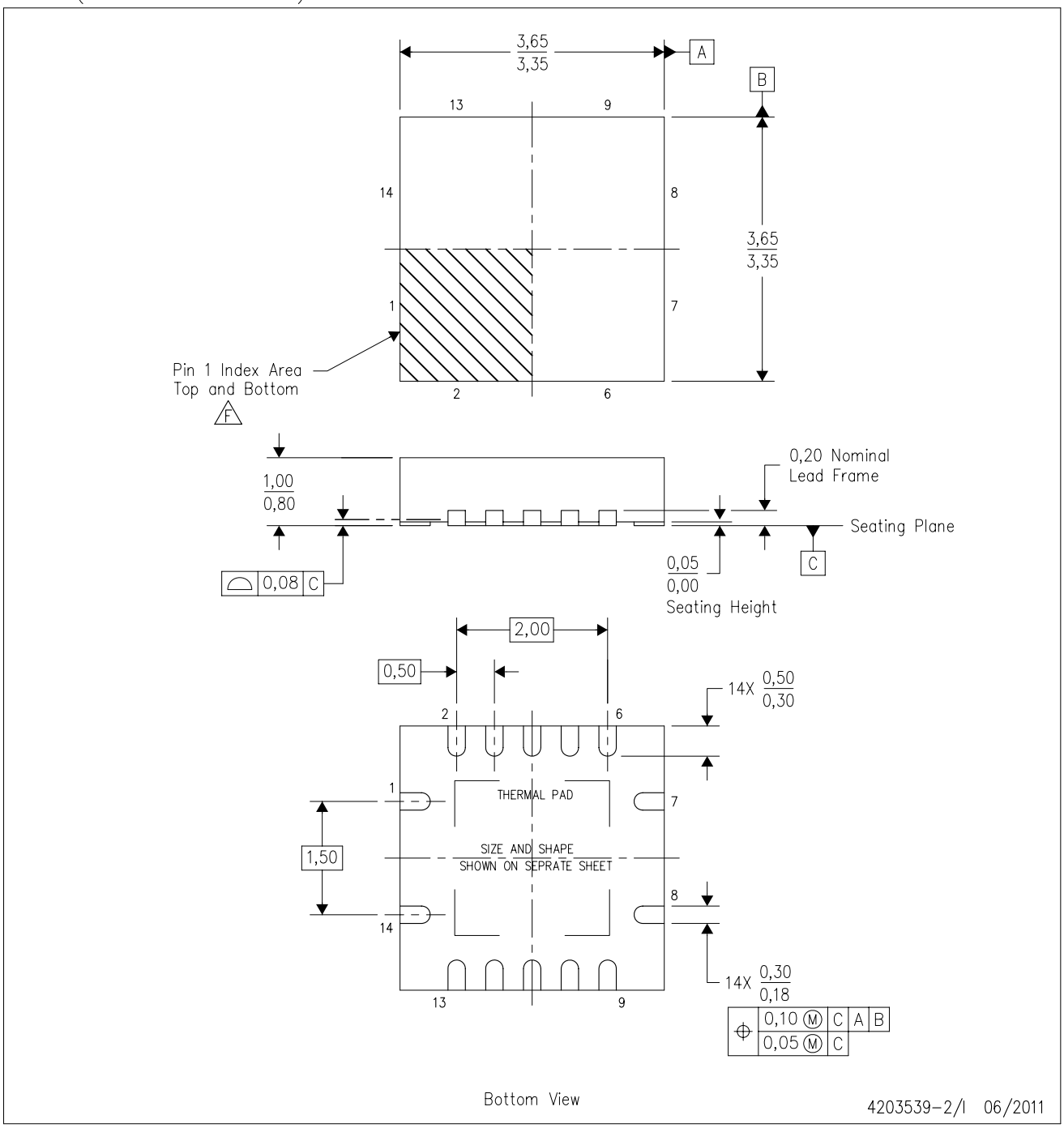
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

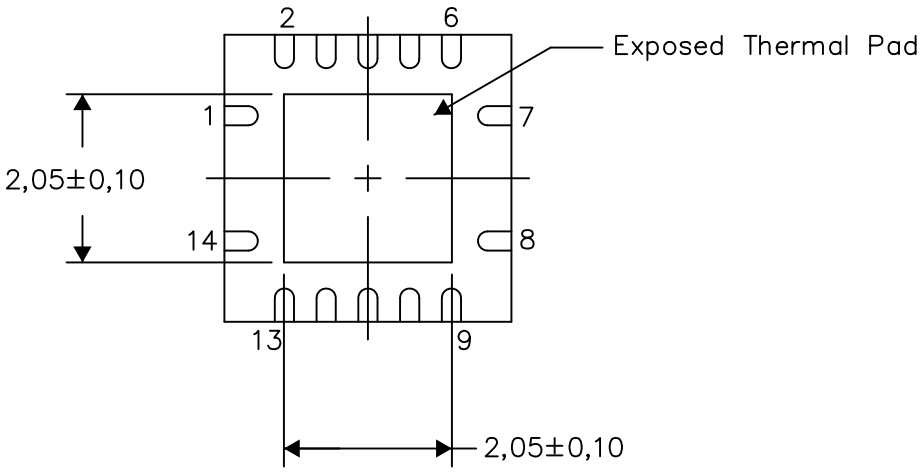
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



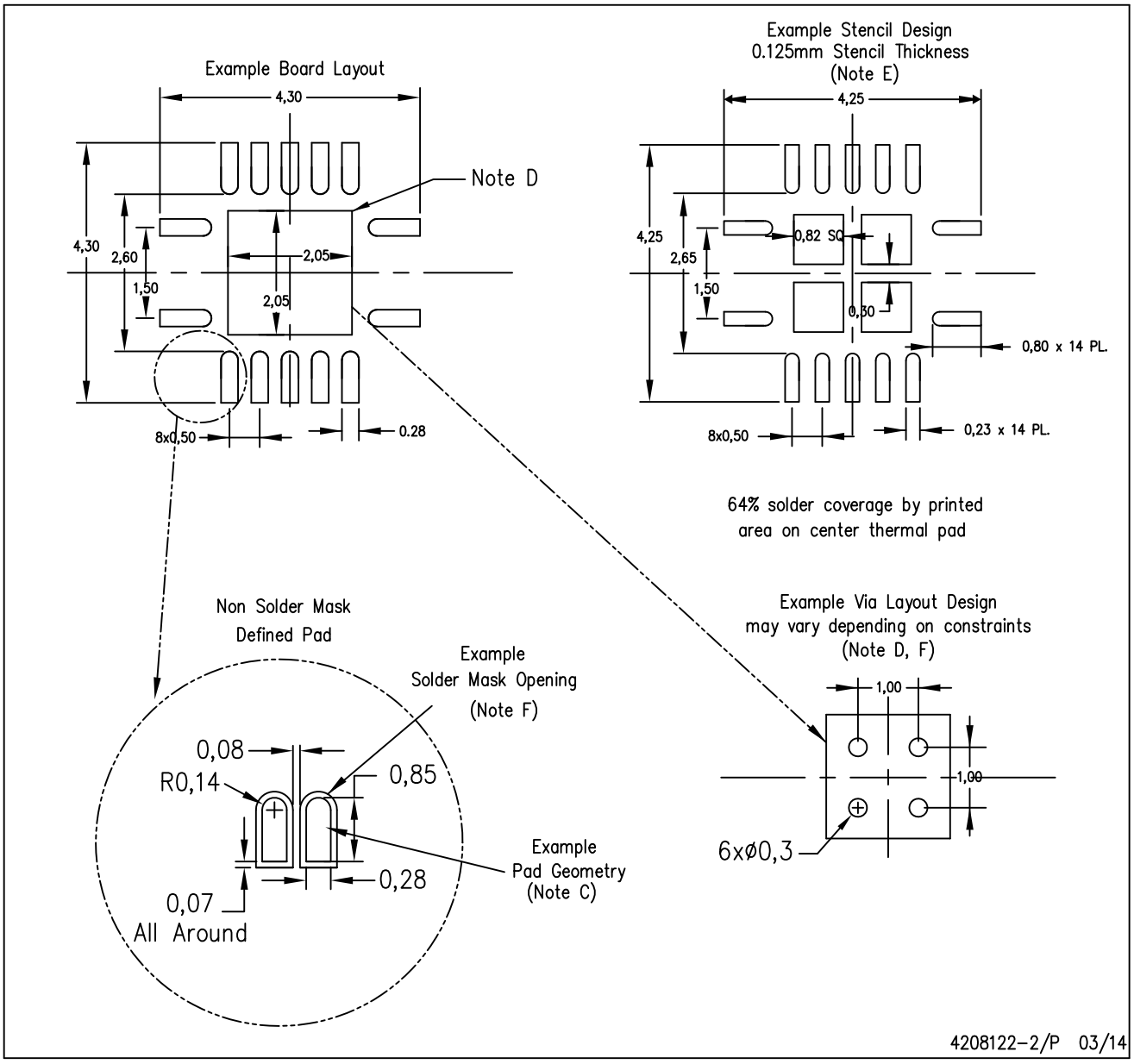
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

GENERIC PACKAGE VIEW

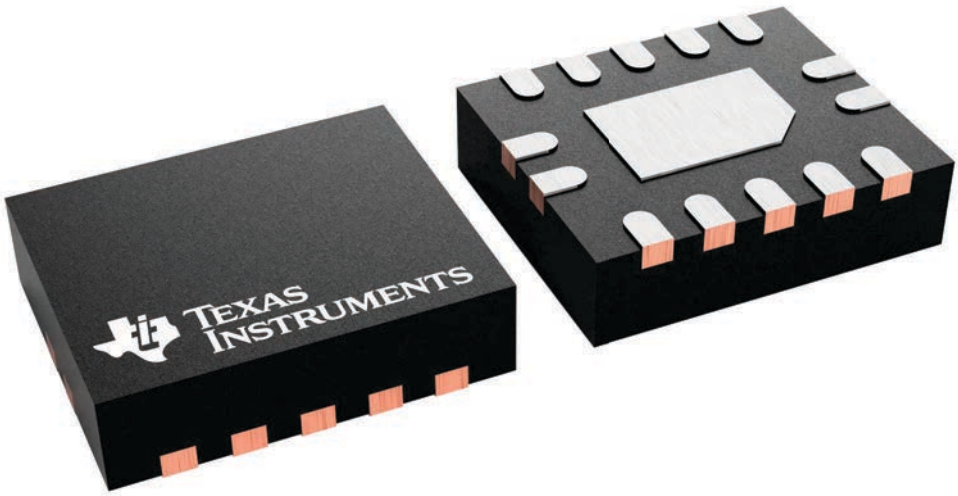
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

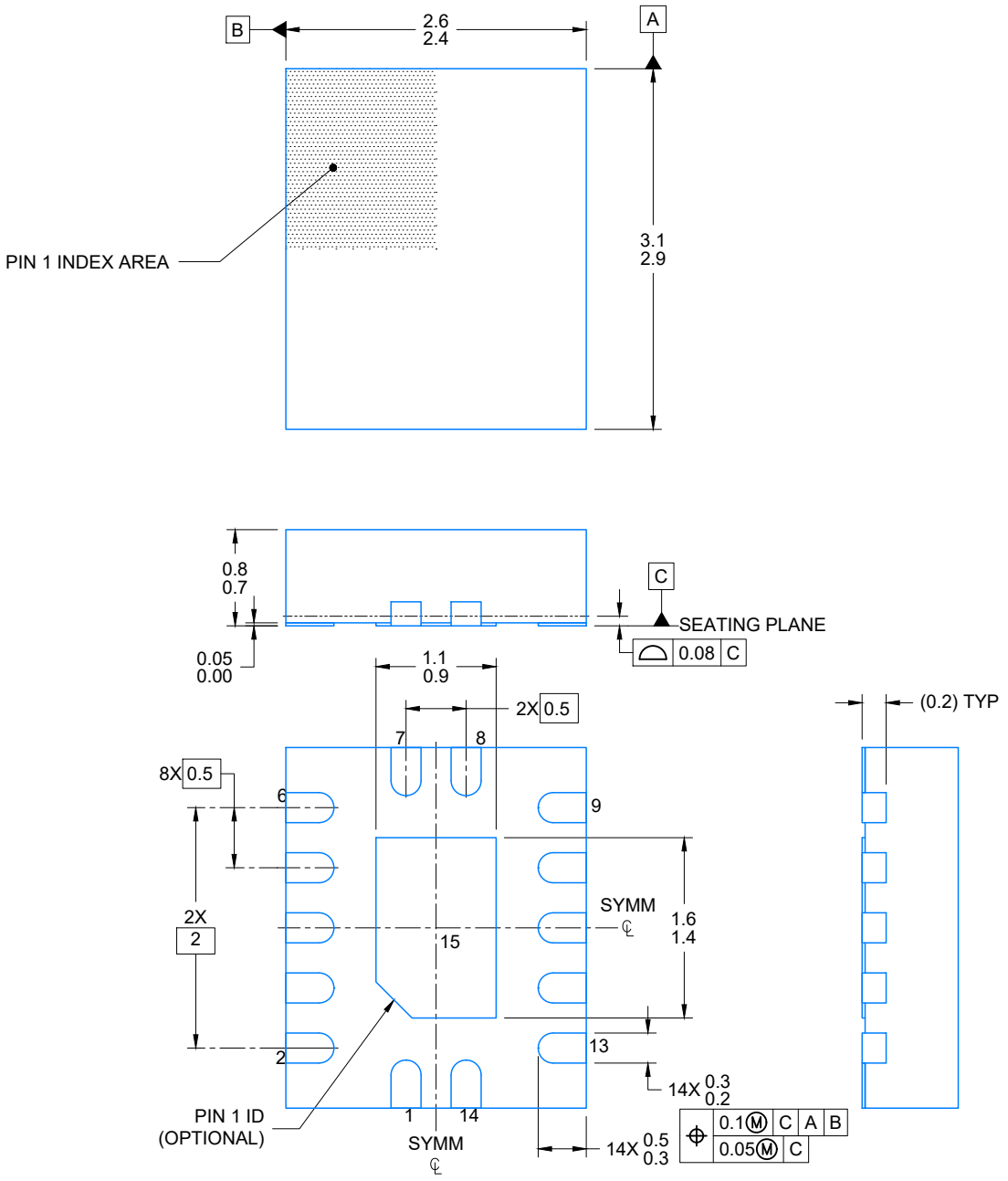


PACKAGE OUTLINE

BQA0014A

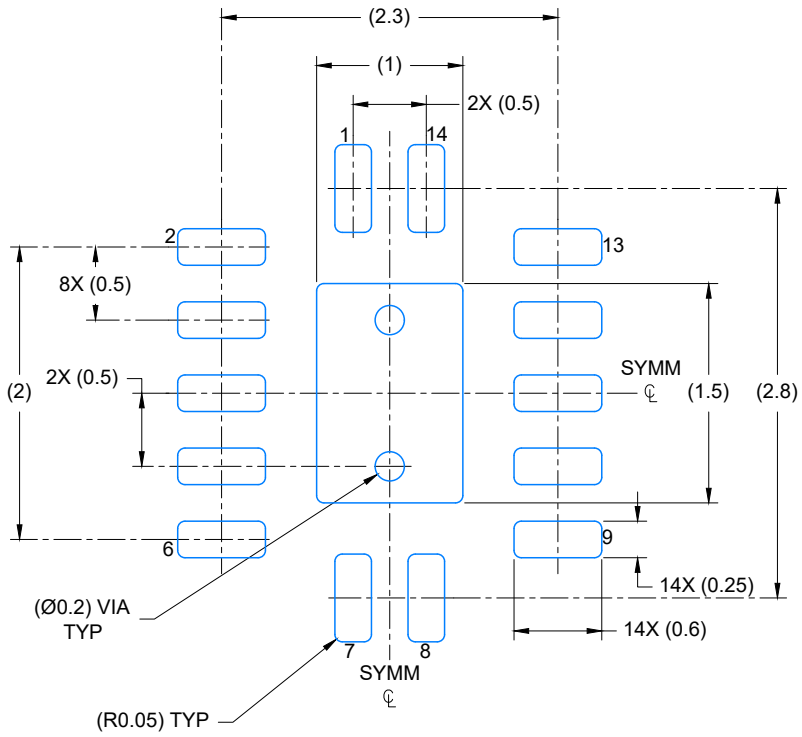
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

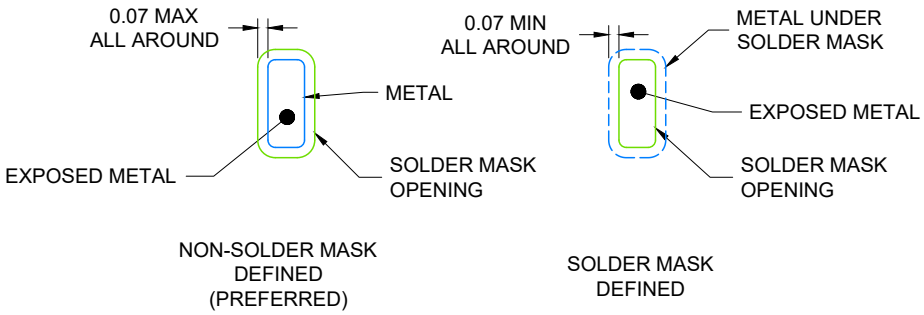


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



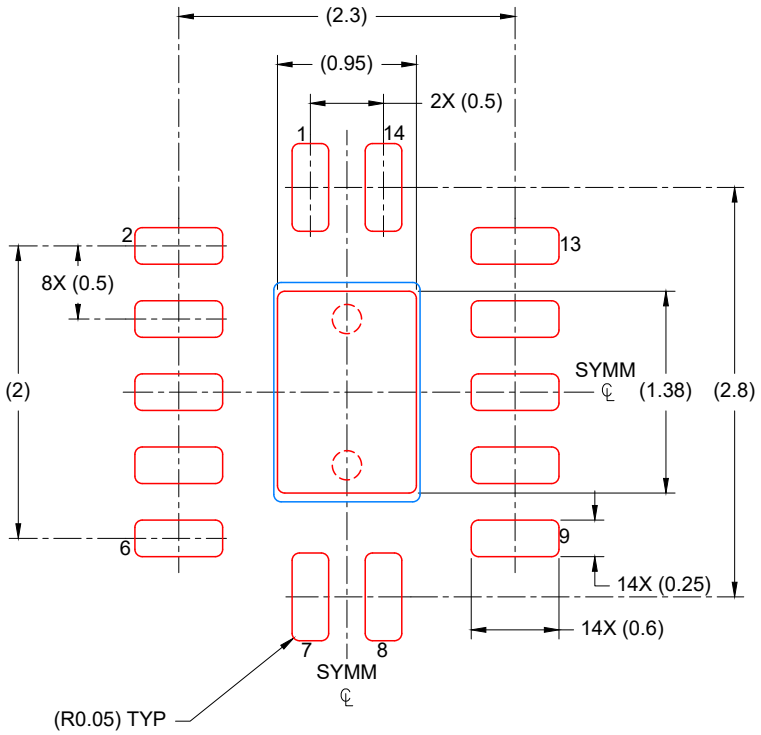
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

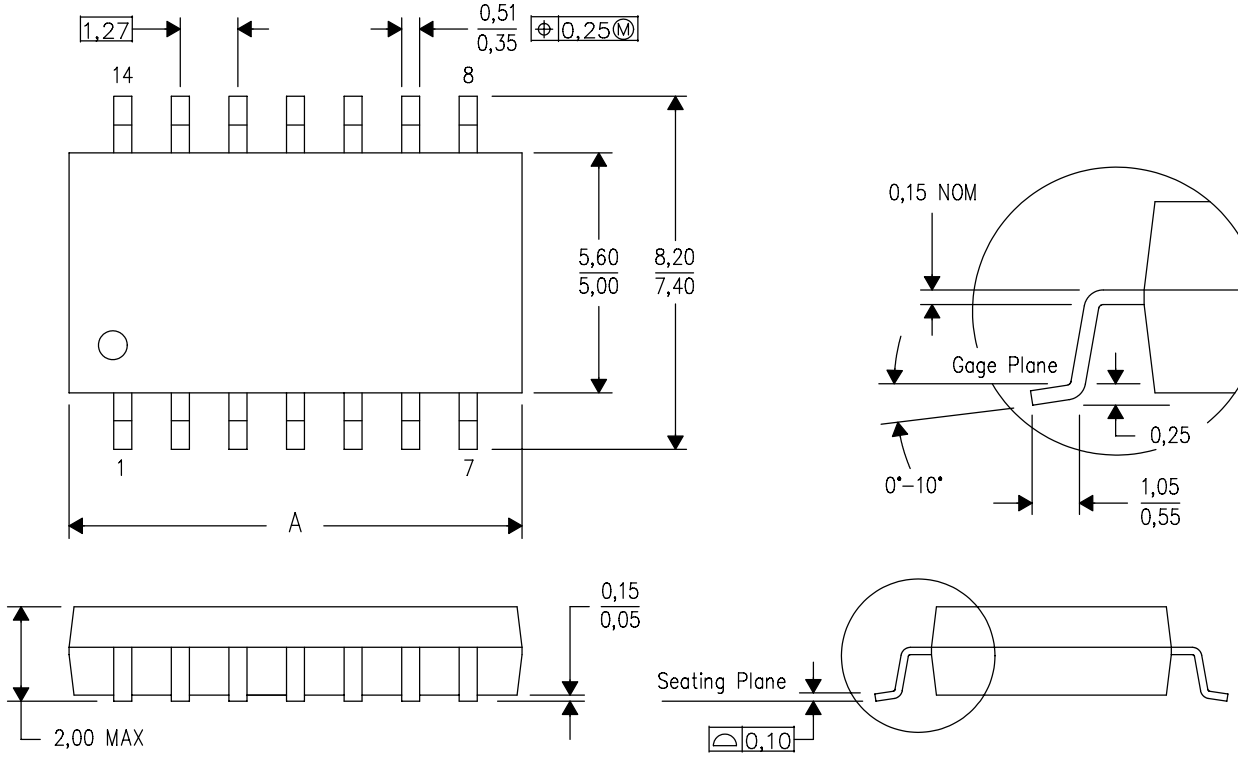
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

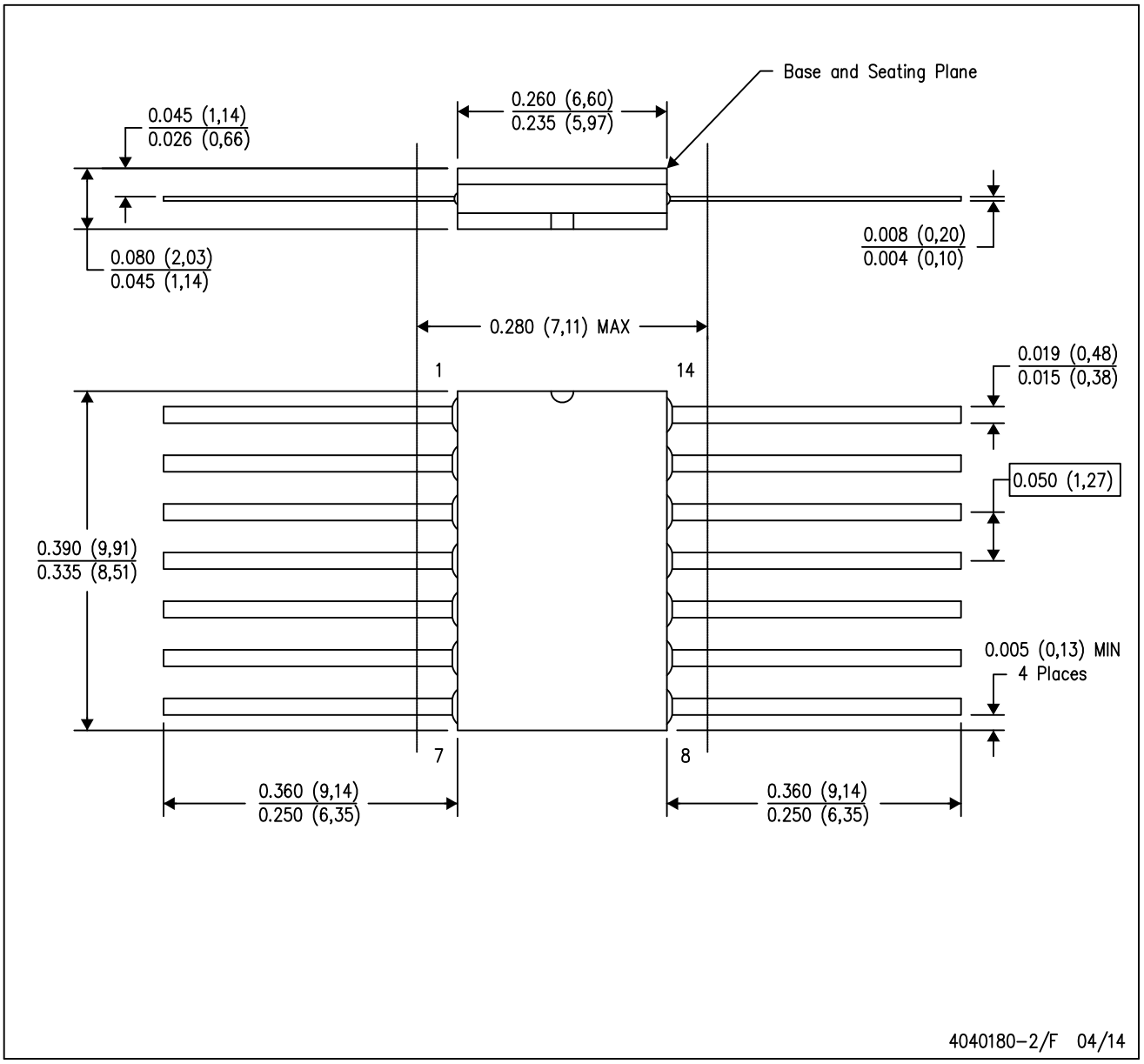


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



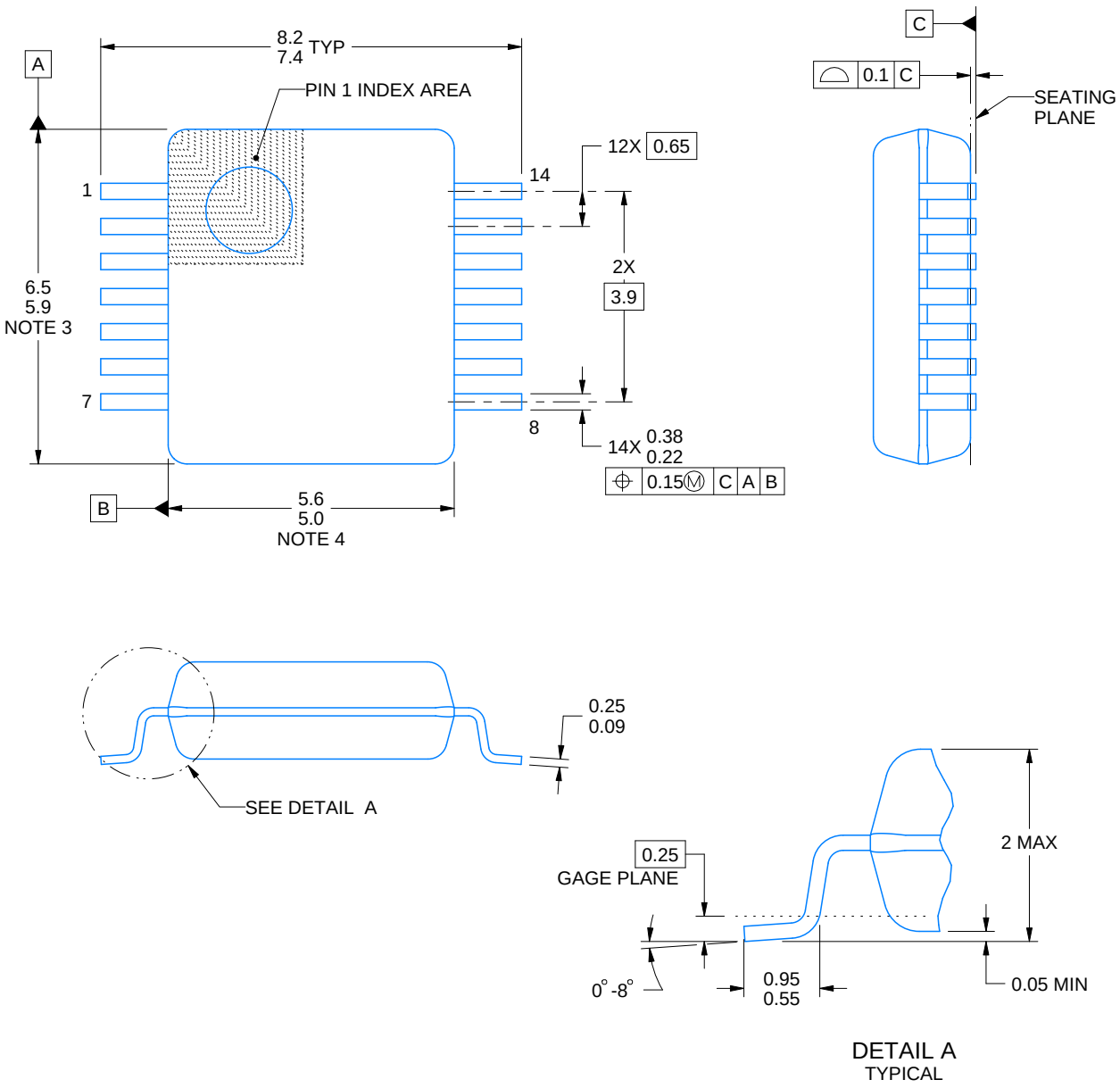
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

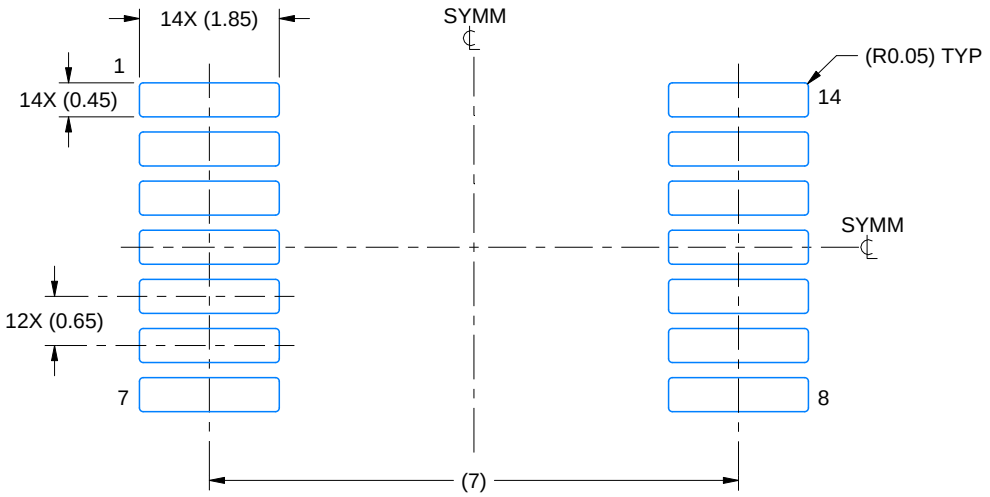
SMALL OUTLINE PACKAGE



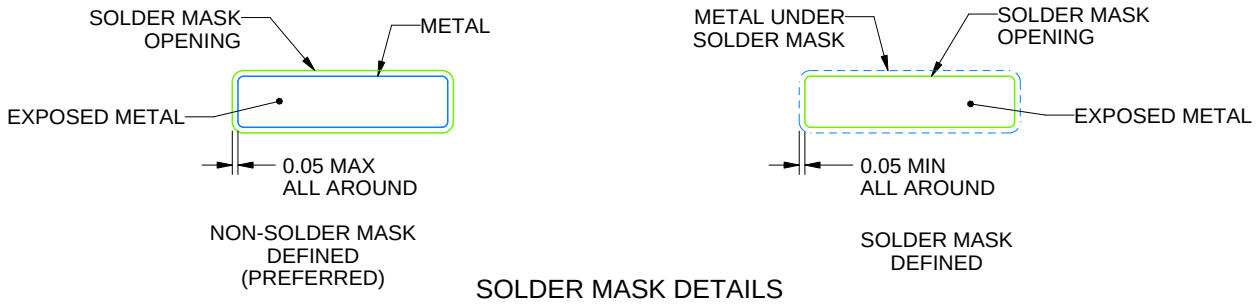
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

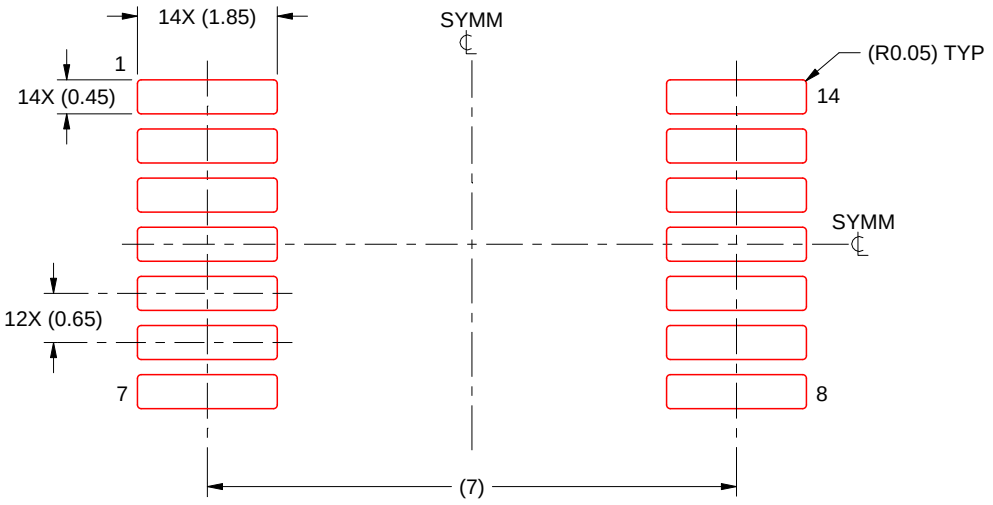


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

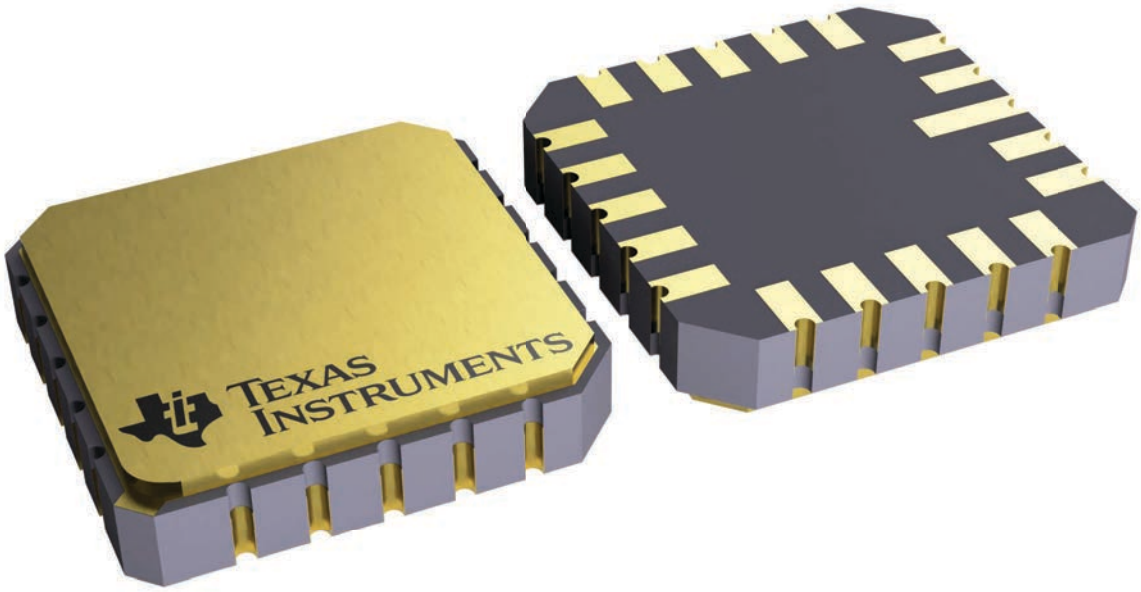
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

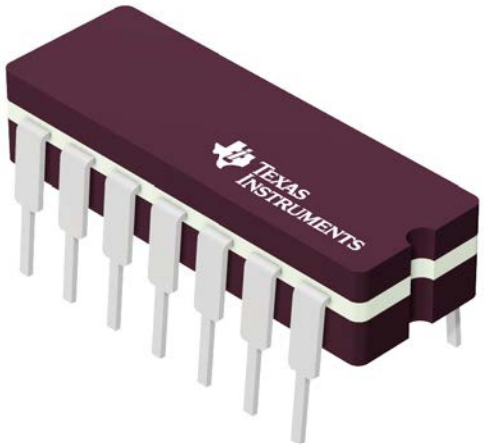


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

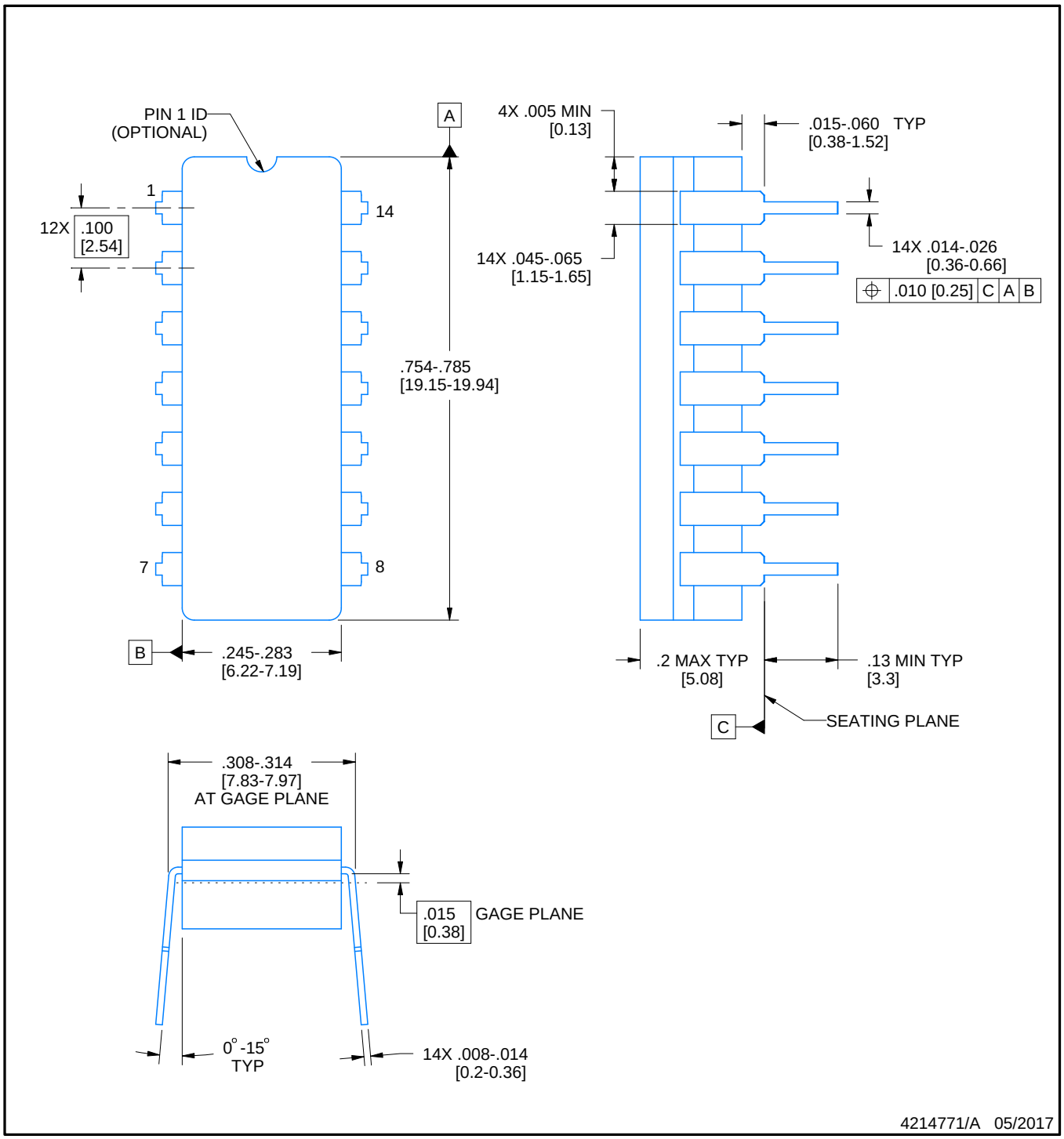
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

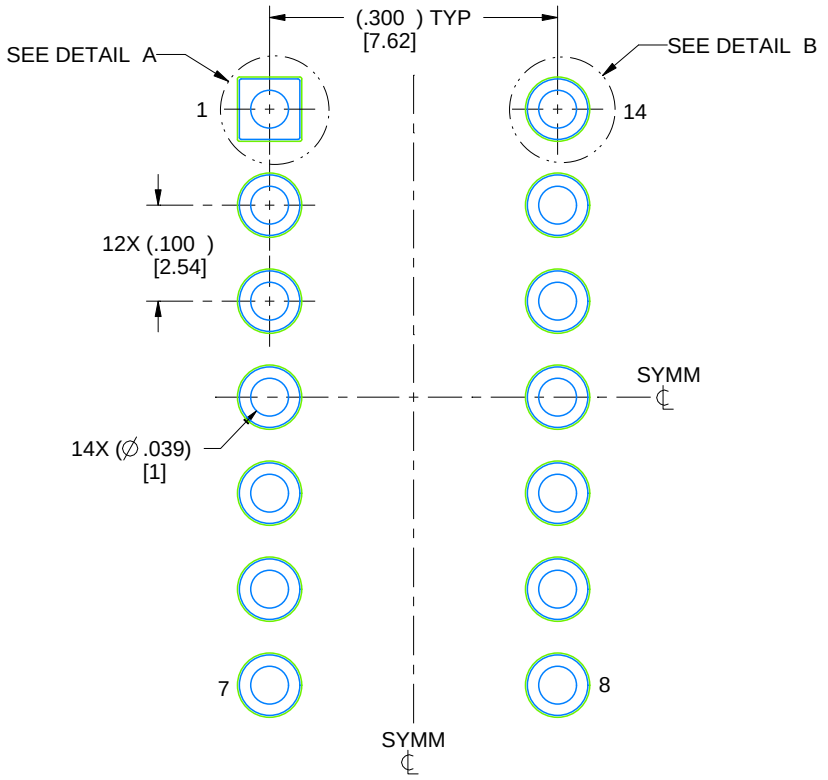
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

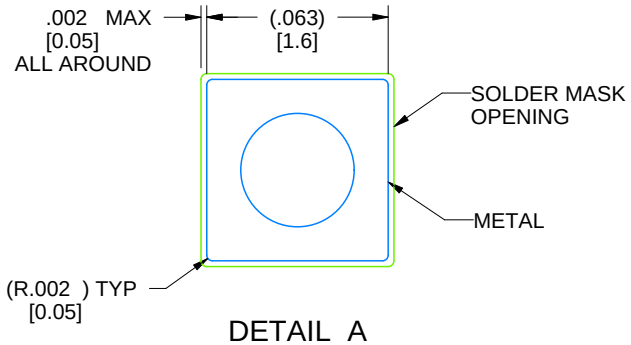
J0014A

CDIP - 5.08 mm max height

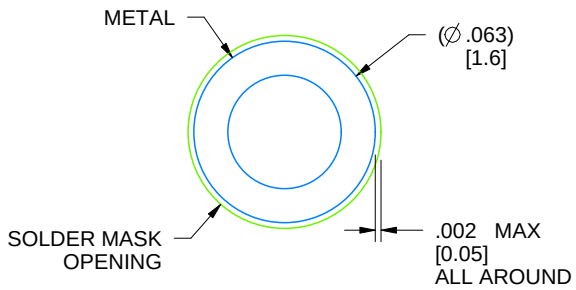
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

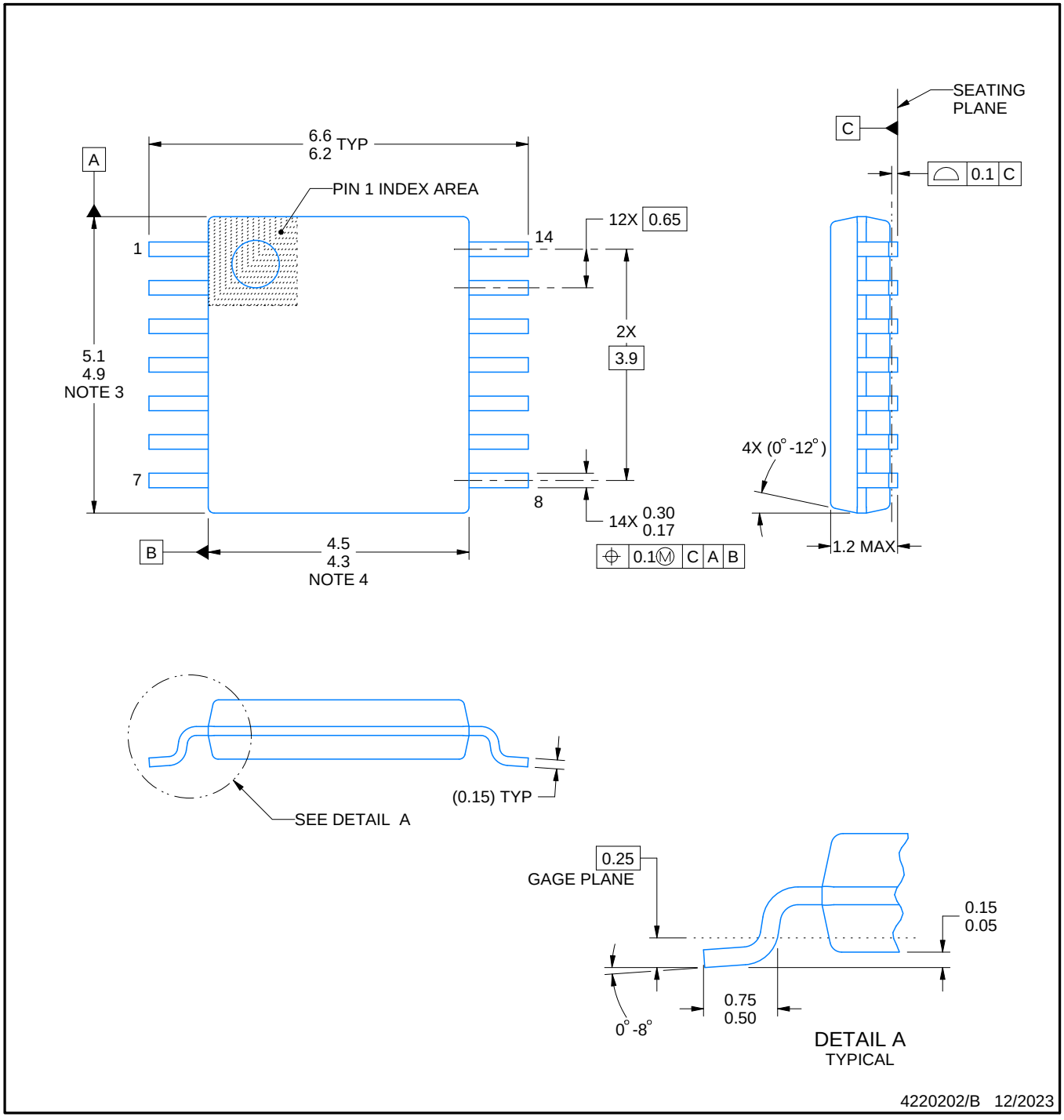
4214771/A 05/2017

PACKAGE OUTLINE

PW0014A

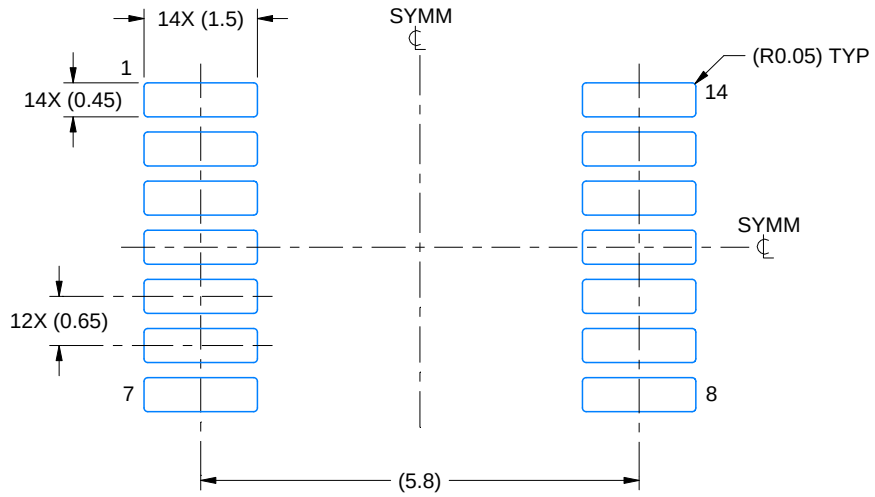
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

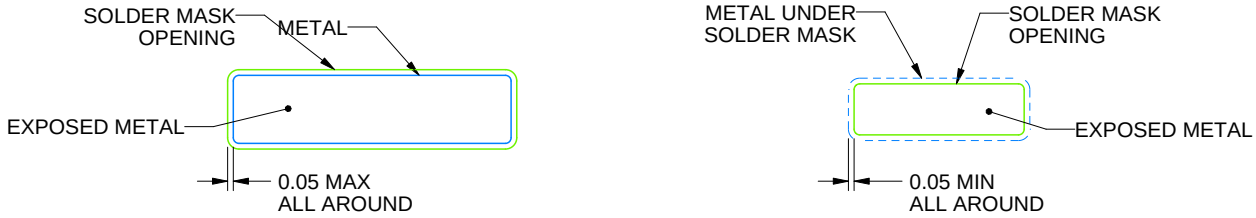


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

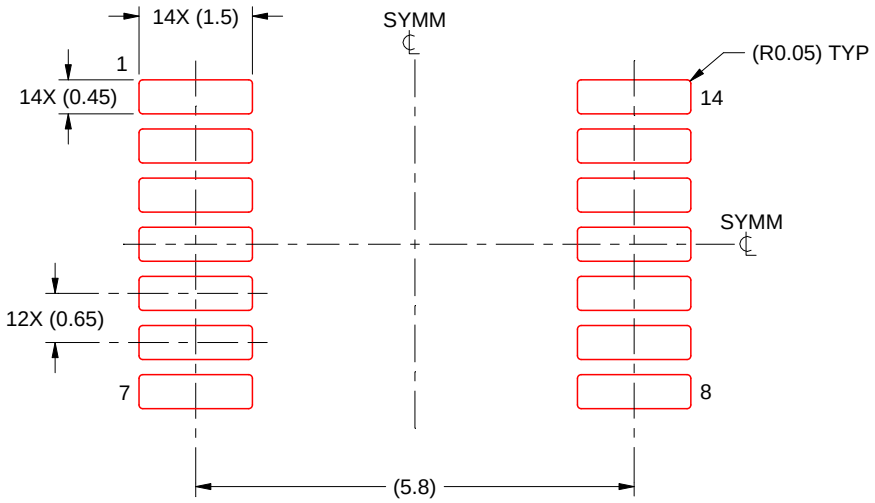


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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