TEXAS INSTRUMENTS

SN75ALS174A 四路差分线路驱动器

1 特性

- 符合或超出 ANSI EIA/TIA-422-B 和 RS-485 的要求
- 高速高级低功耗肖特基电路
- 专为在串行和并行应用中达到 20Mbit/s 的运行速度而设计
- 适用于嘈杂环境中长总线上的多点传输
- 低电源电流，最高 55mA
- 宽正负输入/输出总线电压范围
- 驱动器输出容量：60mA
- 热关断保护
- 驱动器正负电流限制
- 与 SN75174 在功能上可以互换

2 应用

- 电机驱动器
- 工厂自动化和控制

3 说明

SN75ALS174A 是一款具有三态差分输出的四路线路驱动器，设计可满足 ANSI 标准 EIA/TIA-422-B 和 RS-485 的要求。该器件经优化，能够以高达 20Mbit/s 的速率实现平衡多点总线传输。

每个驱动器都具有宽的正负共模输出电压范围，因此适用于嘈杂环境中的合用线应用。

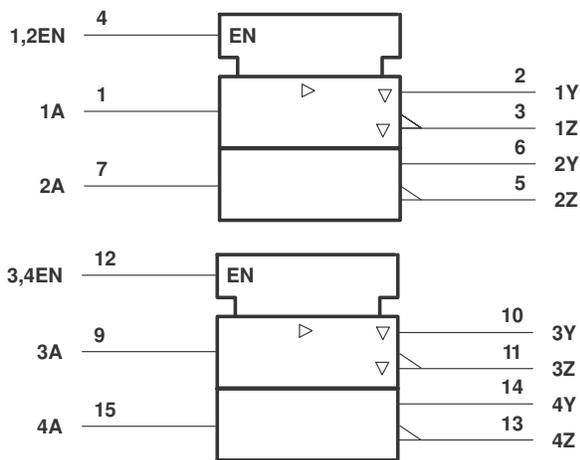SN75ALS174A 可提供正负电流限制和热关断功能，避免传输总线出现线路故障状况。在结温大概为 150°C 时发生关断。

SN75ALS174A 的工作温度范围是 0°C 至 70°C。

封装信息

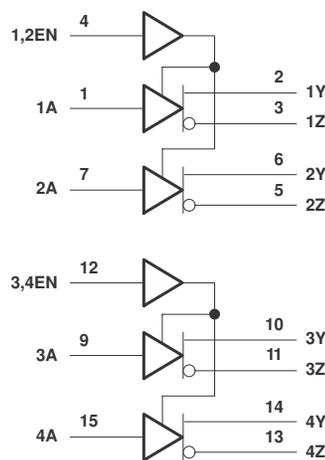| 器件型号	封装[1]	封装尺寸[2]
SN75ALS174A	PDIP (N) (16)	19.3mm x 9.4mm
	SOIC (DW) (20)	12.8mm x 10.3mm
	TSSOP (PW) (20)	6.5mm x 6.4mm

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

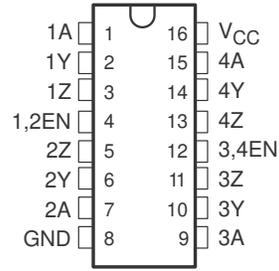A. 所示引脚编号适用于 N 封装。

逻辑符号 [1]

A. 所示引脚编号适用于 N 封装。

逻辑图（正逻辑）

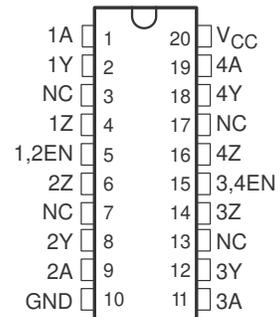[1] 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

Table of Contents

Product Folder Links: *SN75ALS174A*

English Data Sheet: SLLS122

4 Pin Configuration and Functions

```
        ┌───┬─────┬───┐
  1A ─┤ 1 │  U  │16 ├─ V_CC
  1Y ─┤ 2 │     │15 ├─ 4A
  1Z ─┤ 3 │     │14 ├─ 4Y
1,2EN ─┤ 4 │     │13 ├─ 4Z
  2Z ─┤ 5 │     │12 ├─ 3,4EN
  2Y ─┤ 6 │     │11 ├─ 3Z
  2A ─┤ 7 │     │10 ├─ 3Y
 GND ─┤ 8 │     │ 9 ├─ 3A
        └───┴─────┴───┘
```

N Package (Top View)

```
        ┌───┬─────┬───┐
  1A ─┤ 1 │  U  │20 ├─ V_CC
  1Y ─┤ 2 │     │19 ├─ 4A
  NC ─┤ 3 │     │18 ├─ 4Y
  1Z ─┤ 4 │     │17 ├─ NC
1,2EN ─┤ 5 │     │16 ├─ 4Z
  2Z ─┤ 6 │     │15 ├─ 3,4EN
  NC ─┤ 7 │     │14 ├─ 3Z
  2Y ─┤ 8 │     │13 ├─ NC
  2A ─┤ 9 │     │12 ├─ 3Y
 GND ─┤10 │     │11 ├─ 3A
        └───┴─────┴───┘
```

NC – No internal connection

DW, PW Package (Top View)

Product Folder Links: SN75ALS174A

English Data Sheet: SLLS122

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltage, V_{CC} [2]	-0.5	7	V
Input voltage, V_I	-0.5	7	V
Output voltage range, V_O	– 9	14	V
Continuous total dissipation	See the *Dissipation Rating* table		
Storage temperature, T_{stg}	– 65	150	°C

(1)   Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2)   All voltage values are with respect to network GND.

5.2 Dissipation Rating Table

PACKAGE	$T_A \leqslant 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	596 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		V_{cc}	V
V_{IL}	Low-level input voltage	0		0.8	V
V_{OC}	Common-mode output voltage	-7		12	V
I_{OH}	High-level output current	0		– 60	mA
I_{OL}	Low-level output current	0		60	mA
T_A	Operating free-air temperature	0		70	°C

5.4 Thermal Information

		SN75ALS174A			UNIT
THERMAL METRIC[1]		N (PDIP)	DW (SOIC)	PW	
		16 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	66.8	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	34.4	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	39.7	53.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	8.9	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.3	39	53.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1)   For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18mA$				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$|V_{OD1}|$	Differential output voltage	$I_O = 0$		1.5		6	V
$|V_{OD2}|$	Differential output voltage	$R_L = 100\,\Omega$	See Note 图 6-1	1/2 V_{OD1} or 2[2]			V
		$R_L = 54\,\Omega$		1.5	2.5	5	V
$|V_{OD3}|$	Differential output voltage	See [5]		1.5		5	V
$\triangle|V_{OD}|$	Change in magnitude of differential output voltage[3]	$R_L = 54\,\Omega$ or $100\,\Omega$	See 图 6-1			±0.2	V
V_{OC}	Common-mode output voltage[4]	$R_L = 54\,\Omega$ or $100\,\Omega$	See 图 6-1			3	V
						−1	V
$\triangle|V_{OC}|$	Change in magnitude of common-mode output voltage[3]	$R_L = 54\,\Omega$ or $100\,\Omega$	See 图 6-1			±0.2	V
I_O	Output current with power off	$V_{CC} = 0$, $V_O = -7V$ to 12V				±100	µA
I_{OZ}	High-impedance-state output current	$V_O = -7V$ to 12V				±100	µA
I_{IH}	High-level input current	$V_I = 2.7V$				20	µA
I_{IL}	Low-level input current	$V_I = 0.4V$				−100	µA
I_{OS}	Short-circuit output current	$V_O = -7V$ to 12V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		36	55	mA
			Outputs disabled		16	30	mA

(1) All typical values are at $V_{CC} = 5V$ and $T_A = 25°C$.
(2) The minimum V_{OD2} with a $100\,\Omega$ load is either 1/2V_{OD1} or 2V, whichever is greater.
(3) $\triangle|V_{OD}|$ and $\triangle|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(4) In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
(5) See EIA Standard RS-485, Figures 3-5, Test Termination Measurement 2.

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted), $C_L = 50pF$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54\,\Omega$, See 图 6-2	9	15	22	ns
t_{PZH}	Output enable time to high level	$R_L = 110\,\Omega$, See 图 6-3	30	45	70	ns
t_{PZL}	Output enable time to low level	$R_L = 110\,\Omega$, See 图 6-4	25	40	65	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\,\Omega$, See 图 6-3	10	20	35	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\,\Omega$, See 图 6-4	10	30	45	ns

6 Parameter Measurement Information
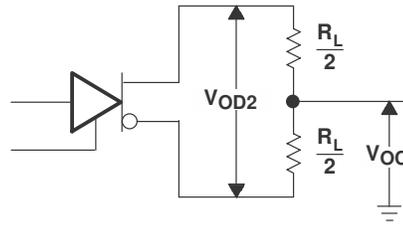
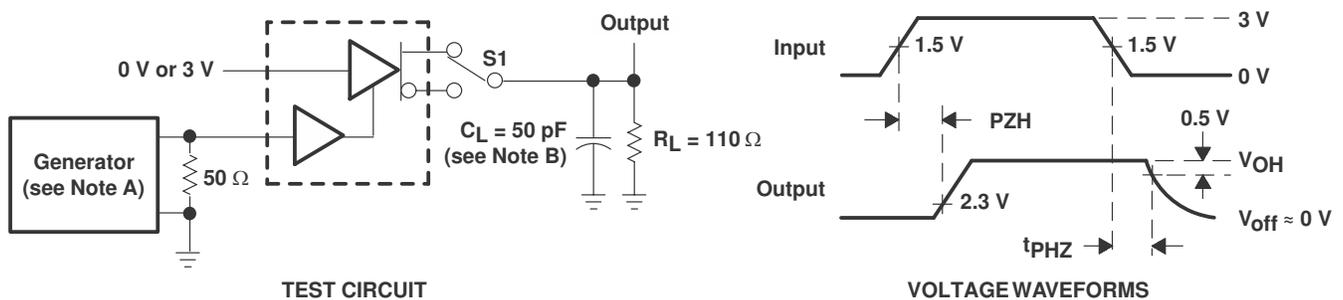Copyright © 2018, Texas Instruments Incorporated

图 6-1. Differential and Common-Mode Output Voltages
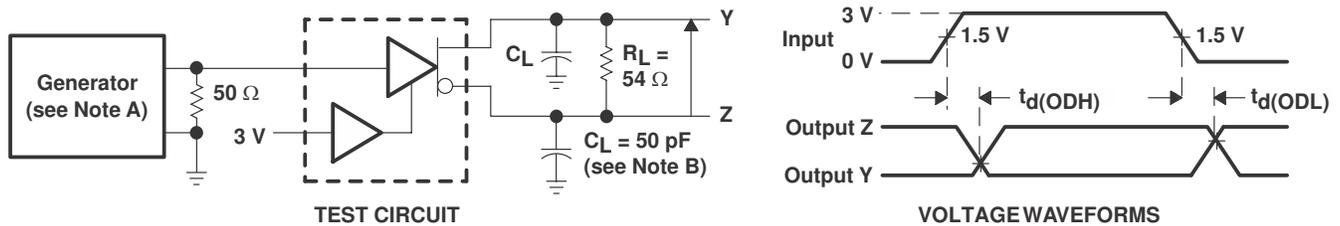
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A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50 Ω, duty cycle = 50%, t_f 5ns, t_r 5ns.
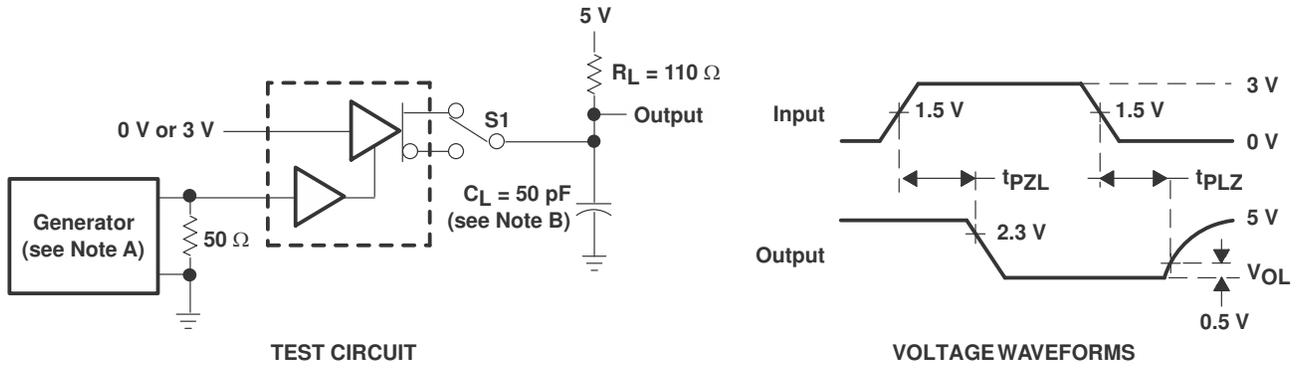
B. C_L includes probe and stray capacitance.

图 6-2. Differential-Output Test Circuit and Delay and Transition Times Voltage Waveforms

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A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50 Ω, duty cycle = 50%, t_f 10ns, t_r 10ns.

B. C_L includes probe and stray capacitance.

图 6-3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

Product Folder Links: *SN75ALS174A*

English Data Sheet: SLLS122

TEST CIRCUIT

VOLTAGE WAVEFORMS

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A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50 Ω, duty cycle = 50%, t_f 5ns, t_r 5ns.

B. C_L includes probe and stray capacitance.

图 6-4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}
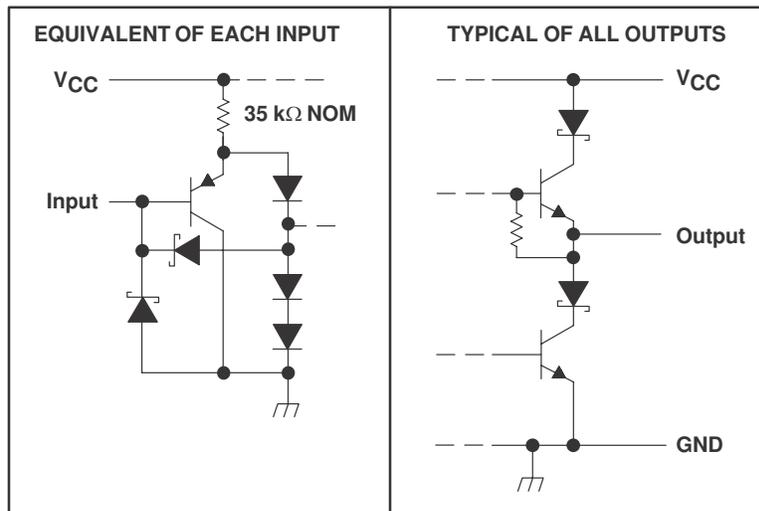
7 Detailed Description

7.1 Device Functional Modes

Function Table (each driver)

INPUT A[1] [2]	ENABLES	OUTPUTS	
		Y	**Z**
H	H	H	L
L	H	L	H
X	L	Z	Z

(1)   H = high level, L = low level, X = irrelevant.

(2)   Z = high impedance (off)

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图 **7-1. Schematics of Inputs and Outputs**

Product Folder Links: *SN75ALS174A*

English Data Sheet: SLLS122

8 Device and Documentation Support

8.1 Documentation Support

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

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8.4 Trademarks

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8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　　　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75ALS174ADW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	0 to 70	
SN75ALS174ADWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A
SN75ALS174ADWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A
SN75ALS174AN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS174AN
SN75ALS174AN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS174AN
SN75ALS174APWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS174A
SN75ALS174APWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS174A

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
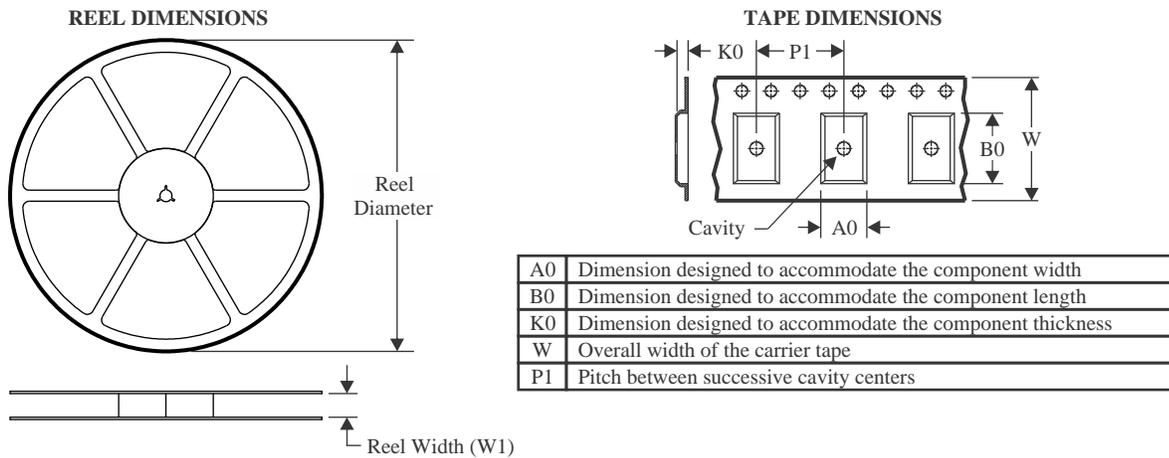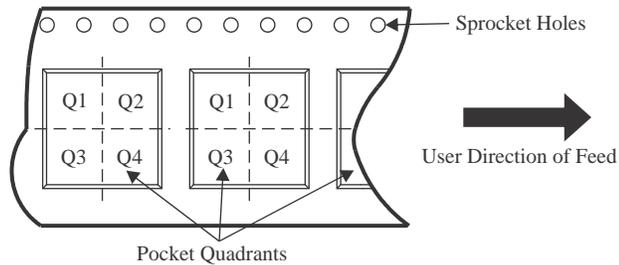
(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS174ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75ALS174APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS
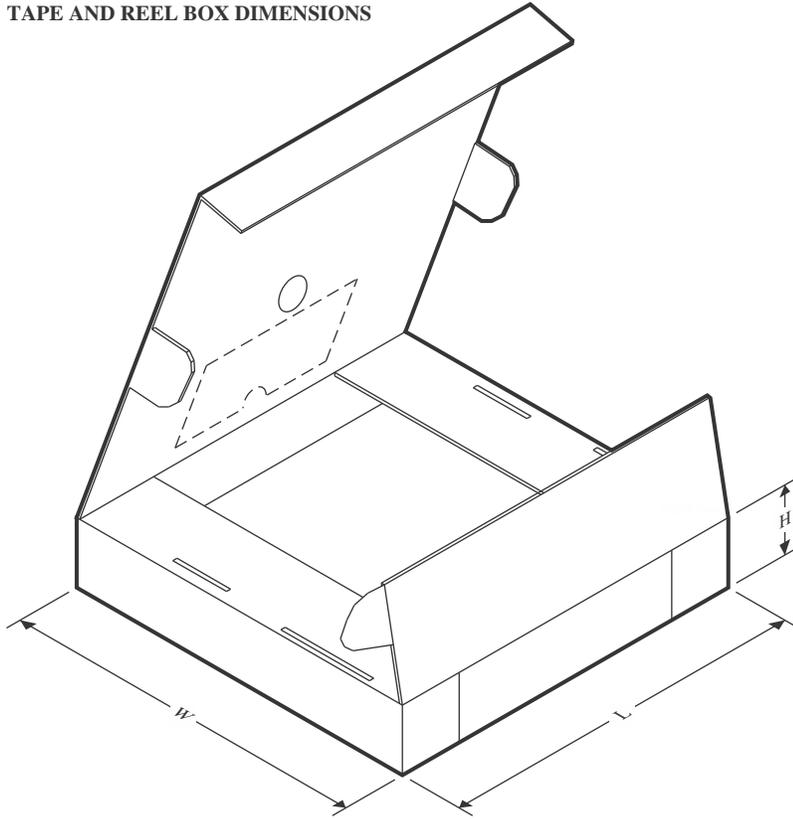
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS174ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN75ALS174APWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
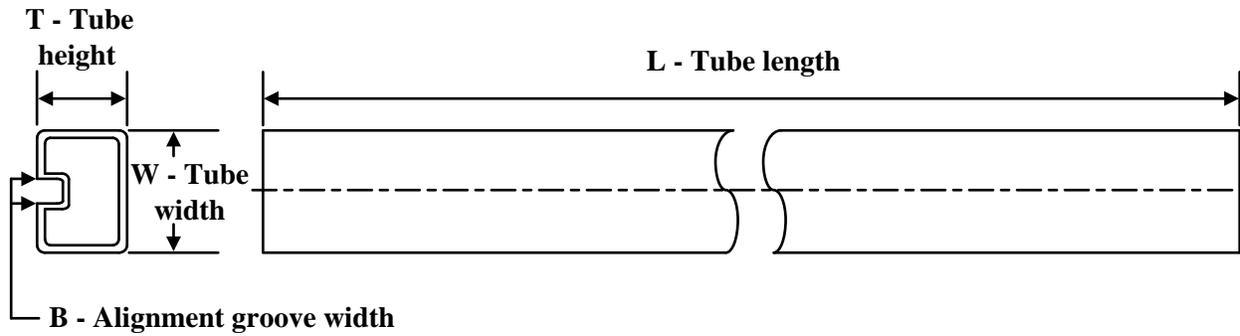
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS174AN	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS174AN.A	N	PDIP	16	25	506	13.97	11230	4.32

PW0020A

SMALL OUTLINE PACKAGE

A

6.6
6.2 TYP

PIN 1 INDEX AREA

1

20

18X [0.65]

6.6
6.4
NOTE 3

2X
[5.85]

10

11

20X 0.30
0.19

B

4.5
4.3
NOTE 4

⊕ [0.1 Ⓜ] C A B

C

SEATING PLANE

[⌒ 0.1 C]

1.2 MAX

SEE DETAIL A

(0.15) TYP

GAGE PLANE

[0.25]

0.15
0.05

0° -8°

0.75
0.50

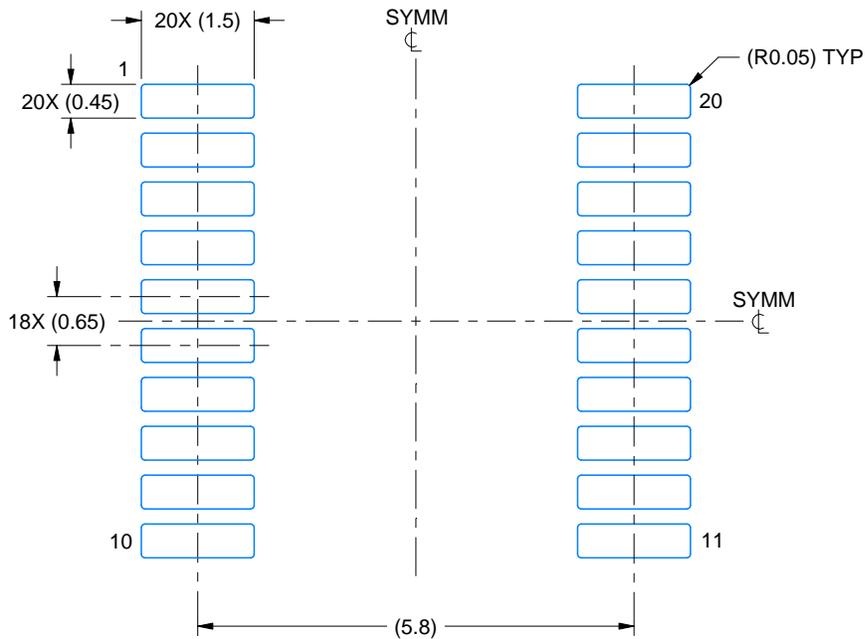DETAIL A
TYPICAL
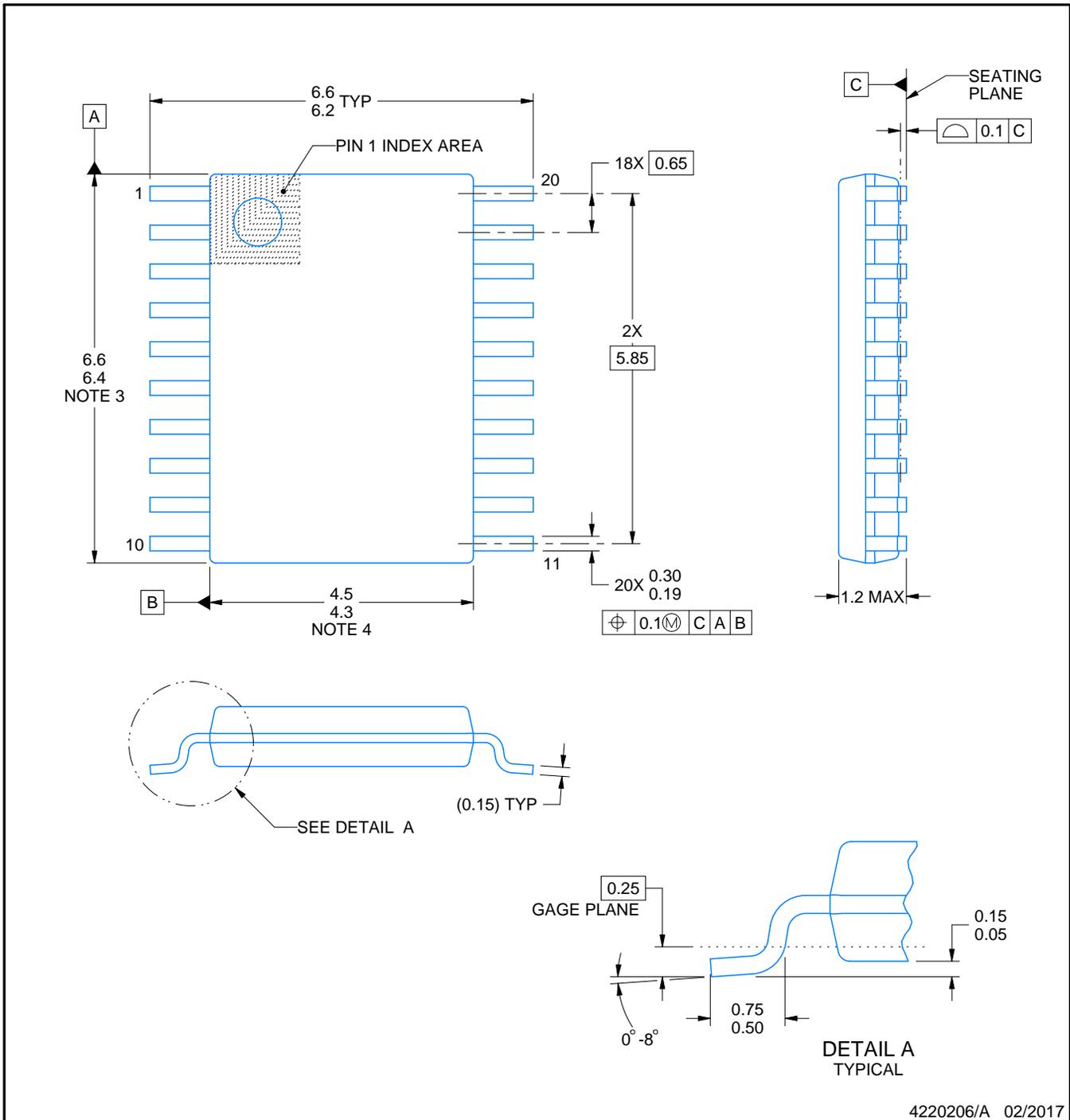
4220206/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

TEXAS
INSTRUMENTS
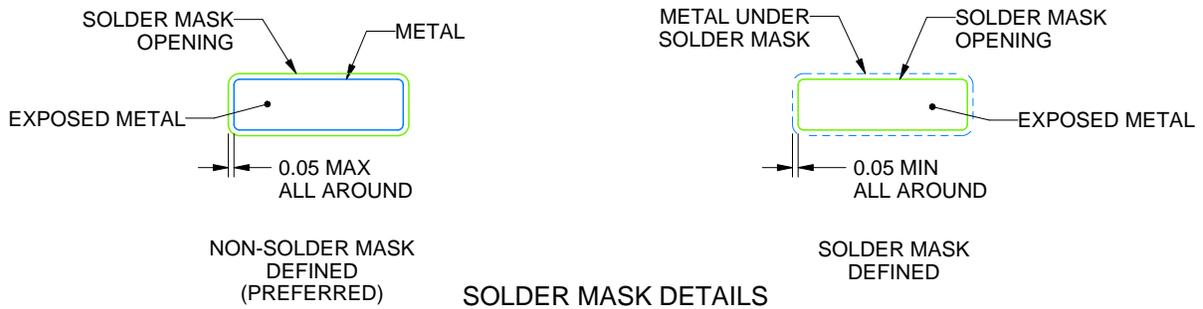www.ti.com

20X (1.5)

SYMM

(R0.05) TYP

1

20

20X (0.45)

18X (0.65)

SYMM

10

11

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS

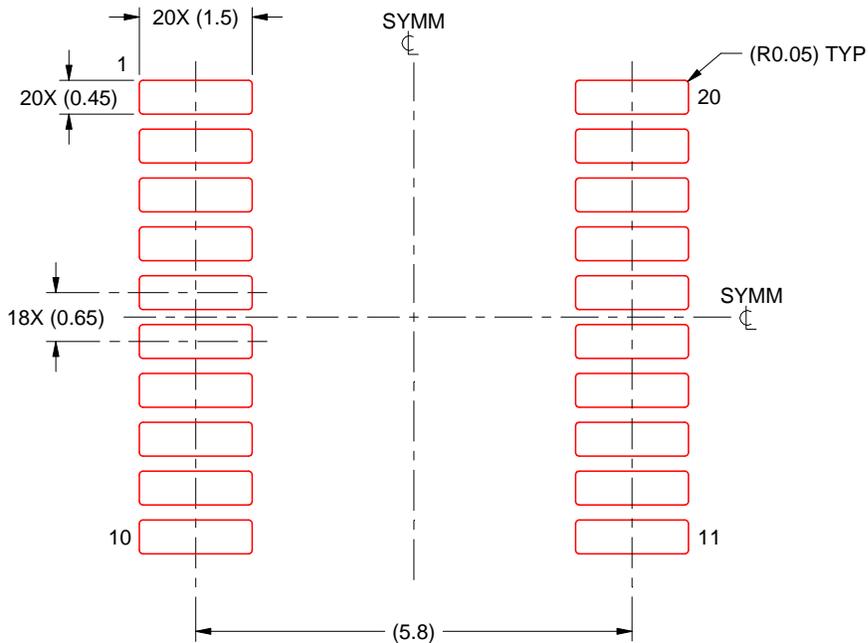SOLDER MASK
DEFINED

4220206/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (1.5)

SYMM

20X (0.45)

1

(R0.05) TYP

20

18X (0.65)

SYMM

10

11

(5.8)

SOLDER PASTE EXAMPLE
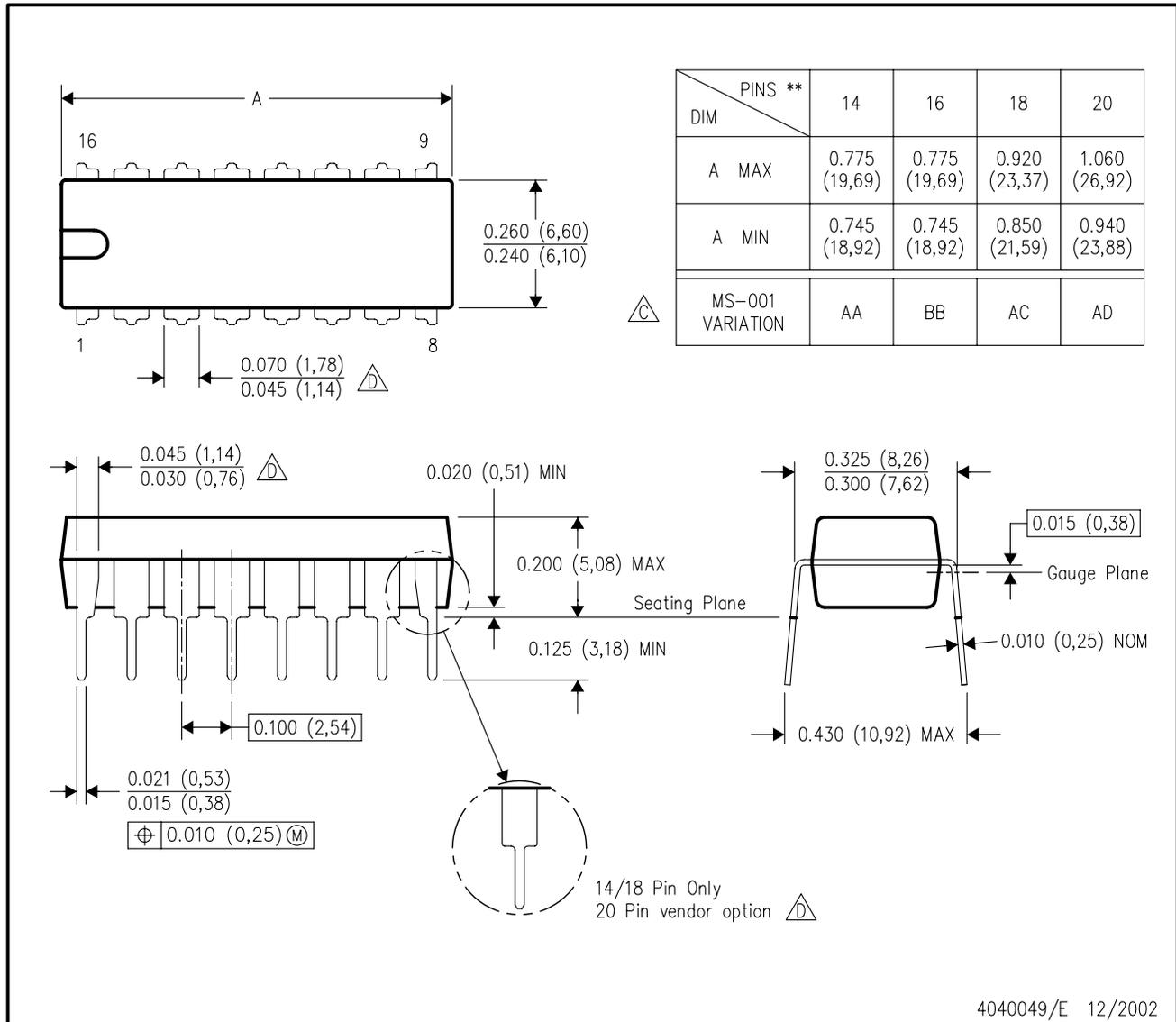BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

$\dfrac{0.260\ (6,60)}{0.240\ (6,10)}$

1   8

$\dfrac{0.070\ (1,78)}{0.045\ (1,14)}$ △D

$\dfrac{0.045\ (1,14)}{0.030\ (0,76)}$ △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

$\dfrac{0.021\ (0,53)}{0.015\ (0,38)}$

⊕ | 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option △D

$\dfrac{0.325\ (8,26)}{0.300\ (7,62)}$

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         D.   The 20 pin end lead shoulder width is a vendor option, either half or full width.
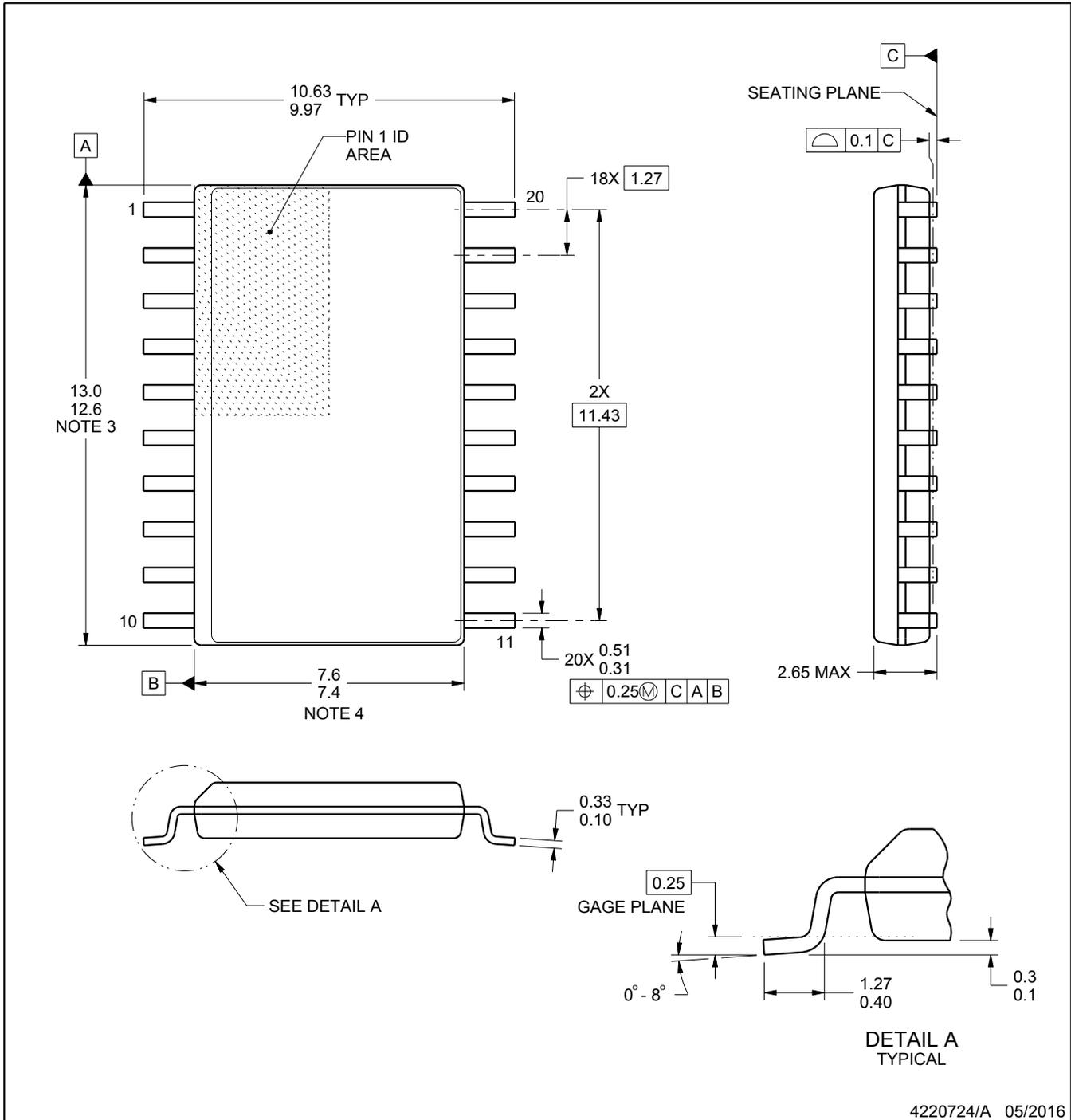
TEXAS
INSTRUMENTS
www.ti.com

DW0020A
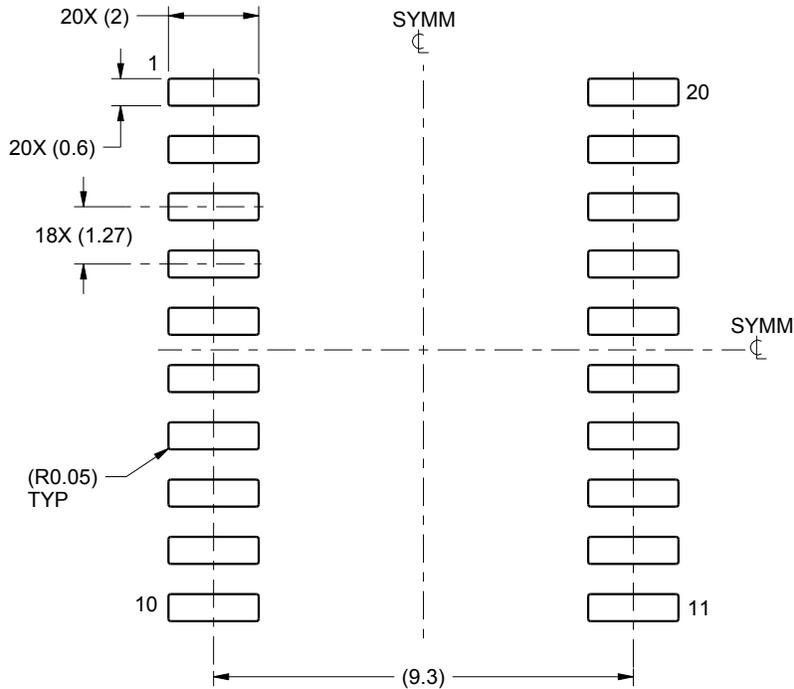
SOIC

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

TEXAS
INSTRUMENTS
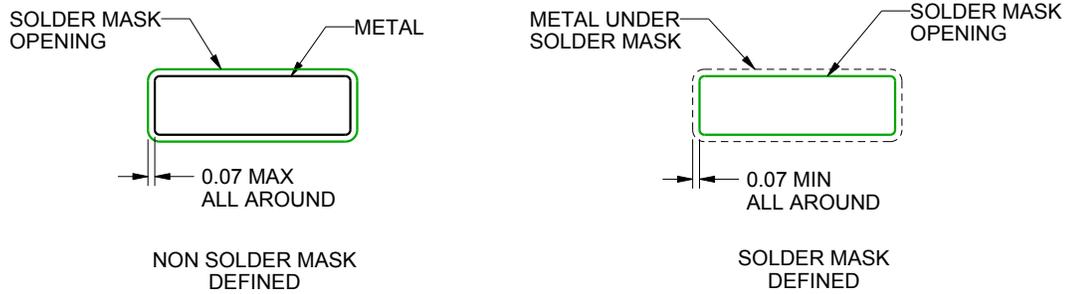www.ti.com

20X (2)

1

SYMM

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

**NON SOLDER MASK
DEFINED**

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND

**SOLDER MASK
DEFINED**

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)
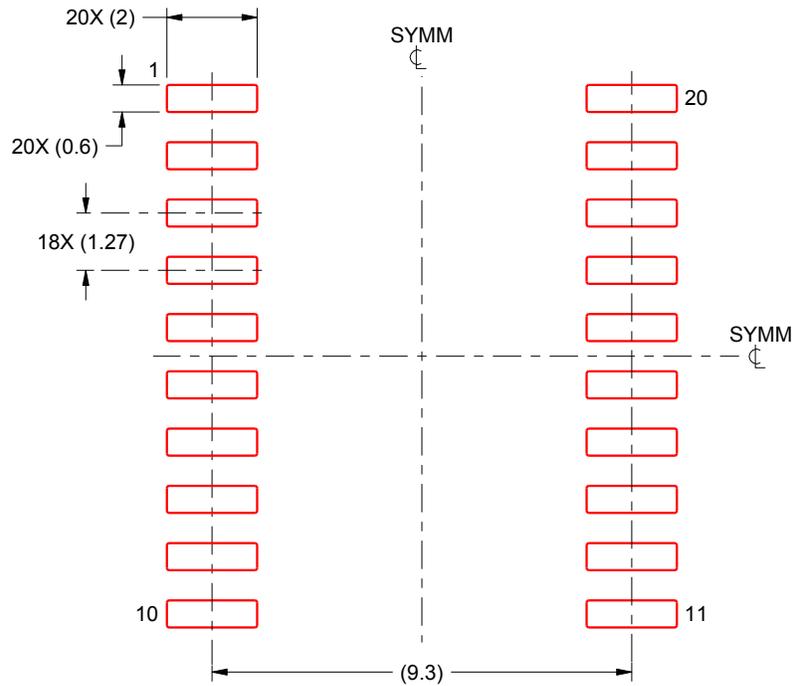
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

SYMM

20

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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