TEXAS INSTRUMENTS
SN55LBC180, SN65LBC180, SN75LBC180
ZHCSQD2I – FEBRUARY 1994 – REVISED OCTOBER 2022

低功耗 RS-485 线路驱动器和接收器对

1 特性

- 专为通过长电缆进行高速多点数据传输而设计
- 以低至 30ns 的脉冲持续时间运行
- 低电源电流：5 mA（最大值）
- 符合或超出 ANSI 标准 RS-485 和 ISO 8482:1987(E) 的要求
- 用于合用总线的三态输出
- -7V 至 12V 的共模电压范围
- 过热关断保护可避免因总线争用导致的驱动器损坏
- 正负输出电流限制
- 引脚与 SN75ALS180 兼容

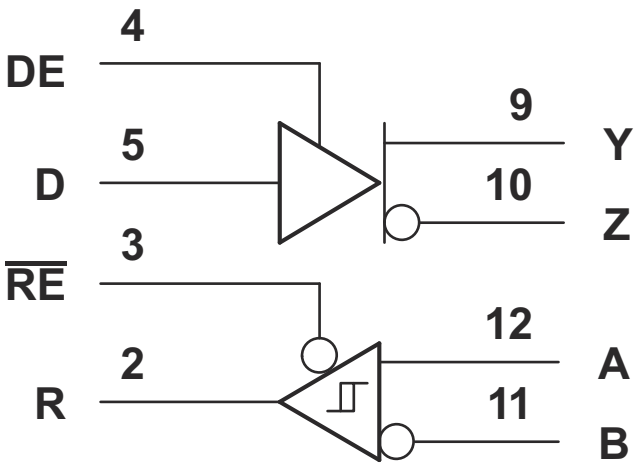
2 说明

SN55LBC180、SN65LBC180 和 SN75LBC180 差分驱动器和接收器对是单片集成电路，设计用于通过具有传输线特性的长电缆进行双向数据通信。它们是平衡或差分电压模式器件，符合或超过行业标准 ANSI RS-485 和 ISO 8482:1987(E) 的要求。这些器件采用 TI 专用 LinBiCMOS™ 进行设计，具有 CMOS 的低功耗以及同一电路中双极晶体管的精度和稳健性。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
SN75LBC180 SN65LBC180	N (PDIP)	19.3 mm x 63.5 mm
	D (SOIC)	8.65mm x 3.91mm
	RSA (QFN)	4mm x 4mm
SN55LBC180	RSA (QFN)	4mm x 4mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图（正逻辑）

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3 说明（续）

SN55LBC180、SN65LBC180 和 SN75LBC180 将差分线路驱动器和接收器与三态输出相结合，并采用 5V 单电源供电。驱动器和接收器分别具有高电平有效和低电平有效使能端，它们可以在外部连接在一起以用作方向控制。驱动器差分输出和接收器差分输入连接到单独的端子以实现全双工工作，并且旨在为总线提供最小负载，无论是禁用还是断电 (V_{CC} = 0)。这些器件具有宽共模电压范围，使其适用于点对点或多点数据总线应用。

这些器件还提供正负输出电流限制和热关断功能，避免出现线路故障状况。线路驱动器在结温约为 172°C 时关闭。

SN75LBC180 可在 0°C 至 70°C 的商业温度范围内运行。SN65LBC180 可在 –40°C 至 85°C 的工业温度范围内运行。

SN55LBC180 的军用级温度范围为 –55°C 至 125°C。

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (June 2022) to Revision I (October 2022) **Page**

- Changed RSA (QFN) values in the *Thermal Information Table* 6

Changes from Revision G (April 2009) to Revision H (June 2022) **Page**

- 将“订购信息”表更改为*封装信息*表....1
- Added the *Pin Configuration and Functions* 4
- Added the *Thermal Information Table* 6
- Fixed the typo in the unit for the Receiver enable I_{IH} to change the unit from A to µA....7
- Updated 图 6-1, 图 6-2, and 图 6-3, limiting the x-axis to a maximum of 70 mA driver output current....9
- Updated 图 9-1 to remove legacy terminology 17

Changes from Revision F (March 2009) to Revision G (April 2009) **Page**

- Added 3 ESD rows to the *Absolute Maximum Ratings* 5

Changes from Revision E (February 2006) to Revision F (March 2009) **Page**

- 将数据表标题中的“差分”更改为“RS-485”....1
- 添加了器件型号 SN55LBC180....1
- 将*两个*更改为*这些*....1
- 添加了“订购信息”表....1
- 更新了*说明 (续)* 部分....2
- 更改了*功能表*并将其从首页移到*说明 (续)* 部分....2
- Deleted condition, moved cross reference....5
- Added all symbols in text that were not appearing in the PDF....5
- Deleted T_A row from the *Absolute Maximum Ratings* 5
- Added the last column to *Dissipation Rating Table* 5
- Added a row to T_A in the *Recommended Operating Conditions* for SN55LBC180....5
- Added SN55LB180 to the $|V_{OD}|$ row....6
- Change: moved 5 max values to the min column (-1.5, -50, -100, -0.8, -0.8)....7
- Added the *Switching Characteristics: SN55LBC180* table 8
- Changed moved schematics to the Typical Characteristics section....16

5 Pin Configuration and Functions

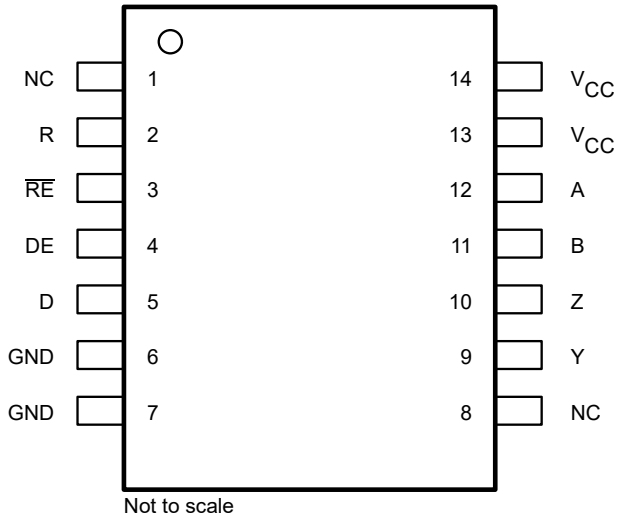


图 5-1. D OR N Package (SOIC)
(Top View)

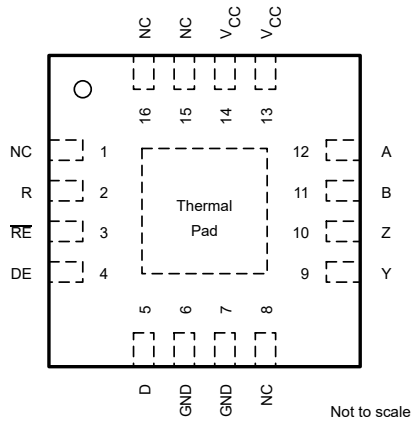


图 5-2. RSA Package (QFN)
(Top View)

表 5-1. Pin Functions

PIN NAME	PIN NO		TYPE(1)	DESCRIPTION
	D Or N	RSA		
NC	1	1	NC	No internal connection
R	2	2	O	Receiver output
$\overline{RE}$	3	3	I	Receiver enable input. Active low.
DE	4	4	I	Driver enable input. Active high
D	5	5	I	Driver input pin
GND	6, 7	6, 7	G	Ground connection. Pins 6 and 7 are connected together internally.
NC	8	8	NC	No internal connection
Y	9	9	O	Bus output port (complementary to Z)
Z	10	10	O	Bus output port (complementary to Y)
B	11	11	I	Bus input port (complementary to A)
A	12	12	I	Bus input port (complementary to B)
V_{CC}	13, 14	13, 14	P	Supply input pins. Pins 13 and 14 are connected together internally.
NC	N/A	15, 16	NC	No internal connection

(1) Signal Types: I = Input, O = Output, P= Power input,

6 Specifications

6.1 Absolute Maximum Ratings

See note (1)

				UNIT
V_{CC}	Supply voltage range (2)		– 0.3 to 7	V
V_{BUS}	Bus voltage range (A, B, Y, Z)(2)		– 10 to 15	V
	Voltage range at D, R, DE, $\overline{RE}$ (2)		– 0.3 to V_{CC} + 0.5	V
	Continuous total power dissipation(3)		Internally limited	
	Total power dissipation		See Dissipation Rating Table	
T_{stg}	Storage temperature range		– 65 to 150	°C
I_O	Receiver output current range		– 50 to 50	mA
ESD	Electrostatic discharge	HBM (Human Body Model) EIA/JESD22-A114	±4	kV
		MM (Machine Model) EIA/JESD22-A115	400	V
		CDM (Charge Device Model) EIA/JESD22-C101	1.5	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

6.2 Dissipation Rating Table

PACKAGE(1)	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	—
N	1150 mW	9.2 mW/°C	736 mW	598 mW	—
RSA	3333 mW	26.67 mW/°C	2133 mW	1733 mW	400 mW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage		– 6(1)		6	V
V_O, V_I, or V_{IC}	Voltage at any bus terminal (separately or common mode)	A, B, Y, or Z	– 7(1)		12	V
I_{OH}	High-level output current	Y or Z			– 60	mA
		R			– 8	
I_{OL}	Low-level output current	Y or Z			60	mA
		R			8	
T_A	Operating free-air temperature	SN55LBC180	– 55		125	°C
		SN65LBC180	– 40		85	
		SN75LBC180	0		70	

(1) The algebraic convention where the least positive (more negative) limit is designated minimum, is used in this data sheet for the differential input voltage, voltage at any bus terminal, operating temperature, input threshold voltage, and common-mode output voltage.

6.4 Thermal Information Table

THERMAL METRIC[1]		D (SOIC)	N (PDIP)	RSA (QFN)	UNIT
		14 Pins	14 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	53.4	38.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.5	40.0	35.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	33.2	17.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.2	19.0	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.9	32.9	17.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	7.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Driver Section

6.5.1 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA				–1.5	V
$\lvert V_{OD} \rvert$	Differential output voltage magnitude[2]	R_L = 54 Ω, See 图 7-1	SN55LBC180	1	2.5	5	V
			SN65LBC180	1.1	2.5	5	
			SN75LBC180	1.5	2.5	5	
		R_L = 60 Ω, See 图 7-2	SN55LBC180	1	2.5	5	
			SN65LBC180	1.1	2	5	
			SN75LBC180	1.5	2	5	
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage[3]	See 图 7-1 and 图 7-2				±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω,	See 图 7-1	1	2.5	3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage[3]					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = –7 V to 12 V			±100	µA
I_{OZ}	High-impedance-state output current	V_O = –7 V to 12 V				±100	µA
I_{IH}	High-level input current	V_I = 2.4 V				100	µA
I_{IL}	Low-level input current	V_I = 0.4 V				100	µA
I_{OS}	Short-circuit output current	–7 V ≤ V_O ≤ 12 V				±250	mA
I_{CC}	Supply current	Receiver disabled	Outputs enabled			5	mA
			Outputs disabled			3	

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) The minimum V_{OD} specification may not fully comply with ANSI RS-485 at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal-transmission distance.
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

6.5.2 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	See 图 7-3	7	12	18	ns
$t_{t(OD)}$	Differential output transition time			5	10	20	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See 图 7-4			35	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See 图 7-5			35	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See 图 7-4			50	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See 图 7-5			35	ns

6.5.3 Switching Characteristics: SN55LBC180

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	See 图 7-3		15		ns
$t_{t(OD)}$	Differential output transition time				21		ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See 图 7-4		32		ns
t_{PHZ}	Output disable time from high level				55		
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See 图 7-5		32		ns
t_{PLZ}	Output disable time from low level				20		

6.6 Receiver Section

6.6.1 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = – 8 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA		– 0.2			V
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})				45		mV
V_{IK}	Enable-input clamp voltage	I_I = – 18 mA		-1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = – 8 mA	3.5	4.5		V
V_{OL}	Low-level output voltage	V_{ID} = – 200 mV,	I_{OL} = 8 mA		0.3	0.5	V
I_{OZ}	High-impedance-state output current	V_O = 0 V to V_{CC}				±20	μA
I_{IH}	High-level enable-input current	V_{IH} = 2.4 V		– 50			μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V		– 100			μA
I_I	Bus input current	V_I = 12 V, V_{CC} = 5 V,	Other input at 0 V		0.7	1	mA
		V_I = 12 V, V_{CC} = 0 V,	Other input at 0 V		0.8	1	
		V_I = -7 V, V_{CC} = 5 V,	Other input at 0 V	– 0.8	-0.5		
		V_I = -7 V, V_{CC} = 0 V,	Other input at 0 V	– 0.8	– 0.5		
I_{CC}	Supply current	Driver disabled	Outputs enabled			5	mA
			Outputs disabled			3	

6.6.2 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = –1.5 V to 1.5 V, See 图 7-6	11	22	33	ns
t_{PLH}	Propagation delay time, low- to high-level output		11	22	33	ns
$t_{sk(p)}$	Pulse skew (| t_{PHL} – t_{PLH}|)			3	6	ns
t_t	Transition time			5	8	ns
t_{PZH}	Output enable time to high level	See 图 7-7			35	ns
t_{PZL}	Output enable time to low level				30	ns
t_{PHZ}	Output disable time from high level				35	ns
t_{PLZ}	Output disable time from low level				30	ns

6.6.3 Switching Characteristics: SN55LBC180

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = –1.5 V to 1.5 V, See 图 7-6		26		ns
t_{PLH}	Propagation delay time, low- to high-level output			23		ns
$t_{sk(p)}$	Pulse skew (| t_{PHL} – t_{PLH}|)			3		ns
$t_{sk(p)t}$	Transition time			4		ns
t_{PZH}	Output enable time to high level	See 图 7-4		30		ns
t_{PHZ}	Output disable time from high level			26		ns
t_{PZL}	Output enable time to low level			30		ns
t_{PLZ}	Output disable time from low level			30		ns

6.7 Typical Characteristics

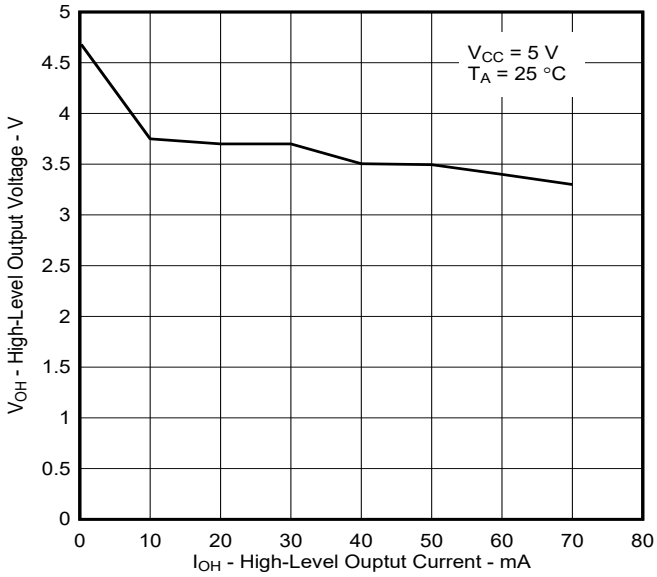


图 6-1. Driver High-Level Output Voltage vs High-Level Output Current

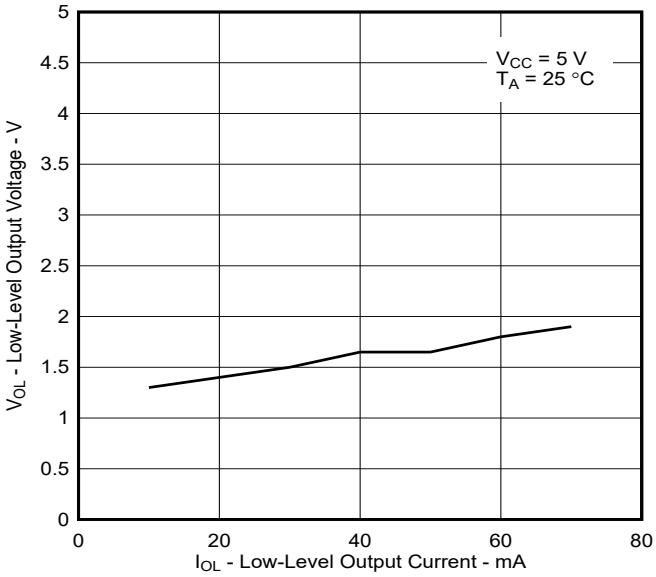


图 6-2. Driver Low-Level Output Voltage vs Low-Level Output Current

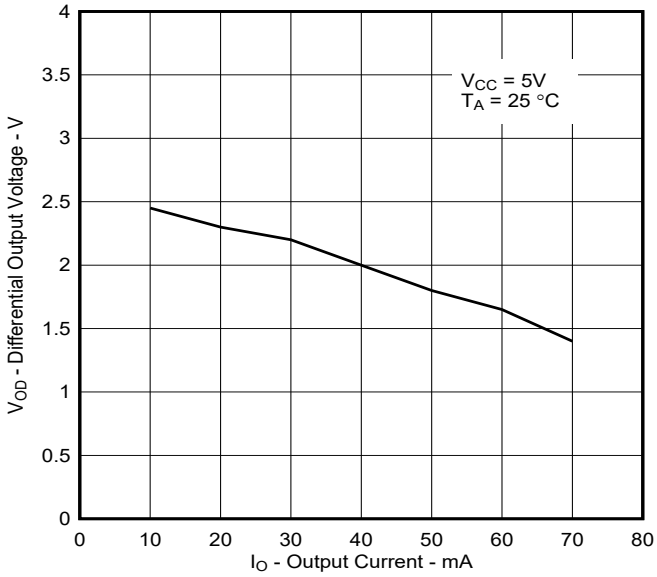


图 6-3. Driver Differential Output Voltage vs Output Current

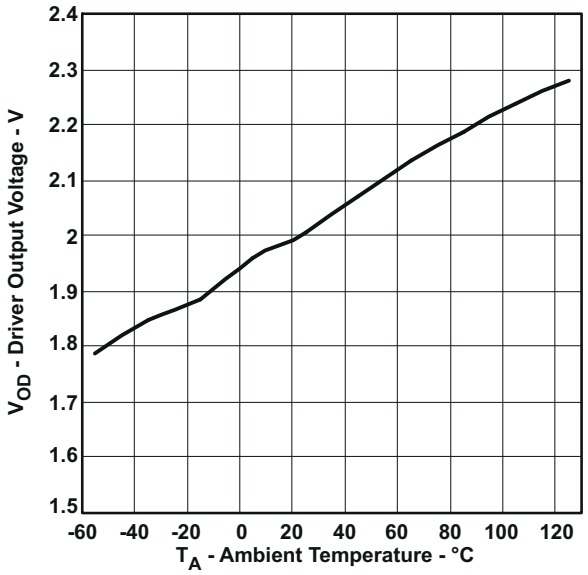


图 6-4. Driver Differential Output Voltage vs Free-Air Temperature

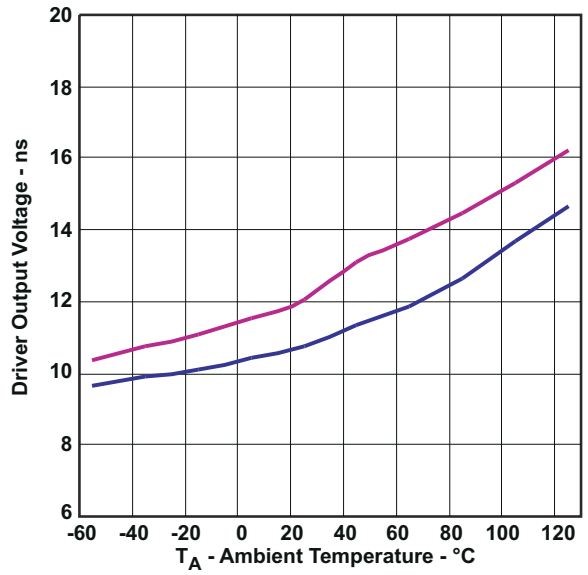


图 6-5. Driver Differential Delay Times vs Free-Air Temperature

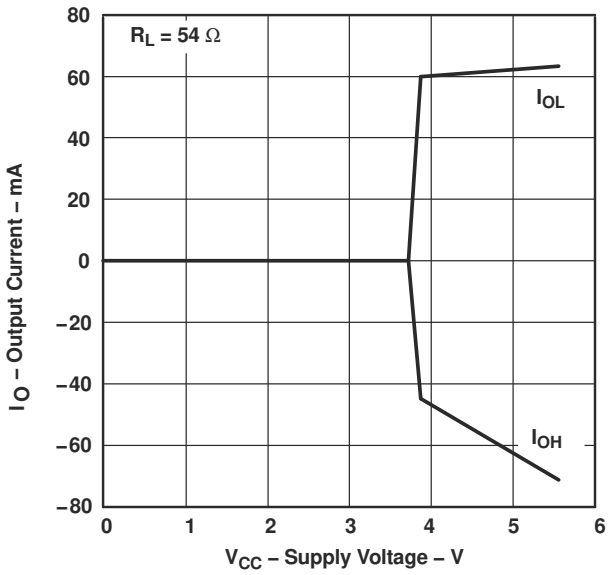


图 6-6. Driver Output Current vs Supply Voltage

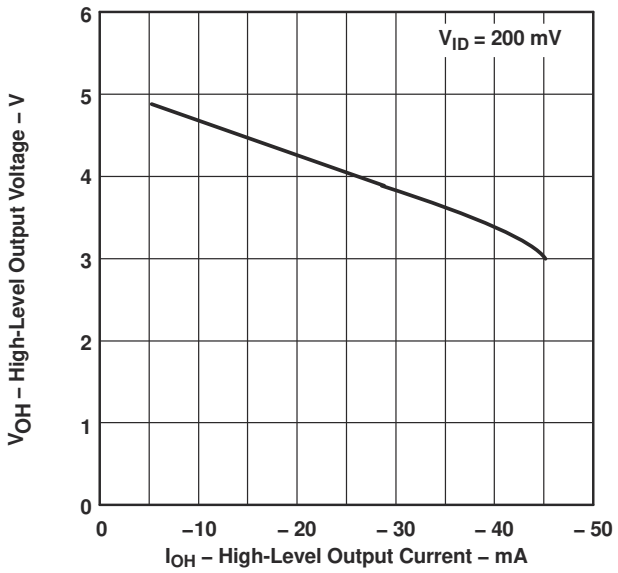


图 6-7. Receiver High-Level Output Voltage vs High-Level Output Current

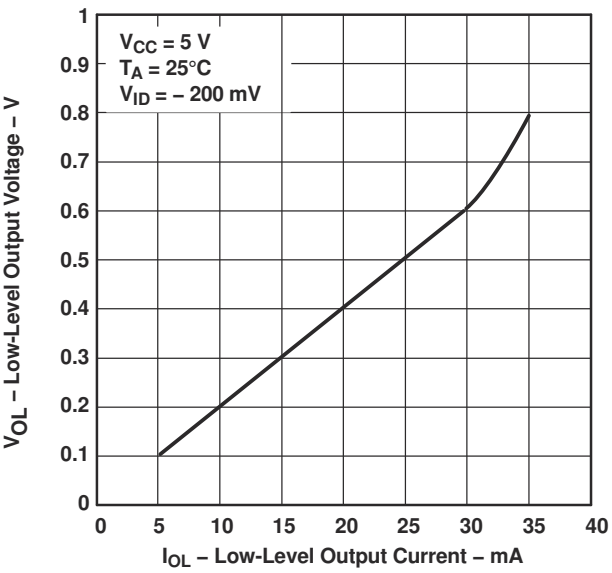


图 6-8. Receiver Low-Level Output Voltage vs Low-Level Output Current

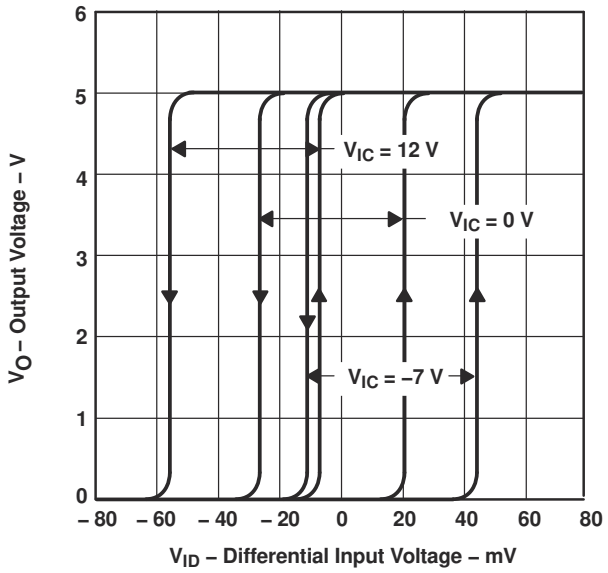


图 6-9. Receiver Output Voltage vs Differential Input Voltage

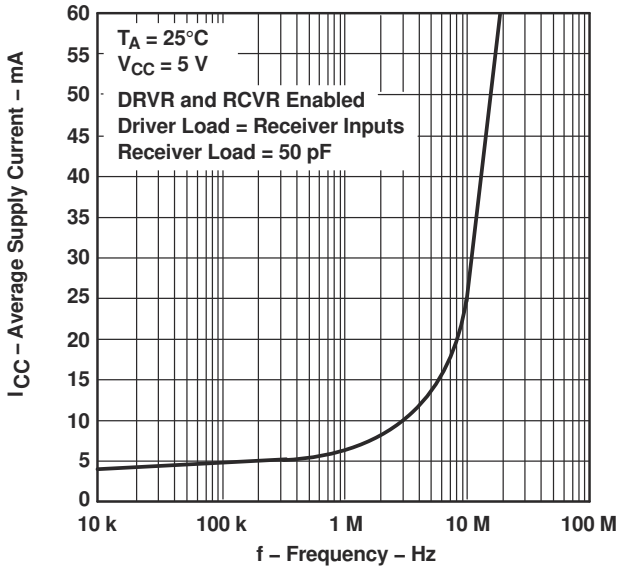


图 6-10. Average Supply Current vs Frequency

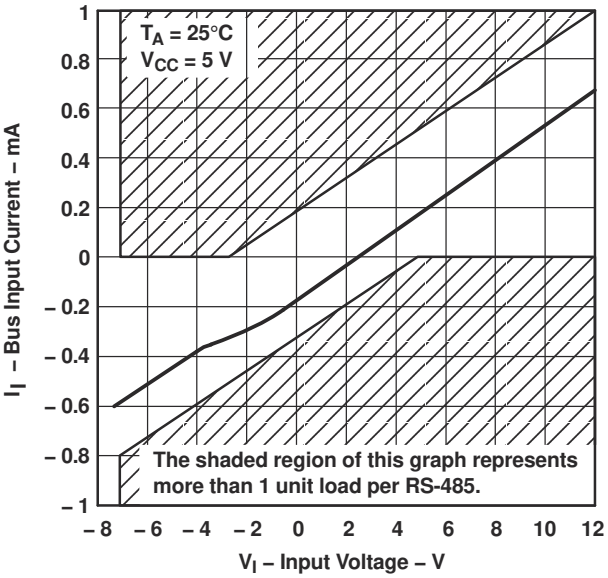


图 6-11. Receiver Bus Input Current vs Input Voltage (Complementary Input at 0 V)

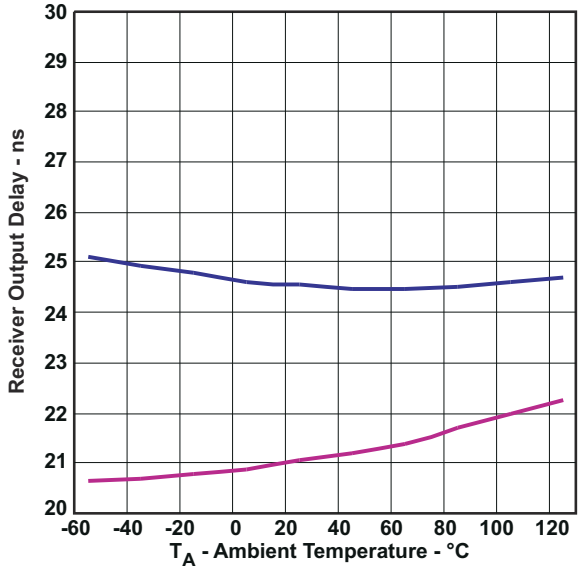


图 6-12. Receiver Propagation DELAY TI vs Free-Air Temperature

7 Parameter Measurement Information

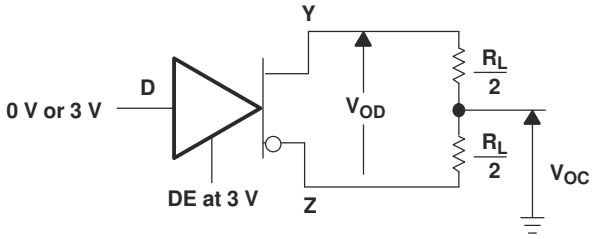


图 7-1. Differential and Common-Mode Output Voltages

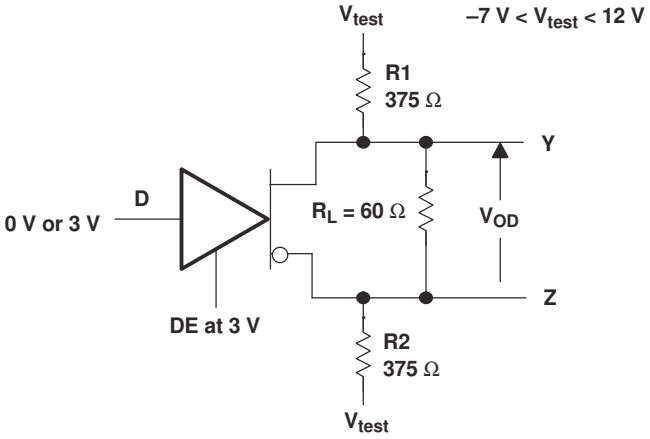
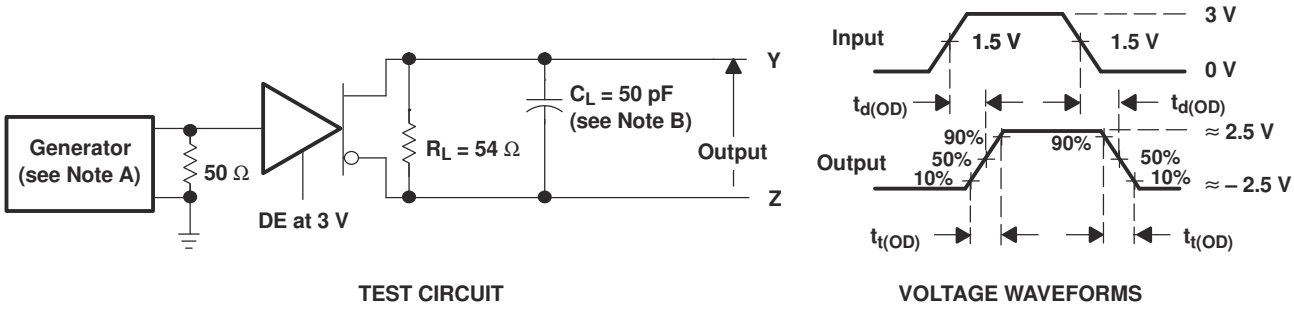


图 7-2. Driver V_{OD} Test Circuit



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR > 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

图 7-3. Driver Test Circuit and Differential Output Delay and Transition Time Voltage Waveforms

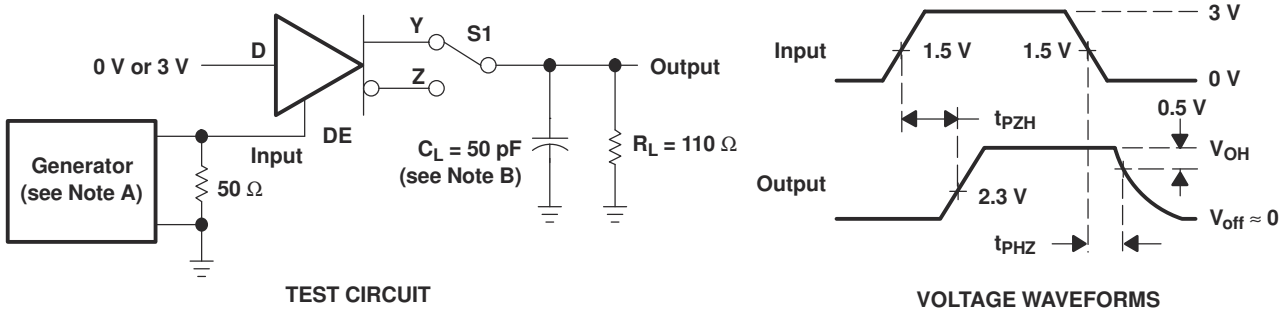


图 7-4. Driver Test Circuit and Enable and Disable Time Waveforms

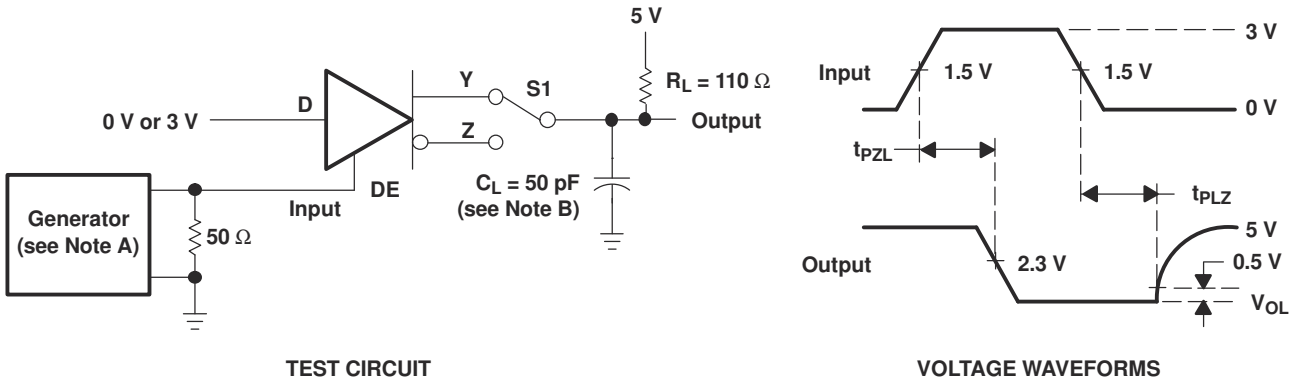
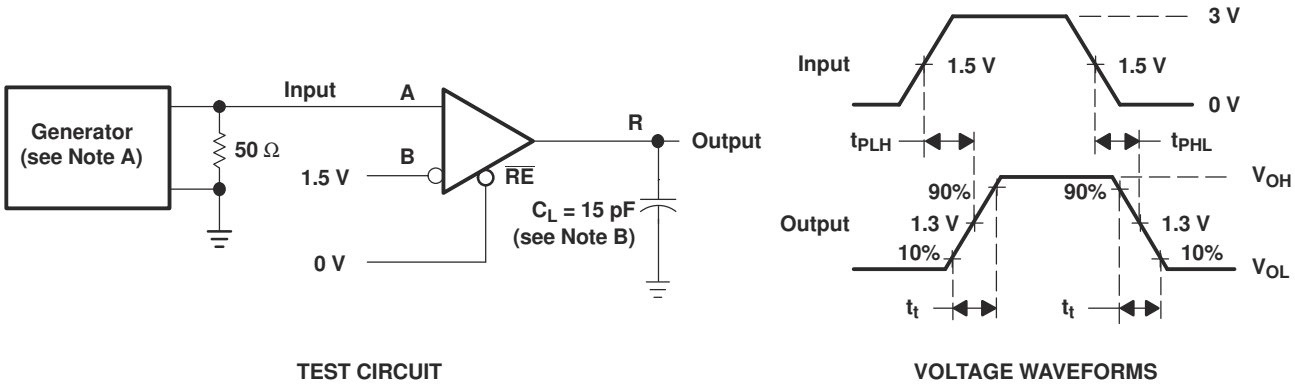
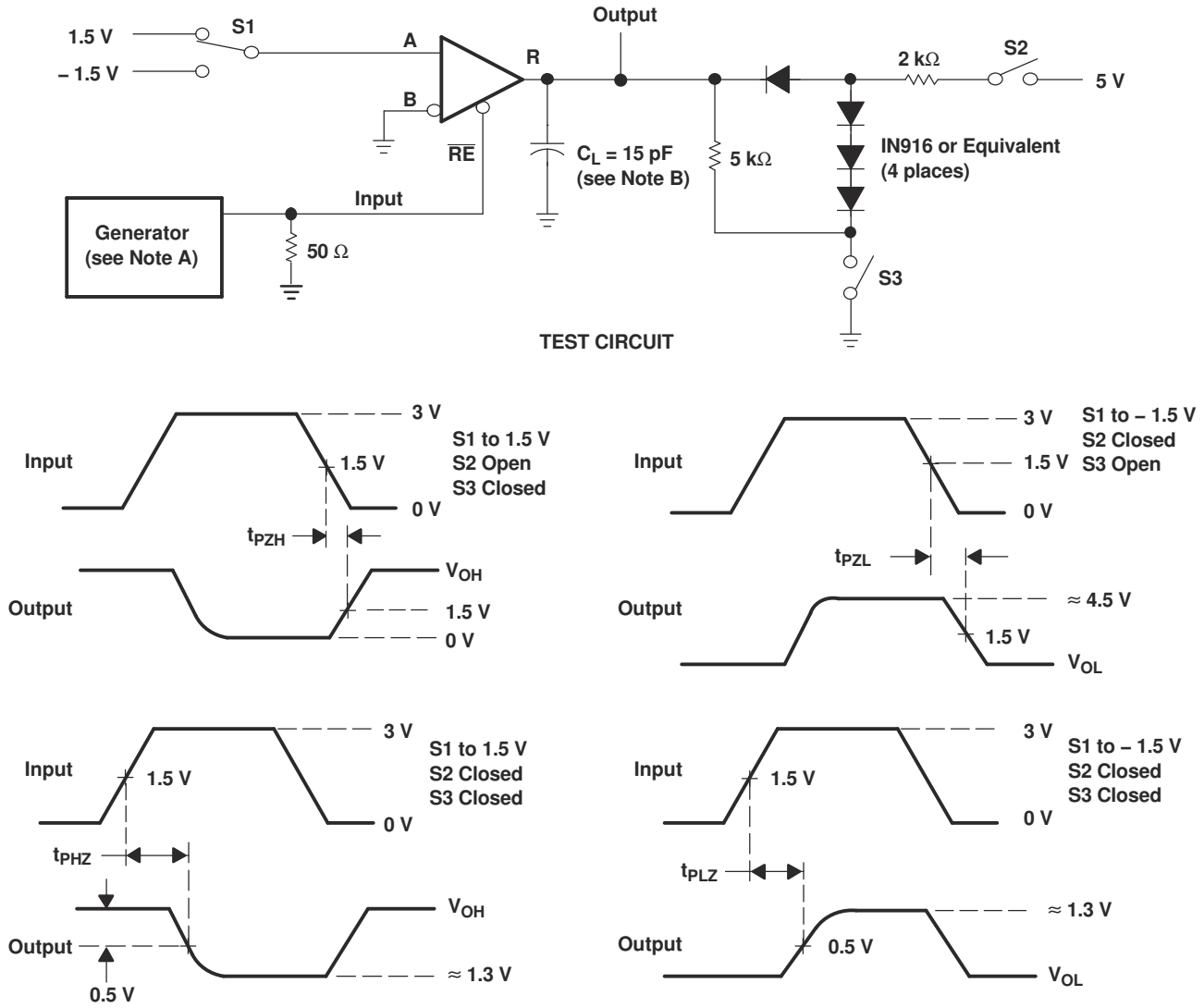


图 7-5. Driver Test Circuit and Enable and Disable Time Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

图 7-6. Receiver Test Circuit and Propagation Delay Time Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

图 7-7. Receiver Output Enable and Disable Times

8 Detailed Description

8.1 Function Tables

表 8-1. DRIVER

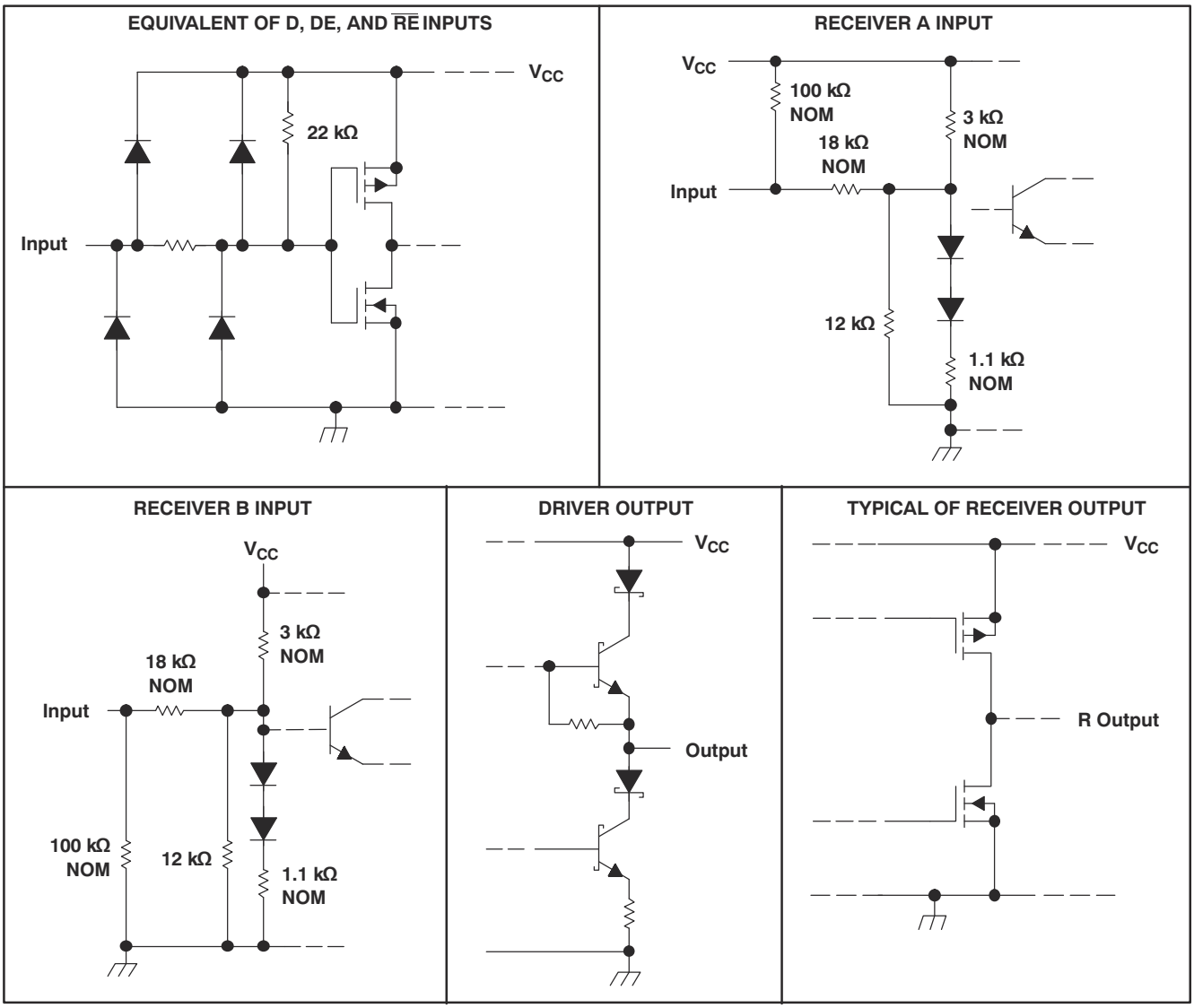
INPUT D(1)	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, ? = Indeterminate, X = irrelevant, Z = high impedance (off)

表 8-2. RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R	
		Y	Z
$V_{ID} \geq 0.2$ V	L	H	
-0.2 V < V_{ID} < 0.2 V	L	?	
$V_{ID} \leq -0.2$ V	L	L	
X	H	Z	
Open circuit	L	H	

8.2 Schematics of Inputs and Outputs



9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

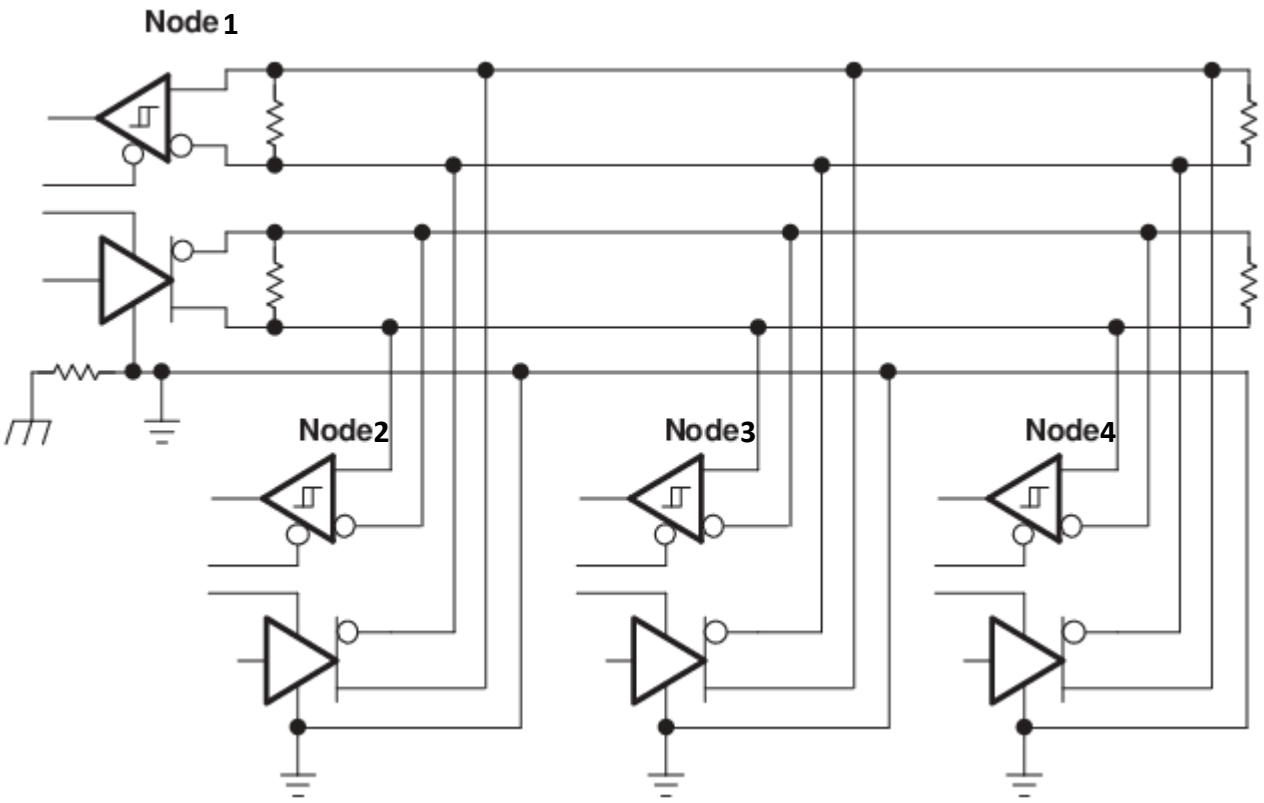


图 9-1. Full Duplex Application Circuit

10 Device and Documentation Support

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 商标

LinBiCMOS™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN55LBC180RSAR	ACTIVE	QFN	RSA	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	SN55 LBC180	Samples
SN65LBC180DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB180	Samples
SN65LBC180DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB180	Samples
SN65LBC180N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN65LBC180N	Samples
SN65LBC180RSAR	ACTIVE	QFN	RSA	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BL180	Samples
SN75LBC180DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	7LB180	
SN75LBC180N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75LBC180N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN55LBC180, SN75LBC180 :

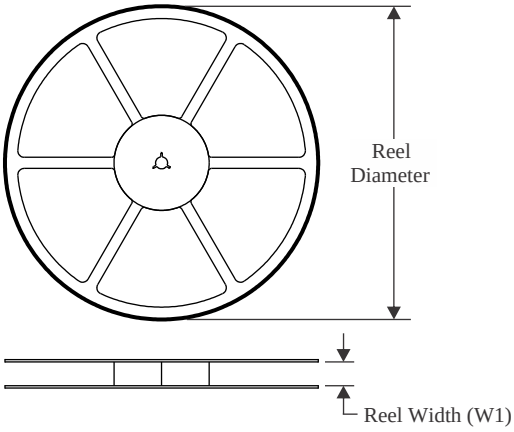
- Catalog : SN75LBC180
- Military : SN55LBC180

NOTE: Qualified Version Definitions:

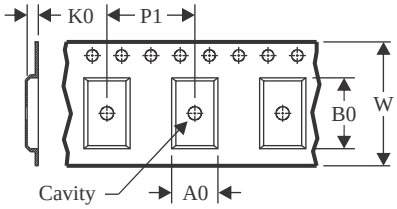
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

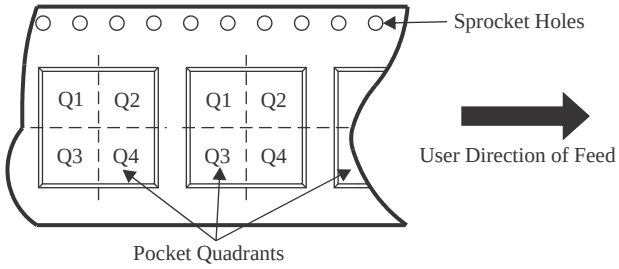


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

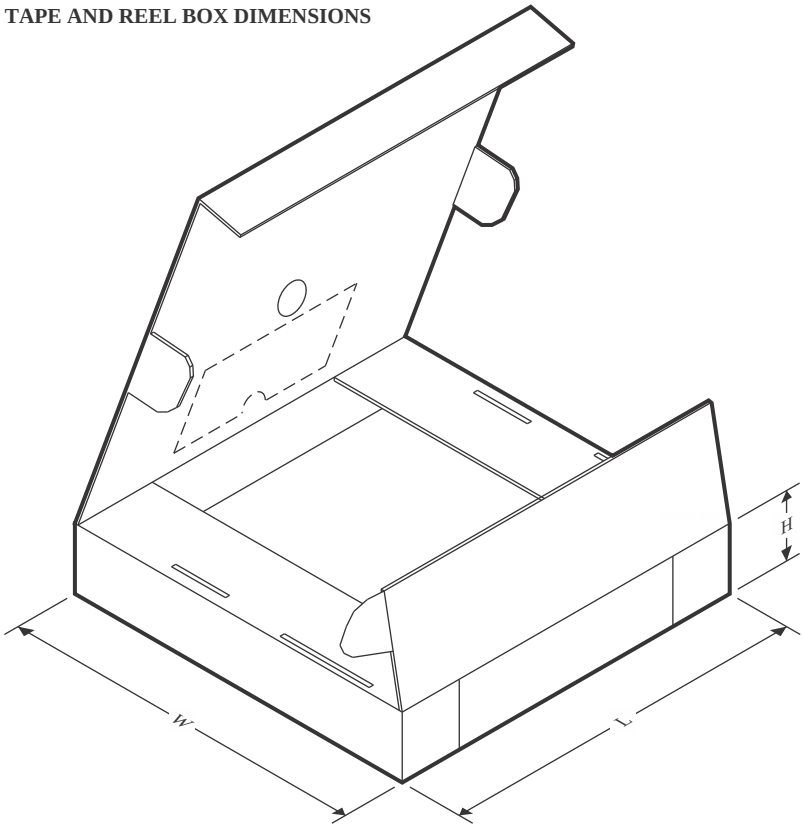
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN55LBC180RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65LBC180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65LBC180RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

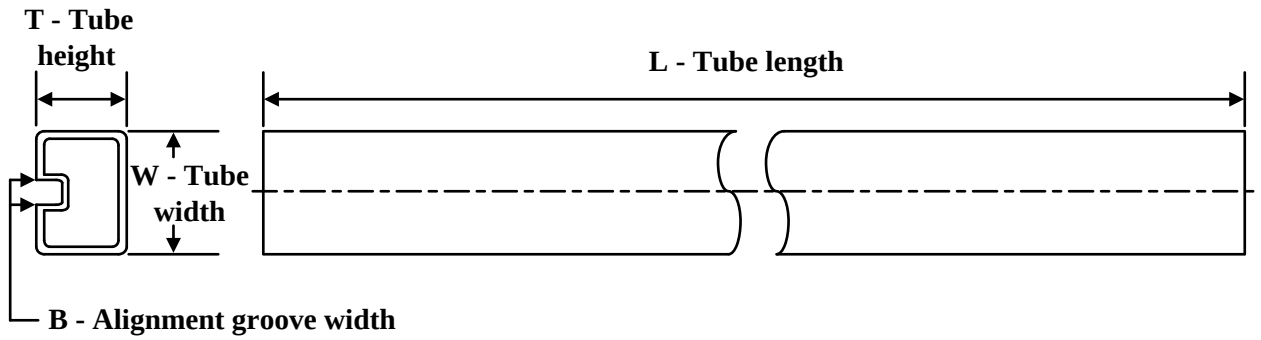
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN55LBC180RSAR	QFN	RSA	16	3000	367.0	367.0	35.0
SN65LBC180DR	SOIC	D	14	2500	356.0	356.0	35.0
SN65LBC180RSAR	QFN	RSA	16	3000	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC180N	N	PDIP	14	25	506	13.97	11230	4.32
SN75LBC180N	N	PDIP	14	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

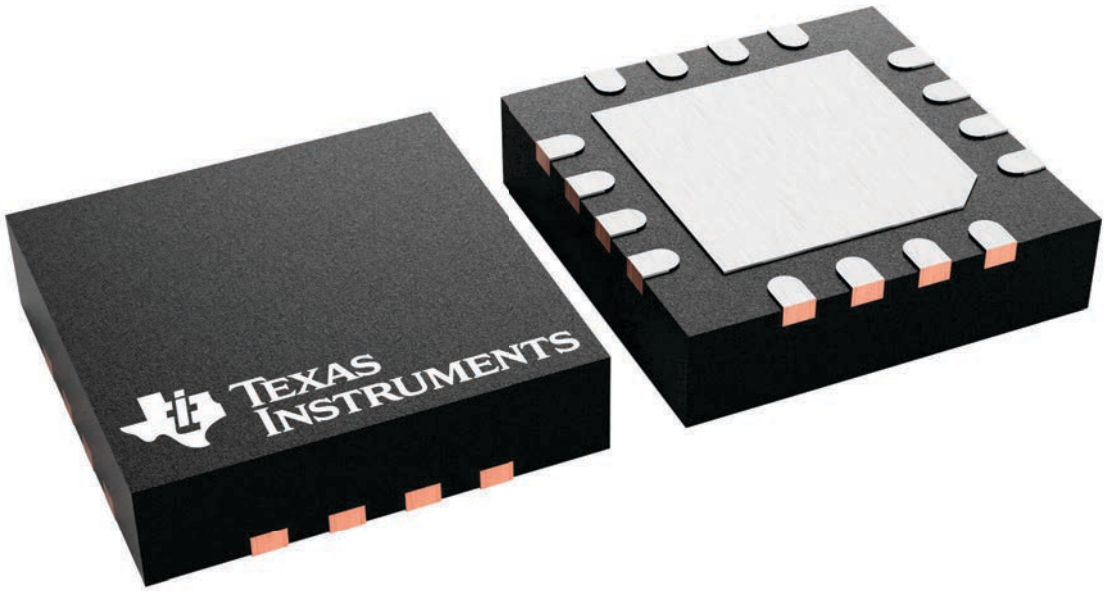
RSA 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

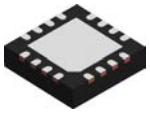
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4230969/A

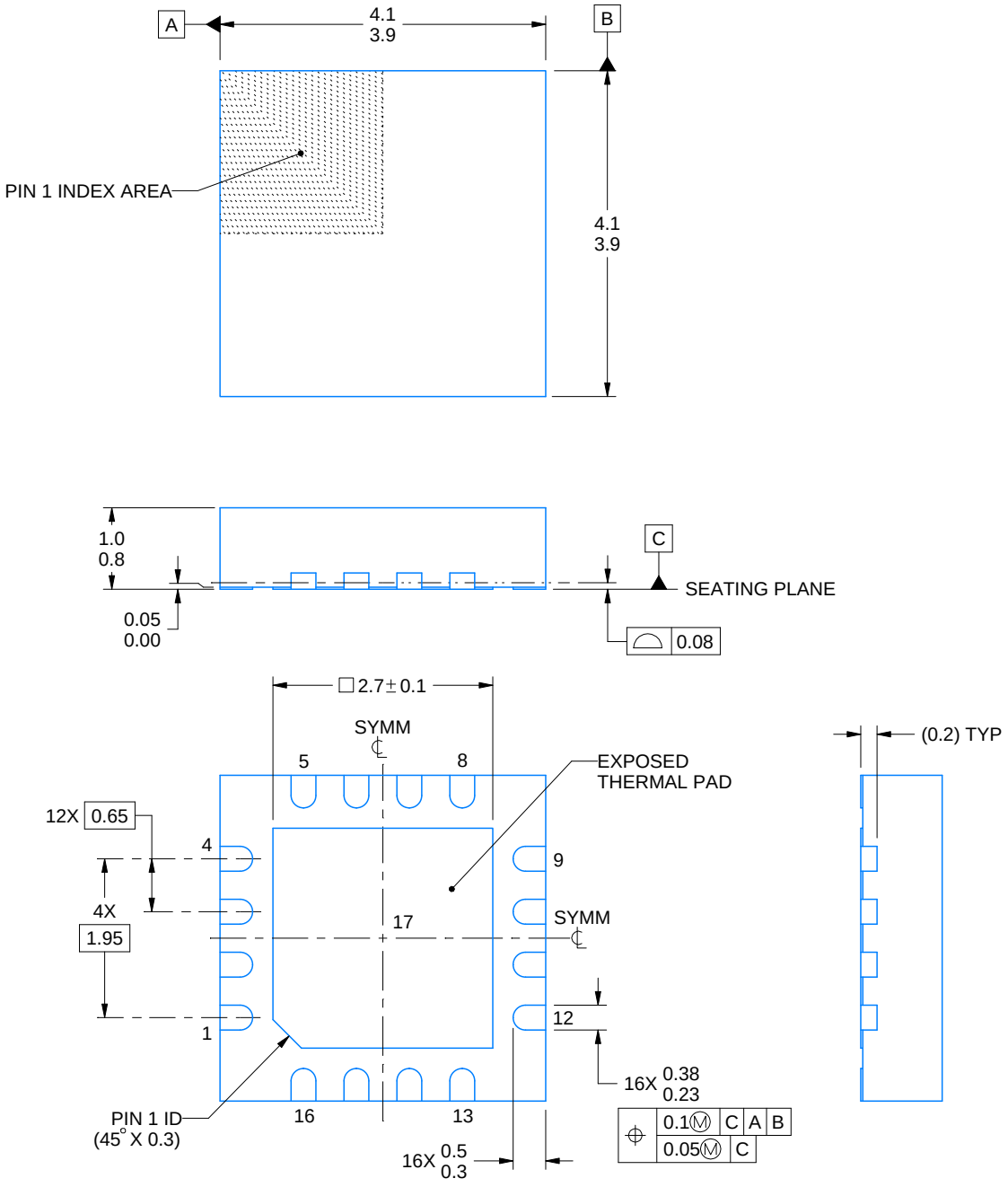
RSA0016B



PACKAGE OUTLINE

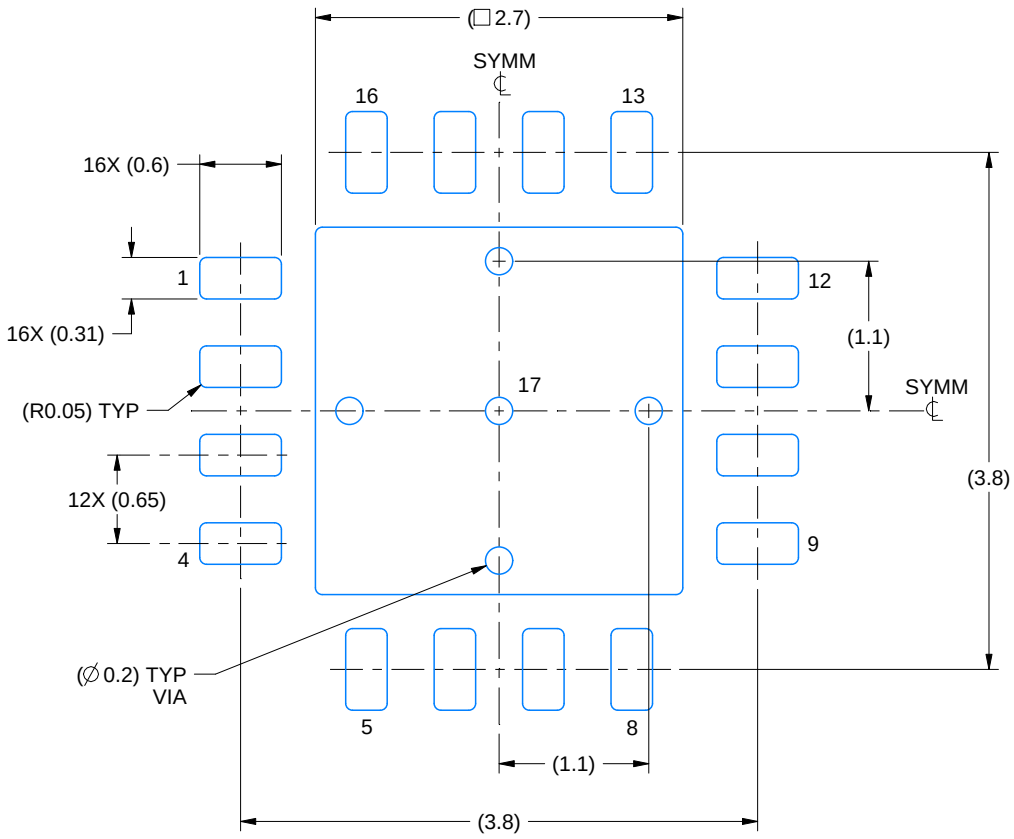
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

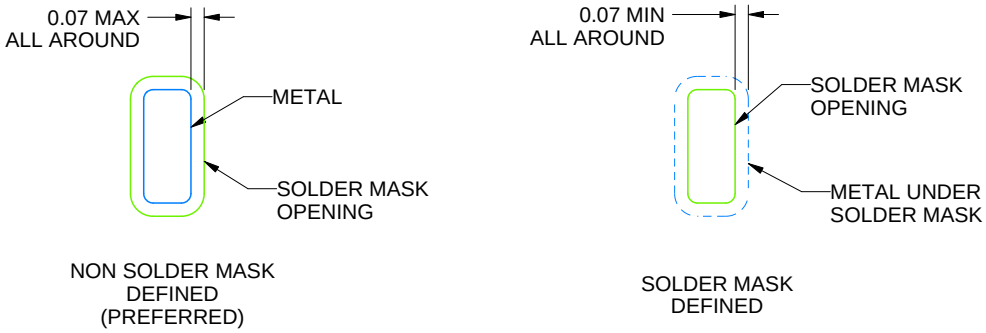


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

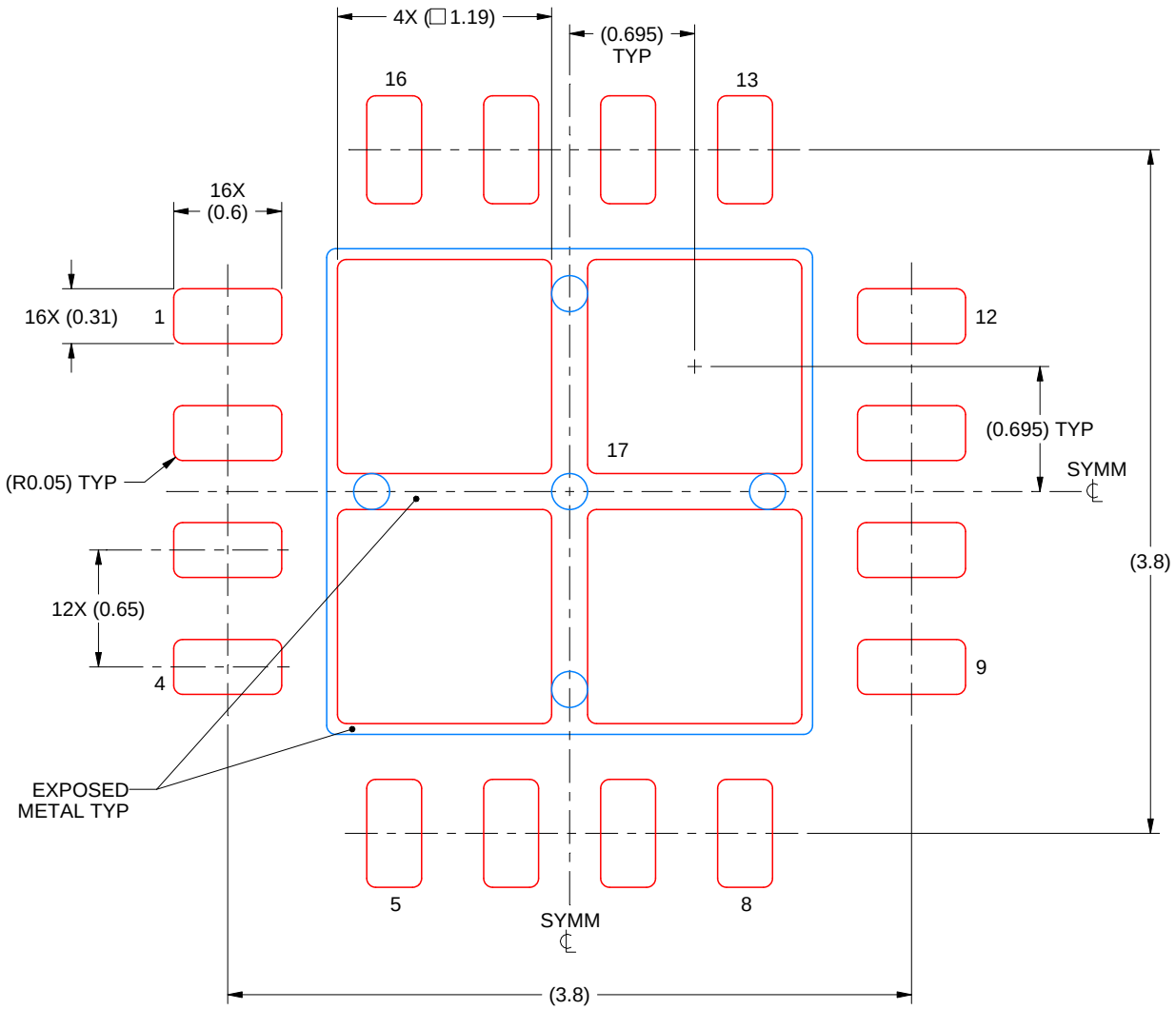


SOLDER MASK DETAILS

4219093/A 08/2021

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4219093/A 08/2021

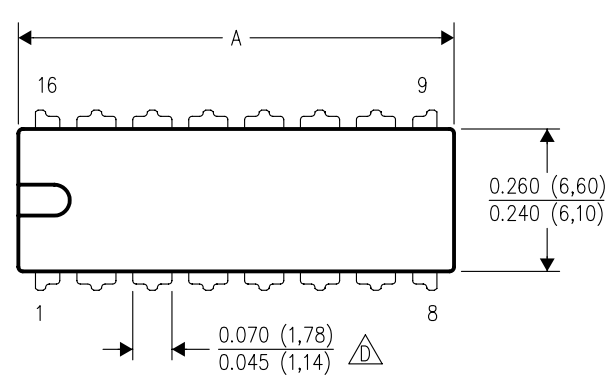
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

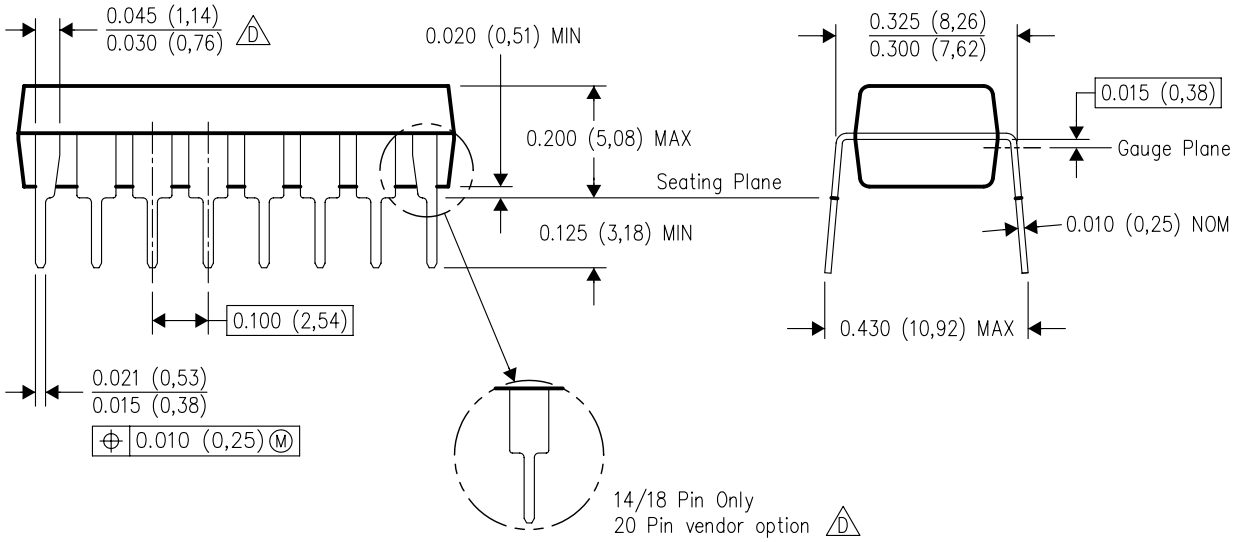
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

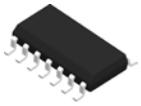


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

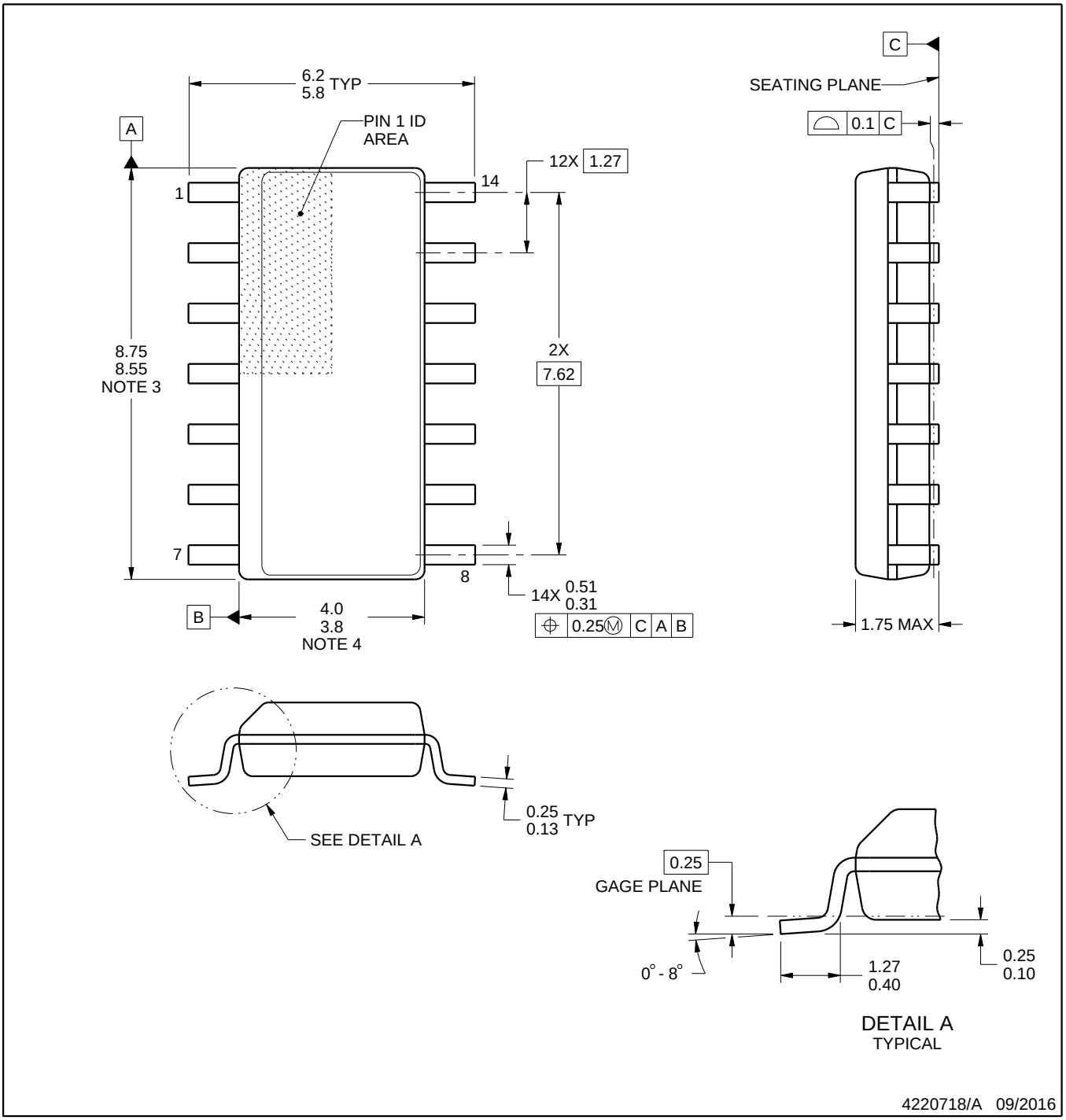


PACKAGE OUTLINE

D0014A

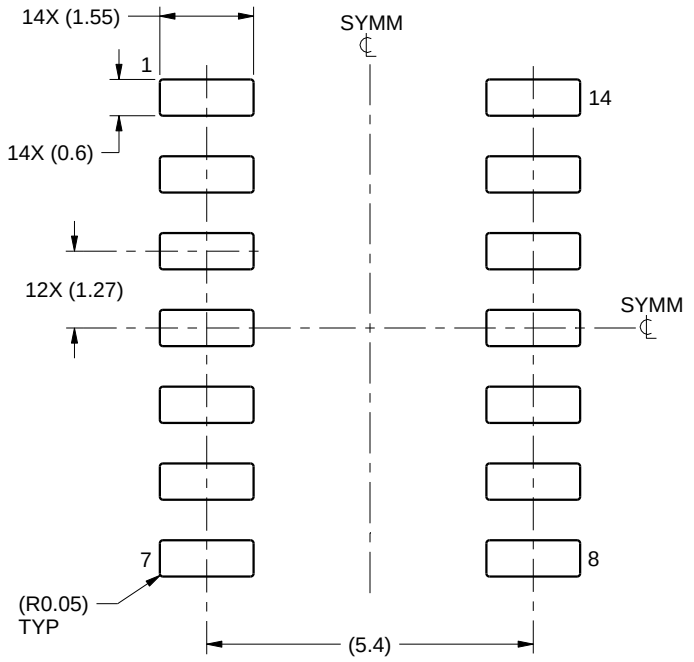
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

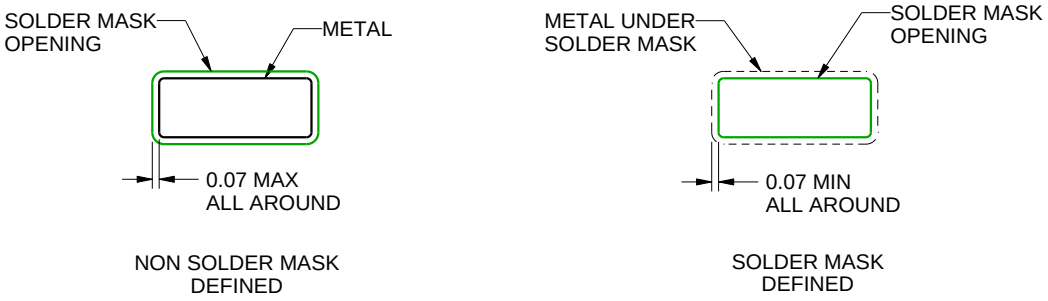


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

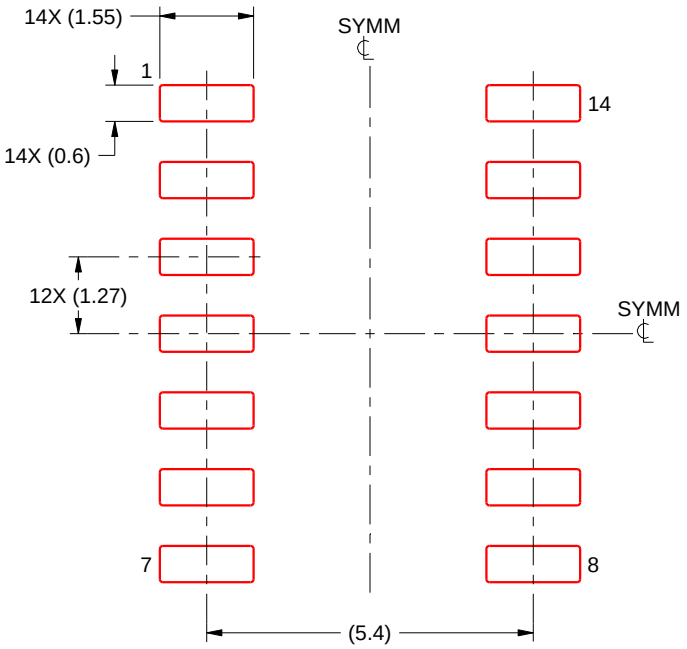
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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