Texas Instruments

TPS54526
ZHCS924D – MAY 2012 – REVISED APRIL 2021

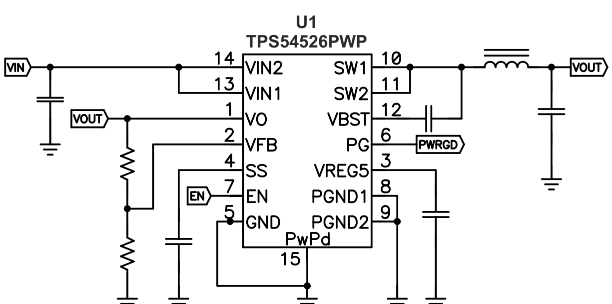
TPS54526 具有 Eco-mode™ 的 4.5V 至 18V 输入、5.5A 同步降压转换器

1 特性

- D-CAP2™ 模式支持快速瞬态响应
- 低输出纹波且支持陶瓷输出电容器
- 宽 V_{IN} 输入电压范围：4.5V 至 18V
- 输出电压范围：0.76V 至 5.5V
- 高效率集成型 FET
  针对较低占空比应用进行了优化
  - 63mΩ（高侧）与 33mΩ（低侧）
- 高效率，关断时流耗少于 10μA
- 高初始带隙基准精度
- 可调软启动
- 预偏置软启动
- 650kHz 开关频率 (f_{SW})
- 逐周期过流限制
- 电源正常状态输出
- 可轻负载下实现高效率的自动跳跃 Eco-mode™

2 应用

- 低电压系统的广泛应用
  - 数字电视电源
  - 高清蓝光光盘™播放器
  - 网络家庭终端设备
  - 数字机顶盒 (STB)



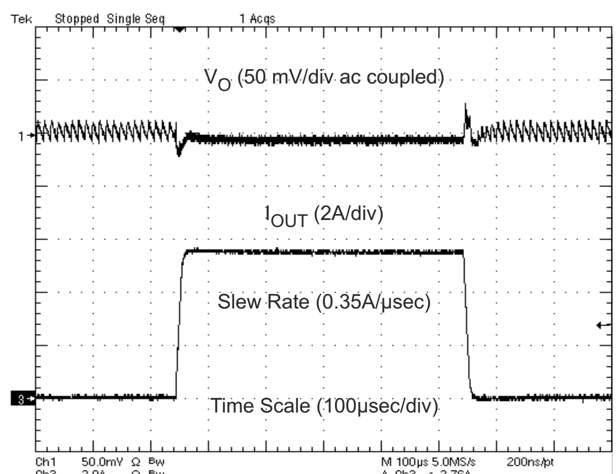
3 说明

TPS54526 是一款自适应接通时间 D-CAP2™ 模式同步降压转换器。TPS54526 可帮助系统设计人员通过成本有效、低组件数量、低待机电流解决方案来完成各种终端设备的电源总线调节器集。TPS54526 的主控制环路采用 D-CAP2™ 模式控制，无需外部补偿组件便可实现极快的瞬态响应。自适应接通时间控制可在更高负载状态下的脉宽调制 (PWM) 模式与轻负载下的 Eco-mode™ 工作之间实现无缝转换。Eco-mode™ 使 TPS54526 能够在较轻负载状况下保持高效率。TPS54526 的专有电路还可使该器件能够适应高分子钽固体电解电容器 (POSCAP) 与高分子聚合物电容器 (SP-CAP) 等低等效串联电阻 (ESR) 输出电容器以及超低 ESR 陶瓷电容器。该器件的工作输入电压介于 4.8V 至 18V VIN 之间。可在 0.76V 至 5.5V 的范围内对输出电压进行设定。此外，该器件还支持可调软启动时间与电源正常功能。TPS54526 采用 14 引脚散热薄型小外形尺寸 (HTSSOP) 封装与 16 引脚四方扁平无引线 (QFN) 封装，设计运行温度范围从 -40°C 到 85°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS54526	HTSSOP (14)	5.00mm x 4.40mm
	VQFN (16)	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



English Data Sheet: SLVSB84

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (June 2014) to Revision D (April 2021) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式.......... 1
- Updated 方程式 3 13

Changes from Revision B (January 2014) to Revision C (June 2014) **Page**

- 已将数据表更改为符合全新的 TI 标准格式.......... 1
- Added the Handling Ratings table.......... 4
- Added the Timing Requirements table.......... 6
- Added the Power Supply Recommendations section.......... 17

Changes from Revision A (July 2013) to Revision B (January 2014) **Page**

- 将数据表标题从“具有 Eco-mode™ 的 4.5V 至 18V 输入、5.5A 同步降压转换器”更改为“具有 Eco-mode™ 的 4.5V 至 18V 输入、3A 同步降压转换器” 1

Changes from Revision * (May 2012) to Revision A (May 2013) **Page**

- Changed the Over/Under Voltage Protection section. From: "as the high-side MOSFET driver turns off and the low-side MOSFET turns on" To: "as both the high-side and low-side MOSFET drivers turn off".......... 10

5 Pin Configuration and Functions

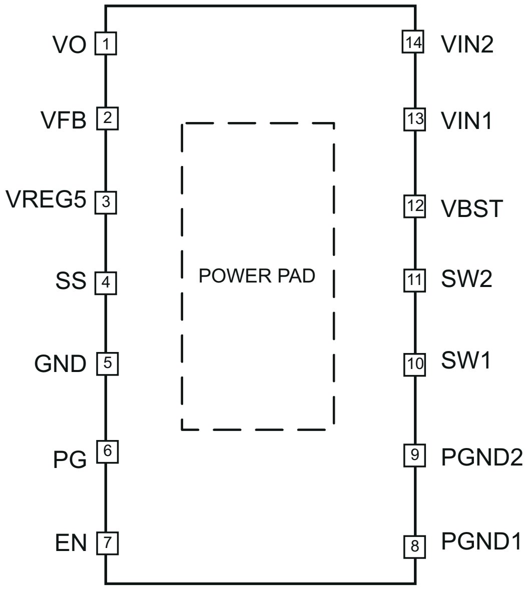


图 5-1. PWP PACKAGE (TOP VIEW)

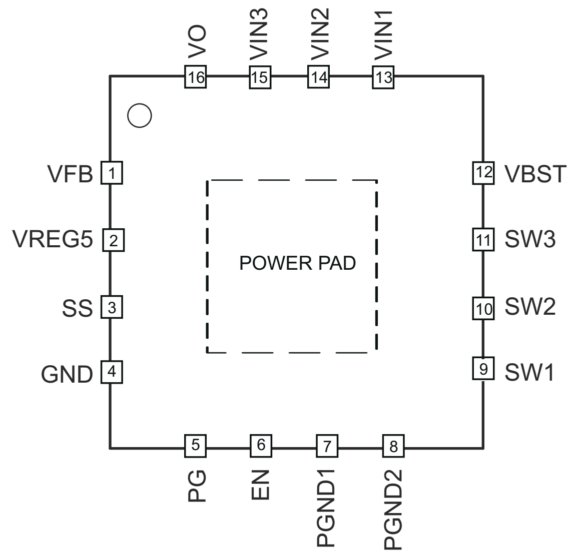


图 5-2. RSA PACKAGE (TOP VIEW)

表 5-1. Pin Functions

PIN			DESCRIPTION
NAME	NUMBER[(1)]		
	PWP 14	RSA 16	
VO	1	16	Connect to output of converter. This pin is used for output discharge function.
VFB	2	1	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	2	5.5 V power supply output. A capacitor (typical 1 µF) should be connected to GND. VREG5 is not active when EN is low.
SS	4	3	Soft-start control. An external capacitor should be connected to GND.
GND	5	4	Signal ground pin.
PG	6	5	Open drain power good output.
EN	7	6	Enable control input. EN is active high and must be pulled up to enable the device.
PGND1, PGND2	8, 9	7, 8	Ground returns for low-side MOSFET. Also serve as inputs of current comparators. Connect PGND and GND strongly together near the IC.
SW1, SW2, SW3[(1)]	10, 11	9, 10, 11	Switch node connection between high-side NFET and low-side NFET. Also serve as inputs to current comparators.
VBST	12	12	Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to respective SW1, SW2 terminals. An internal PN diode is connected between VREG5 to VBST pin.
VIN1, VIN2, VIN3[(1)]	13, 14	13, 14, 15	Power input and connected to high side NFET drain. Supply input for 5-V internal linear regulator for the control circuitry.
PowerPAD™	Back side	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Should be connected to PGND.

(1) SW3, VIN3 applies to 16 pin package only.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
Input voltage range	VIN1, VIN2, EN	–0.3	20	V
	VBST	–0.3	26	V
	VBST (10 ns transient)	–0.3	28	V
	VBST (vs Sw1, SW2)	–0.3	6.5	V
	VFB, VO, SS, PG	–0.3	6.5	V
	SW1, SW2	–2	20	V
	SW1, SW2 (10 ns transient)	–3	22	V
Output voltage range	VREG5	–0.3	6.5	V
	PGND1, PGND2	–0.3	0.3	V
Voltage from GND to PowerPAD™, V_{diff}		–0.2	0.2	V
Operating junction temperature, T_J		–40	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	–2	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage range		4.5	18	V
V_I	Input voltage range	VBST	–0.3	24	V
		VBST (10 ns transient)	–0.3	27	
		VBST (vs Sw1, SW2)	–0.3	5.7	
		SS, PG	–0.3	5.7	
		EN	–0.3	18	
		VO, VFB	–0.3	5.5	
		SW1, SW2	–1.8	18	
		SW1, SW2 (10 ns transient)	–3	21	
		PGND1, PGND2	–0.3	0.1	
V_O	Output voltage range	VREG5	–0.3	5.7	V
I_O	Output Current range	I_{VREG5}	0	5	mA
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	150	°C

6.4 Thermal Information

THERMAL METRIC		TPS54526 PWP (14) PINS	TPS54526 RSA (16) PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.7	35.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	33.1	40.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.4	12.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.2	12.4	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	4.7	3.6	°C/W

6.5 Electrical Characteristics

over operating free-air temperature range, V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating - non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5 V, V_{VFB} = 0.8 V		900	1400	µA
I_{VINSDN}	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V		3.6	10	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage		1.6			V
V_{ENL}	EN low-level input voltage				0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V	220	440	880	kΩ
VFB VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	VFB threshold voltage	VFB voltage light load mode, T_A = 25°C, V_O = 1.05 V, I_O = 10mA		771		mV
		T_A = 25°C, V_O = 1.05 V, continuous mode	757	765	773	mV
		T_A = 0°C to 85°C, V_O = 1.05 V, continuous mode[(1)]	753		777	mV
		T_A = –40°C to 85°C, V_O = 1.05 V, continuous mode[(1)]	751		779	mV
I_{VFB}	VFB input current	V_{VFB} = 0.8 V, T_A = 25°C		0	±0.15	µA
R_{Dischg}	V_O discharge resistance	V_{EN} = 0 V, V_O = 0.5 V, T_A = 25°C		50	100	Ω
VREG5 OUTPUT						
V_{VREG5}	VREG5 output voltage	T_A = 25°C, 6 V < V_{IN} < 18 V, 0 < I_{VREG5} < 5 mA	5.2	5.5	5.7	V
V_{VREG5}	VREG5 Line regulation	6.0 V < V_{IN} < 18 V, I_{VREG5} = 5 mA			20	mV
V_{VREG5}	VREG5 Load regulation	0 mA < I_{VREG5} < 5 mA			100	mV
I_{VREG5}	VREG5 Output current	V_{IN} = 6 V, V_{VREG5} = 4 V, T_A = 25°C		60		mA
MOSFET						
R_{dsonh}	High side switch resistance	T_A = 25°C, V_{BST} - $V_{SW1,2}$ = 5.5 V		63		mΩ
R_{dsonl}	Low side switch resistance	T_A = 25°C		33		mΩ

over operating free-air temperature range, V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
I_{ocl}	Current limit	L_{OUT} = 1.5 μH[(1)],	6.1	6.9	8.4	A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature [(1)]		165		°C
		Hysteresis [(1)]		35		
SOFT START						
I_{SSC}	SS charge current	V_{SS} = 1.0 V	4.2	6.0	7.8	μA
I_{SSD}	SS discharge current	V_{SS} = 0.5 V	0.1	0.2		mA
POWER GOOD						
V_{THPG}	PG threshold	V_{VFB} rising (good)	85	90	95	%
		V_{VFB} falling (fault)		85		%
I_{PG}	PG sink current	V_{PG} = 0.5 V	2.5	5		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	120	125	130	%
V_{UVP}	Output UVP trip threshold	UVP detect	60	65	70	%
		Hysteresis		10		%
UVLO						
V_{UVLO}	UVLO threshold	Wake up VREG5 voltage	3.31	3.61	3.91	V
		Fall VREG5 voltage	2.82	3.12	3.42	
		Hysteresis VREG5 voltage	0.37	0.49	0.61	

(1) Not production tested.

6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		155		ns
$t_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{FB} = 0.7 V		260	330	ns
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
t_{OVPDEL}	Output OVP prop delay			10		μs
t_{UVPDEL}	Output UVP delay			0.25		ms
t_{UVPEN}	Output UVP enable delay	Relative to soft-start time		x 1.7		

6.7 Typical Characteristics

V_{IN} = 12 V, T_A = 25 °C (unless otherwise noted)

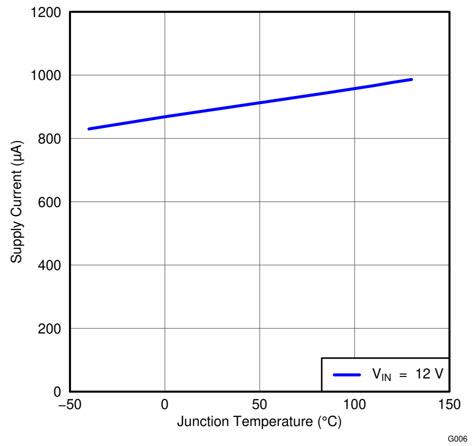


图 6-1. V_{IN} Current vs Junction Temperature

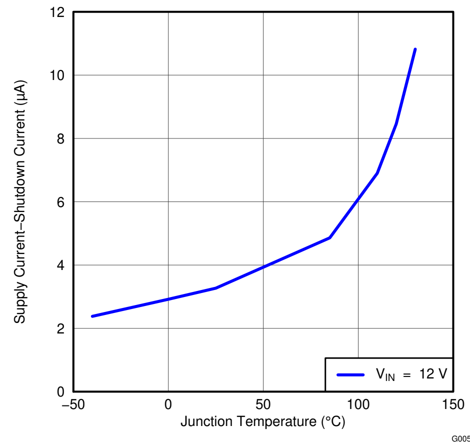


图 6-2. V_{IN} Shutdown Current vs Junction Temperature

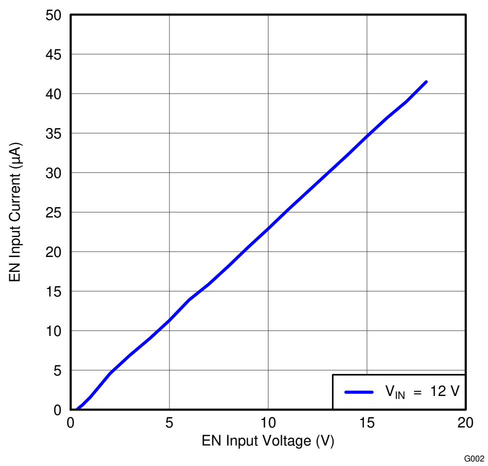
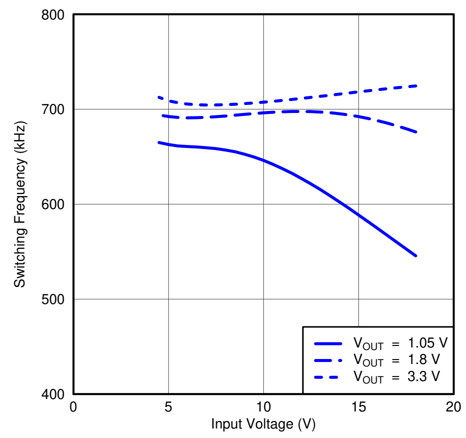


图 6-3. EN Current vs EN Voltage



I_O = 1A

图 6-4. Switching Frequency vs Input Voltage

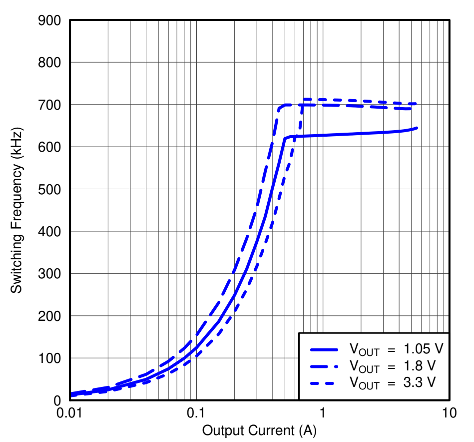


图 6-5. Switching Frequency vs Output Current

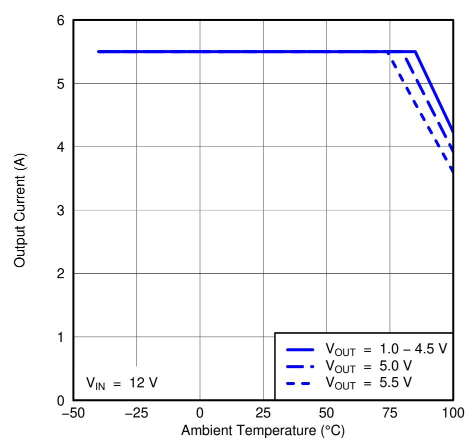


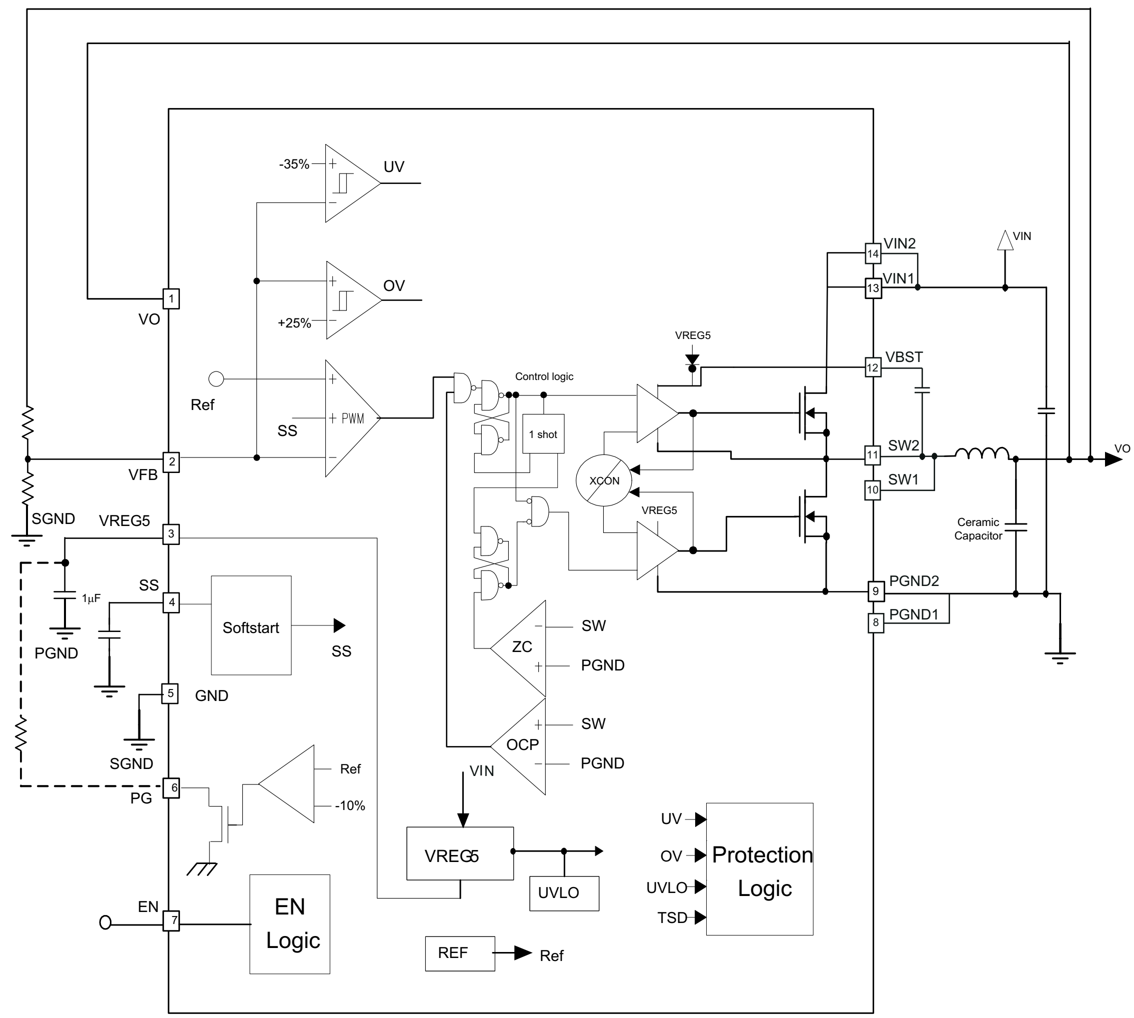
图 6-6. Output Current vs Ambient Temperature

7 Detailed Description

7.1 Overview

The TPS54526 is a 5.5-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs and auto-skip Eco-mode™ to improve light lode efficiency. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

7.2 Functional Block Diagram



A. The block diagram shown is for the PWP 14 pin package. The QFN 16 pin package block diagram is identical except for the pin out.

7.3 Feature Description

7.3.1 PWM Operation

The main control loop of the TPS54526 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. The MOSFET is turned off after the internal one-shot timer expires. The one-shot timer is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

7.3.2 PWM Frequency and Adaptive On-Time Control

TPS54526 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54526 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

7.3.3 Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6 μA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in 方程式 1. VFB voltage is 0.765 V and SS pin source current is 6 μA.

$$t_{SS}(\mathrm{ms}) = \frac{C_{SS}(\mathrm{nF}) \times V_{REF} \times 1.1}{I_{SS}(\mu A)} = \frac{C_{SS}(\mathrm{nF}) \times 0.765 \times 1.1}{6} \tag{1}$$

The TPS54526 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage V_{FB}), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

7.3.4 Power Good

The TPS54526 has power-good open drain output. The power good function is activated after soft start has finished. The power good function becomes active after 1.7 times soft-start time. When the output voltage is within -10% of the target value, internal comparators detect power good state and the power good signal becomes high. Rpg resister value ,which is connected between PG and VREG5, is required from 25kΩ to 150kΩ. If the feedback voltage goes under 15% of the target value, the power good signal becomes low after a 5 μs internal delay.

7.3.5 VREG5

VREG5 is an internally generated voltage source used by the TPS54526. It is derived directly from the input voltage and is nominally regulated to 5.5 V when the input voltage is above 5.6 V. The output of the VREG5 regulator is the input to the internal UVLO function. VREG5 must be above the UVLO wake up threshold voltage (3.6 V typical) for the TPS54526 to function. Connect a 1 µF capacitor between pin 3 of the TPS54526 and power ground for proper regulation of the VREG5 output. The VREG5 output voltage is available for external use. It is recommended to use no more than 5 mA for external loads. The VREG5 output is disabled when the TPS54526 EN pin is open or pulled low.

7.3.6 Output Discharge Control

TPS54526 discharges the output when EN is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO and thermal shutdown). The output is discharged by an internal 50-Ω MOSFET which is connected from VO to PGND. The internal low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

7.3.7 Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time, and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the measured voltage is above the voltage proportional to the current limit. Then, the device constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time.

The converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The load current one half of the peak-to-peak inductor current higher than the overcurrent threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output under-voltage protection circuit to be activated. When the overcurrent condition is removed, the output voltage will return to the regulated value. This protection is non-latching.

7.3.8 Over/Under Voltage Protection

TPS54526 monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and the circuit latches as both the high-side and low-side MOSFET drivers turns off. When the feedback voltage becomes lower than 65% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250 μs, the device latches off both internal top and bottom MOSFET. This function is enabled approximately 1.7 x softstart time.

7.3.9 UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the V_{REG5} pin. When the V_{REG5} voltage is lower than UVLO threshold voltage, the TPS54526 is shut off. This is protection is non-latching.

7.3.10 Thermal Shutdown

TPS54526 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.

7.4 Device Functional Modes

7.4.1 Auto-Skip Eco-Mode™ Control

The TPS54526 is designed with Auto-Skip Eco-mode™ to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in 方程式 2.

$$I_{OUT(LL)}=\frac{1}{2\times L\times f_{SW}}\times\frac{\left(V_{IN}-V_{OUT}\right)\times V_{OUT}}{V_{IN}} \tag{2}$$

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI' s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application

The TPS54526 is an adaptive on-time D-CAP2™ mode synchronous buck converter. Idea applications are: Digital TV Power Supply, High Definition Blu-ray Disc™ Player, Networking Home Terminal and Digital Set Top Box.

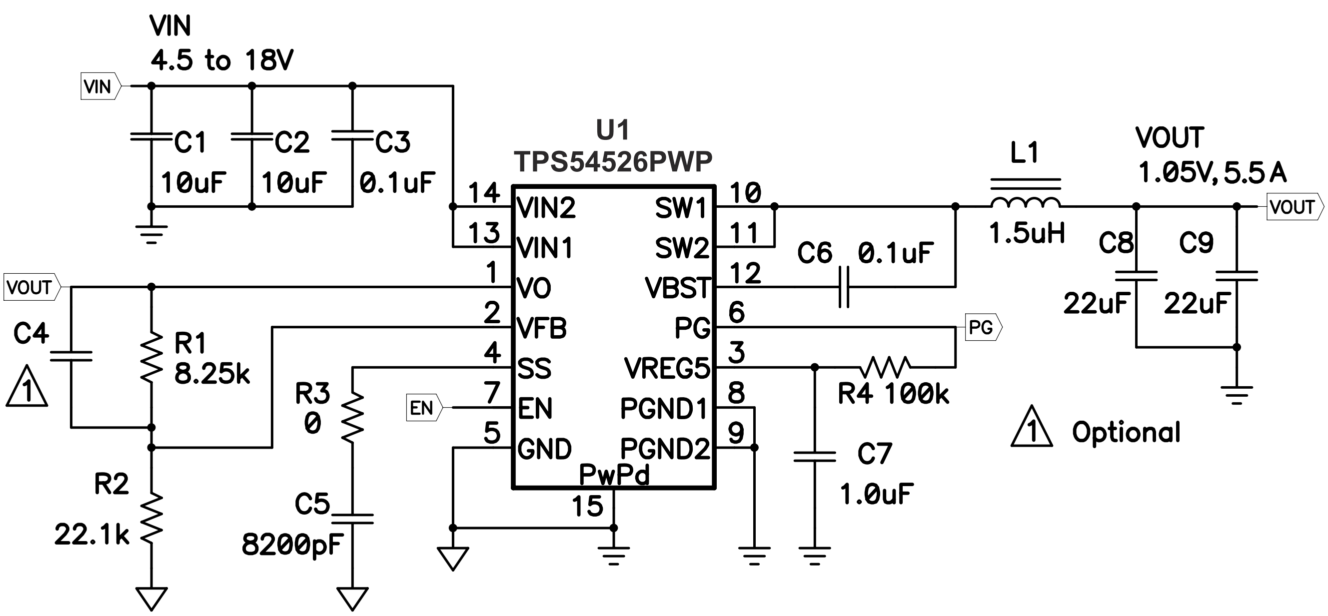


图 8-1. Schematic Diagram for This Design Example

8.2.1 Design Requirements

For this design example, use the following input parameters.

表 8-1. Design Parameters

DESIGN PARAMETERS	VALUES
Input voltage range	4.5V – 18 V
Output voltage	1.05 V
Output current rating	0 – 5.5 A
Output voltage ripple	7 mV_{PP} (12 V_{IN} / 5.5 A)

8.2.2 Detailed Design Procedure

8.2.2.1 Step By Step Design Procedure

To begin the design process, the designer must know a the following application parameters:

- Input voltage range
- Output voltage

- Output current
- Output voltage ripple
- Input voltage ripple

8.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using 方程式 3 to calculate V_{OUT}

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable

$$V_{OUT} = (0.7651 - 0.0011 \times VOUT\_SET) \times \left(1 + \frac{R1}{R2}\right)$$

where VOUT_SET is target VOUT voltage (3)

8.2.2.3 Output Filter Selection

The output filter used with the TPS54526 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{4}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54526. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a -40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of 方程式 4 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 8-2

表 8-2. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)(1)	L1 (µH)	C8 + C9 (µF)
1	6.81	22.1		1.0 - 1.5	22 - 68
1.05	8.25	22.1		1.0 - 1.5	22 - 68
1.2	12.7	22.1		1.0 - 1.5	22 - 68
1.5	21.5	22.1		1.5	22 - 68
1.8	30.1	22.1	5 - 22	1.5	22 - 68
2.5	49.9	22.1	5 - 22	2.2	22 - 68
3.3	73.2	22.1	5 - 22	2.2	22 - 68
5	124	22.1	5 - 22	3.3	22 - 68

(1) Optional

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1.

Since the DC gain is dependent on the output voltage, the required inductor value increases as the output voltage increases. For higher output voltages above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 方程式 5, 方程式 6 and 方程式 7. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for f_{SW}.

$$Ilp\text{-}p = \frac{V_{OUT}}{V_{IN\,(max)}} \bullet \frac{V_{IN\,(max)} - V_{OUT}}{L_O \bullet f_{SW}} \tag{5}$$

$$I_{lpeak} = I_O + \frac{Ilp\text{-}p}{2} \tag{6}$$

$$I_{Lo(RMS)} = \sqrt{I_O^{\,2} + \frac{1}{12} Ilp\text{-}p^{2}} \tag{7}$$

For this design example, the calculated peak current is 6.01 A and the calculated RMS current is 5.5 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54526 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22uF to 68uF. Use 方程式 8 to determine the required RMS current rating for the output capacitor

$$I_{CO(RMS)} = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{\sqrt{12} \bullet V_{IN} \bullet L_O \bullet f_{SW}} \tag{8}$$

For this design two TDK C3216X5R0J226M 22uF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is .284 A and each output capacitor is rated for 4 A.

8.2.2.4 Input Capacitor Selection

The TPS54526 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 uF. is recommended for the decoupling capacitor. An additional 0.1 μF capacitor from pin 14 to ground is recommended to improve the stability of the over-current limit function. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.2.2.5 Bootstrap Capacitor Selection

A 0.1 μF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

8.2.2.6 VREG5 Capacitor Selection

A 1.0 μF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

8.2.3 Application Curve

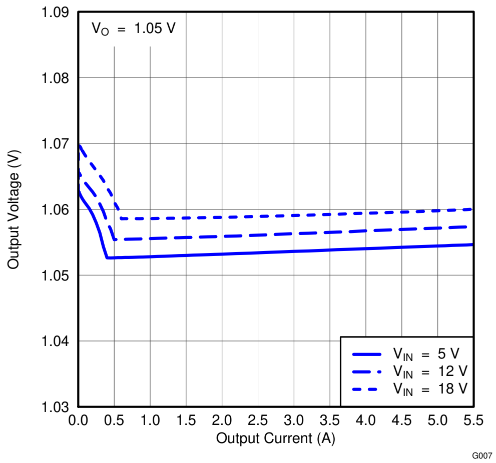


图 8-2. 1.05V Output Voltage vs Output Current

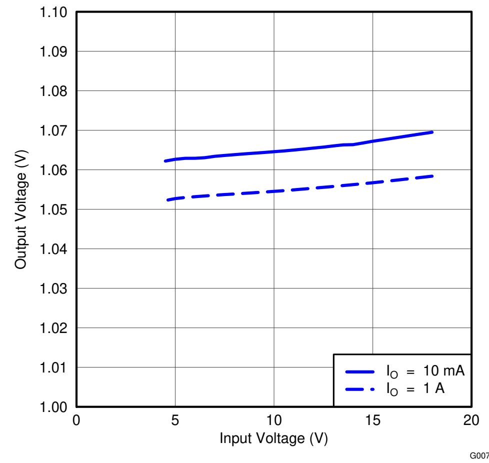


图 8-3. 1.05V Output Voltage vs Input Voltage

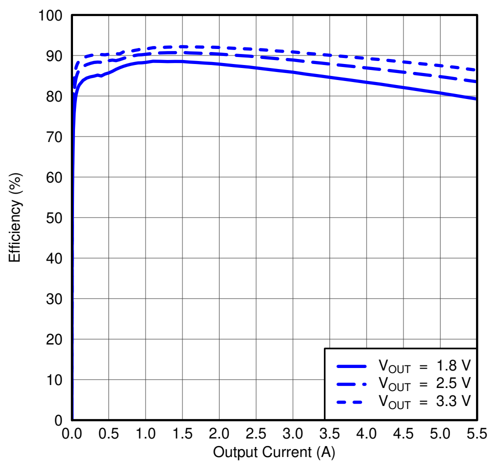


图 8-4. Efficiency vs Output Current

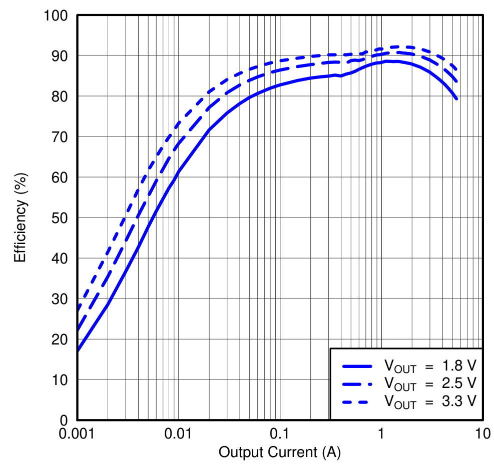
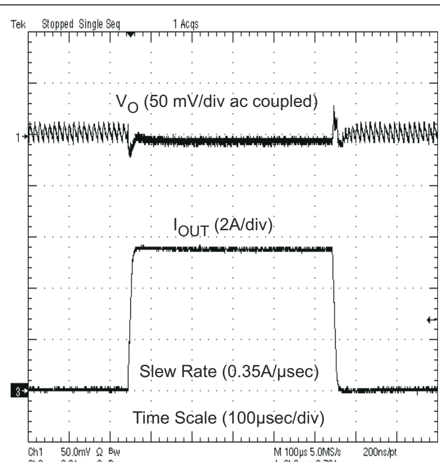


图 8-5. Light Load Efficiency vs Output Current



1.05 V 50 mA to 5.5 A

图 8-6. Load Transient Response

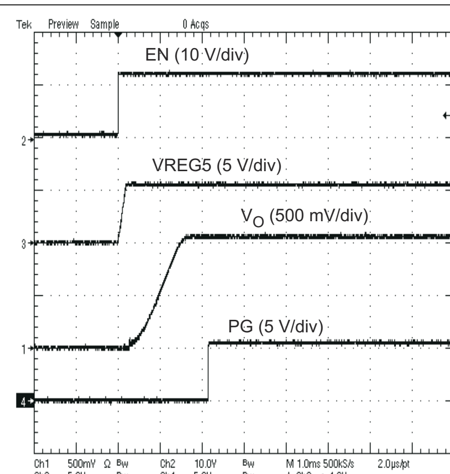
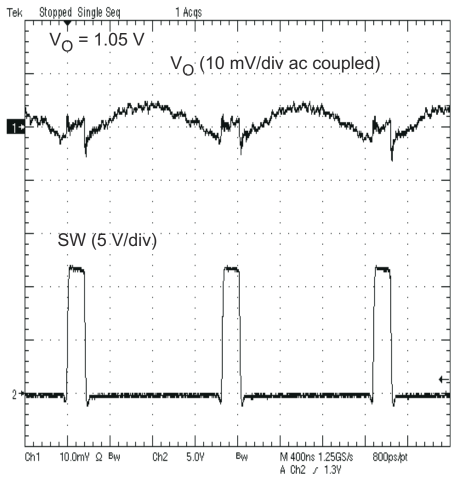
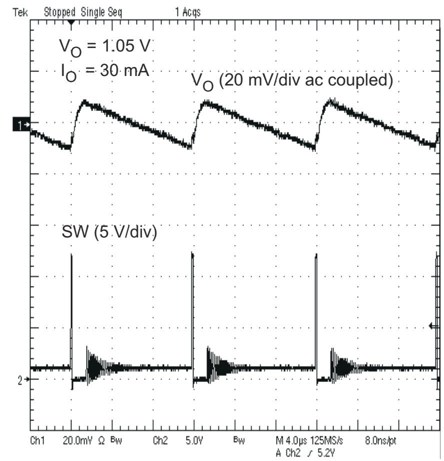


图 8-7. Startup Waveform



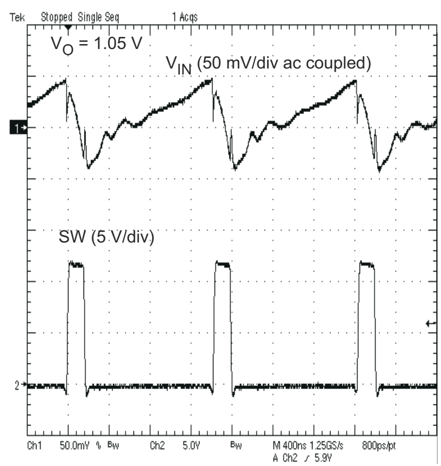
I_O= 5.5A

图 8-8. Voltage Ripple at Output



I_O = 30 mA

图 8-9. Eco-mode Voltage Ripple at Output



I_O= 5.5A

图 8-10. Voltage Ripple at Input

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4.5 V and 18 V. This input supply should be well regulated. If the input supply is located more than a few inches from the TPS54526 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

- Keep the input switching current loop as small as possible.
- Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.
- VREG5 capacitor should be placed near the device, and connected PGND.
- Output capacitor should be connected to a broad pattern of the PGND.
- Voltage feedback loop should be as short as possible, and preferably with ground shield.
- Lower resistor of the voltage divider which is connected to the VFB pin should be tied to AGND.
- Providing sufficient via is preferable for VIN, SW and PGND connection.
- PCB pattern for VIN and SW should be as broad as possible.
- VIN Capacitor should be placed as near as possible to the device.
- The top side power ground (PGND) copper fill area near the IC should be as large as possible. This will aid in thermal dissipation as well lower conduction losses in the ground return
- Exposed pad of device must be connected to PGND with solder. The PGND area under the IC should be as large as possible and completely cover the exposed thermal pad. The bottom side of the board should contain a large copper area under the device that is directly connected to the exposed area with small diameter vias. Small diameter vias will prevent solder from being drawn away from the exposed thermal pad. Any additional internal layers should also contain copper ground areas under the device and be connected to the thermal vias.

10.2 Layout Example

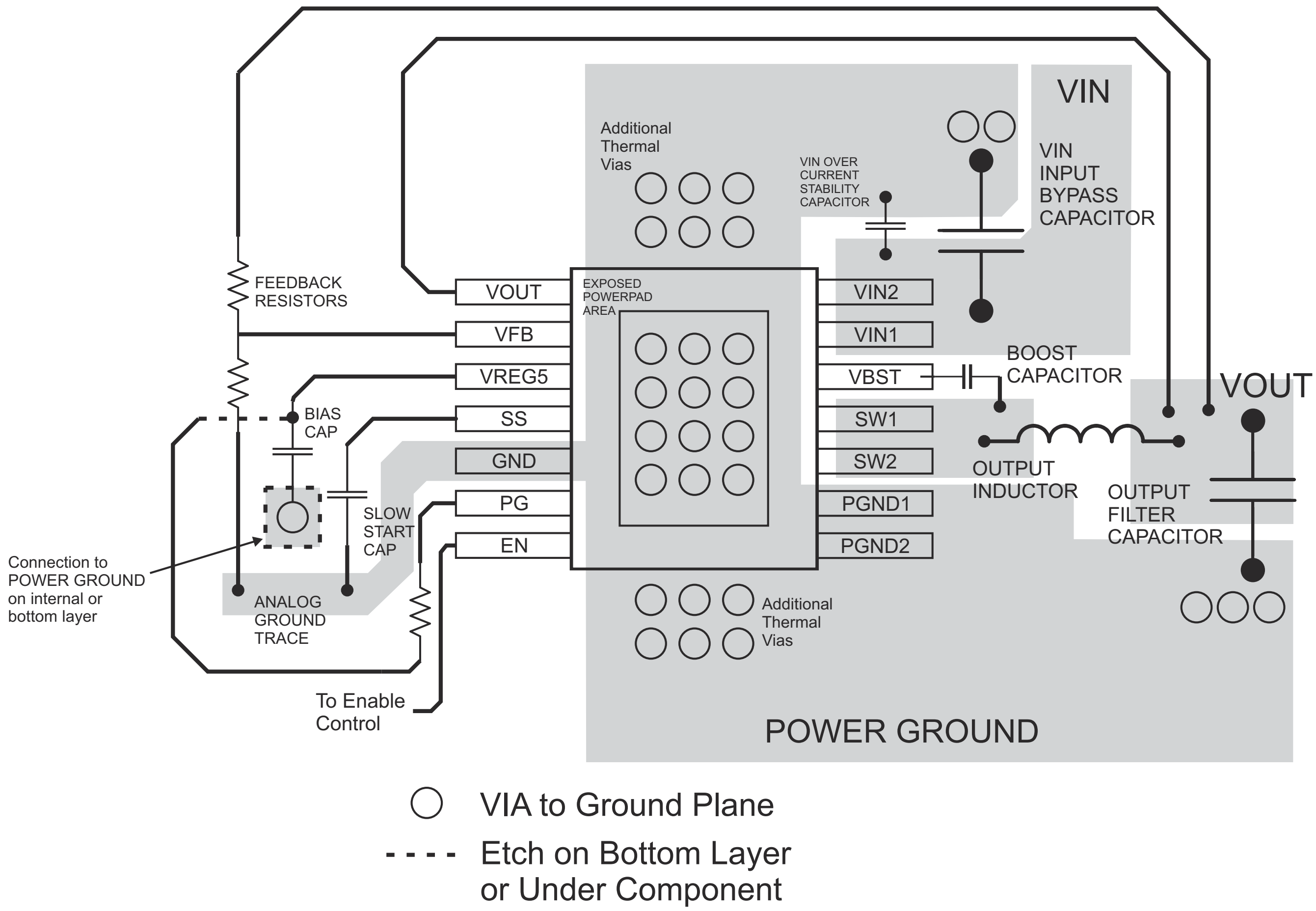


图 10-1. PCB Layout for PWP Package

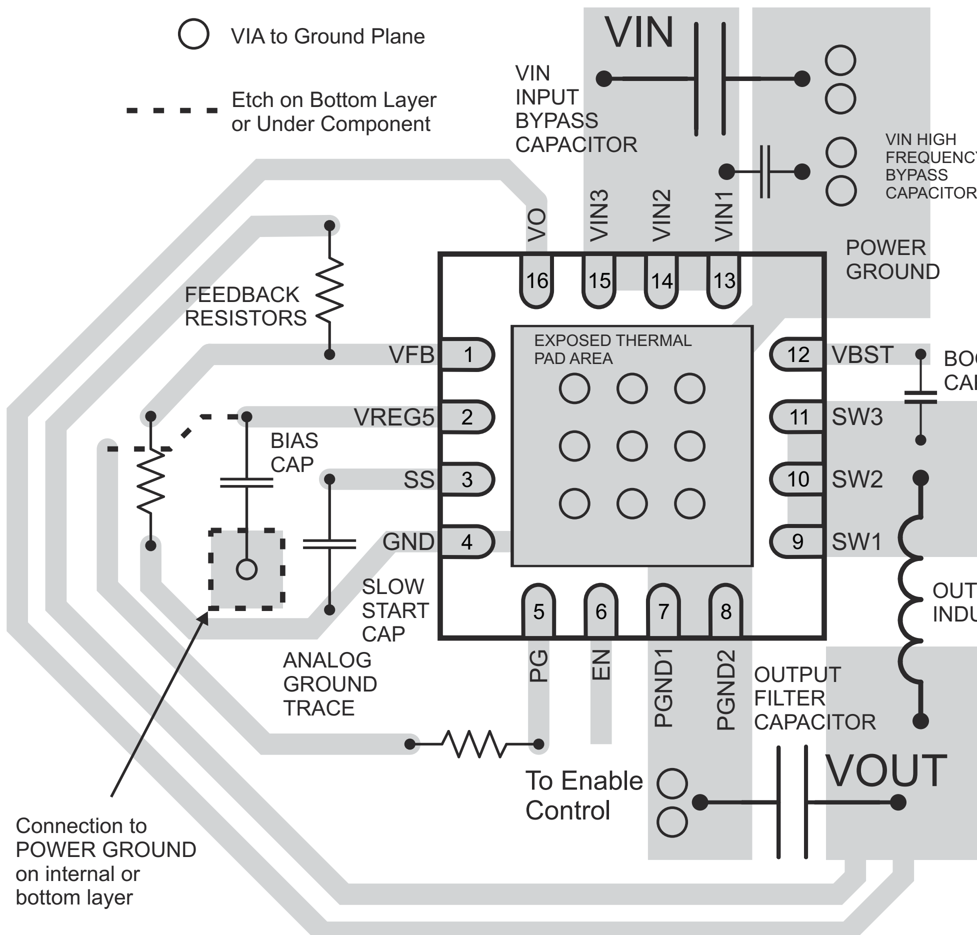


图 10-2. PCB Layout for RSA Package

11 Device and Documentation Support

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.3 Trademarks

D-CAP2™, Eco-mode™, TI E2E™ are trademarks of Texas Instruments.
蓝光光盘™ is a trademark of Blu-ray Disc Association.
is a trademark of TI.
所有商标均为其各自所有者的财产。

11.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Thermal Information

This PowerPad™ package incorporates an exposed thermal pad that is designed to be directly to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for this package are shown in the following illustration.

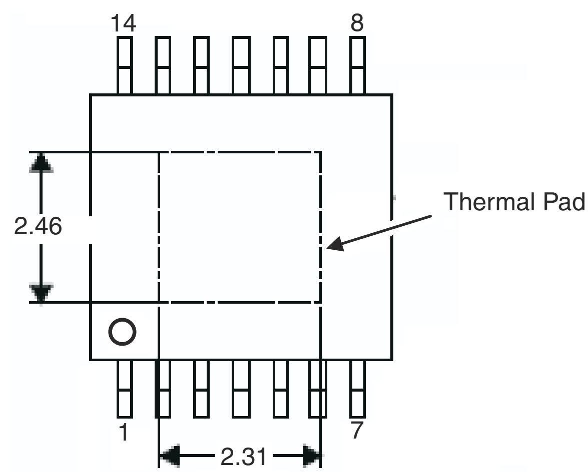


图 12-1. Thermal Pad Dimensions

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54526PWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54526	Samples
TPS54526PWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54526	Samples
TPS54526RSAR	ACTIVE	QFN	RSA	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54526	Samples
TPS54526RSAT	ACTIVE	QFN	RSA	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54526	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

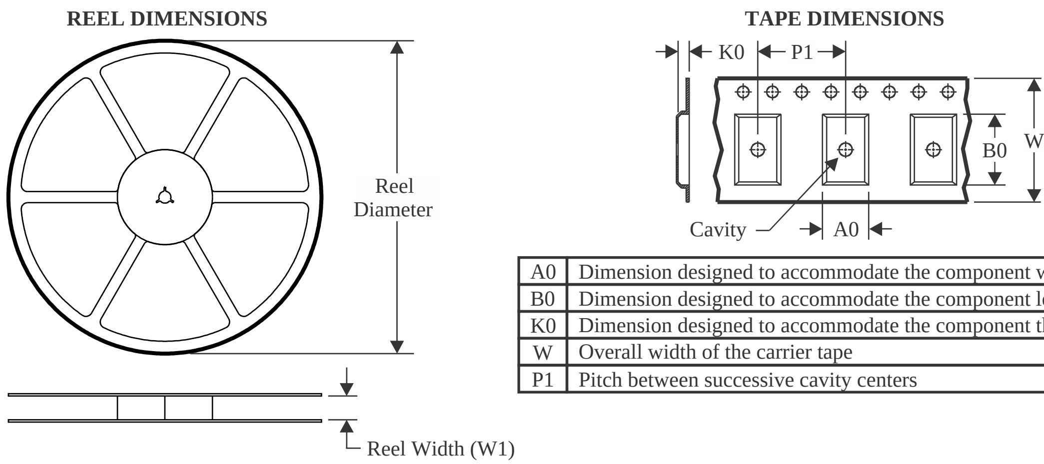
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

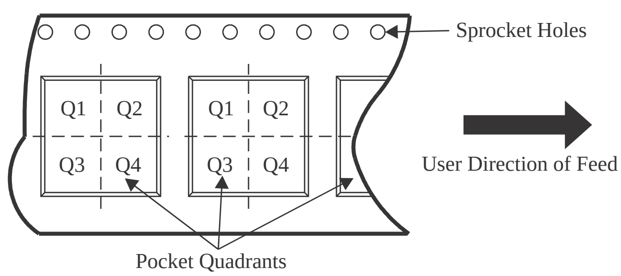
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

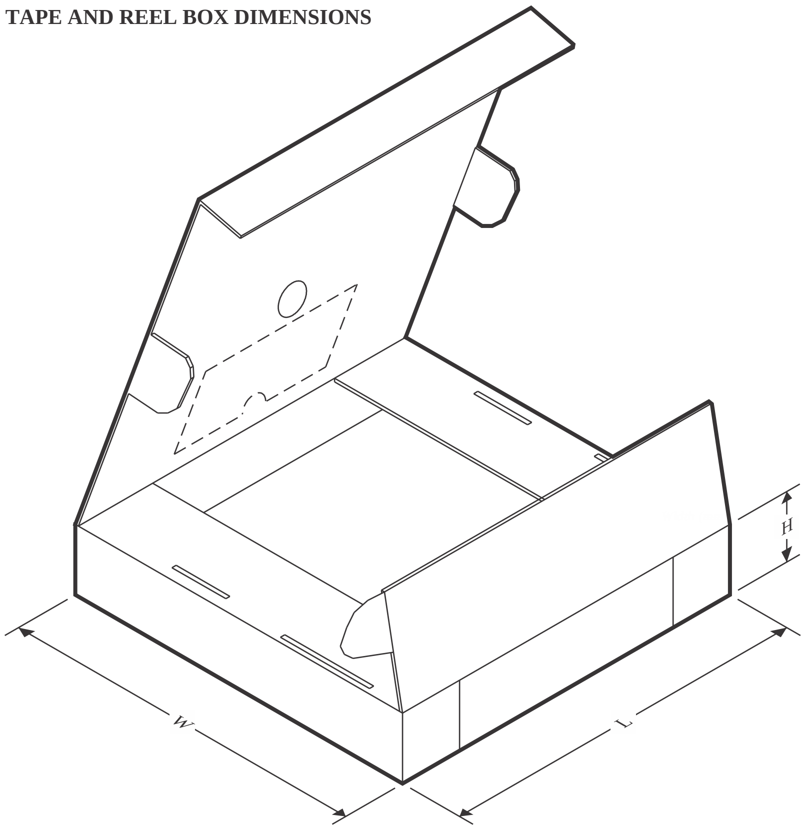


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

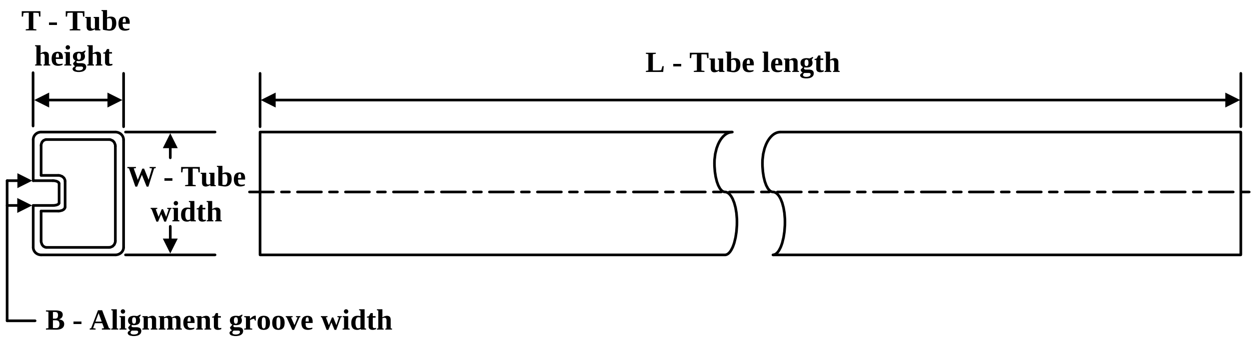
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54526PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS54526RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS54526RSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54526PWPR	HTSSOP	PWP	14	2000	356.0	356.0	35.0
TPS54526RSAR	QFN	RSA	16	3000	346.0	346.0	33.0
TPS54526RSAT	QFN	RSA	16	250	182.0	182.0	20.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54526PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5
TPS54526PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5

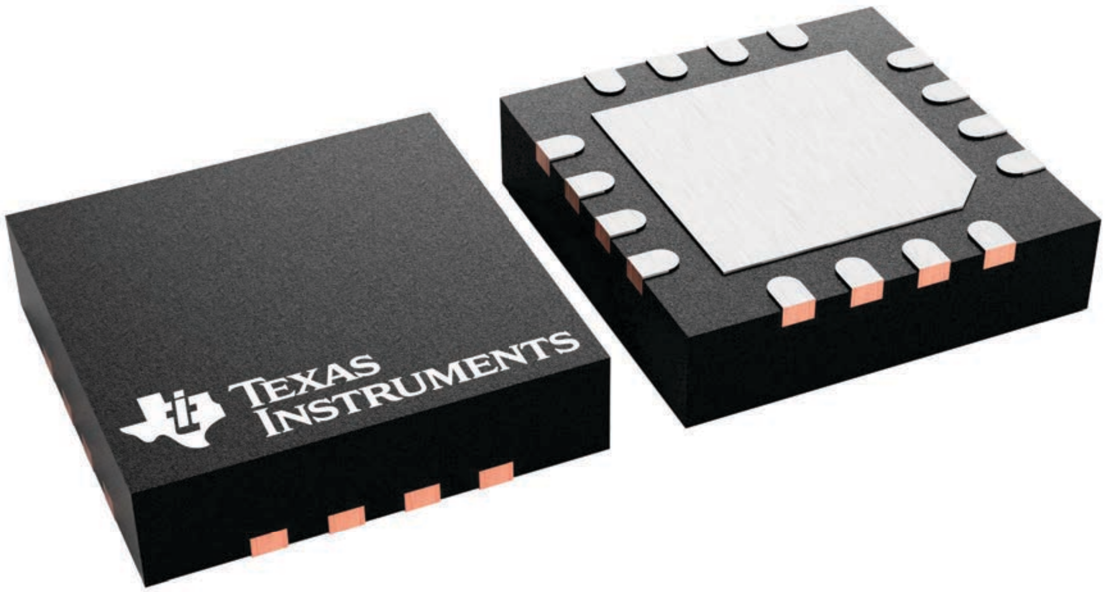
RSA 16

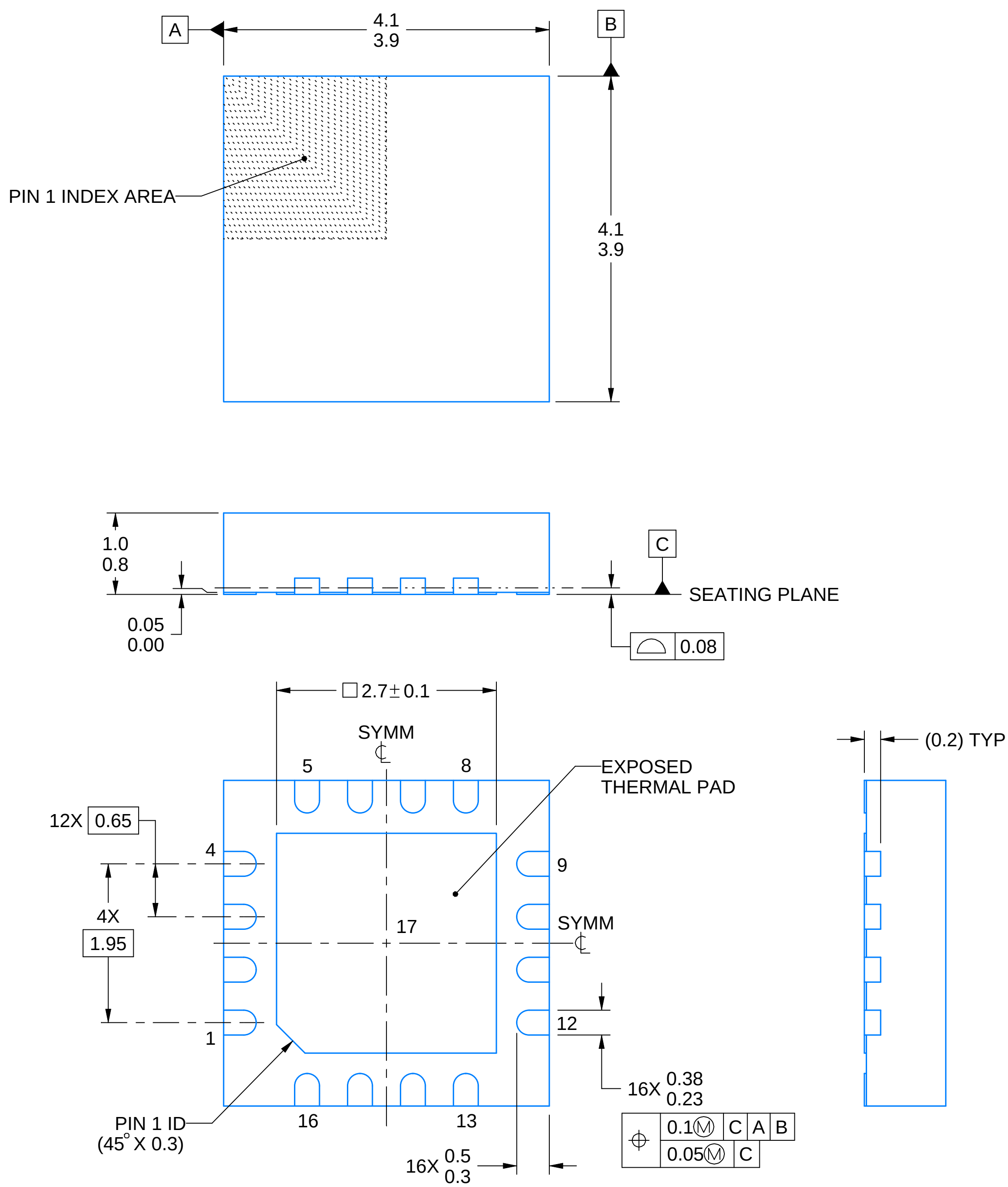
VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

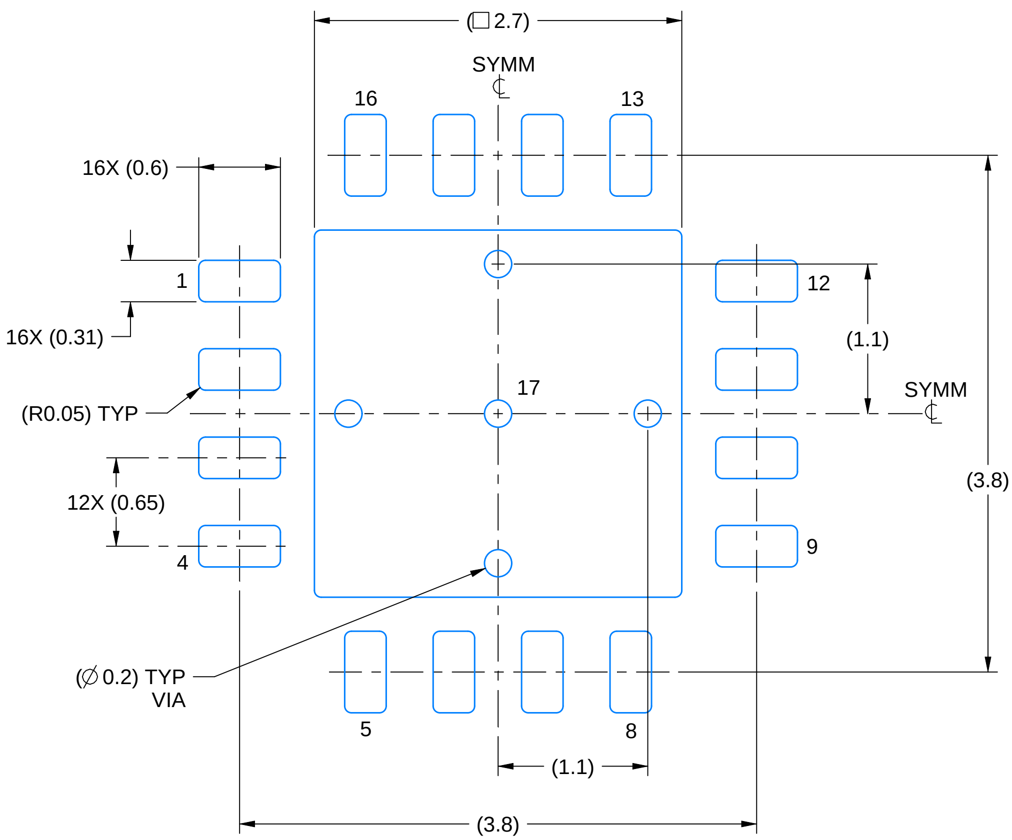




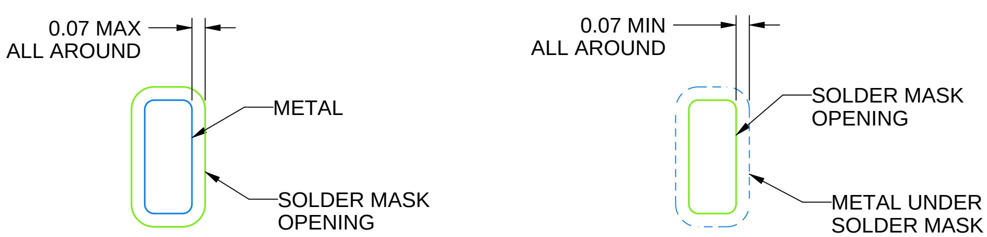
4219093/A 08/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

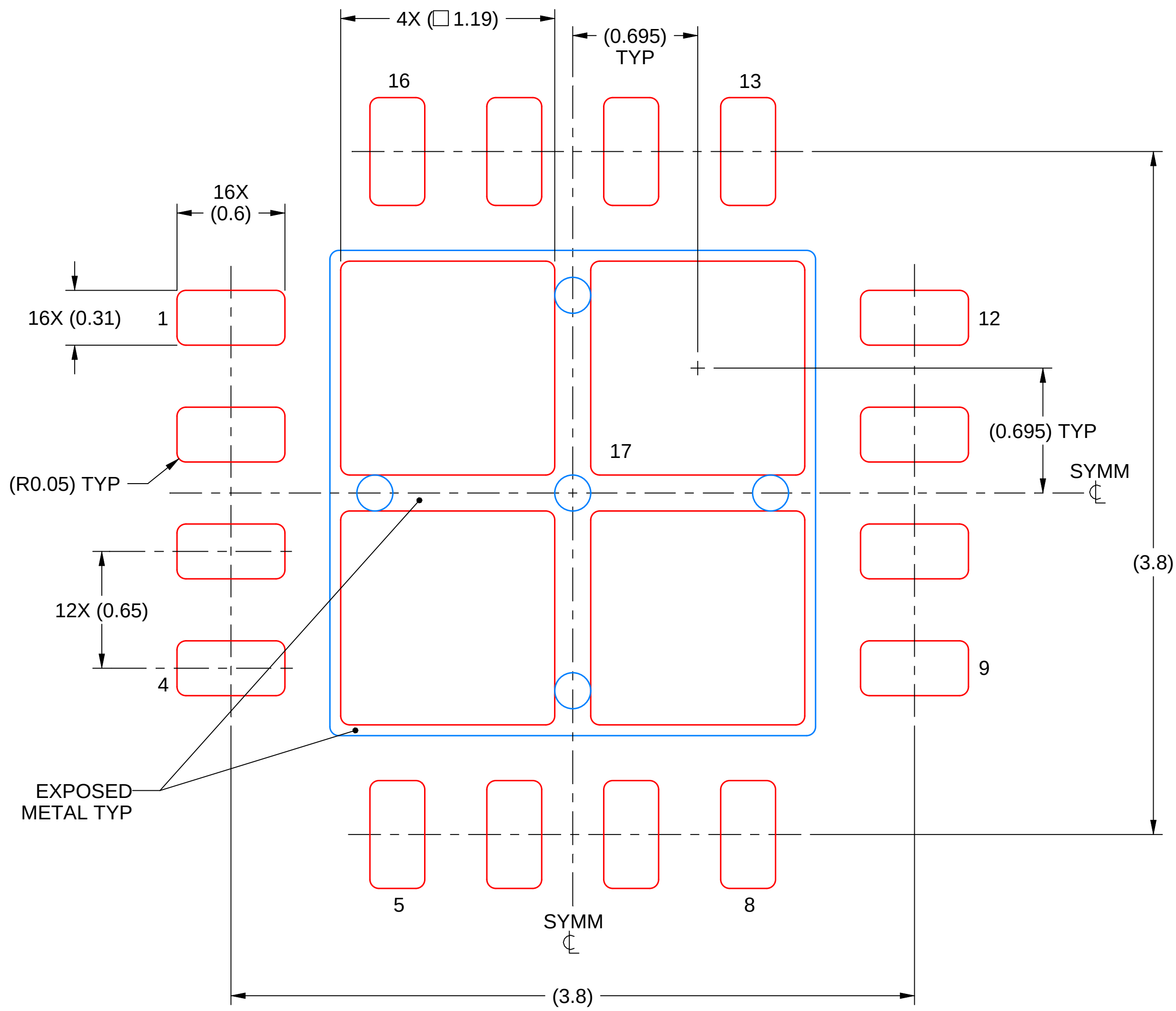
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219093/A 08/2021

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

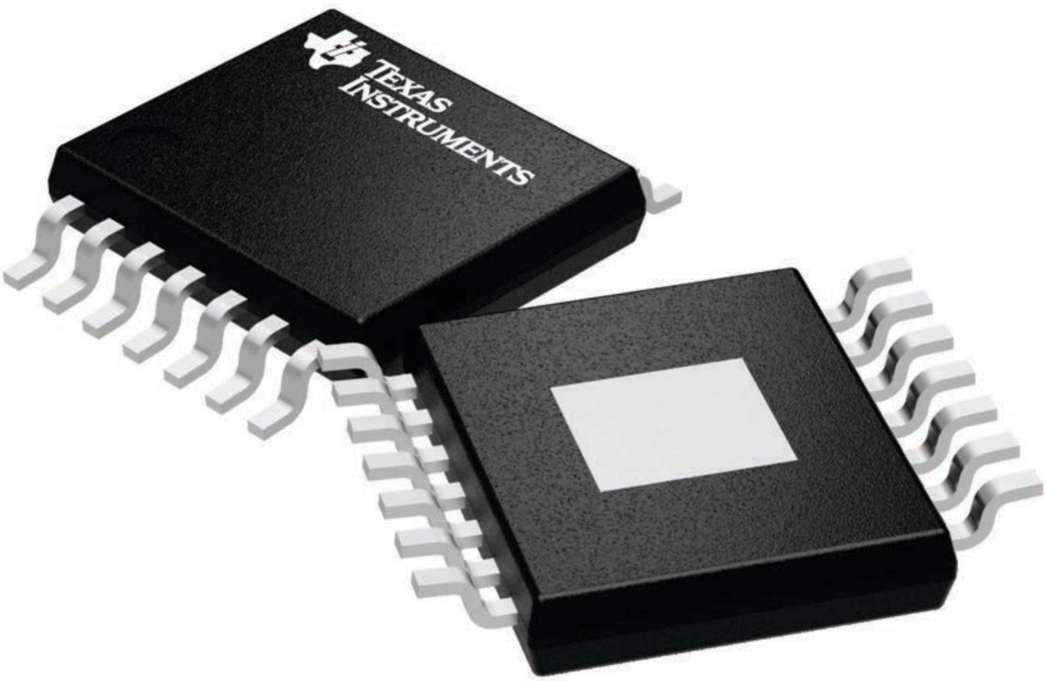
EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4219093/A 08/2021

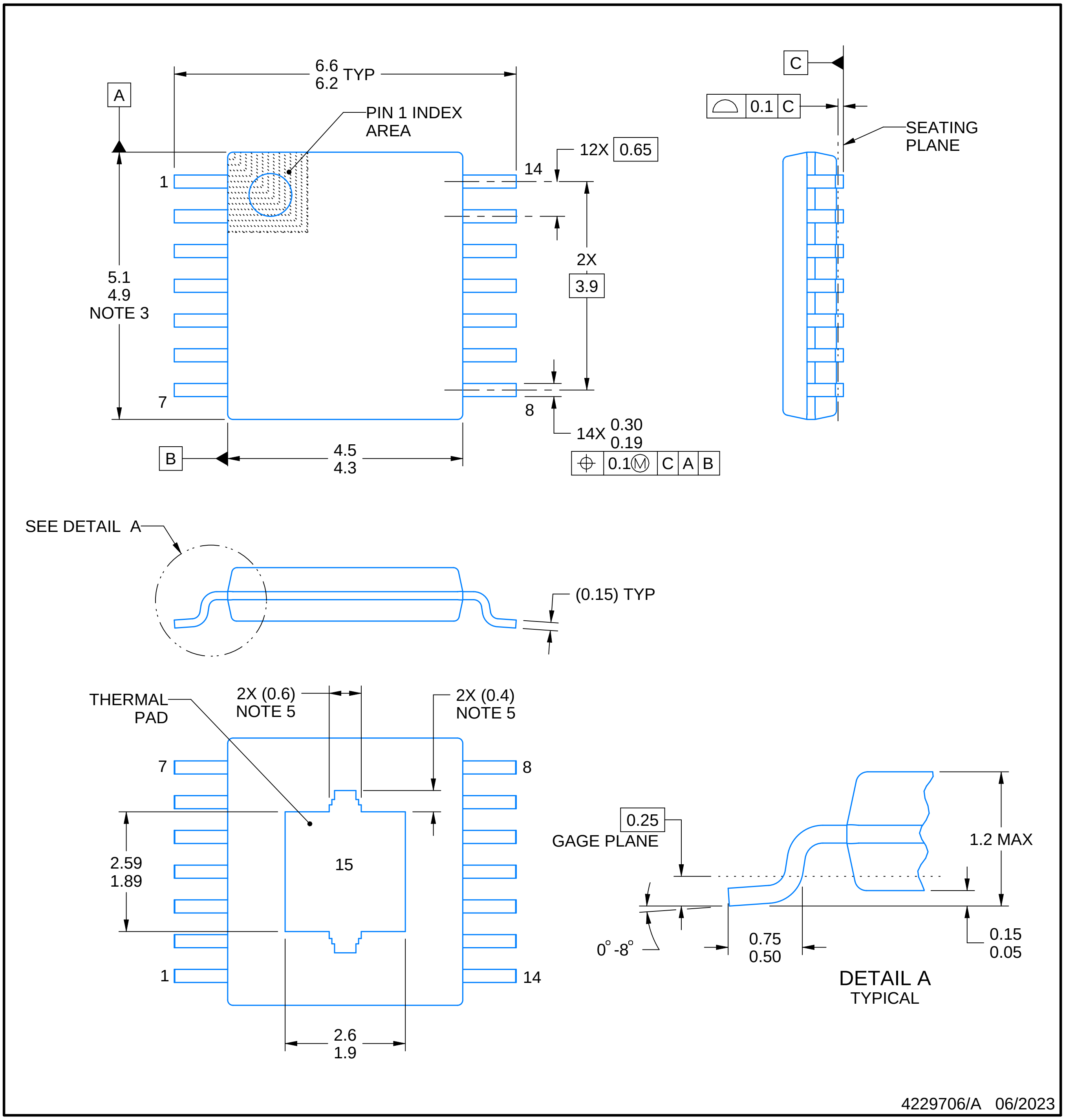
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



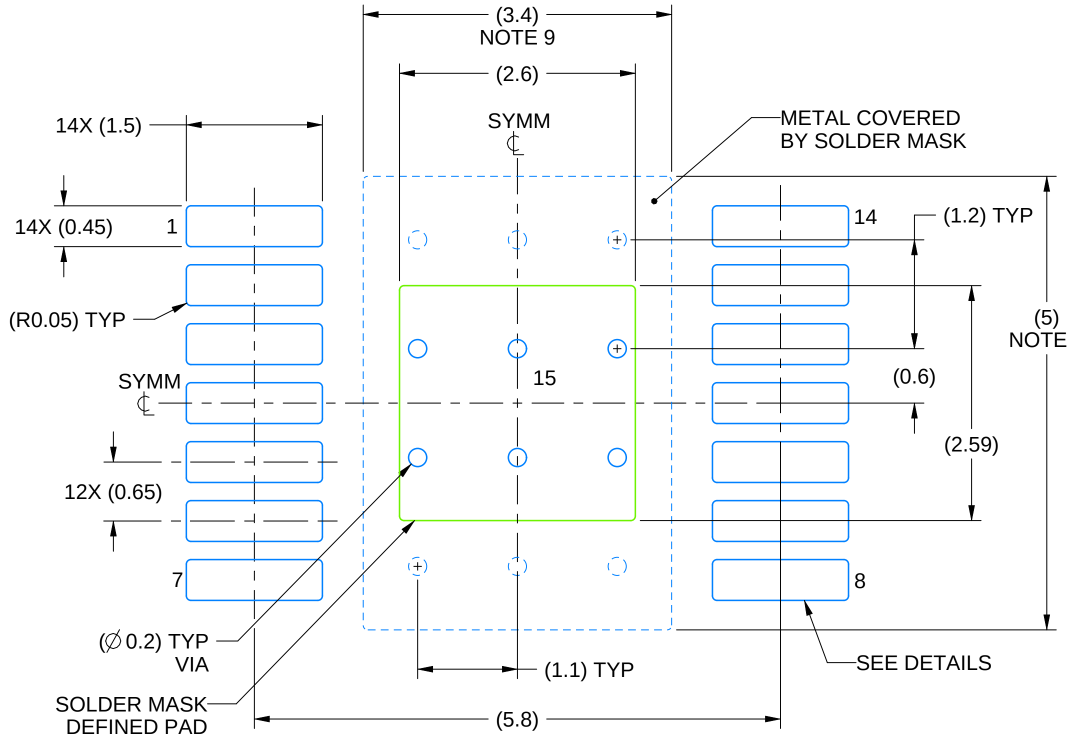
4224995/A



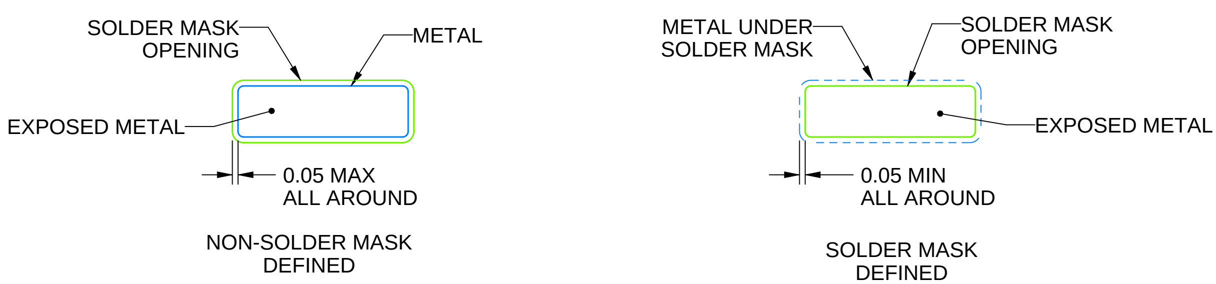
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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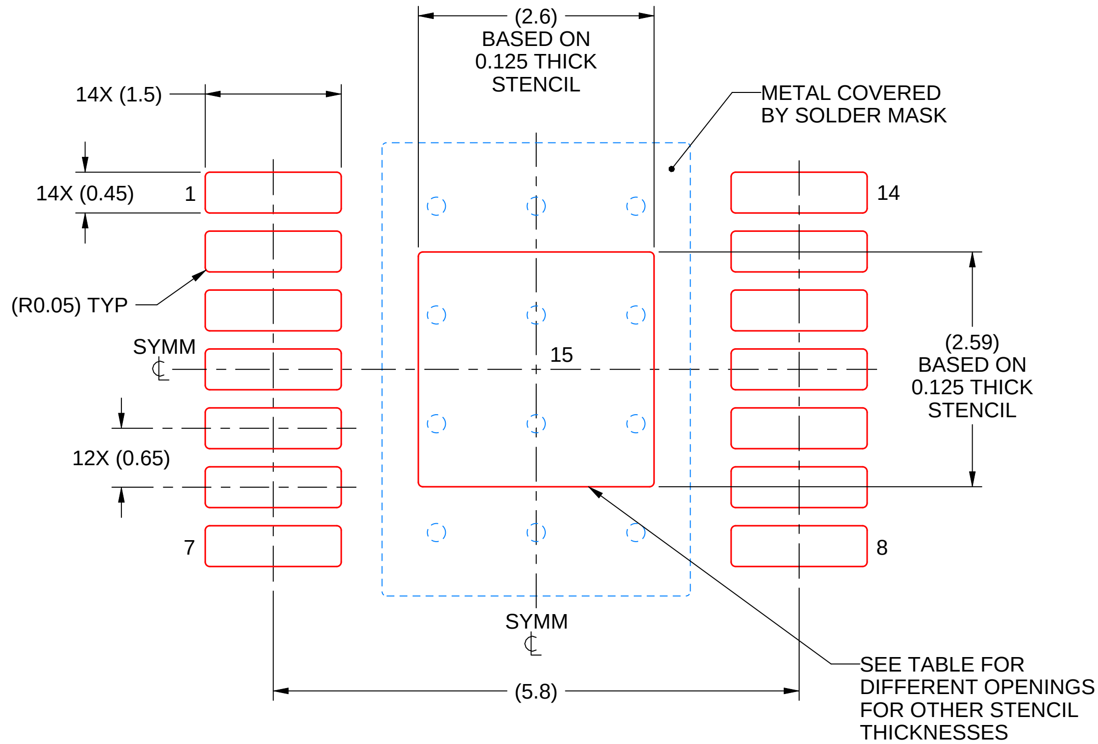
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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