采用 1x1.5 无引线小外形(SON)封装的 3MHz 超小型降压转换器

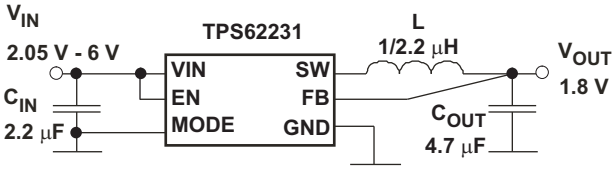
查询样品: TPS62231-Q1, TPS622314-Q1

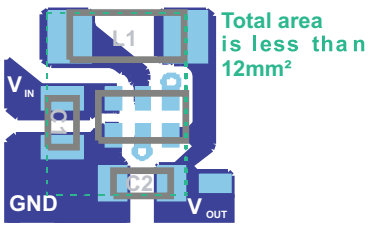
特性

- 符合汽车应用要求
- 开关频率**3MHz**
- 效率高达 **94%**
- 峰值输出电流高达 **500mA**
- 出色的 **AC** 和瞬态负载稳压
- 高电源抑制比**(PSRR)**（高达 **90dB**）
- 小型外部输出滤波器组件**1μH/4.7μF**
- 从**2.05V**至**6V**的V_{IN}范围
- 低输出波纹电压的优化省电模式
- 强制脉宽调制**(PWM)**模式工作
- 典型值**.22 μA** 静态电流
- 最低压降的 **100%** 占空比
- 小型 **1 × 1.5 × 0.6mm³SON** 封装
- **12 mm²**最小解决方案尺寸
- 支持的最大解决方案高度为**0.6mm**
- 具有**100μs**（典型值）启动时间的软启动

应用范围

- 低压降**(LDO)**替代产品
- 便携式音频、便携式媒体
- 手机
- 低功耗无线应用
- 低功耗数字信号处理器**(DSP)**核心电源
- 数码摄像机





说明

TPS6223x-Q1系列产品是一款高频同步降压型直流(DC)-DC转换器，此转换器非常适合电池供电的便携式应用。 它支持高达500mA的输出电流并且允许使用小型和低成本芯片电感器和电容器。

2.05V至6V的宽输入电压使得此器件能够支持由锂离子电池（具有拓展电压范围）供电的应用。 2.05V最小输入电压也允许使用一次性锂电池或者2节碱性电池。在1.0V至3.3V间可选择不同的固定输出电压版本。

TPS6223x-Q1系列产品特有高达3.8MHz的开关频率。从中等程度的负载到高负载，此转换器运行在PWM模式并在轻负载电流时自动进入省电模式运行以在全部负载电流范围内保持高效率。

由于它出色的PSRR和AC负载调节性能，此器件适合于取代线性稳压器以获得更好的电源转换效率。

TPS6223x-Q1的省电模式在轻负载运行时将静态流耗减至22μA。 已对此器件进行了优化，即使外部组件较小，此器件也可实现非常低的输出电压纹波并特有出色的ac负载调节。

对于那些对噪音非常敏感的应用，通过将MODE引脚电平拉高，此器件可被强制进入PWM模式运行。 在关断模式下，流耗减少至小于1μA。 TPS6223x-Q1采用1 × 1.5mm²6引脚SON封装。

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PART NUMBER	OUTPUT VOLTAGE	FREQUENCY [MHz]	PACKAGE DESIGNATOR	ORDERING	PACKAGE MARKING
–40°C to 105°C	TPS62231-Q1	1.8 V	3	DRY	TPS62231TDRYRQ1	31
	TPS622314-Q1	1.5 V	3	DRY	TPS622314TDRYRQ1	14

(1) For detailed ordering information see the PACKAGE OPTION ADDENDUM at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE		UNIT
			MIN	MAX	
V_I	Voltage at VIN and SW Pin(2)		–0.3	7	V
	Voltage at EN, MODE Pin(2)		–0.3	V_{IN} +0.3, ≤7	V
	Voltage at FB Pin (2)		–0.3	3.6	V
	Peak output current		internally limited		A
	ESD rating(3)	Human Body Model (HBM)		2	kV
		Charged Device Model CDM)		1	
		Machine Model (MM)		200	V
	Power dissipation		Internally limited		
T_J	Maximum operating junction temperature		–40	125	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JA}$	POWER RATING FOR $T_A \le 25°C$	DERATING FACTOR ABOVE $T_A = 25°C$
1 × 1.5 SON	234°C/W(2)	420 mW	4.2 mW/°C

(1) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_{J(max)} – T_A] / \theta_{JA}$.
(2) This thermal data is measured with high-K board (4 layers board according to JESD51-7 JEDEC standard).

RECOMMENDED OPERATING CONDITIONS

operating ambient temperature T_A = –40 to 105°C (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
Supply voltage V_{IN} (2)			2.05		6	V
Effective inductance				2.2		µH
Effective capacitance			2	4.7		µF
Recommended minimum supply voltage	$V_{OUT} \le V_{IN}$ -1 V(3)	500 mA maximum I_{OUT} (4)		3	3.6	V
		350 mA maximum I_{OUT} (4)		2.5	2.7	
	$V_{OUT} \le$ 1.8V	60 mA maximum output current(4)			2.05	
Operating junction temperature range, T_J			–40		125	°C

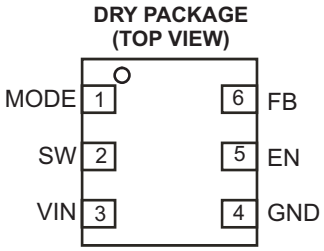
(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$.
(2) The minimum required supply voltage for startup is 2.05 V. The part is functional down to the falling UVL (Under Voltage Lockout) threshold.
(3) For a voltage difference between minimum V_{IN} and V_{OUT} of ≥ 1 V
(4) Typical value applies for T_A = 25°C, maximum value applies for T_A = 105°C with $T_J \le$ 125°C, PCB layout needs to support proper thermal performance.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, V_{OUT} = 1.8V, EN = V_{IN}, MODE = GND, T_A = –40°C to 105°C(1) typical values are at T_A = 25°C (unless otherwise noted), C_{IN} = 2.2µF, L = 2.2µH, C_{OUT} = 4.7µF, see parameter measurement information

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range (2)			2.05		6	V
I_Q	Operating quiescent current	I_{OUT} = 0mA. PFM mode enabled (Mode = 0) device not switching			22	40	µA
		I_{OUT} = 0mA. PFM mode enabled (Mode = 0) device switching, V_{IN} = 3.6V, V_{OUT} = 1.2V			25		µA
		I_{OUT} = 0 mA. Switching with no load (MODE/DATA = V_{IN}), PWM operation, V_{OUT} = 1.8V, L = 2.2µH			3		mA
I_{SD}	Shutdown current	EN = GND(3)			0.1	1	µA
UVLO	Undervoltage lockout threshold	Falling			1.8	1.9	V
		Rising			1.9	2.05	V
ENABLE, MODE THRESHOLD							
$V_{IH\ TH}$	Threshold for detecting high EN, MODE	2.05 V ≤ V_{IN} ≤ 6V , rising edge			0.8	1	V
$V_{IL\ TH\ HYS}$	Threshold for detecting low EN, MODE	2.05 V ≤ V_{IN} ≤ 6V , falling edge		0.4	0.6		V
I_{IN}	Input bias Current, EN, MODE	EN, MODE = GND or V_{IN} = 3.6V			0.01	0.5	µA
POWER SWITCH							
$R_{DS(ON)}$	High side MOSFET on-resistance	V_{IN} = 3.6V, T_{Jmax} = 105°C; $R_{DS(ON)}$ max value			600	850	mΩ
	Low Side MOSFET on-resistance				350	480	
I_{LIMF}	Forward current limit MOSFET high-side	V_{IN} = 3.6V, open loop		690	850	1050	mA
	Forward current limit MOSFET low side			550	840	1220	mA
T_{SD}	Thermal shutdown	Increasing junction temperature			150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature			20		°C
CONTROLLER							
t_{ONmin}	Minimum ON time	V_{IN} 3.6V, V_{OUT} = 1.8V, Mode = high, I_{OUT} = 0 mA			135		ns
t_{OFFmin}	Minimum OFF time				40		ns
OUTPUT							
V_{REF}	Internal Reference Voltage				0.70		V
V_{OUT}	Output voltage accuracy(4)	V_{IN} = 3.6V, Mode = GND, device operating in PFM Mode, I_{OUT} = 0mA			0%		
		V_{IN} = 3.6V, MODE = V_{IN}, I_{OUT} = 0 mA	T_A = 25°C	–2.0%		2.0%	
			T_A = –40°C to 105°C	–2.5%		2.5%	
	DC output voltage load regulation	PWM operation, Mode = V_{IN} = 3.6V, V_{OUT} = 1.8 V			0.001		%/mA
	DC output voltage line regulation	I_{OUT} = 0 mA, Mode = V_{IN}, 2.05V ≤ V_{IN} ≤ 6V			0		%/V
t_{Start}	Start-up Time	Time from active EN to V_{OUT} = 1.8V, V_{IN} = 3.6V, 10Ω load			100		µs
I_{LK_SW}	Leakage current into SW pin	V_{IN} = V_{OUT} = V_{SW} = 3.6 V, EN = GND(5)			0.1	0.5	µA

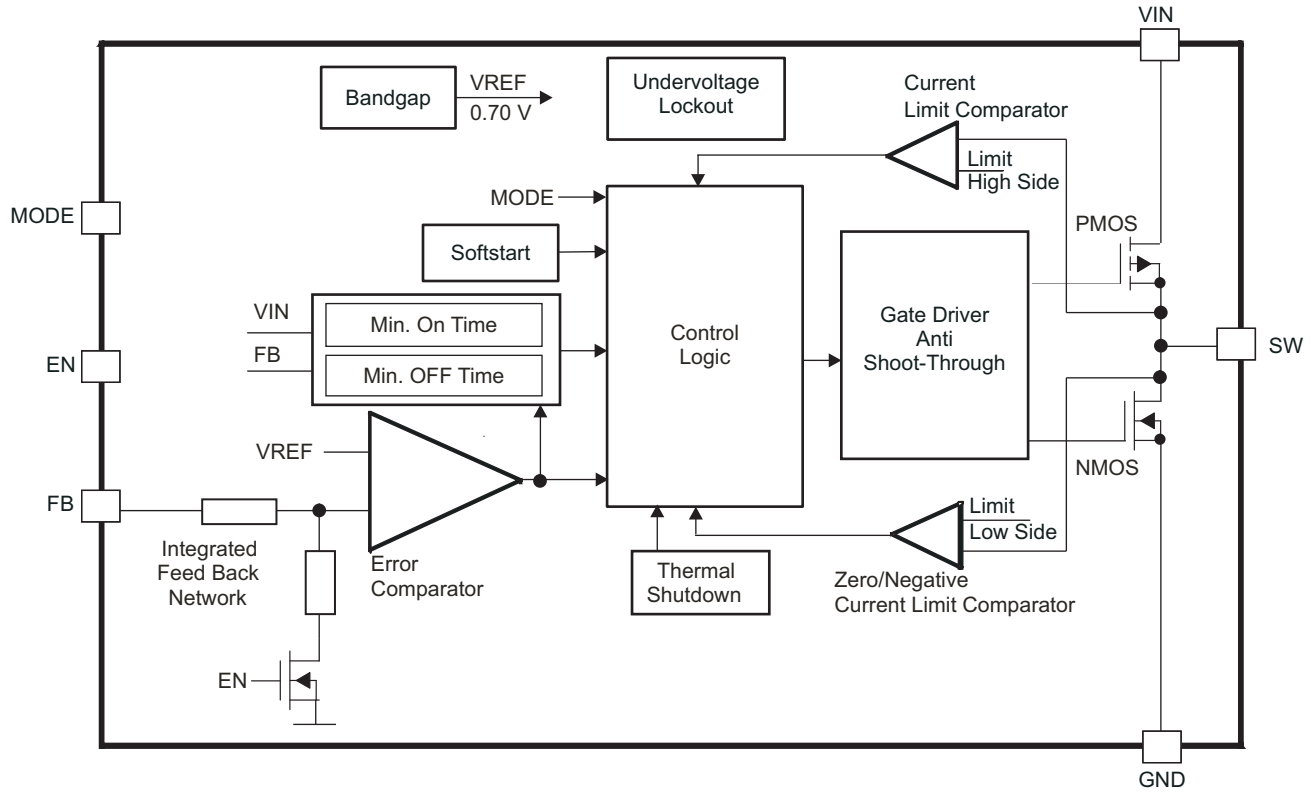
(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application (PD(max)), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$.
(2) The minimum required supply voltage for startup is 2.05V. The part is functional down to the falling UVL (Under Voltage Lockout) threshold
(3) Shutdown current into VIN pin, includes internal leakage
(4) $V_{IN} = V_O + 1.0$ V
(5) The internal resistor divider network is disconnected from FB pin.



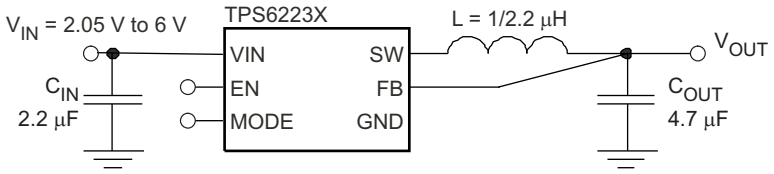
PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO		
VIN	3	PWR	V_{IN} power supply pin.
GND	4	PWR	GND supply pin
EN	5	IN	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
SW	2	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this terminal
FB	6	IN	Feedback Pin for the internal regulation loop. Connect this pin directly to the output capacitor.
MODE	1	IN	MODE pin = high forces the device to operate in PWM mode. Mode = low enables the Power Save Mode with automatic transition from PFM (Pulse frequency mode) to PWM (pulse width modulation) mode.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



C_{IN}: Murata GRM155R60J225ME15D 2.2 µF 0402 size

C_{OUT}: Murata GRM188R60J475ME 4.7 µF 0603 size, VOUT >= 1.8 V

C_{OUT}: Taiyo Yuden AMK105BJ475MV 4.7 µF 0402 size, VOUT = 1.2 V

l: Murata LQM2HPN1R0MJ0 1 µH, LQM2HPN2R2MJ0 2.2 µH,
size 2.5x2.0x1.2mm^3

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Load current	1, 2, 3, 4, 5, 6, 7
η	Efficiency	vs Output Current	8, 9, 10, 11
V_O	Output voltage	vs Output current	12, 13, 14, 15, 16, 17
	Switching frequency	vs Output current	18, 19, 20, 21, 22, 23, 24, 25, 26, 27
	Output voltage peak to peak	vs Output current	28,29
I_Q	Quiescent current	vs Ambient temperature	30
I_{SD}	Shutdown current	vs Ambient temperature	31
$r_{DS(ON)}$	PMOS Static drain-source on-state resistance	vs Supply voltage and ambient temperature	32
	NMOS Static drain-source on-state resistance	vs Supply voltage and ambient temperature	33
PSRR	Power supply rejection ratio	vs Frequency	34
	Typical operation		35, 36, 37
	Line transient response	PFM	38
		PWM	39
	Mode transition PFM / forced PWM		40
	AC - load regulation performance		41 42, 43
	Load transient response		44, 45, 46, 47
	Start-up		48, 49
	Spurious Output Noise, 12R Load		50
	Spurious Output Noise, 100R Load		51

TYPICAL CHARACTERISTICS (continued)

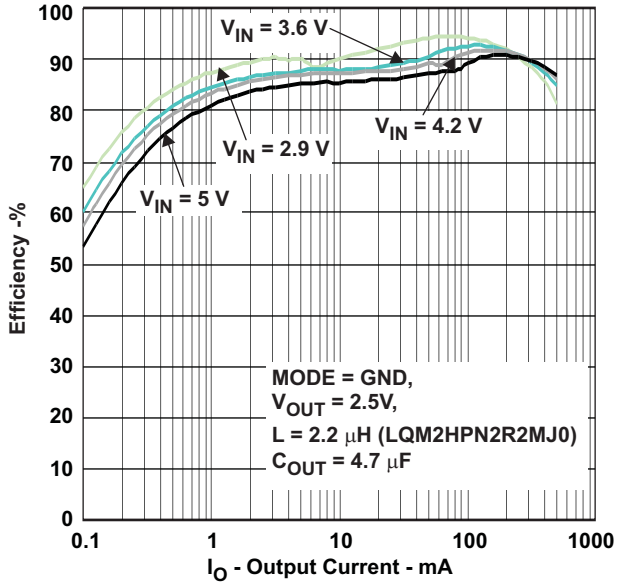


Figure 1. Efficiency PFM/PWM Mode 2.5V Output Voltage

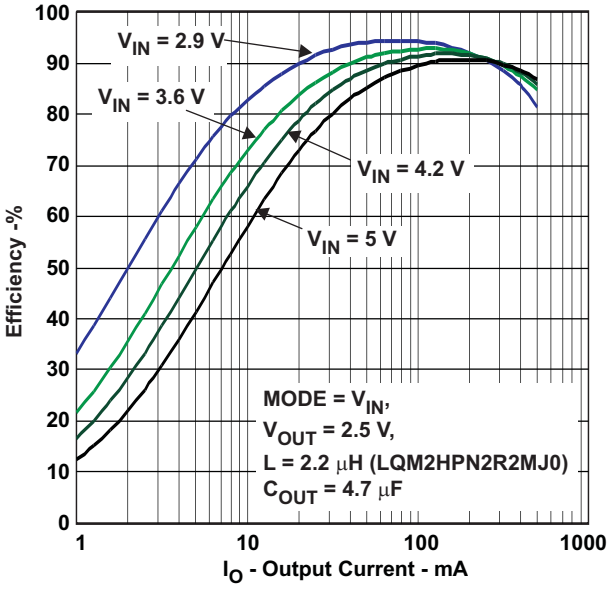


Figure 2. Efficiency Forced PWM Mode 2.5V Output Voltage

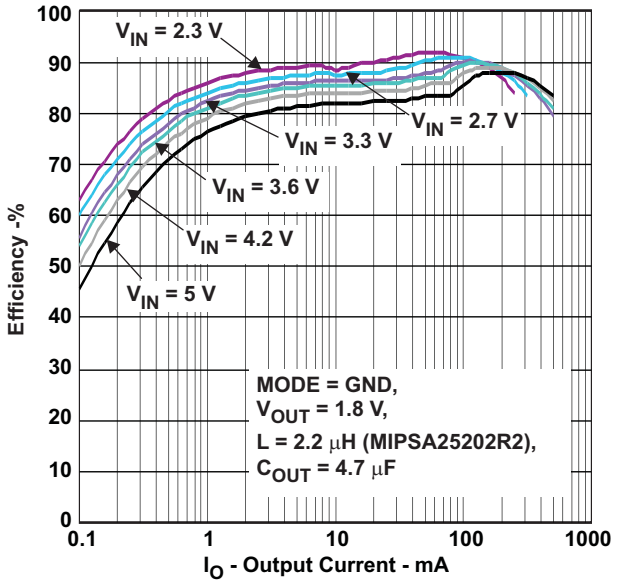


Figure 3. Efficiency PFM/PWM MODE 1.8V Output Voltage

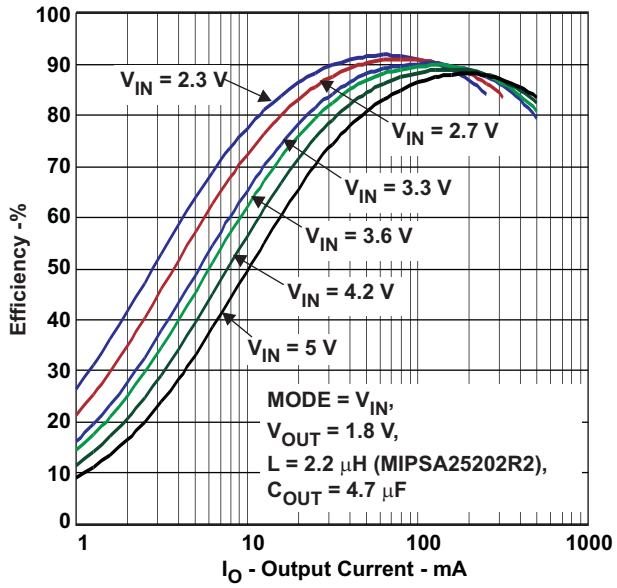


Figure 4. Efficiency Forced PWM Mode 1.8V Output voltage

TYPICAL CHARACTERISTICS (continued)

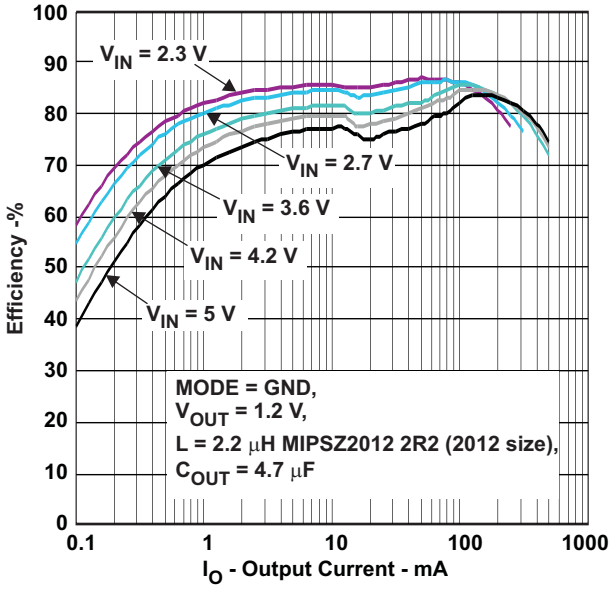


Figure 5. Efficiency PFM/PWM Mode 1.2V Output voltage

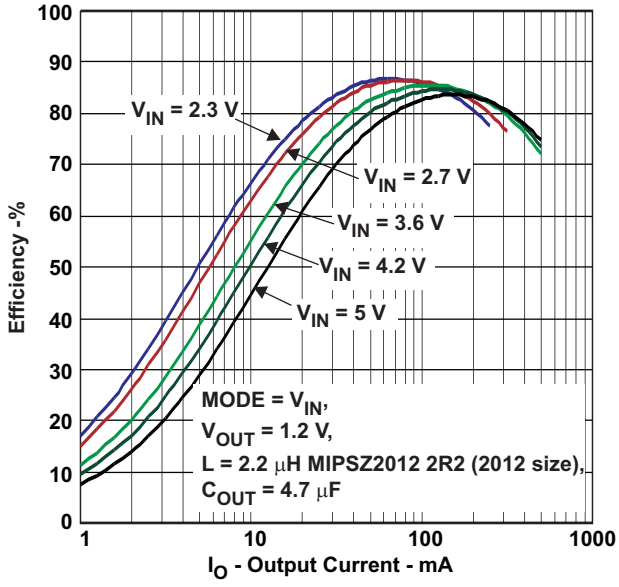


Figure 6. Efficiency Forced PWM Mode 1.2V Output Voltage

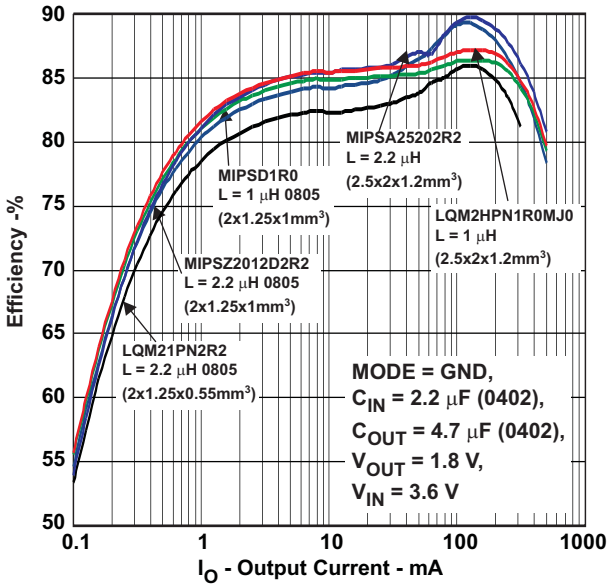


Figure 7. Comparison Efficiency vs Inductor Value and Size

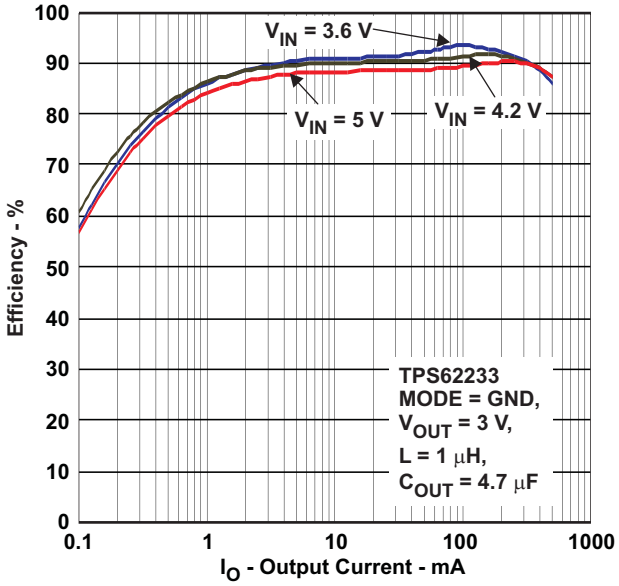


Figure 8. Comparison Efficiency vs I_{OUT} – TPS62233

TYPICAL CHARACTERISTICS (continued)

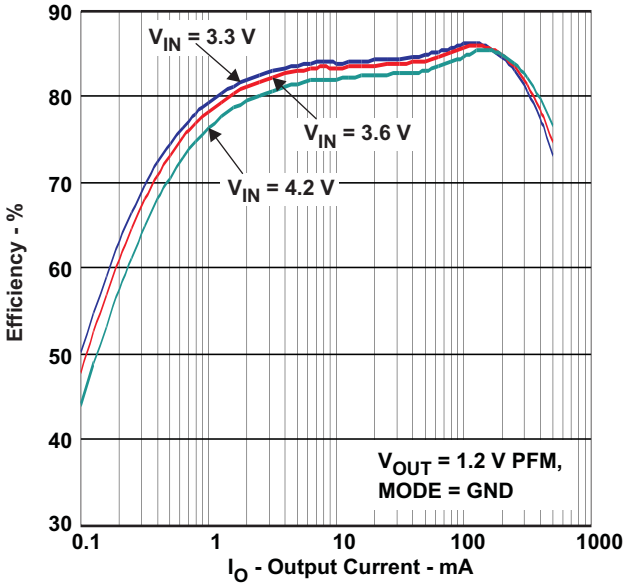


Figure 9. Comparison Efficiency vs I_{OUT} – TPS62235

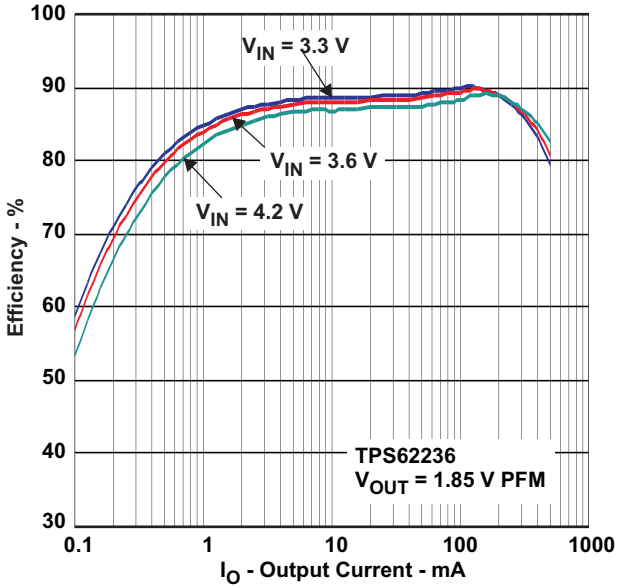


Figure 10. Comparison Efficiency vs I_{OUT} – TPS62236

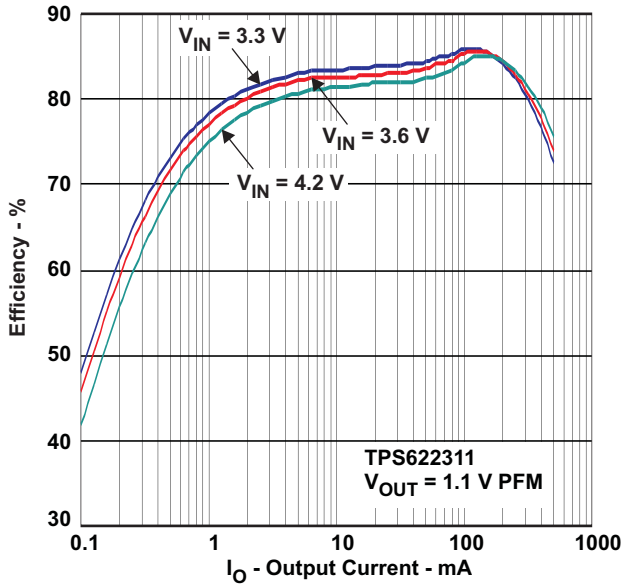


Figure 11. Comparison Efficiency vs I_{OUT} – TPS622311

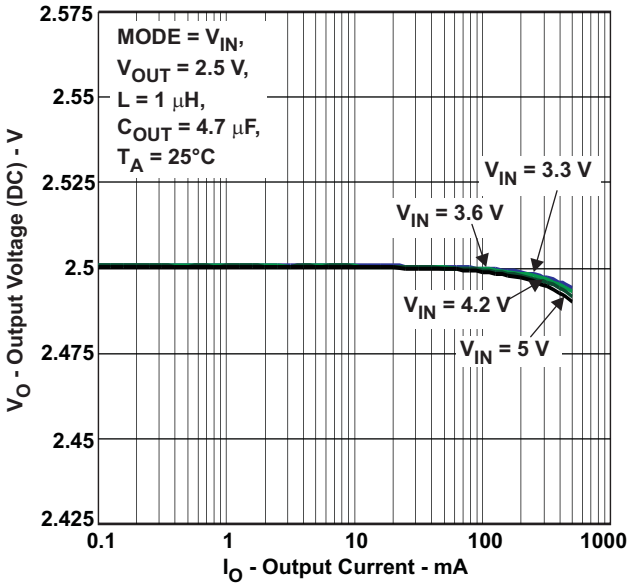


Figure 12. 2.5V Output Voltage Accuracy forced PWM Mode

TYPICAL CHARACTERISTICS (continued)

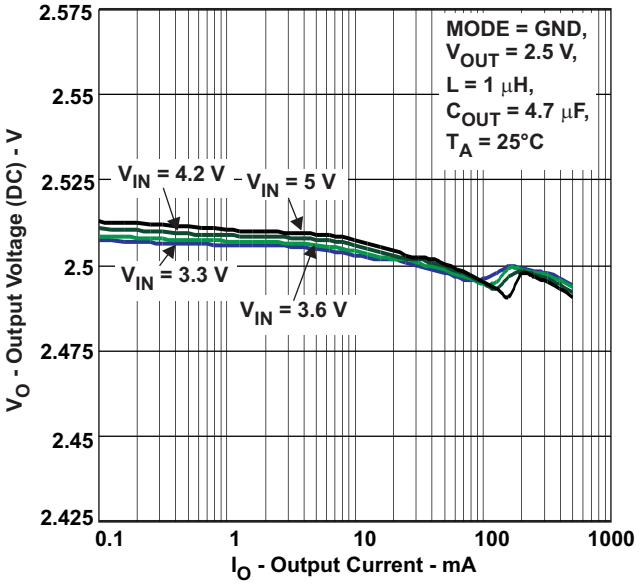


Figure 13. 2.5V Output Voltage Accuracy PFM/PWM Mode

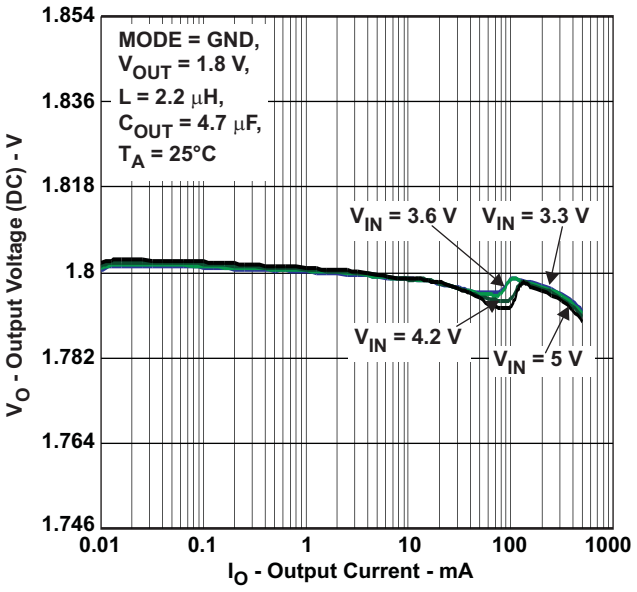


Figure 14. 1.8V Output Voltage Accuracy PFM/PWM Mode

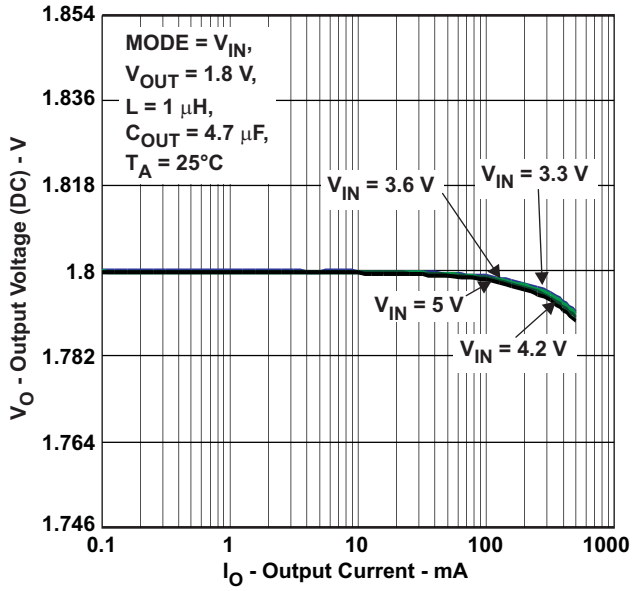


Figure 15. 1.8V Output Voltage Accuracy Forced PWM MODE

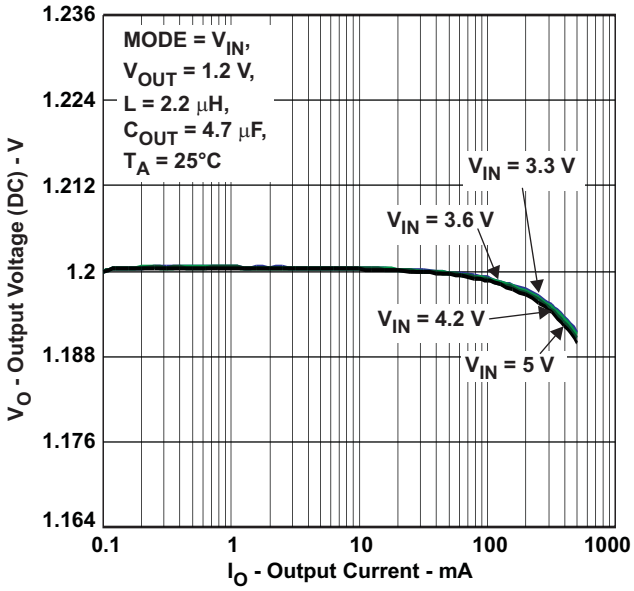


Figure 16. 1.2V Output Voltage Accuracy Forced PWM MODE

TYPICAL CHARACTERISTICS (continued)

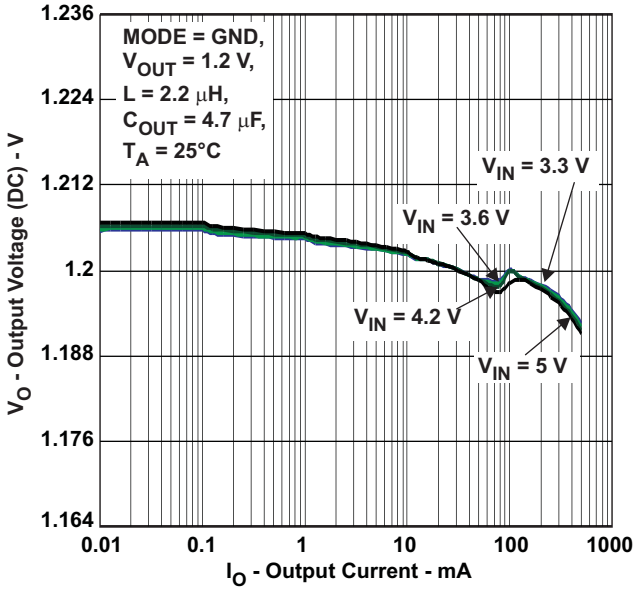


Figure 17. 1.2V Output Voltage Accuracy PFM/PWM MODE

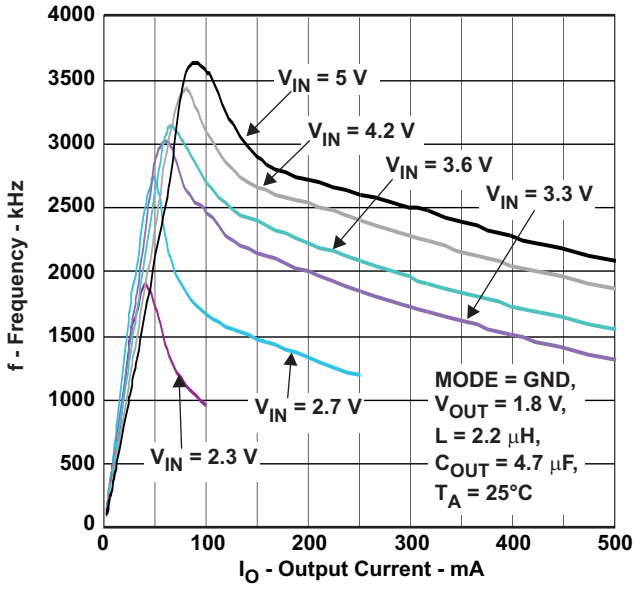


Figure 18. Switching Frequency vs Output Current, 1.8V Output Voltage MODE = GND

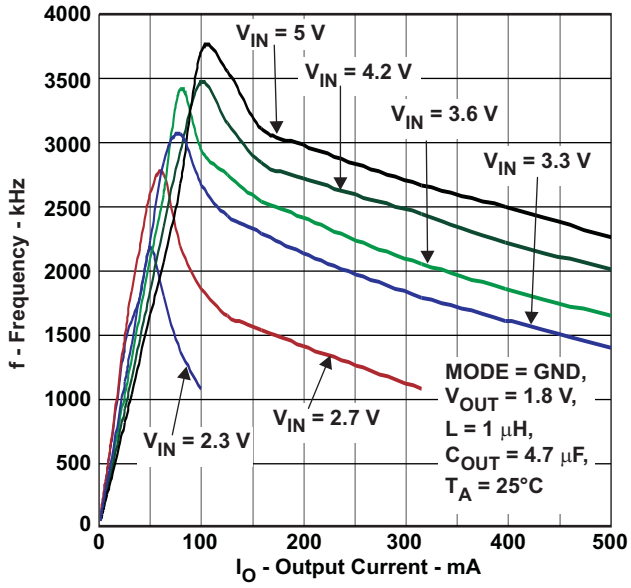


Figure 19. Switching Frequency vs Output Current, 1.8V Output Voltage MODE = GND

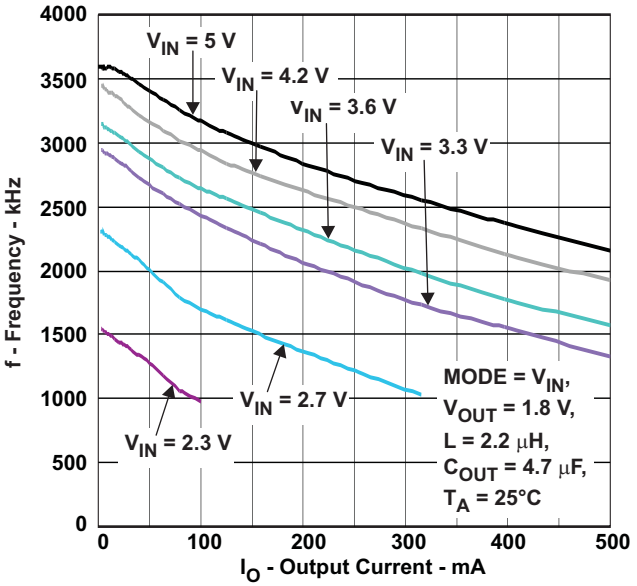


Figure 20. Switching Frequency vs Output Current, 1.8V Output Voltage MODE = V_{IN}

TYPICAL CHARACTERISTICS (continued)

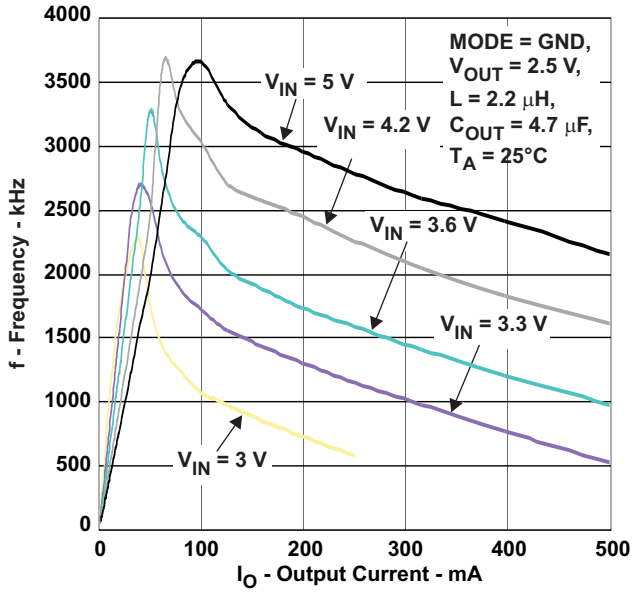


Figure 21. Switching Frequency vs Output Current, 2.5V Output Voltage MODE = GND

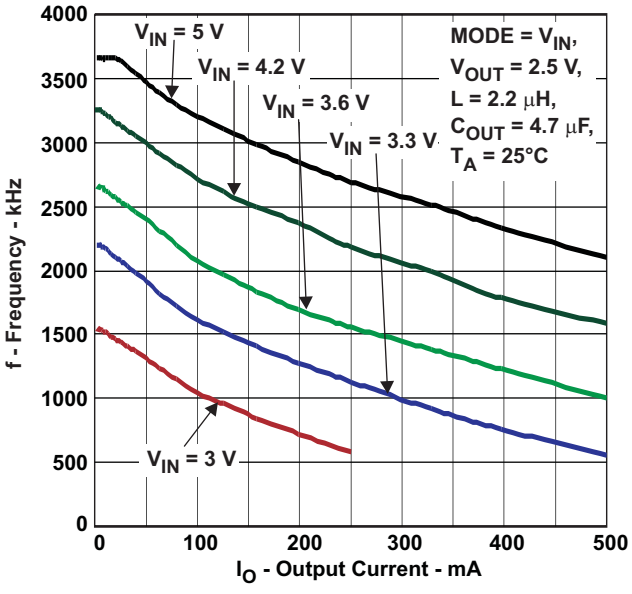


Figure 22. Switching Frequency vs Output Current, 2.5V Output Voltage MODE = V_{IN}

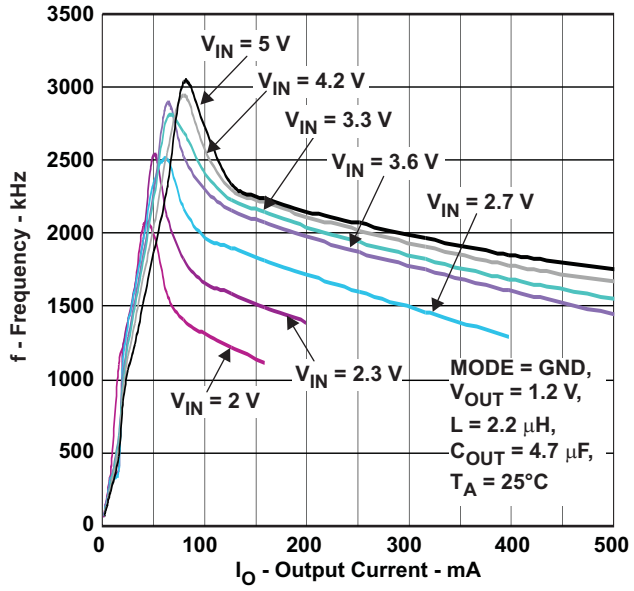


Figure 23. Switching Frequency vs Output Current, 1.2V Output Voltage MODE = GND

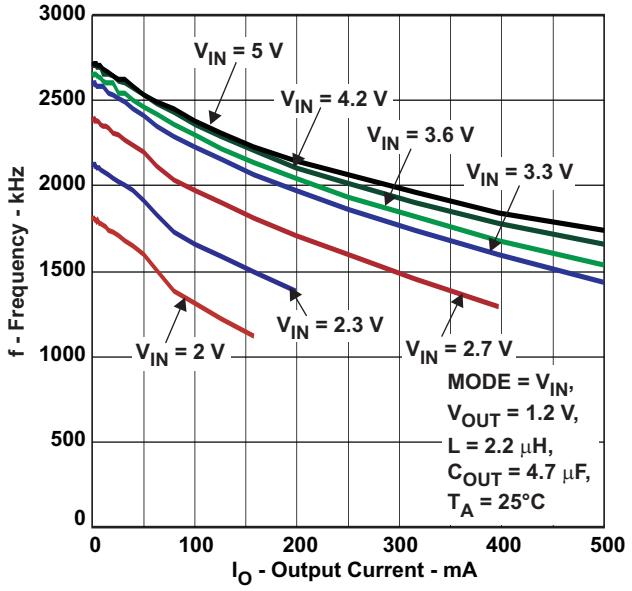


Figure 24. Switching Frequency vs Output Current, 1.2V Output Voltage MODE = V_{IN}

TYPICAL CHARACTERISTICS (continued)

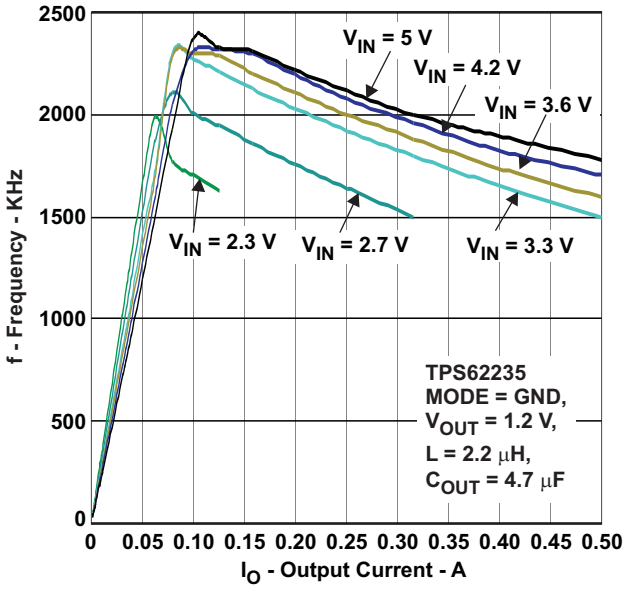


Figure 25. Switching Frequency vs Output Current, 1.2V Output Voltage MODE = PFM – TPS62235

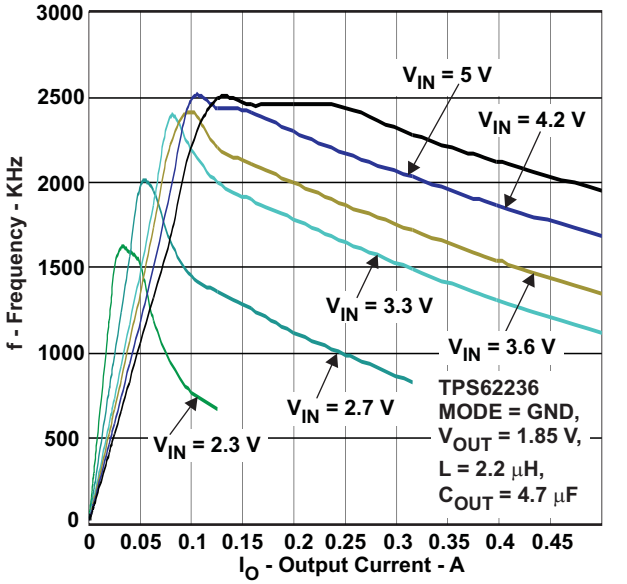


Figure 26. Switching Frequency vs Output Current, 1.85V Output Voltage MODE = PFM –TPS62236

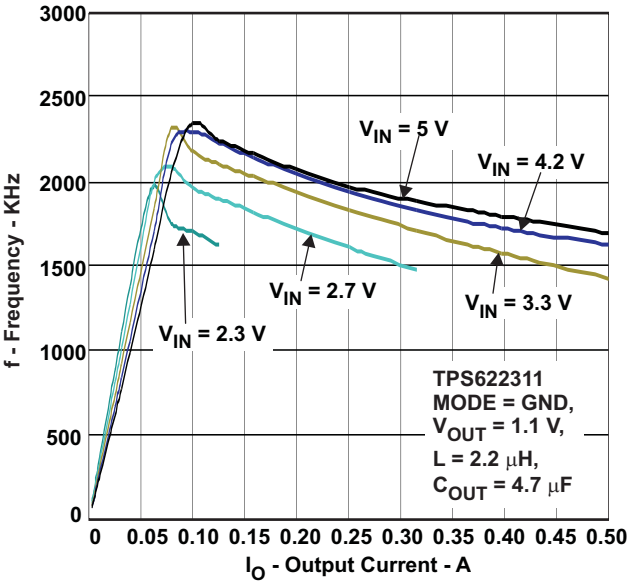


Figure 27. Switching Frequency vs Output Current, 1.1V Output Voltage MODE = PFM – TPS622311

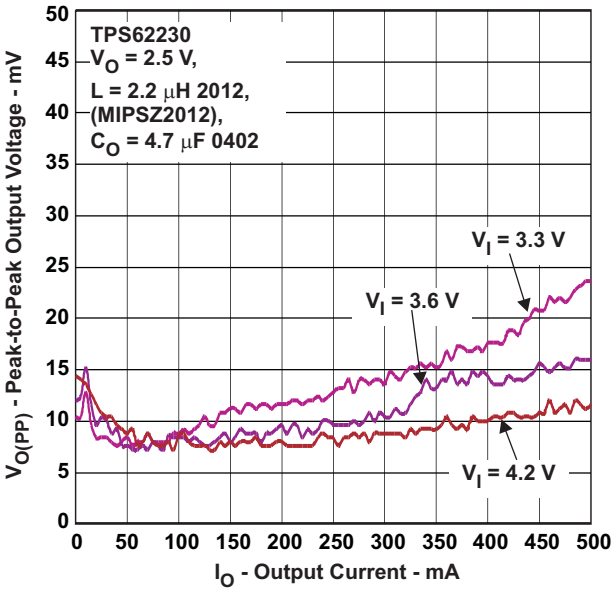


Figure 28. Output Voltage, Peak-to-Peak vs Output Current - TPS62230

TYPICAL CHARACTERISTICS (continued)

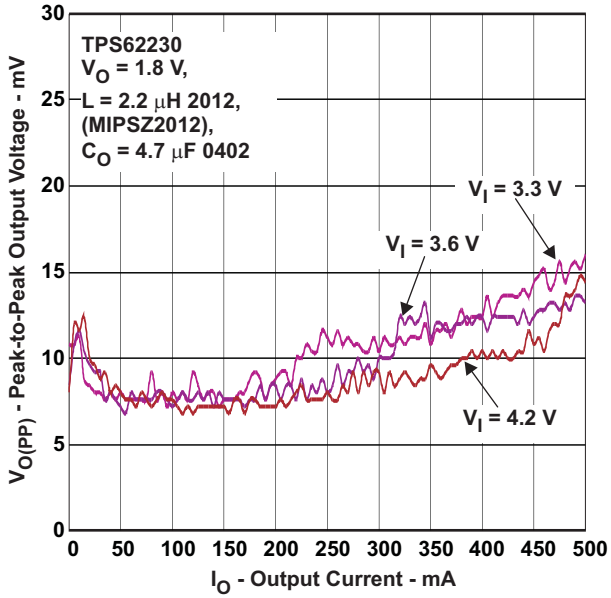


Figure 29. Output Voltage, Peak-to-Peak vs Output Current – TPS62231-Q1

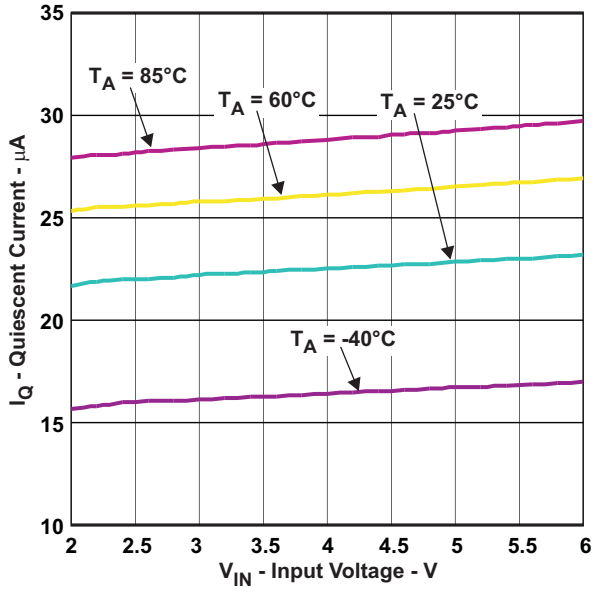


Figure 30. Quiescent Current I_Q vs Ambient Temperature T_A

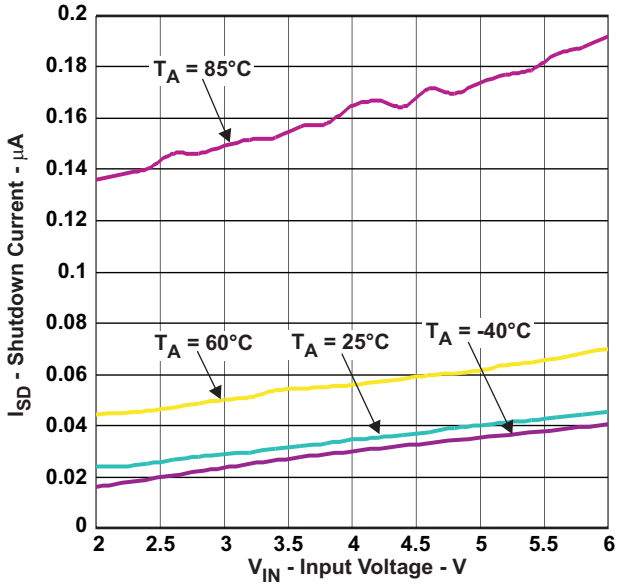


Figure 31. Shutdown Current I_{SD} vs Ambient Temperature T_A

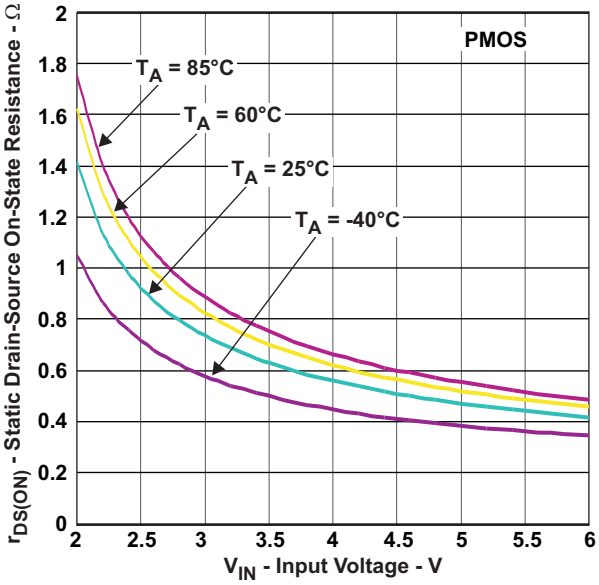


Figure 32. PMOS $R_{DS(ON)}$ vs Supply Voltage V_{IN} and Ambient Temperature T_A

TYPICAL CHARACTERISTICS (continued)

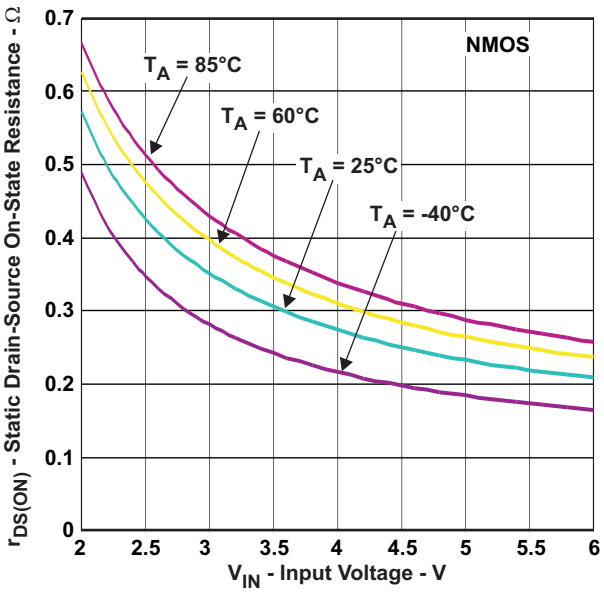


Figure 33. NMOS $R_{DS(ON)}$ vs Supply Voltage V_{IN} and Ambient Temperature T_A

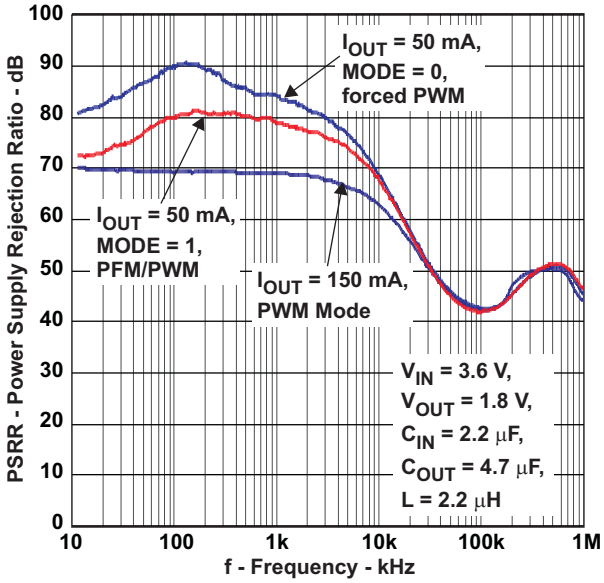


Figure 34. TPS62231 1.8V PSRR

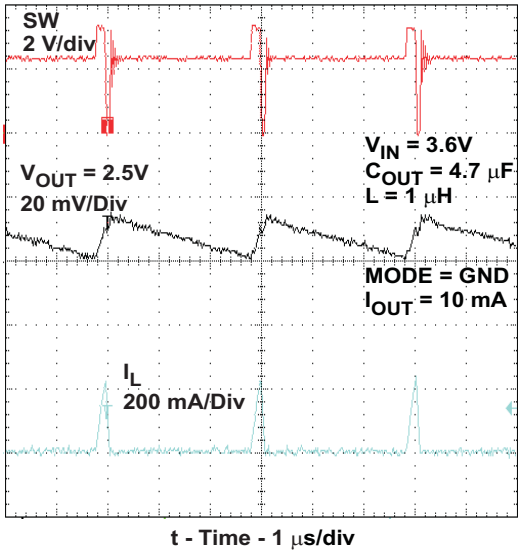


Figure 35. PFM Mode Operation I_{OUT} = 10mA

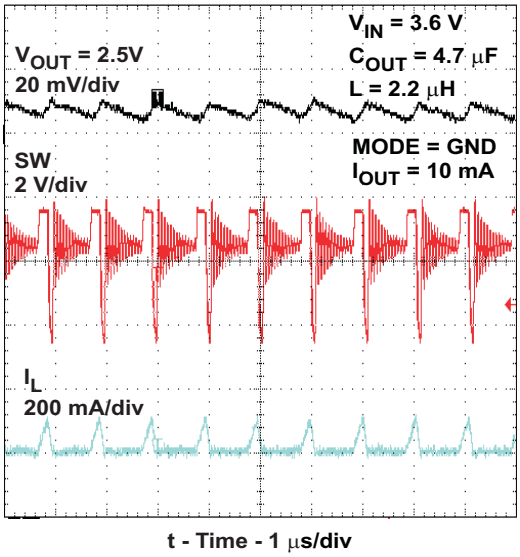


Figure 36. PFM Mode Operation I_{OUT} = 10mA

TYPICAL CHARACTERISTICS (continued)

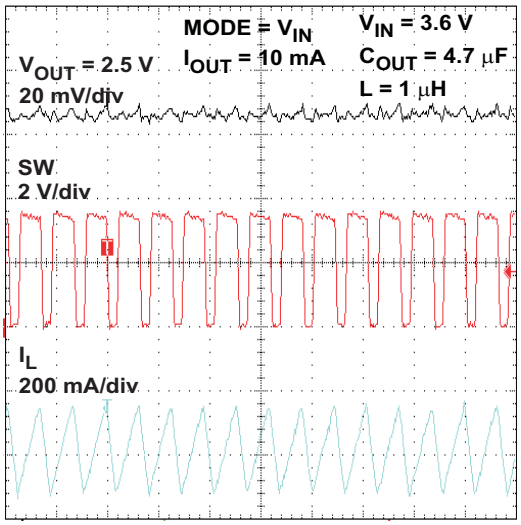


Figure 37. Forced PWM Mode Operation I_{OUT} = 10mA

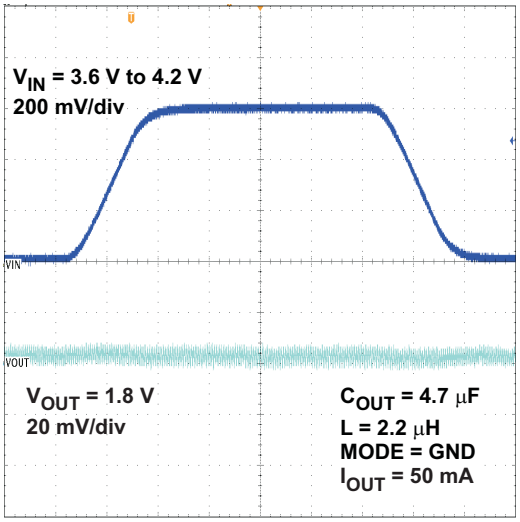


Figure 38. Line Transient Response PFM Mode

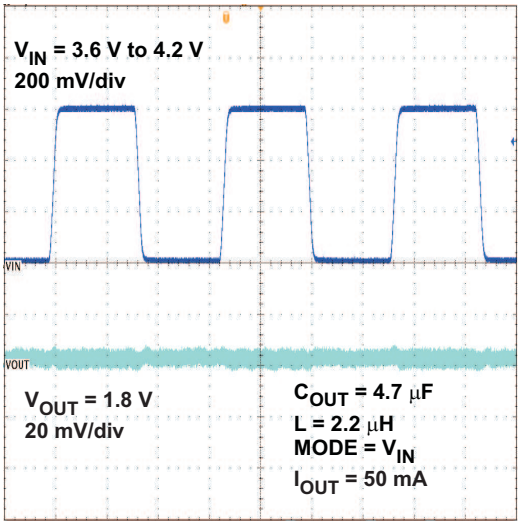


Figure 39. Line Transient Response PWM Mode

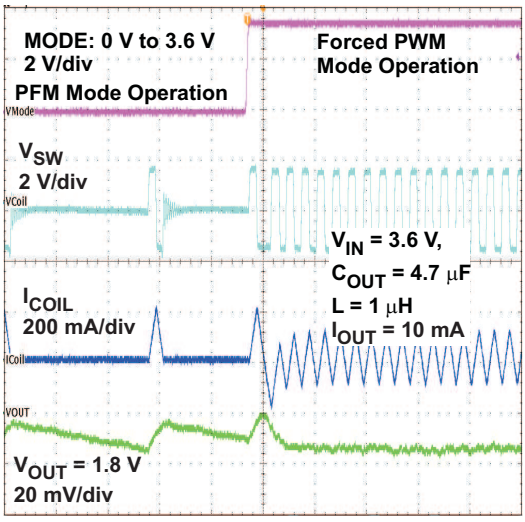


Figure 40. Mode Transition PFM / Forced PWM Mode

TYPICAL CHARACTERISTICS (continued)

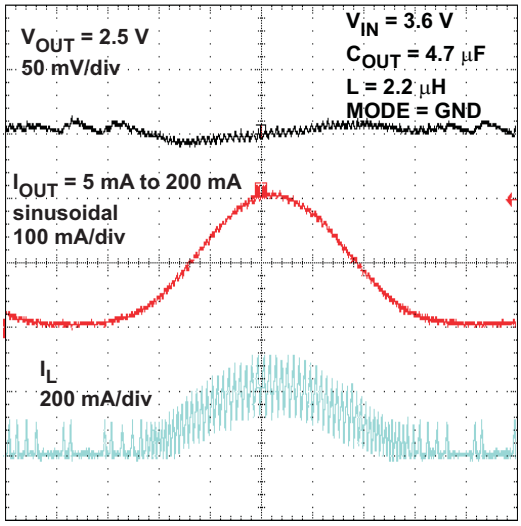


Figure 41. AC – Load Regulation Performance 2.5V V_{OUT} PFM Mode

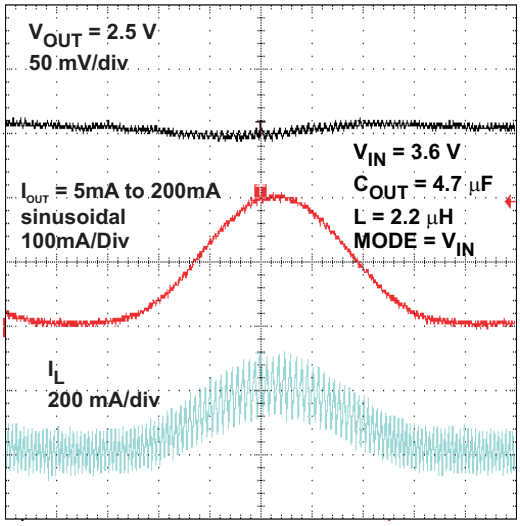


Figure 42. AC – Load Regulation Performance 2.5V V_{OUT} PWM Mode

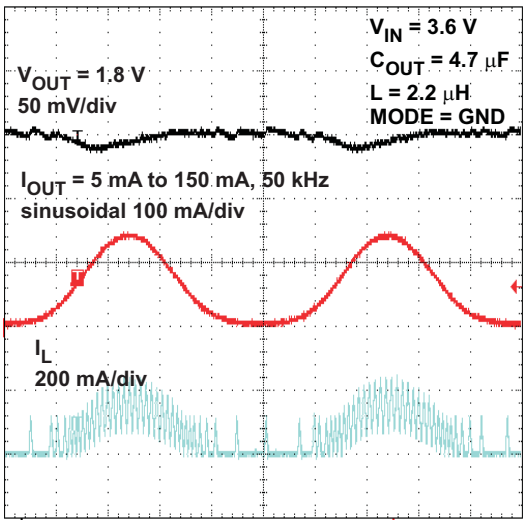


Figure 43. AC – Load Regulation Performance 1.8V V_{OUT} PFM Mode

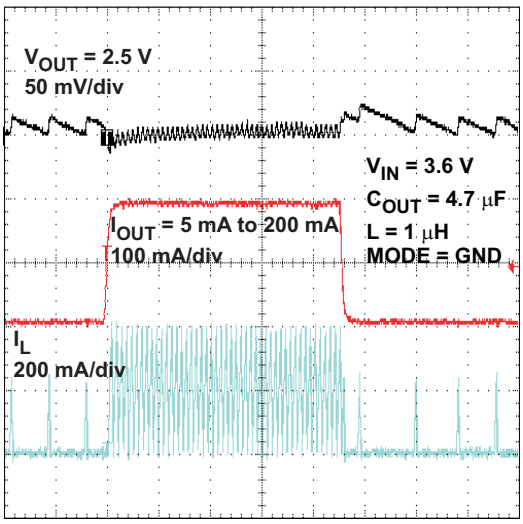


Figure 44. Load Transient Response 5mA to 200mA PFM to PWM Mode, V_{OUT} 2.5V

TYPICAL CHARACTERISTICS (continued)

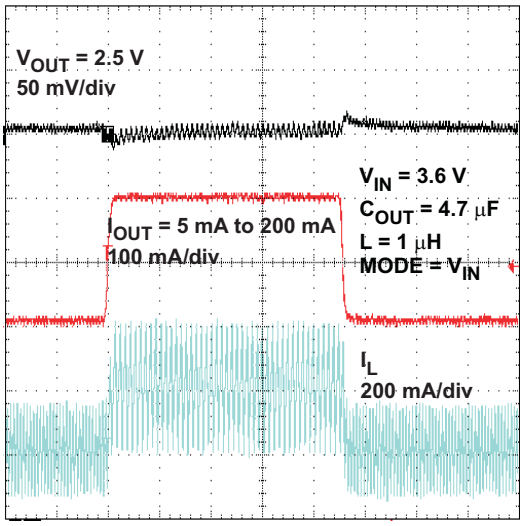


Figure 45. Load Transient Response 5mA to 200mA, Forced PWM Mode, V_{OUT} 2.5V

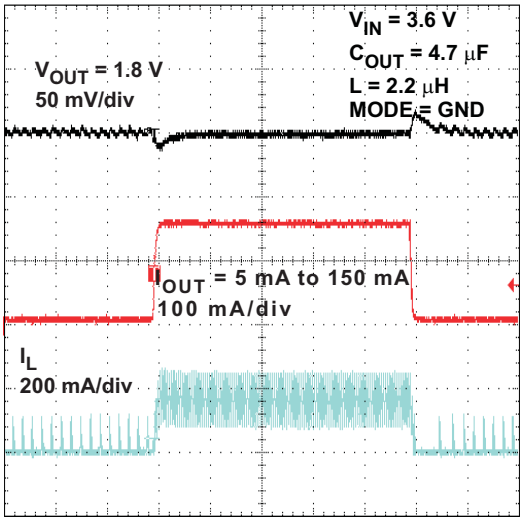


Figure 46. Load Transient Response 5mA to 150mA, PFM to PWM Mode, V_{OUT} 1.8V

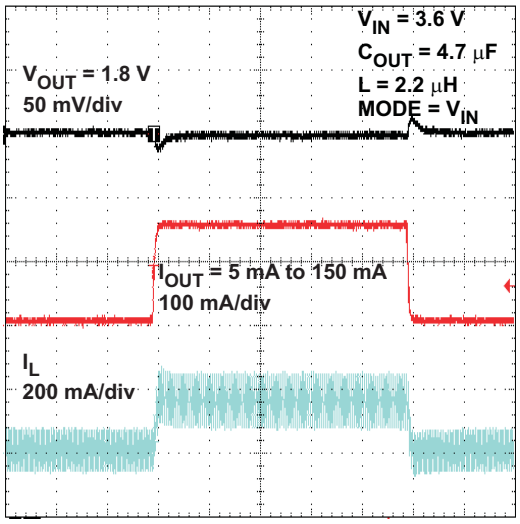


Figure 47. Load Transient Response 5mA to 150mA, Forced PWM Mode, V_{OUT} 1.8V

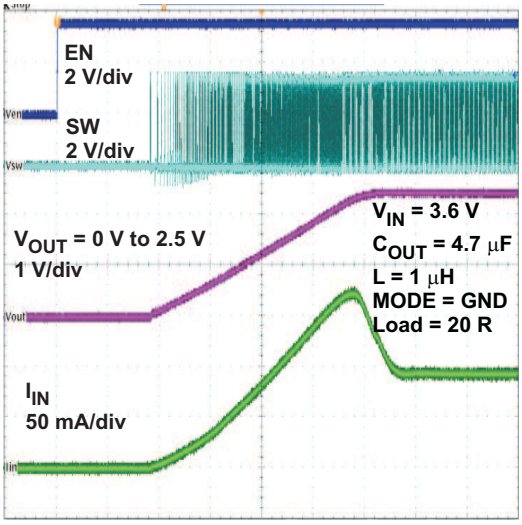


Figure 48. Start Up into 20Ω Load, V_{OUT} 2.5V

TYPICAL CHARACTERISTICS (continued)

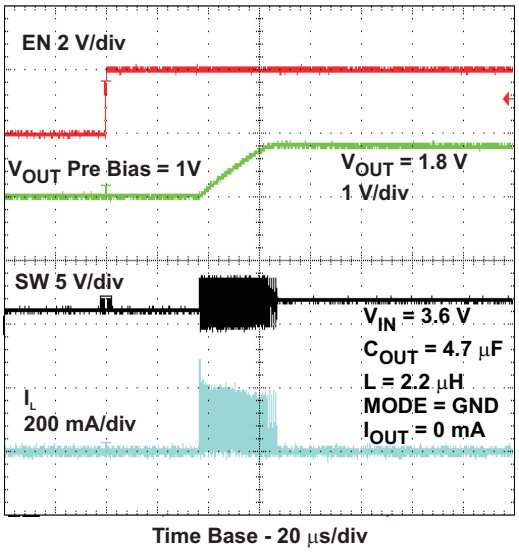


Figure 49. Startup in 1V Pre-biased Output

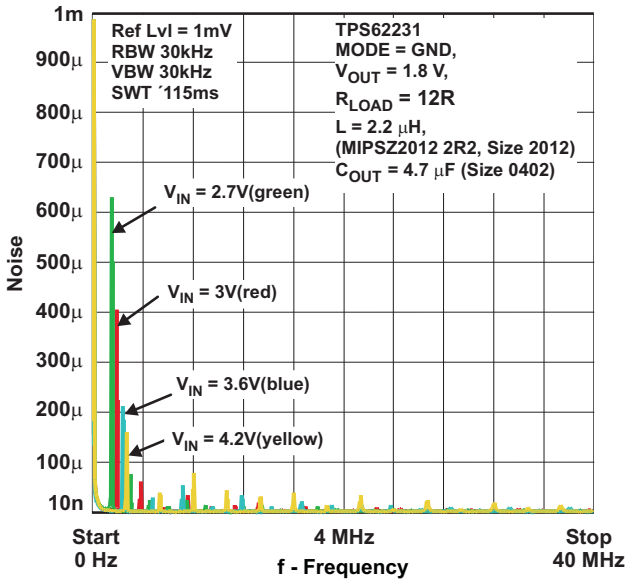


Figure 50. Spurious Output Noise, 12R Load, TPS62231-Q1

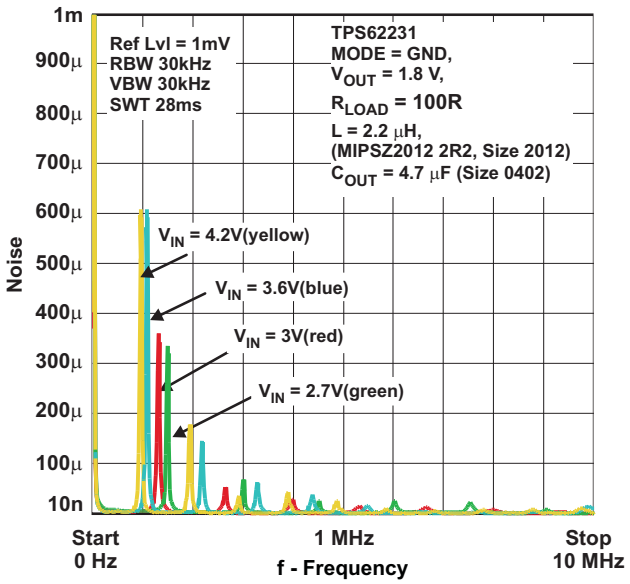


Figure 51. Spurious Output Noise, 100R Load, TPS62231-Q1

DETAILED DESCRIPTION

The TPS6223x-Q1 synchronous step down converter family includes a unique hysteretic PWM controller scheme which enables switch frequencies over 3MHz, excellent transient and AC load regulation as well as operation with cost competitive external components.

The controller topology supports forced PWM Mode as well as Power Save Mode operation. Power Save Mode operation reduces the quiescent current consumption down to 22 µA and ensures high conversion efficiency at light loads by skipping switch pulses. In forced PWM Mode, the device operates on a quasi fixed frequency, avoids pulse skipping, and allows filtering of the switch noise by external filter components.

The TPS6223x-Q1 devices offer fixed output voltage options featuring smallest solution size by using only three external components.

The internal switch current limit of typical 850 mA supports output currents of up to 500 mA, depending on the operating condition.

A significant advantage of TPS6223x-Q1 compared to other hysteretic PWM controller topologies is its excellent DC and AC load regulation capability in combination with low output voltage ripple over the entire load range which makes this part well suited for audio and RF applications.

OPERATION

Once the output voltage falls below the threshold of the error comparator, a switch pulse is initiated, and the high side switch is turned on. It remains turned on until a minimum on time of t_{ONmin} expires and the output voltage trips the threshold of the error comparator or the inductor current reaches the high side switch current limit. Once the high side switch turns off, the low side switch rectifier is turned on and the inductor current ramps down until the high side switch turns on again or the inductor current reaches zero.

In forced PWM Mode operation, negative inductor current is allowed to enable continuous conduction mode even at no load condition.

POWER SAVE MODE

Connecting the MODE pin to GND enables the automatic PWM and power-save mode operation. The converter operates in quasi fixed frequency PWM mode at moderate to heavy loads and in the PFM (Pulse Frequency Modulation) mode during light loads, which maintains high efficiency over a wide load current range. In PFM Mode, the device starts to skip switch pulses and generates only single pulses with an on time of t_{ONmin}. The PFM Mode frequency depends on the load current and the external inductor and output capacitor values. The PFM Mode of TPS6223x-Q1 is optimized for low output voltage ripple if small external components are used. Even at low output currents, the PFM frequency is above the audible noise spectrum and makes this operation mode suitable for audio applications.

The on time t_{ONmin} can be estimated to:

$$t_{ONmin} = \frac{V_{OUT}}{V_{IN}} \times 260\ ns \quad (1)$$

Therefore, the peak inductor current in PFM mode is approximately:

$$I_{LPFMpeak} = \frac{(V_{IN} - V_{OUT})}{L} \times t_{ONmin} \quad (2)$$

The transition from PFM into PWM mode and vice versa can be estimated to:

$$I_{OUT\_PFM/PWM} = 0.5 \times I_{LPFMpeak} \quad (3)$$

With

t_{ON}: High side switch on time [ns]
V_{IN}: Input voltage [V]
V_{OUT}: Output voltage [V]
L : Inductance [µH]
$I_{LPFMpeak}$: PFM inductor peak current [mA]
$I_{OUT\_PFM/PWM}$: Output current for PFM to PWM mode transition and vice versa [mA]

FORCED PWM MODE

Pulling the MODE pin high forces the converter to operate in a continuous conduction PWM mode even at light load currents. The advantage is that the converter operates with a quasi fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

For additional flexibility, it is possible to switch from power-save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

100% DUTY CYCLE LOW DROPOUT OPERATION

The device starts to enter 100% duty cycle mode once the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the High Side switch is turned on 100% for one or more cycles.

With further decreasing V_{IN} the High Side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_{OUT}max + I_{OUT}max \times \left(R_{DS(on)}max + R_L\right) \quad (4)$$

With:

$I_{OUT}max$ = maximum output current plus inductor ripple current
$R_{DS(on)}max$ = maximum P-channel switch RDSon.
R_L = DC resistance of the inductor
$V_{OUT}max$ = nominal output voltage plus maximum output voltage tolerance

UNDER VOLTAGE LOCKOUT

The under voltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions. The TPS6223x-Q1 devices have a UVLO threshold set to 1.8V (typical). Fully functional operation is permitted for input voltage down to the falling UVLO threshold level. The converter starts operation again once the input voltage trips the rising UVLO threshold level.

SOFT START

The TPS6223x-Q1 has an internal soft-start circuit that controls the ramp up of the output voltage and limits the inrush current during start-up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input of the converter.

The soft-start system generates a monotonic ramp up of the output voltage and reaches the nominal output voltage typically 100µs after EN pin was pulled high.

Should the output voltage not have reached its target value by this time, such as in the case of heavy load, the converter then operates in a current limit mode set by its switch current limits.

TPS6223x-Q1 is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

ENABLE / SHUTDOWN

The device starts operation when EN is set high and starts up with the soft start as previously described. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN pin low forces the device into shutdown, with a shutdown quiescent current of typically 0.1 µA. In this mode, the P and N-channel MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal-control circuitry is switched off.

The EN input can be used to control power sequencing in a system with various DC/DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails.

SHORT-CIRCUIT PROTECTION

The TPS6223x-Q1 integrates a High Side and Low Side MOSFET current limit to protect the device against heavy load or short circuit. The current in the switches is monitored by current limit comparators. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on to ramp down the current in the inductor. The High Side MOSFET switch can only turn on again, once the current in the Low Side MOSFET switch has decreased below the threshold of its current limit comparator.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the High Side and Low Side MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

APPLICATION INFORMATION

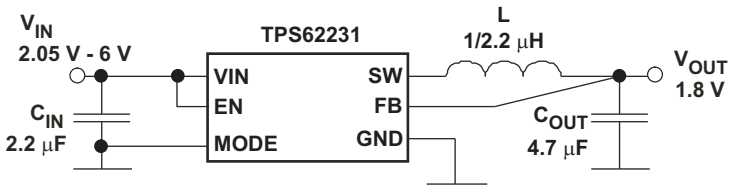


Figure 52. TPS62231 1.8V Output

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The TPS6223x-Q1 is optimized to operate with effective inductance values in the range of 0.7 µH to 4.3 µH and with effective output capacitance in the range of 2 µF to 15 µF. The internal compensation is optimized to operate with an output filter of L = 1 µH/2.2 µH and C_{OUT} = 4.7 µF. Larger or smaller inductor/capacitor values can be used to optimize the performance of the device for specific operation conditions. For more details, see the *CHECKING LOOP STABILITY* section.

INDUCTOR SELECTION

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}. Equation 5 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 6. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (5)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (6)$$

With:

f = Switching Frequency
L = Inductor Value
ΔI_L = Peak to Peak inductor ripple current
I_{Lmax} = Maximum Inductor current

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e., quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance, $R_{(DC)}$, and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS6223x-Q1 converters.

Table 1. List of inductors

INDUCTANCE [µH]	DIMENSIONS [mm3]	INDUCTOR TYPE	SUPPLIER
1.0/2.2	2.5 × 2.0 × 1.2	LQM2HPN1R0MJ0	Murata
2.2	2.0 × 1.2 × 0.55	LQM21PN2R2	Murata
1.0/2.2	2.0 × 1.2 × 1.0	MIPSZ2012	FDK
1.0/2.2	2.0 × 2.5 × 1.2	MIPSA2520	FDK
1.0/2.2	2.0 × 1.2 × 1.0	KSLI2012 series	Hitachi Metal

OUTPUT CAPACITOR SELECTION

The unique hysteretic PWM control scheme of the TPS62230 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents the converter operate in Power Save Mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM Mode and tighten DC output accuracy in PFM Mode.

INPUT CAPACITOR SELECTION

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications a 2.2 µF to 4.7 µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering. Because ceramic capacitor loses up to 80% of its initial capacitance at 5 V, it is recommended to use 4.7 µF input capacitors for input voltages > 4.5 V.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 2 shows a list of tested input/output capacitors.

Table 2. List of Capacitor

CAPACITANCE [µF]	SIZE	CAPACITOR TYPE	SUPPLIER
2.2	0402	GRM155R60J225	Murata
4.7	0402	AMK105BJ475MV	Taiyo Yuden
4.7	0402	GRM155R60J475	Murata
4.7	0402	CL05A475MQ5NRNC	Samsung
4.7	0603	GRM188R60J475	Murata

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between

the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Use a common Power GND node and a different node for the Signal GND to minimize the effects of ground noise. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The FB line should be connected to the output capacitor and routed away from noisy components and traces (e.g. SW line).

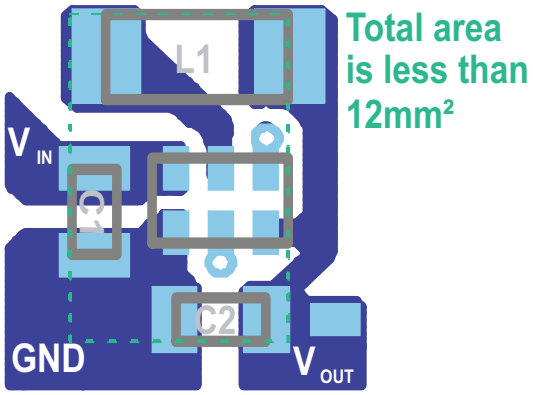


Figure 53. Recommended PCB Layout for TPS6223x-Q1

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS622314TDRYRQ1	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	14
TPS622314TDRYRQ1.A	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	14
TPS62231TDRYRQ1	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	31
TPS62231TDRYRQ1.A	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	31

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

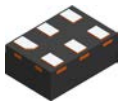
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

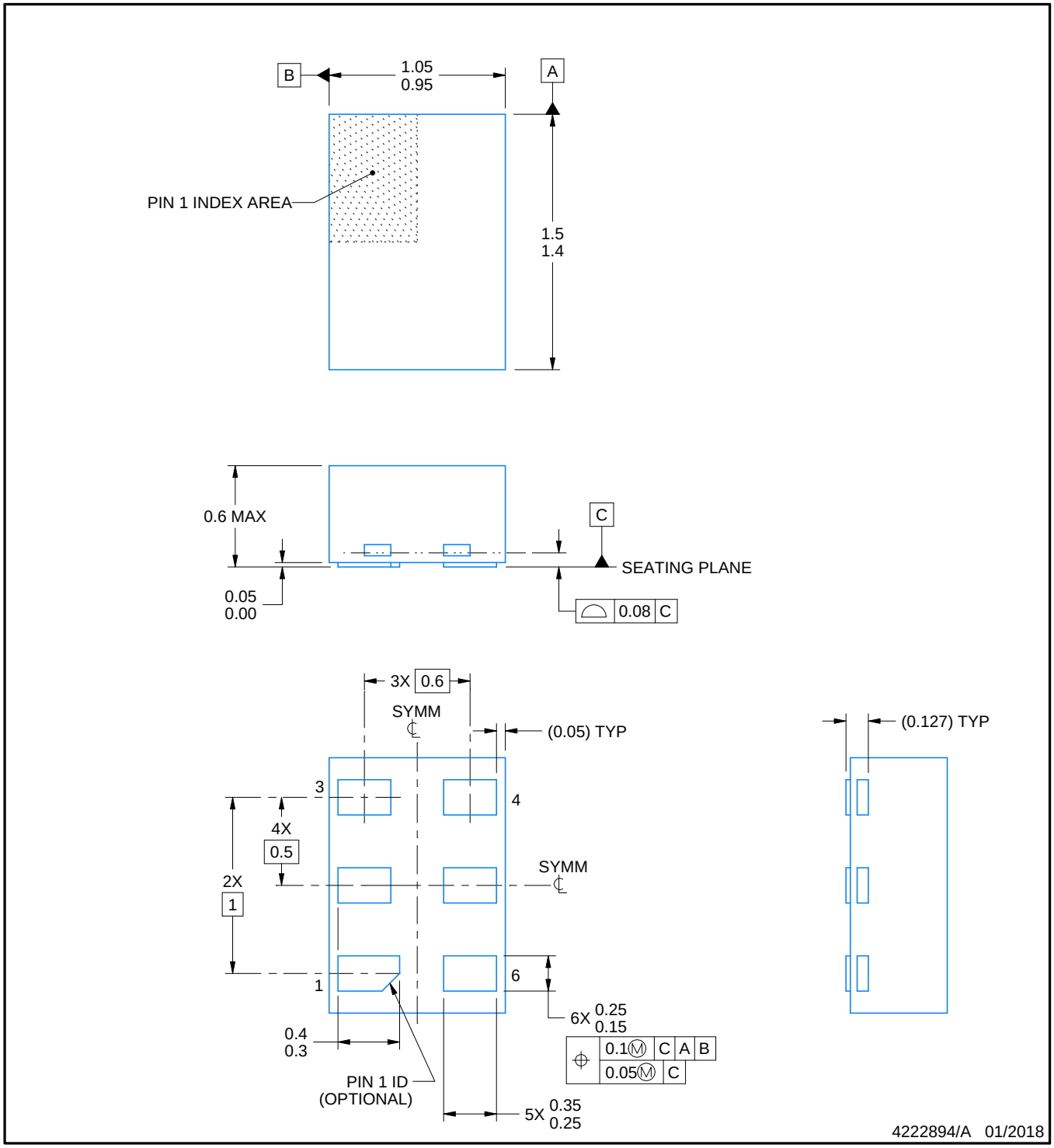
DRY0006A



PACKAGE OUTLINE

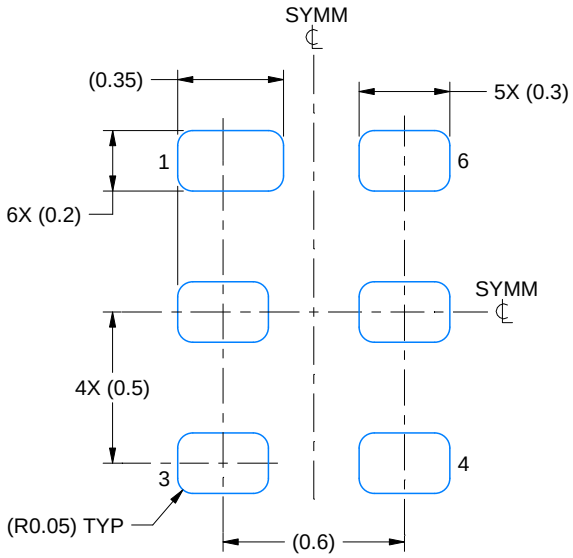
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

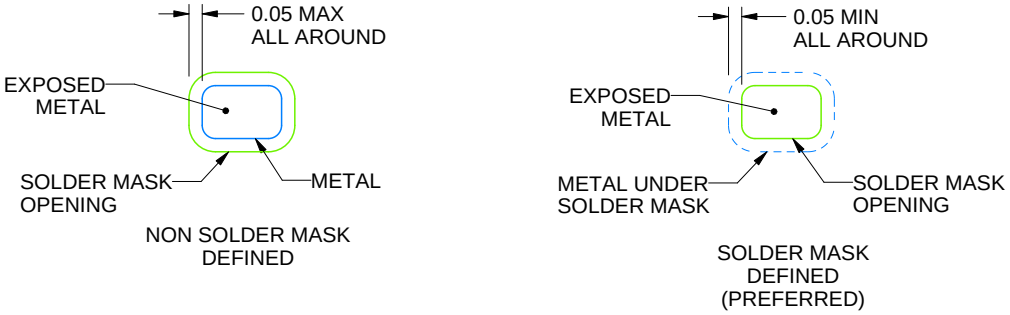


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

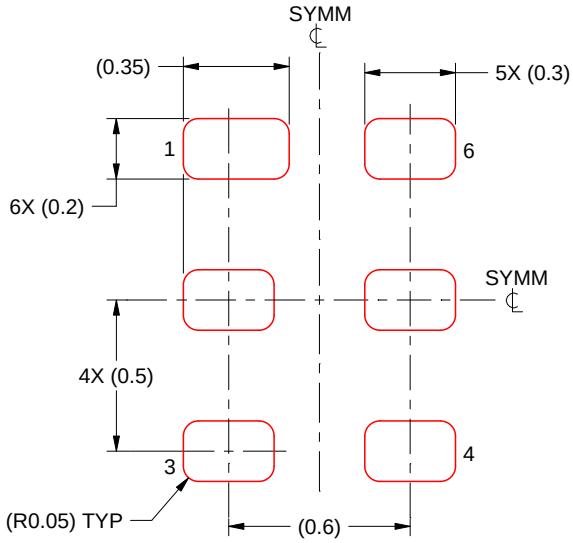
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

最后更新日期：2025 年 10 月