TPS65300-Q1 3MHz 降压稳压器和三重线性稳压器

1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 标准的下列结果
  - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 H2
  - 器件组件充电模式 (CDM) ESD 分类等级 C4B
- 输入 VIN 电压范围介于 5.6V 至 40V 之间，瞬态电压高达 45V
- 为了实现稳定性，所有的输出支持陶瓷输出电容器
- 带有集成高侧开关的开关模式稳压器
  - 建议的开关模式频率范围为 2MHz 至 3MHz
  - 过流保护和 1.2A 峰值开关电流
- 一个电压基准为 0.8V ± 1.5% 的线性稳压器和两个线性稳压器控制器
- IGN_EN 输入的状态指示器输出
- 点火 (IGN_EN) / 使能输入 (EN) 周期上的软启动
- 用于同步的外部时钟输入
- 针对快速负瞬态的可编程加电复位延迟、复位功能滤波器定时器
- 针对下列电源的电压监视器
  - VREG，3.3V，1.234V
- 针对过多功率耗散的热关断保护
- 工作结温范围：-40°C 至 150°C
- 耐热增强型 24 引脚散热薄型小外形尺寸 (HTSSOP) 封装或 24 引脚超薄四方扁平无引线 (VQFN) 封装

2 应用范围

- 用于 TMS570 微控制器的电源
- 用于 C28XXX 数字信号处理器 (DSP) 的电源
- 面向汽车应用的 通用电源
  - 微控制器和 DSP

3 说明

TPS65300-Q1 电源是一个单开关模式降压电源和三个线性稳压器的组合。这款器件是单片高压开关稳压器，此稳压器具有一个集成型 1.2A 峰值电流开关，45V 功率金属氧化物半导体场效应晶体管 (MOSFET)，和一个低压线性稳压器以及两个电压稳压器控制器。

此器件配有电压监控器，可监视开关模式电源、3.3V 线性稳压器和 1.234V 线性稳压器的输出电压。一个外部定时电容器用于设定加电延迟时间和复位输出 nRST 的释放时间。该复位输出还用于指示开关模式电源、3.3V 线性稳压器电源或 1.234V 线性稳压器电源是否在设定的限值之外。5V 稳压器在指定的限制范围内跟踪 3.3V 线性稳压器。

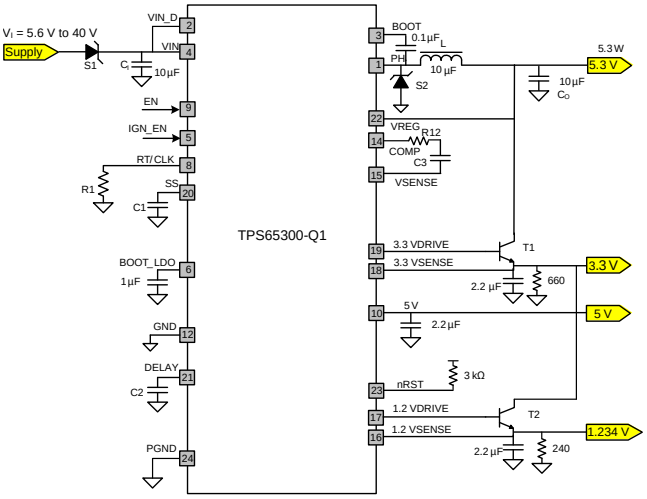
TPS65300-Q1 器件开关频率范围介于 2MHz 至 3MHz 之间，从而实现半高电感器和低值输入以及输出陶瓷电容器的使用。外部环路补偿为用户提供了针对适当运行条件而进行转换器响应优化的灵活性。

此器件内置多种保护 特性，例如软启动（IGN_EN 开启或使能期间）、逐脉冲电流限制、热感应、以及在功耗过大时关断。

器件信息

器件编号	封装	封装尺寸（标称值）
TPS65300-Q1	带散热片薄型小外形尺寸封装 (HTSSOP) (24)	7.80mm × 4.40mm
	VQFN (24)	5.00mm × 4.00mm

典型应用电路原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (March 2014) to Revision F — **Page**

- Changed the word *terminal* back to *pin* throughout the document ... 3
- Changed the MIN, TYP, and MAX values for the 1.2VSENSE output voltage in the *Electrical Characteristics* table ... 6
- Changed the y-axis intervals for the *1.2VSENSE vs Temperature* graph ... 9

Changes from Revision D (August 2013) to Revision E — **Page**

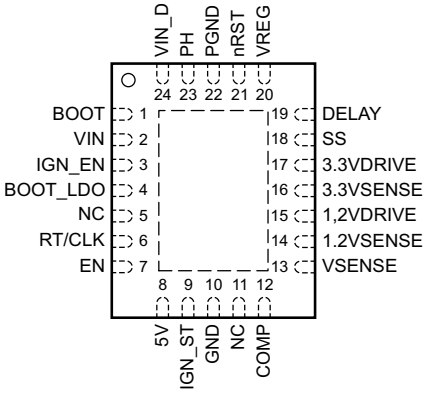
- 已添加 *器件信息* 表和以下全新部分：*电源建议*，*器件和文档支持*，以及*机械封装和可订购信息* ... 1
- Changed the word *pin* to *terminal* throughout the document ... 3
- Moved the *Pin Functions* section into the *Pin Configuration and Functions* section ... 3
- Changed *DC CHARACTERISTICS* condition statement from T_J = –40°C to 150°C to $T_{J\text{-}Max}$ = 150°C ... 5
- Changed min value for V_{IL} of IGN_EN from 2 to 2.2 in the *DC CHARACTERISTICS* table ... 5
- Moved all timing requirements out of the *Electrical Characteristics* table and into the *Timing Requirements* table ... 7
- Combined the general application equations with the practical equations to streamline the *Typical Application* section ... 18
- Changed Y-axis name from *Current (mA)* to *Efficiency* in Figure 17 ... 25
- Moved the *Efficiency vs Output Current on VREG* graph and the scope plots from the *Typical Characteristics* section to the *Application Curves* section ... 25

Changes from Revision C (April 2013) to Revision D — **Page**

- Changed V_{IH} max limit from 4 to 3.6 V in *DC Characteristics* table ... 5
- Added 3.7 V condition and values to Input High I_{IH} parameter in *DC Characteristics* table ... 5
- Changed I_{Charge} unit from V to µA in *DC Characteristics* table ... 6
- Changed internal resistor limit text in *Ignition Enable Input, IGN_EN* pin description ... 11

5 Pin Configuration and Functions

RHF Package
24-Pin VQFN With Exposed Thermal Pad
Top View



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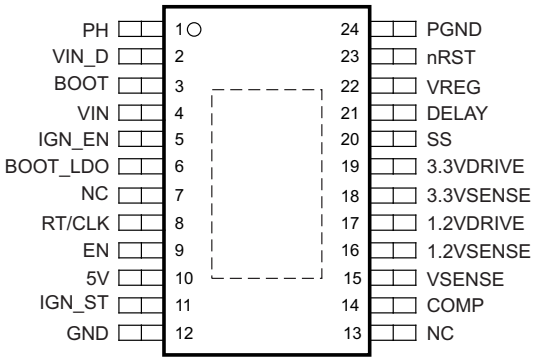
PWP Package
24-Pin HTSSOP With PowerPAD™
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	PWP	RHF		
1.2VDRIVE	17	15	O	Output current source to drive the base of an external bipolar transistor to regulate the 1.234-V supply
1.2VSENSE	16	14	I	Voltage node of 1.234-V supply
3.3VDRIVE	19	17	O	Output current source to drive the base of an external bipolar transistor to regulate the 3.3-V supply
3.3VSENSE	18	16	I	Voltage node of 3.3-V supply
5V	10	8	O	External capacitor to ground for stability of regulated output
BOOT	3	1	O	External bootstrap capacitor connected to PH (pin 1) to drive gate of internal switching FET
BOOT_LDO	6	4	O	External capacitor connected to ground for stability of internal regulator
COMP	14	12	O	Error amplifier output to connect external compensation components
DELAY	21	19	O	External capacitor to ground to program the power-on-reset delay
EN	9	7	I	A high logic-level input signal to enable and low signal to disable device. Internally pulled down to ground
GND	12	10	O	Ground pin, must be electrically connected to exposed pad on PCB for proper thermal performance
IGN_EN	5	3	I	Ignition input (high-voltage tolerant) internally pulls to ground. Must be externally pulled up to enable
IGN_ST	11	9	O	Active-low, open-drain ignition input indicator, output connected to external bias voltage through a resistor. Asserted high after ignition input is high
NC	7	5	—	Connect to ground
	13	11		
nRST	23	21	O	Active-low, open-drain reset output connected to external bias voltage through a resistor. This output is asserted high after the preregulator, 3.3-V, and 1.234-V regulator outputs are regulating and the delay timer has expired. Also, output is asserted low if any one of these three supplies is out of the set regulation, this threshold is internally set.
PGND	24	22	O	Power ground pin, must be electrically connected to exposed pad on PCB for proper thermal performance
PH	1	23	O	Source of internal switching FET
RT/CLK	8	6	I/O	External resistor connected ground to program the internal oscillator. Alternative option is to feed an external clock to provide reference for switching frequency.
SS	20	18	O	External capacitor to ground to program soft-start time
VIN	4	2	I	Unregulated input voltage supply. Pins 2 and 4 must be connected together externally.
VIN_D	2	24	I	Drain input for internal high-side MOSFET. Pins 2 and 4 must be connected together externally.
VREG	22	20	I	Buck converter output. Integrated internal low-side FET to load output during startup or limit voltage overshoot
VSENSE	15	13	I	Inverting node of error amplifier for voltage-mode control of preregulated supply
Thermal pad			—	Electrically connect to ground and solder to ground plane of PCB for thermal efficiency

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Buck regulator	VIN, VIN_D	–0.3	45	V
	BOOT	–0.3	50	V
	PH	–1 –2 for 30 ns	45	V
	VSENSE	–0.3	5.5	V
Control	IGN_EN	–0.3	45	V
	EN, 3.3VSENSE, 1.2VSENSE, RT/CLK, VREG	–0.3	5.5	V
Output	3.3VDRIVE, 1.2VDRIVE	–0.3	8	V
	nRST, IGN_ST	–0.3	5.5	V
	DELAY, COMP	–0.3	7	V
	BOOT_LDO, 5V	–0.3	9	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}Moved the storage temperature and ESD ratings out of the *Absolute Maximum Ratings* table and into the new *Handling Ratings* table		–55	165	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 12, 13, and 24)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VIN, VIN_D	5.6		40	V
BOOT	5.6		48	V
PH	–1		40	V
IGN_EN	0		40	V
EN, VSENSE, 3.3VSENSE, 1.2VSENSE, RT/CLK, nRST, IGN_ST	0		5.25	V
VREG, 3.3VDRIVE, 1.2VDRIVE	0		7.5	V
SS, DELAY, COMP	0		6.5	V
BOOT_LDO	0		8.1	V
Operating ambient temperature range, T_A	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS65300-Q1		UNIT
		PWP (HTSSOP)	RHF (VQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.6	30.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.6	30.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.5	8.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.3	8.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 DC Characteristics

VIN = 6 V to 27 V, IGN_EN = VIN, $T_{J\text{-}Max}$ = 150°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN, VIN_D (Input Power Supply)						
VIN, VIN_D	Supply voltage on VIN, line	Normal mode, after initial start-up	5.6	14	40	V
$I_{q\text{-Normal}}$	Current normal mode	Open-loop test		4.57		mA
$I_{SD\ VIN}$	Shut down	IGN = 0 V, VIN = 12 V, T_A = -40°C to 125°C		2.2	15	µA
$I_{SD\ VIND}$	Shut down	IGN = 0 V, VIN = 12 V, T_A = -40°C to 125°C		2.2	15	µA
IGN_EN (Ignition Input)						
V_{IGN_EN}	Input voltage range	Input into IGN_EN pin		14	40	V
V_{IH}	Input high	Enable device to be ON (rising signal)		3.16	3.6	V
V_{IL}	Input low	Enable device to be OFF (falling signal)	2.2	3.03		V
I_{IH}	Input high	Enable device to be ON, V_{IGN_EN} = 18 V		23.7	50	µA
I_{IH}	Input high	Enable device to be ON, V_{IGN_EN} = 3.7 V		4	7	µA
EN (Logic Level Enable)						
V_{IH}	Input high	Enable device to be ON (rising signal)		1.7	2.3	V
V_{IL}	Input low	Enable device to be OFF (falling signal)	0.7	1.53		V
Switch-Mode Output 5.3 V						
VREG	Regulator output internal resistor network	Fixed output based on internal resistor network	5.178	5.3	5.542	V
C_O	Output capacitor for 5.3 V	ESR = 0.001 Ω to 100 mΩ; large output capacitance may be required for load transients	10			µF
$r_{ds(on)}$	Internal switch resistance	Measured across VIN_D and PH pins, I_{VREG} = 1 A		0.3		Ω
$I_{O\text{-}CL}$	Switch current-limit	VIN = 12 V	1.2	2	3	A
VSENSE (Internal Reference Voltage)						
VREG ref	Internal reference voltage		1.954	2	2.046	V
SS (Soft-Start Timer for Switch-Mode Converter)						
I_{SS}	Soft-start source current	Css = 0.001 µF to 0.01 µF	40	50	60	µA
IGN_ST (Ignition Input Status)						
V_{OL}	Output low	Output asserted low when IGN_EN < 2.2 V, I_{OL} = 1 mA		0.056	0.4	V
I_{IH}	Leakage test	IGN_ST = 5 V		0.05	2	µA
5V (5-V Linear Regulator)						
5Vo	Output voltage	I_O = 1 mA, VREG = 5.3 V	4.9	5	5.1	V
$\Delta V_{O\text{-}Line}$	Line regulation	5.15 V < VREG < 5.45 V, I_O = 1 mA, VIN = 12 V		10	20	mV

DC Characteristics (continued)

VIN = 6 V to 27 V, IGN_EN = VIN, T_{J-Max} = 150°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_{O-Load}	Load regulation	1 mA < I_O < 200 mA, VREG = 5.3 V, VIN = 12 V		10	30	mV
V_{DO}	Dropout voltage	I_O = 150 mA, measure VREG when V_O(nom) – 0.1 V, then V_{DO} = VREG – ($5V_O$ – 0.1) V, VREG > 5 V		0.15	0.26	V
I_{5V-CL}	Current-limit	$5V_O$ = 0.8 × $5V_O$ (nominal)	350	1080		mA
C_O	Output capacitor	ESR = 0.001 Ω to 2 Ω. Larger output capacitance may be required for load transients.	1	2.2	10	µF
PSRR	Power-supply rejection ratio	f = 100 Hz, VREG = 5.3 V, I_O = 100 mA, VIN = 12 V	45	60	75	dB
3.3-V Linear Regulator Controller (3.3VSENSE)						
$3.3V_O$	Output voltage	Io = 5 mA, Vnpn_power input = 5.3 V	3.234	3.3	3.366	V
$\Delta 3.3V_{O-Line}$	Line regulation	3.8 V < Vnpn_power input < 7 V (with nRST not triggered)		1	10	mV
$\Delta 3.3V_{O-Load}$	Load regulation	5 mA < I_O < 550 mA		7.5	30	mV
C_O	Output capacitor for 3.3 V	ESR = 0.001 Ω to 2 Ω. Large output capacitance may be required for load transients.	1	4.7	10	µF
PSRR	Power-supply rejection ratio	f = 100 Hz, VREG = 5.3 V, I_O = 200 mA, VIN = 12 V	45	60	75	dB
3.3VDRIVE (Ex. Switch Control Output)						
I_{OH}	Base drive current. NPN turn ON	3.3VDRIVE – 3.3VSENSE = 1 V	10	28	50	mA
I_{OL}	NPN turn off	3.3VDRIVE – 3.3VSENSE at 0.2V	0.1	0.412		mA
1.2-V Linear Regulator Controller (1.2VSENSE)						
$1.2V_O$	Output voltage	Io = 5 mA, Vnpn_power input = 5.3 V	1.209	1.234	1.259	V
$\Delta 1.2V_{O-Line}$	Line regulation	3.25 V < Vnpn_power input < 7 V (with nRST not triggered)		1	10	mV
$\Delta 1.2V_{O-Load}$	Load regulation	5 mA < I_O < 350 mA		5	15	mV
C_O	Output capacitor for 1.2 V	ESR = 0.001 Ω to 100 mΩ. Large output capacitance may be required for load transients.	8	10	12	µF
PSRR	Power-supply rejection ratio	f = 100 Hz, VREG = 6 V, I_O = 200 mA, VIN = 12 V	45	60	75	dB
1.2VDRIVE (Ex. Switch Control Output)						
I_{OH}	Base drive current. NPN turn ON	1.2VDRIVE – 1.2VSENSE = 1 V	10	27	50	mA
I_{OL}	NPN turn off	1.2VDRIVE – 1.2VSENSE at 0.2 V	0.1	0.47		mA
DELAY (Power-On-Reset Delay)						
$V_{Threshold}$	Threshold voltage	Threshold to release nRST high	1.3	2.05	2.6	V
I_{Charge}	Capacitor charging current		1.4	2	2.6	µA
nRST (Reset Indicator)						
V_{OL}	Output low	Reset asserted due to falling VREG or $3.3V_O$ or $1.2V_O$ output voltages, I_{OL} = 1 mA	0	0.16	0.4	V
V_{TH_VREG}	Trigger nRST for VREG output	VREG ramp down	0.87	0.9	0.93	VREG
	Trigger nRST for $3.3V_O$		0.9	0.93	0.96	$3.3 V_O$
	Trigger nRST for $1.2V_O$		0.9	0.93	0.96	$1.2 V_O$
I_{IH}	Leakage test	Reset = 5 V		0.07	2	µA
RT/CLK (Oscillator Setting of External Clock Input)						
V_{IH}	Input high				2.3	V
V_{IL}	Input low		0.6			V

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Switch-Mode Output 5.3 V					
t_{ON-min}	Minimum ON time		40		ns
D_{max}	Maximum duty cycle		97%		

6.7 Switching Characteristics

VIN = 6 V to 27 V, IGN_EN = VIN, T_{J-Max} = 150°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
5V (5-V Linear Regulator)						
$V_{soft-start}$	Soft start on enable cycle	$5V_O$ = 0 V (initially) with fsw = 2.5 MHz		13		ms
3.3-V Linear Regulator Controller (3.3VSENSE)						
t_{ss}	Soft-start time	$3.3V_O$ = 0 V (initially) with fsw = 2.5 MHz		12.3		ms
1.2-V Linear Regulator Controller (1.2VSENSE)						
t_{ss}	Soft-start time	$1.2V_O$ = 0 V (initially) with fsw= 2.5 MHz		8.5		ms
nRST (Reset Indicator)						
$t_{nRSTdly}$	Filter time	Delay before nRST is asserted low		11		µs
RT/CLK (Oscillator Setting of External Clock Input)						
fsw	Switching freq using RT mode		2		3	MHz
	Switching freq using CLK mode		2		3	MHz
	Minimum clock input pulse duration			40		ns
	Internal oscillator frequency	Switching frequency tolerance for clock	–14%		14%	
	External clock input	Switching frequency tolerance for clock	–20%		10%	

6.8 Typical Characteristics

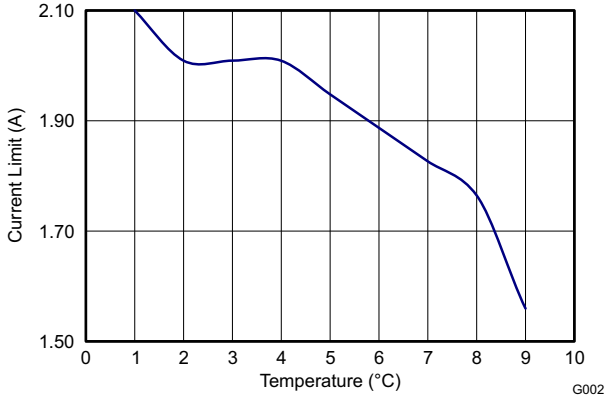


Figure 1. Buck Current-Limit vs Temperature

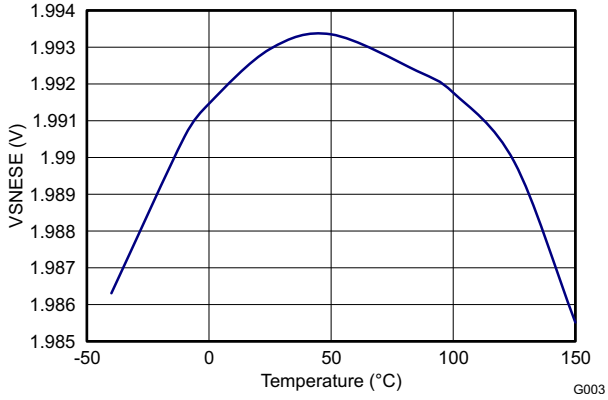


Figure 2. VSENSE Reference Voltage vs Temperature

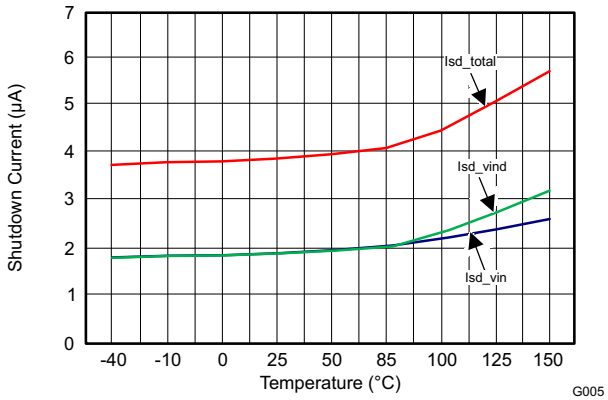


Figure 3. Current Consumption I_{IN} vs Temperature

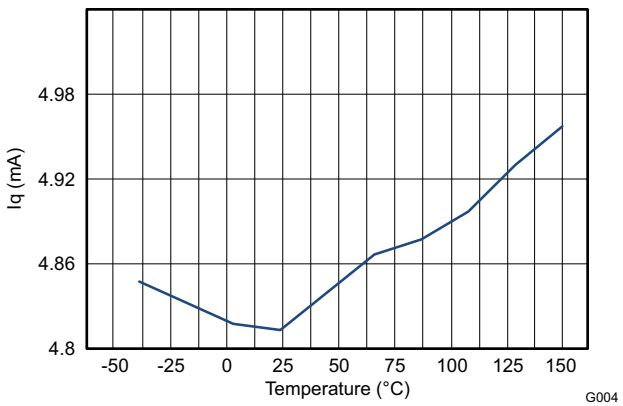


Figure 4. Quiescent Current vs Temperature

6.9 5-V Linear Regulator ($5V_O$)

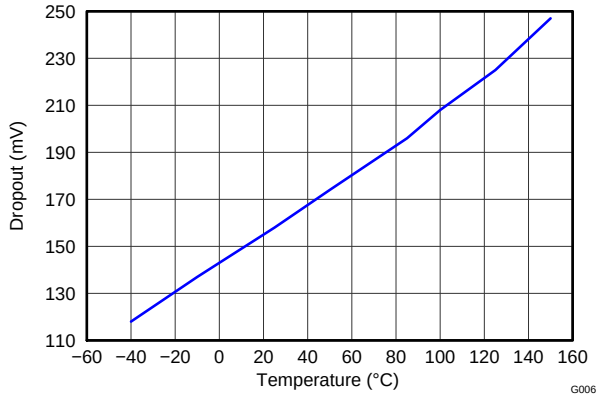


Figure 5. Dropout Voltage vs Temperature

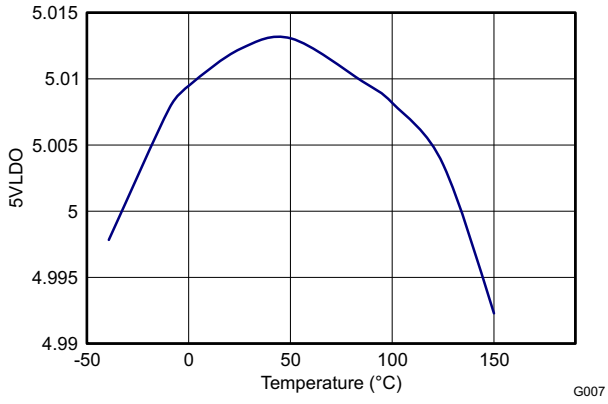


Figure 6. Output Voltage $5V_O$ vs Temperature

6.10 3.3-V Linear Regulator Controller ($3.3V_O$)

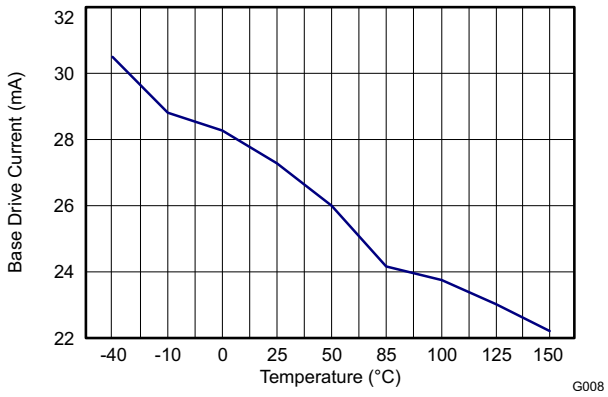


Figure 7. Output Base Drive vs Temperature

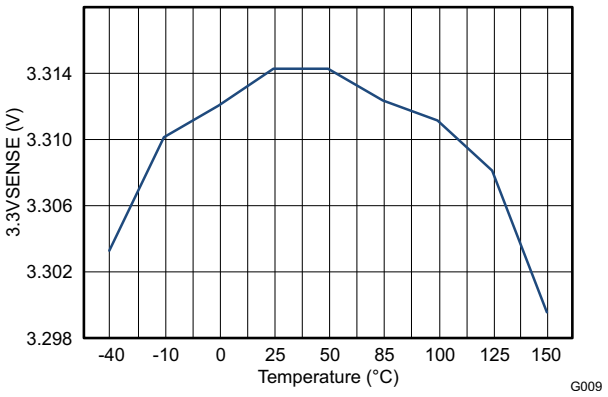


Figure 8. 3.3VSENSE vs Temperature

6.11 1.234-V Linear Regulator Controller ($1.2V_O$)

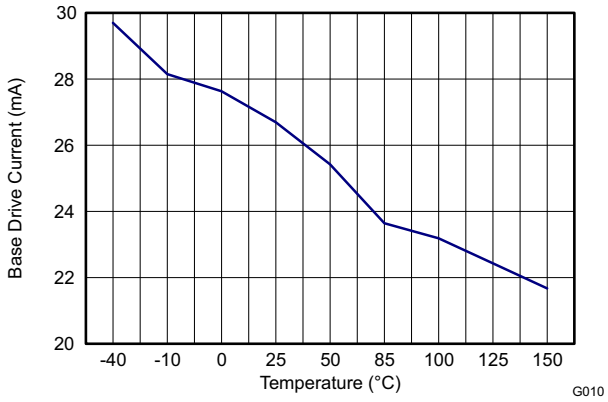


Figure 9. Output Base Drive vs Temperature

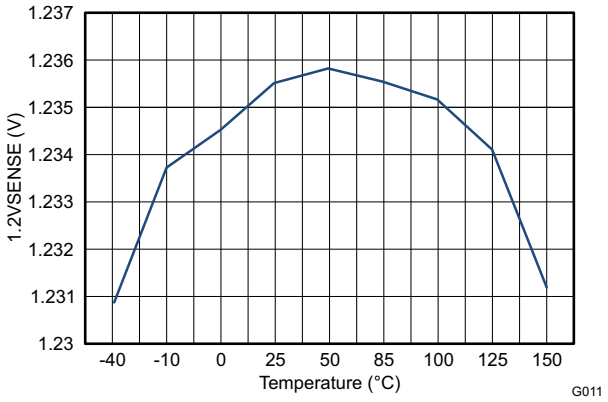


Figure 10. 1.2VSENSE vs Temperature

7 Detailed Description

7.1 Overview

The device integrates an asynchronous switch-mode power-supply converter with a internal FET that converts the input battery voltage to a 5.3-V pre-regulator output. This 5.3-V output supplies the other regulators. The frequency range is from 2 MHz to 3 MHz, allowing the use of low-profile inductors and low value input and output capacitors. External loop compensation provides flexibility which optimizes the converter response for the appropriate operating condition.

A fixed 5-V linear regulator with an internal FET is integrated as an external peripheral supply. A fixed 3.3-V linear regulator controller with external bi-polar transistor is used for an IO supply, for example. A fixed 1.234-V linear regulator controller with external bi-polar transistor is used for a CPU Core supply, for example. The device has a voltage supervisor which monitors the output of the switch-mode power supply, the 3.3-V linear regulator, and the 1.234-V linear regulator.

An external timing capacitor sets the power-on delay and the release of the reset output nRST. This reset output is also used to indicate if the switch-mode supply, the 3.3-V linear regulator supply, or the 1.234-V linear regulator supply is outside the set limits. The 5-V regulator tracks the 3.3-V linear regulator within the specified limits.

7.2 Functional Block Diagram

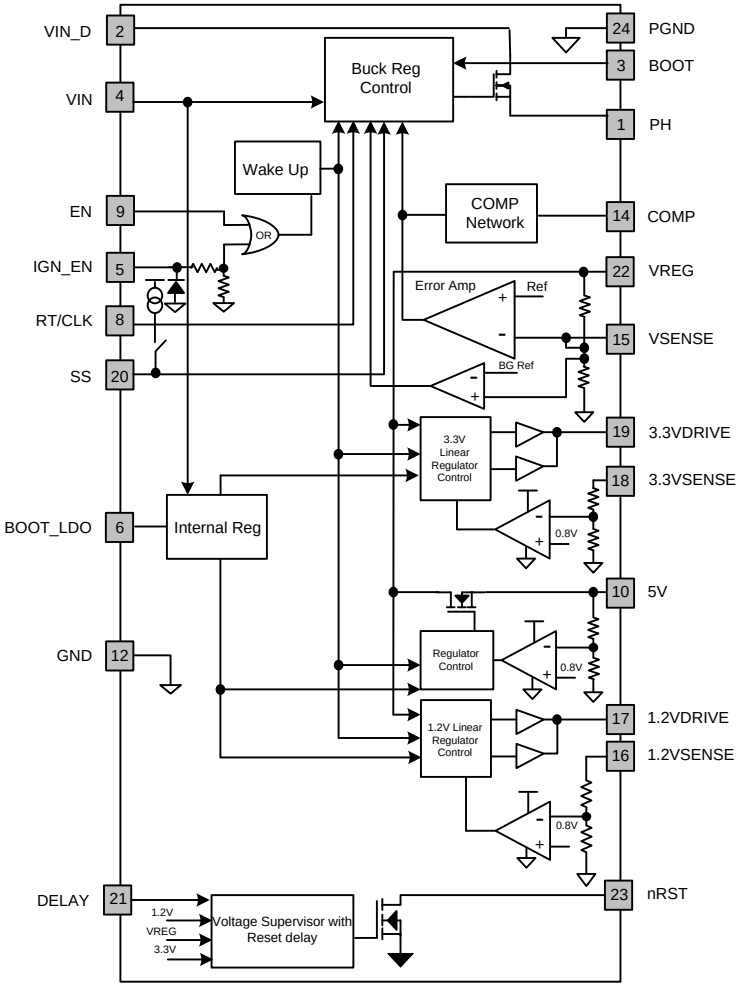


Figure 11. Internal Functional Blocks

7.3 Feature Description

7.3.1 Detailed Pin Descriptions

Buck Supply, VIN_D The buck supply is an input power source for the internal high-side MOSFET of the switch-mode power supply.

Phase Node for Buck Regulator, PH This pin provides the floating voltage reference for the internal drive circuitry.

Bootstrap, BOOT The ceramic capacitor on this pin acts a as a voltage supply for the internal high-side MOSFET gate-drive circuitry. The capacitor connects between the BOOT and PH pins. Operating with a duty cycle of 100% automatically reduces the duty cycle to approximately 95% on every fifth cycle to allow this capacitor to recharge.

Voltage-Sense Node, VSENSE An internal resistor between VREG and this pin and another internal resistor between this pin and ground form the voltage-sense network. This pin is the inverting input for the error amplifier of the control loop. This input is compared to an internal reference of 2 V for the control circuitry.

Error Amplifier Output, COMP The error amplifier output forms a compensation network for the voltage mode control topology. The amplifier changes state with increase in voltage output on this pin.

Internal Regulated Boot Supply, BOOT_LDO The internally regulated supply acts as a refresh power source for the bootstrap capacitor every switching cycle. An external capacitor to ground is needed to stabilize the voltage source.

Clock Pulse, RT/CLK A resistor to ground on this pin sets the buck converter switching frequency. Alternatively, an external clock input on this pin overrides the internal free-running clock (default value) by detecting positive edges of consecutive pulses and synchronizing to the external input signal. If the external clock input is removed, the system synchronizes to the internal clock signal of 2.2 MHz.

Output Voltage, VREG This pin represents the buck (step-down) output voltage VREG of the converter. The output voltage of the buck-mode regulator is fixed at 5.3 V. This output requires a ceramic capacitor (4.7 µF to 10 µF range).

Ignition Enable Input, IGN_EN The IGN_EN pin acts as an enable/disable input to activate the step-down power-supply output. The input is high-voltage tolerant up to 45 V. An internal resistor limits current into this pin for such high input voltage.

Logic Level Enable Input, EN The EN pin is a logic-level disable input to all outputs when IGN_EN is low and all outputs are active.

Regulated Output, 5V This pin is the regulated output and requires a low-ESR ceramic capacitor to ground for loop stabilization. This capacitor must be placed close to the pin of the IC. The output requires larger capacitance to compensate for wide load transient steps.

Power-On Delay, DELAY A capacitor on this pin sets the desired delay time. The output of this pin provides a source current to charge the external capacitor once the VREG, 3.3 V and 1.234 V supplies have all exceeded the internally set threshold (0.9 × their respective regulated supply values).

3.3-V Drive Output, 3.3VDRIVE This pin provides an output to drive an external bipolar transistor (BJT) for the 3.3 V supply. The output is protected by current limiting of both the source and sink capabilities.

3.3-V Voltage Sense, 3.3VSENSE This pin is the voltage node of 3.3 V supply. Voltage of approximately 1.65 V on this pin initiates a current foldback during shorts on the regulated output.

1.2-V Drive Output, 1.2VDRIVE This pin provides an output to drive an external bipolar transistor (BJT) for the 1.234 V supply. The output is protected by current limiting of both the source and sink capabilities.

1.2-V Voltage Sense, 1.2VSENSE This pin is the voltage node of 1.234 V supply. Voltage of approximately 0.6 V on this pin initiates a current foldback during shorts on the regulated output.

Soft Start, SS A ceramic capacitor is connected from this pin to ground to set a soft-start timer for the buck regulator supply. There is an internal pullup current source of 50 µA typical, which is activated on IGN_EN to charge the external capacitor on the SS pin.

Feature Description (continued)

Input Voltage, VIN The VIN pin is the input power source for the device. This pin must be externally protected against voltage levels greater than 45 V and against a reversed battery. This input line requires a filter capacitor to minimize noise. Additionally, for EMI considerations, an input filter inductor may also be required.

Reset Indicator, nRST The nRST pin is an open-drain output. The power-on reset output is asserted low until the output voltages on the VREG, 3.3 V, and 1.234 V supplies exceed their set thresholds and the power-on delay timer has expired. Additionally, whenever the IGN_EN and EN_LIN_REG pins are low or open, nRST is immediately asserted low regardless of the output voltage. If a thermal shutdown occurs due to excessive thermal, conditions this pin is asserted low.

Ignition Input Status, IGN_ST The IGN_ST pin is an open-drain output. This output indicates whether input signal IGN_EN is present. Additionally, whenever the IGN pin is low or open, IGN_ST is immediately asserted low.

Power Ground, PGND Power ground pin, which is internally connected to the exposed thermal pad.

Ground, GND Signal ground pin, which is internally connected to the exposed thermal pad.

7.3.2 Buck Converter

7.3.2.1 PWM Operation

The switch-mode power supply (SMPS) operates in a fixed-frequency adaptive on-time control pulse-width modulation (PWM). The switching frequency is set by an external resistor or synchronized with an external clock input. The internal N-channel MOSFET is turned on (SET) at the beginning of each cycle. This MOSFET is turned off (RESET) when the PWM comparator resets the latch. When the high external FET is turned OFF, the external Schottky diode recirculates the energy stored in the inductor for the remainder of the switching period.

The external bootstrap capacitor acts as a voltage supply for the internal high side MOSFET. This capacitor is recharged on every recirculation cycle (when the internal high-side MOSFET is turned OFF). In the case of commanding 100% duty cycle for the internal high side MOSFET, the device automatically reverts to 87% to allow the bootstrap capacitor to recharge.

7.3.2.2 Voltage-Mode Control Loop

The voltage-mode control monitors the set output voltage and processes the signal to control the internal MOSFET. A voltage feedback signal is compared to a constant ramp waveform, resulting in a PWM modulation pulse. An input line-voltage feedforward technique is incorporated to compensate for changes in the input voltage and ensures the output voltage is stable by adjusting the ramp waveform for the correct duty cycle. The internal MOSFET is protected from excess power dissipation with a current-limit and frequency foldback circuitry during an output-to-ground short-circuit event.

A combination of internal and external components forms a compensation network to ensure error-amplifier gain does not cause instability because of input voltage changes or load perturbations.

7.3.2.3 Output Voltage 5.3 V (VREG)

The output voltage VREG is generated by the converter supplied from the battery voltage VIN and the external components (L, C). The output is sensed through an internal resistor divider and compared with an internal reference voltage.

This output requires larger output capacitors (4.7-µF to 10-µF range) to ensure that during load transients the output does not drop below the reset threshold for a period longer than the reset deglitch filter time.

An internal load is enabled for a short period when the following occurs:

- A start-up condition occurs, that is, during power up or when IGN_EN or EN is toggled.
- An overvoltage condition exists on this output.

Feature Description (continued)

7.3.2.4 Switching Frequency (RT/CLK)

The oscillator frequency of the buck regulator is selectable by means of a resistor placed at the RT/CLK pin to ground. The switching frequency (f_{SW}) can be set in the range 2 MHz to 3 MHz in this resistor mode. Alternatively, if there is an external clock input signal, the internal oscillator synchronizes to this signal within 10 µs.

The Equation 1 calculates the value of resistor (RT) for the required switching frequency f_{SW}.

$$RT = \frac{98.4 \times 10^9}{f_{SW}} \quad \text{(Ohms)} \tag{1}$$

7.3.2.5 Boost Capacitor (BOOT)

This capacitor provides the gate-drive voltage for the internal MOSFET switch. X7R and X5R grade dielectrics are recommended because of their stable values over temperature. Selecting a lower value of boost capacitor for low-Vreg, high-frequency, or both types of applications, or selecting a higher value for high-Vreg, low-frequency, or both types of applications (for example, 100 nF for 500 kHz/5 V and 220 nF for 500 kHz/8 V) may be necessary. In general, a 0.1-µF capacitor is used for the boot capacitor.

7.3.2.6 Soft Start (SS)

To limit the start-up inrush current for the switch-mode supply, an internal soft-start circuit is used to ramp up the reference voltage from 0 V to the final value of 0.8 V. The regulator uses the internal reference or the SS-pin voltage as the power-supply reference voltage to regulate the output accordingly. Use Equation 2 to calculate the soft-start timing.

$$\text{Time } (t_{SS}) = \frac{C \times 0.8\ V}{50 \times 10^{-6}}$$

where

- C = Capacitor on the SS pin, typically 0.1 µF or lower (2)

7.3.2.7 Power-On Delay (DELAY)

The power-on delay function delays the release of the nRST line. The method of operation is to detect when all VREG (5.3-V), 3.3-V, and 1.234-V power-supply outputs are above 90% (typical) of the set value. This detection then triggers a current source to charge the external capacitor on the DELAY pin. When this capacitor is charged to approximately 2 V, the nRST line is asserted high. The delay time is calculated using Equation 3.

$$t_{DELAY} = \frac{2\ V \times C}{2\ \mu A}$$

where

- C = capacitor on DELAY pin.

Example: For a 20-ms delay, C = 20 nF. (3)

7.3.2.8 Reset (nRST)

The nRST pin is an open-drain output. The power-on reset signal is a voltage-supervisor output to indicate the output voltages on VREG (5.3 V), 3.3 V, and 1.234 V are within the specified tolerance of the set regulated voltages. Additionally, whenever both the IGN_EN and EN pins are low or open, the nRST pin is immediately asserted low regardless of the output voltage. If a thermal shutdown occurs because of excessive thermal conditions, this pin is asserted low.

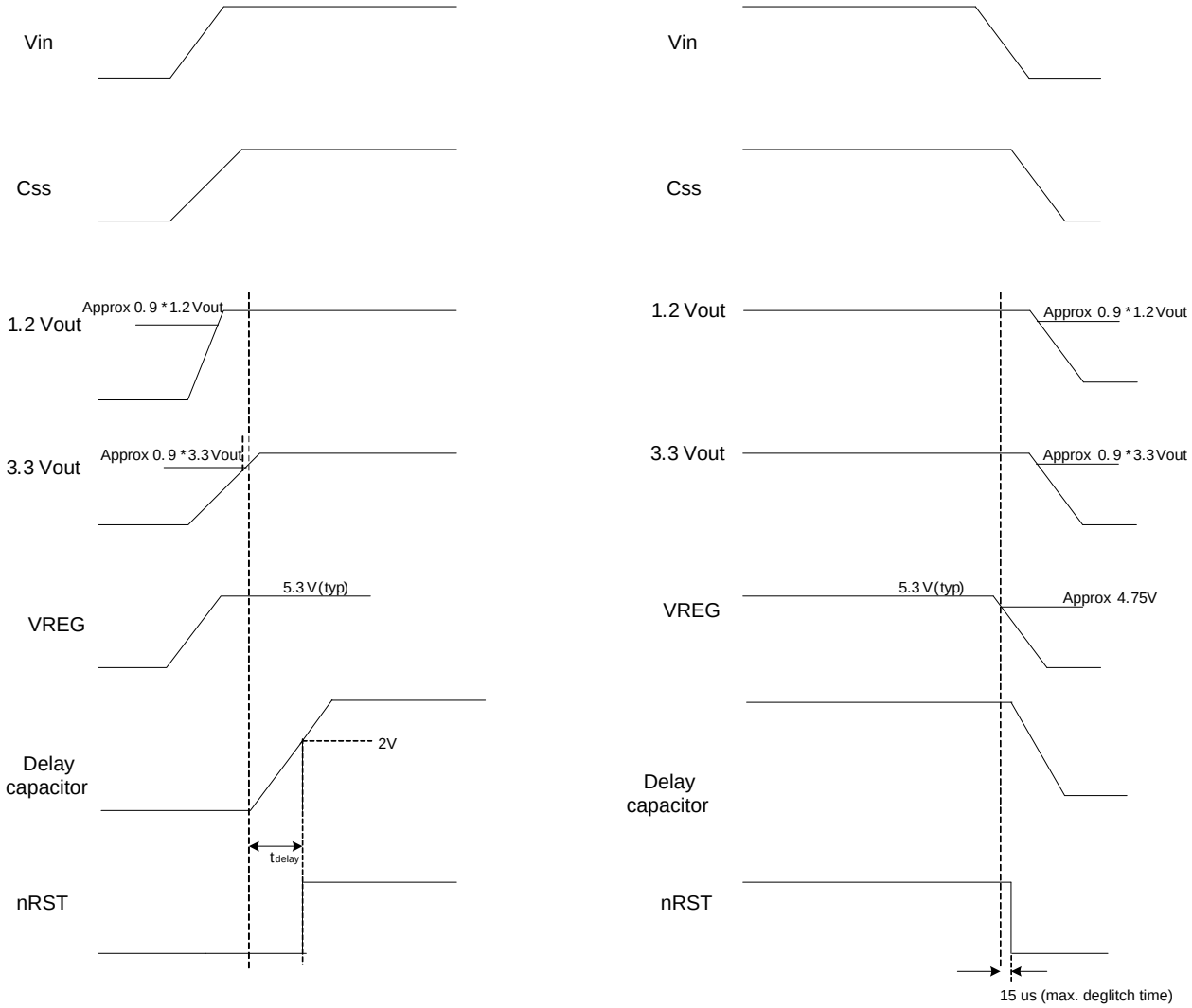
Conversely on power down, when the VREG or 3.3-V or 1.234-V output voltage falls below 90% of the respective set threshold, the nRST pin is pulled low after a de-glitch filter delay of approximately 15 µs (maximum). This feature is implemented to prevent nRST from being invoked because of noise on the output supplies.

Feature Description (continued)

7.3.2.9 Thermal Shutdown

This device has independent two thermal sensing circuits for the VREG (5.3 V), 5-V regulators; if either one of these circuits detects the power FET junction temperature to be greater than the set threshold, that particular output-power switch is turned OFF. The appropriate FET turns back ON once it is allowed to cool sufficiently. The thermal sensing and shutdown circuitry is only activated when nRST is high.

7.3.2.10 Reset Function



On power up, ALL three regulated supplies, VREG, 3.3 V, and 1.234 V, must be more than 90% of their respective values before the delay timer capacitor on the DELAY pin can start charging.

On power down, if any one of the three regulated supplies, VREG, 3.3 V, or 1.234 V, drops below 90% of its value, nRST is asserted low after a small deglitch filter time. Once nRST is asserted low, it can only go high again after ALL three supplies are above the 90% value and the DELAY pin voltage is higher than 2 V.

Figure 12. Reset Function

Feature Description (continued)

7.3.3 Linear Regulators

7.3.3.1 Fixed Linear Regulator Output (5.3 V)

This linear regulator is a fixed, regulated output of 5.3 V ±2% over temperature and input supply using a precision voltage-sense resistor network. A low-ESR ceramic capacitor is required for loop stabilization; this capacitor must be placed close to the pin of the IC. This output is protected against shorts to ground by a foldback current limit for safe operating conditions, and a current-limit for limiting inrush current because of depleted charge on the output capacitor. Initial IGN_EN or EN initiates power cycle of the soft-start circuit on this regulator. This typically is in the 1-ms to 2-ms range. This output may require a larger output capacitor to ensure that during load transients the output does not drop below the required regulated specifications.

7.3.3.2 Fixed Linear Regulator Controller (3.3 V)

The linear regulator controller requires an external NPN bipolar pass transistor of sufficient gain stage to support the maximum load current required. The base-drive output current is protected by current limiting both the source and sink drive circuitry. The 3.3VSENSE pin is the remote sense input of the output of the REG3 supply and controls the 3.3VDRIVE output accordingly. This regulator is a fixed 3.3-V with ±2% tolerance using a precision voltage-sense resistor network. A low-ESR ceramic output capacitor is used for loop compensation of the regulator. A voltage on this pin of less than approximately 50% of the regulated value initiates a current limit on the 3.3VDRIVE output.

This output may require larger output capacitors to support load transients, so the output does not drop below 90% of 3.3 V.

7.3.3.3 Fixed Linear Regulator Controller (1.2 V)

The linear regulator controller requires an external NPN bipolar pass transistor of sufficient gain stage to support the maximum load current required. The 1.2VSENSE pin is the remote sense input of the output of 1.234-V supply and controls the 1.2VDRIVE output accordingly. This regulator output is 1.234 V with ±2% tolerance using a precision voltage-sense resistor network. A low-ESR ceramic output capacitor is used for loop compensation of the regulator. A voltage on this pin of less than approximately 50% of the regulated value initiates a current limit on the 1.2VDRIVE output.

This output may require larger output capacitors to support load transients, so the output does not drop below 90% of 1.234 V.

7.4 Device Functional Modes

7.4.1 Operational Mode

The purpose of the EN input is to keep the regulated supplies ON for a period for the microprocessor to log information into the memory locations when the ignition input is disabled. The microprocessor disables the power supplies by pulling EN low after this activity is complete.

7.4.2 Buck Converter Modes of Operation

The converter operates in different modes based on load current, input voltage, and component selection.

Device Functional Modes (continued)

7.4.2.1 Continuous-Conduction Mode (CCM)

This mode of operation is typically when the inductor current is non-zero and the load current is greater than $I_{L\ CCM}$.

$$I_{IND\_CCM} \geq \frac{(1-D) \times VREG}{2 \times f_{SW} \times L} \quad (4)$$

where

- I_{IND_CCM} = Inductor current in continuous-conduction mode
- D = duty cycle
- VREG = output voltage
- L = Inductor
- f_{SW} = switching frequency

In this mode, the duty cycle must always be greater than the minimum t_{ON} or the converter may go into burst mode.

7.4.2.2 Discontinuous Mode (DCM)

$$I_{IND\_DCM} \geq \frac{(1-D) \times VREG}{2 \times f_{SW} \times L} \quad (5)$$

This mode of operation is typically when the inductor current goes to zero and the load current is less than $I_{IND\ DCM}$.

7.4.2.3 Tracking Mode

When the input voltage is low and the converter approaches approximately 100% duty cycle, Equation 6 calculates the output voltage.

$$VREG = \left(1 - \frac{t_{OFF\_MIN}}{T}\right) \times (VIN - I_{Load} \times R_{DS}) \quad (6)$$

where

- T = Period
- R_{DS} = Internal FET resistance
- I_{LOAD} = output load current

8 Application and Implementation

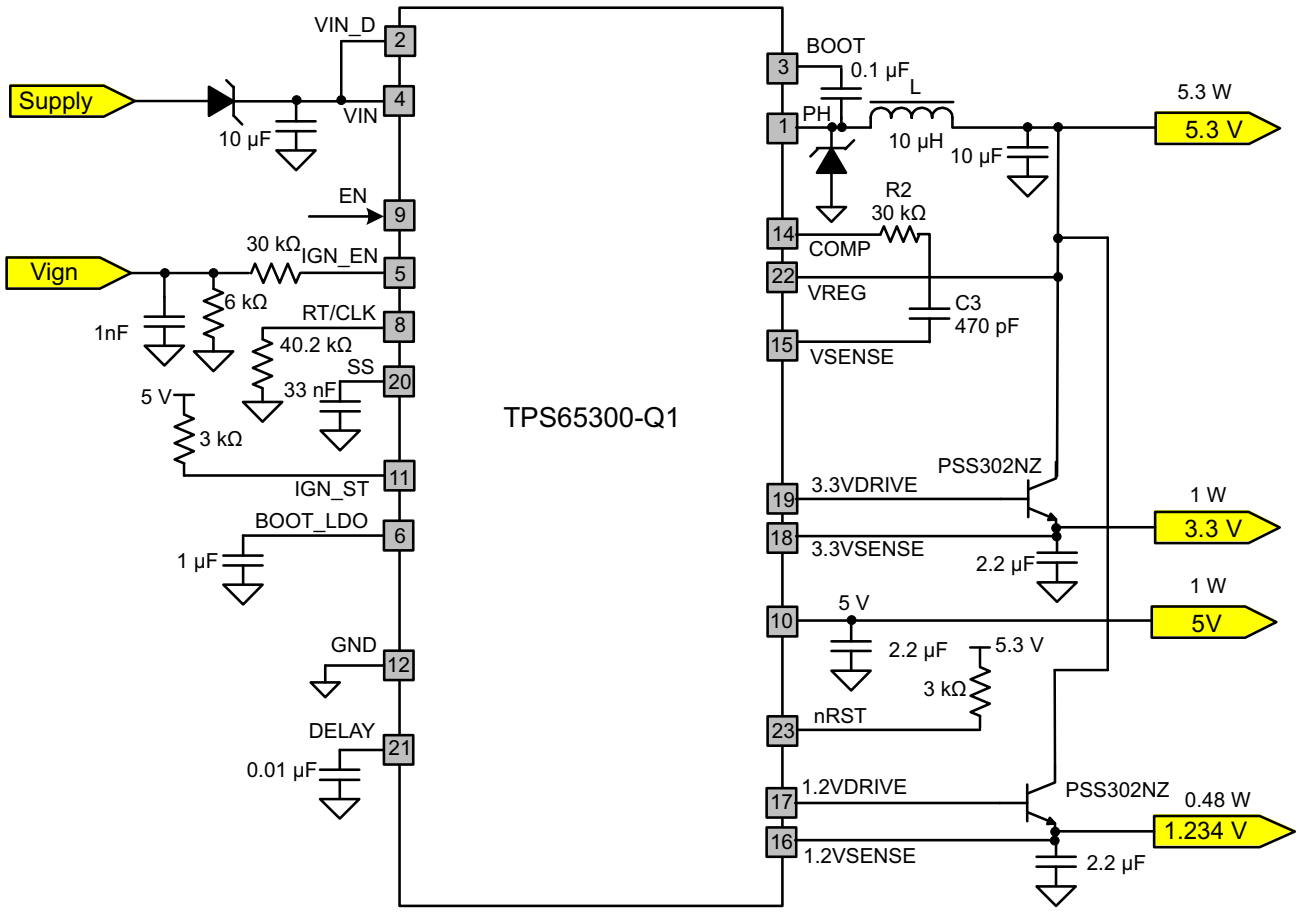
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This section is a starting point and theoretical representation of the values to be used for the application, further optimization of the components derived may be required to improve the performance of the device.

8.2 Typical Application



L: B82462G4103MOOO (EPCOS) or XFL4020 472MEB (Coilcraft)
S1: MBRS310T3 (ON Semiconductors) or SS3H10 (Vishay)
S2: B240A, SS16 (Vishay)
External BJT: PBSS302NZ (NXP)

Figure 13. Application Schematic for a Switching Regulator

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Switching Regulator Requirements

Parameter	Requirement
Input voltage, V_I	6.5 V to 27 V, typical 14 V
Output voltage, 5.3 V	5.3 V_O ±2% at 5.3 W
Maximum output current $I_{5.3V\_max}$	1 A
Minimum output current $I_{5.3V\_min}$	0.01 A
Transient response 0.01A to 0.8 A	5%
Reset threshold	90% of output voltage
5V	5V_O at 1 W
3.3V	3.3V_O at 1 W
1.234V	1.234V_O at 0.5 W
Switching frequency f_{SW}	2.5 MHz
Overvoltage threshold	106% of output voltage
Undervoltage threshold	95% of output voltage

8.2.2 Detailed Design Procedure

The following design procedure provides typical application procedures as well as the details of a switching regulator design using the requirements listed in Table 1.

8.2.2.1 Duty Cycle

Use Equation 7 to calculate the duty cycle.

$$D = \frac{V_O}{V_I} = \frac{5.3}{14} = 0.378 \quad (7)$$

where

- V_O = Output voltage
- V_I = Input voltage

8.2.2.2 Output Inductor Selection (L)

The minimum inductor value is calculated using the coefficient K_{IND} that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor, and so the typical range of this ripple current is in the range of K_{IND} = 0.2 to 0.3, depending on the ESR and the ripple-current rating of the output capacitor.

For this design example, use Equation 8 to calculate the inductor ripple current

$$I_{Ripple} = K_{IND} \times I_O = 0.25 \times 1 = 0.25 \text{ A} \quad (8)$$

where

- I_O = Output current

Benefits of Low Inductor Value

- Low inductor value gives high di/dt, which allows for fewer output capacitors for good load transient response.
- Gives higher saturation current for the core due to fewer turns
- Fewer turns yields low DCR and therefore less dc inductor losses in the windings.
- High di/dt provides faster response to load steps.

Benefits of High Inductor Value

- Low ripple current leads to lower conduction losses in MOSFETs
- Low ripple; means lower RMS ripple current for capacitors

- Low ripple; yields low ac inductor losses in the core (flux) and windings (skin effect)
- Low ripple; gives continuous inductor current flow over a wide load range

For this design example a value of 10 µH was selected because of variations in temperature and manufacture. Use Equation 9 to find the value of L_{Min}.

$$L_{Min} = \frac{(V_{I\text{-}Max} - V_O) \times V_O}{f_{SW} \times I_{RIPPLE} \times V_{I\text{-}Max}} = \frac{(27 - 5.3) \times 5.3}{2.5\,MHz \times 10^6 \times 0.25 \times 27} = 6.8\ \mu H$$

where

- f_{SW} is the regulator switching frequency
- I_{Ripple} = Allowable ripple current in the inductor, typically ±20% of maximum output load I_O

(9)

For this design example, use Equation 10 to calculate the inductor peak current.

$$I_{L\text{-}Peak} = I_O + \frac{I_{Ripple}}{2} = 1 + \frac{0.25}{2} = 1.125\ A \quad (10)$$

8.2.2.3 Output Capacitor Selection (C_O)

The selection of the output capacitor determines several parameters in the operation of the converter, the modulator pole, the voltage droop on the out capacitor, and the output ripple.

During a load step from no load to full load or changes in the input voltage, the output capacitor must hold up the output voltage above a certain level for a specified time and not issue a reset until the main regulator control loop responds to the change. The capacitance value determines the modulator pole and the roll-off frequency due to because of the LC output-filter double pole—the output ripple voltage is a product of the output capacitor ESR and ripple current.

Use Equation 11 to calculate the minimum capacitance required to maintain desired output voltage during a high-to-low load transition and prevent overshoot.

$$C_O = \frac{L\left((I_{O\text{-}max})^2 - (I_{O\text{-}min})^2\right)}{(V_{O\text{-}max})^2 - (V_{O\text{-}min})^2} = \frac{10 \times 10^{-6}\left[(1)^2 - (0.01)^2\right]}{(5.45)^2 - (5.15)^2} = 3.18\ \mu F$$

where

- $I_{O\text{-}max}$ is maximum output current
- $I_{O\text{-}min}$ is minimum output current
- The difference between the output current, maximum to minimum, is the worst-case load step in the system.
- $V_{O\text{-}max}$ is maximum tolerance of regulated output voltage
- $V_{O\text{-}min}$ is the minimum tolerance of regulated output voltage

(11)

Use Equation 12 to calculate the output capacitor root-mean-square (RMS) ripple current I_{O_RMS}. This is to prevent excess heating or failure due to high ripple currents.

This parameter is sometimes specified by the manufacturer. Therfore, because of variations in temperature and manufacture, use a 10-µF capacitor with a voltage rating greater than the maximum 10-V output.

$$I_{O\_RMS} = \frac{L\left((I_{O\text{-}max})^2 - (I_{O\text{-}min})^2\right)}{(V_{O\text{-}max})^2 - (V_{O\text{-}min})^2} = \frac{5.3 \times (27 - 5.3)}{\sqrt{12} \times 27 \times 10 \times 10^{-6} \times 2.5 \times 10^6} = 0.049\ A \quad (12)$$

8.2.2.4 External Schottky Diode (D)

The TPS65300-Q1 device requires an external ultrafast Schottky diode with fast reverse-recovery time connected between the PH and power ground pins. The diode conducts the output current during the off-state of the internal power switch. This diode must have a reverse breakdown higher than the maximum input voltage of the application. A Schottky diode is selected for lower forward voltage. The Schottky diode is selected based on the appropriate power rating, which factors in the DC-conduction losses and the AC losses because of the high switching frequencies. The power dissipation P_D is calculated with Equation 13.

$$P_D = I_O \times V_{FD} \times (1-D) + \frac{(V_I - V_{FD})^2 \times f_{SW} \times C_J}{2} = 1 \times 0.55 \times (1-0.378) + \frac{(14-0.55)^2 \times 2.5\ \text{MHz} \times 30\ \text{pF}}{2} = 0.34\ \text{W} \quad (13)$$

where

- V_{FD} = forward conducting voltage of Schottky diode
- C_J = junction capacitance of the Schottky diode

8.2.2.5 Input Capacitor (C_I)

The TPS65300-Q1 device requires an input ceramic decoupling capacitor type X5R or X7R and bulk capacitance to minimize input ripple voltage. The DC voltage rating of this input capacitance must be greater than the maximum input voltage. The capacitor must have an input ripple-current rating higher than the maximum input ripple current of the converter for the application. The input capacitors for power regulators are selected to have reasonable capacitance-to-volume ratio and to be fairly stable over temperature. The value of the input capacitance is based on the input voltage desired (ΔV_I).

Use Equation 14 to calculate the input capacitance.

$$C_I = \frac{I_{O\_max} \times 0.25}{\Delta V_I \times f_{SW}} = \frac{1 \times 0.25}{0.3 \times 2.5\ \text{MHz}} = 0.33\ \mu\text{F} \quad (14)$$

Use Equation 15 to calculate the input-capacitor root-mean-square (RMS) ripple current I_{I_RMS}.

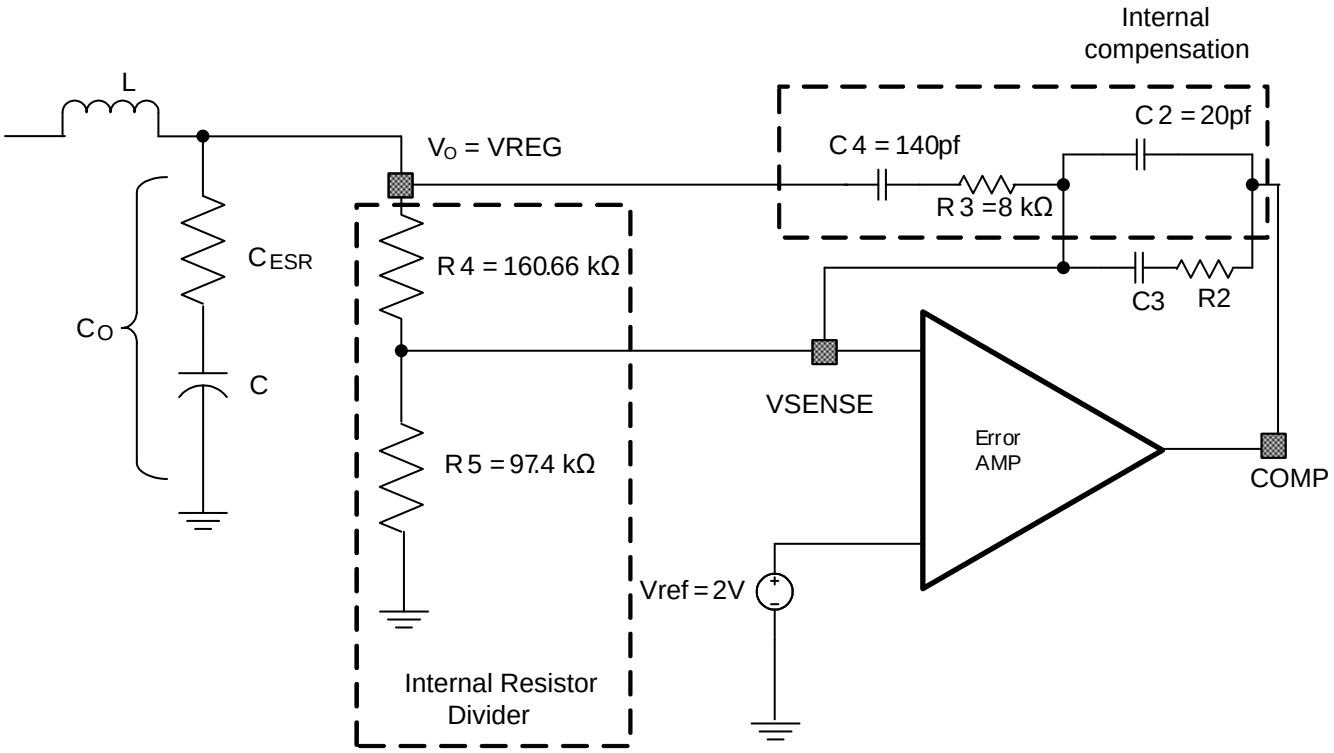
Because of variations in temperature and manufacture, use a 10-µF capacitor with a voltage rating greater than the maximum 45-V transient.

$$I_{I\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{I\_min}} \times \left(\frac{V_{I\_min} - V_O}{V_{I\_min}} \right)} = 1 \times \sqrt{\frac{5.3}{6} \times \left(\frac{6-5.3}{6} \right)} = 0.32\ \text{A} \quad (15)$$

8.2.2.6 Loop Compensation

The double pole is because of the output-filter components inductor and capacitor. The calculations for the following equations use values taken from Figure 14.

8.2.2.7 Loop-Control Frequency Compensation



Type III Compensation

Figure 14. Loop-Control Frequency Compensation

8.2.2.7.1 Type III Compensation

$f_{CO} = f_{SW} \times 0.1$ (the cutoff frequency when the gain is 1 is called the unity-gain frequency).

f_{CO} is typically 1/5 to 1/10 of the switching frequency double-pole frequency response due to the LC output filter. The LC output filter gives a *double pole*, which has a –180° phase shift.

Make the two zeroes close to the double pole (LC), for example, $f_{Z1} \approx f_{Z2} \approx 1/2\pi(LC_{OUT})^{1/2}$.

1. Make the first zero below the filter double pole (approximately 50% to 75% of f_{LC})
2. Make the second zero at the filter double pole (f_{LC})

   Make the two poles above the crossover frequency f_{CO}.
3. Make the first pole at the ESR frequency (f_{ESR})
4. Make the second pole at 0.5 the switching frequency

The following compensation components are integrated in the device with the following typical values. Guidelines for compensation components:

R3 = 8 kΩ, C4 = 140 pF, C2 = 20 pF

Use Equation 16 to calculate the double pole to calculate the output filter components LC.

$$f_{LC} = \frac{1}{2\pi\sqrt{LC_O}} = \frac{1}{2\pi\sqrt{10\ \mu H \times 10 \mu F}} = 15.9\ kHz \quad (16)$$

The ESR of the output capacitor C gives a zero that has a 90° phase shift. The ESR of the output capacitor must be in the range of 1 mΩ to 100 mΩ. Use Equation 17 to calculate the value of f_{ESR}.

$$f_{ESR} = \frac{1}{2\pi \times C_O \times ESR} = \frac{1}{2\pi \times 10\ \mu F \times 0.005} = 3.2\ MHz \quad (17)$$

8.2.2.7.2 PWM Modulator Gain K

$$K = \frac{V_I}{V_{ramp}}$$

where

- $V_{ramp} = V_I / 10$, V_I = Input operating voltage

(18)

8.2.2.7.3 Resistor Values

In this design example, select a value of 97.4 k Ω for R5 and use Equation 19 to calculate the value of R4.

$$R4 = \frac{R5 \times (V_O - Vref)}{Vref} = \frac{97.4\ k\Omega \times (5.3 - 2)}{2} = 160.7\ k\Omega$$

where

- V_{ref} = 2 V

(19)

Use Equation 20 to calculate the value of R2 for this design example.

$$R2 = \frac{f_{CO} \times V_{ramp} \times R4}{f_{LC} \times V_I} = \frac{250\ kHz \times 1.4 \times 160\ k\Omega}{15.9\ kHz \times 14} = 251.6\ k\Omega \quad (20)$$

Calculate C3 based on placing a zero at 50% to 75% of the output-filter double-pole frequency (below set at 50%).

For this design example, use Equation 21 to calculate the value of C3 as 80 pF.

$$C3 = \frac{1}{\pi \times R2 \times f_{LC}} = \frac{1}{\pi \times 251.6\ k\Omega \times 15.9\ kHz} = 80\ pF \quad (21)$$

8.2.2.7.4 Gain of Amplifier

$$A_V = \frac{R2 \times (R4 + R3)}{(R4 \times R3)} \quad (22)$$

8.2.2.7.5 Poles and Zero Frequencies

The following equations were used in this design example:

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2} = \frac{1}{2\pi \times 251.6\ k\Omega \times 20\ pF} = 31.6\ kHz$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C4} = \frac{1}{2\pi \times 8\ k\Omega \times 140\ pF} = 142.1\ kHz$$

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C3} = \frac{1}{2\pi \times 251.6\ k\Omega \times 80\ pF} = 7.91\ kHz$$

$$f_{Z2} = \frac{1}{2\pi \times R4 \times C4} = \frac{1}{2\pi \times 160.7\ k\Omega \times 140\ pF} = 7.07\ kHz \quad (23)$$

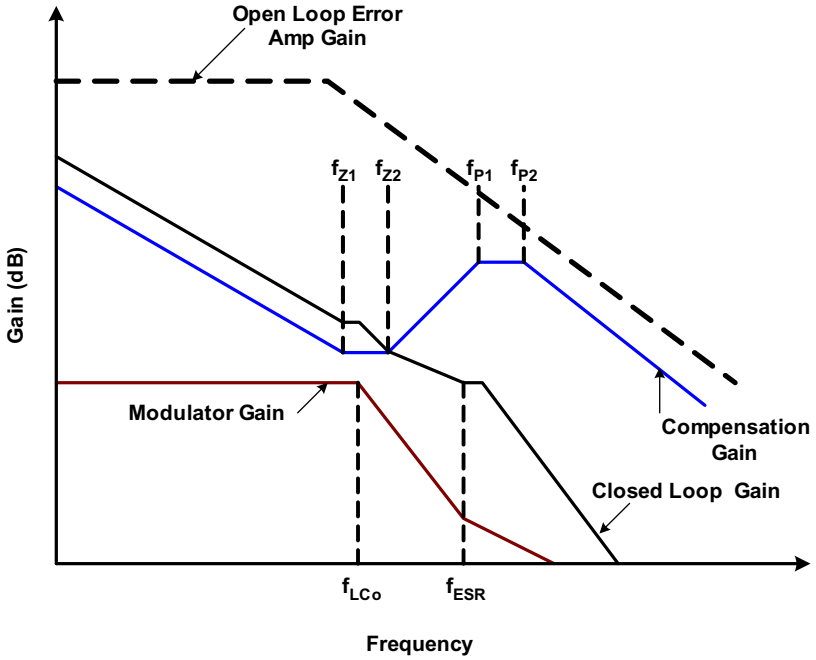


Figure 15. Typical Gain Versus Frequency

8.2.2.8 Power Dissipation

8.2.2.8.1 Switch-Mode Power-Supply Losses

The power dissipation losses are applicable for continuous-conduction mode operation (CCM).

1. Conduction losses

   $P_{5.3V\_CON} = I_O^2 \times R_{ds(on)} \times (V_O/V_I)$

   where

   - I_O = Output current
   - V_O = VREG = Output voltage
   - V_I = Input voltage
   - f_{SW} = Switching frequency (24)

2. Switching losses

   $P_{5.3V\_SW} = ½ \times V_I \times I_O \times (t_r + t_{f)} \times f_{SW}$

   where

   - t_r = FET switching rise time (t_r max = 20 ns)
   - t_f = FET switching fall time (t_f max = 20 ns) (25)

3. Gate drive losses

   $P_{5.3V\_Gate} = V_{drive} \times Qg \times f_{SW}$

   where

   - V_{drive} = FET gate-drive voltage (typically V_{drive} = 6 V and V_{drive} max = 8 V)
   - $Qg = 1 \times 10^{-9}$ (nC) (typical) (26)

4. Supply losses

   $P_{IC} = V_I \times I_q$-normal (27)

Therefore:

$$P_{Total} = P_{CON} + P_{SW} + P_{Gate} + P_{5V\_Lin\ Reg} + P_{IC} \quad (28)$$

$$P_{5V\_Lin\ Reg} = (VREG - 5\ V) \times I_O \quad (29)$$

Therefore, for this design, the following equations were used:

$$P_{5.3V\_CON} = I_O^2 \times r_{ds(on)} \times (V_O / V_I) = 1^2 \times 0.5 \times (5.3 / 14) = 0.189\ W$$

$$P_{5.3V\_SW} = 1/2 \times V_I \times I_O \times (t_r + t_f) \times f_{SW}$$
$$= 1/2 \times 14 \times 1 \times (20 \times 10^{-9} + 20 \times 10^{-9}) \times 2.5 \times 10^6 = 0.7\ W$$

$$P_{5.3V\_Gate} = V_{drive} \times Qg \times f_{SW} = 8 \times 1 \times 10^{-9} \times 2.5 \times 10^6 = 0.02\ W$$

$$P_{5V\_LinReg} = (VREG - 5V) \times I_O = (5.3 - 5.0) \times 0.2 = 0.06\ W$$

$$P_{IC} = V_I \times I_{IC} = 14 \times 5\ mA = 0.07\ W$$

$$P_{Total} = P_{5.3V\_CON} + P_{5.3V\_SW} + P_{5.3V\_Gate} + P_{5V\_LinReg} + P_{IC}$$
$$= 0.189 + 0.7 + 0.02 + 0.06 + 0.07 = 1.039\ W \quad (30)$$

For given operating ambient temperature T_A

$$T_J = T_A + R_{th} \times P_{Total}$$

where

- T_J = Junction temperature in °C
- T_A = Ambient temperature in °C
- P_{Total} = Total power dissipation (watts) (31)

For a given max junction temperature $T_{J\text{-}Max}$ = 150°C

$$T_{A\text{-}Max} = T_{J\text{-}Max} - R_{th} \times P_{Total}$$

where

- $T_{A\text{-}Max}$ = Maximum ambient temperature in °C
- $T_{J\text{-}Max}$ = Maximum junction temperature in °C
- R_{th} = Thermal resistance of package in (°C/W) (32)

Other factors not included in the foregoing information which affect the overall efficiency and power losses are

- Inductor AC and DC losses
- Trace resistance and losses associated with the copper trace routing connection
- Schottky diode

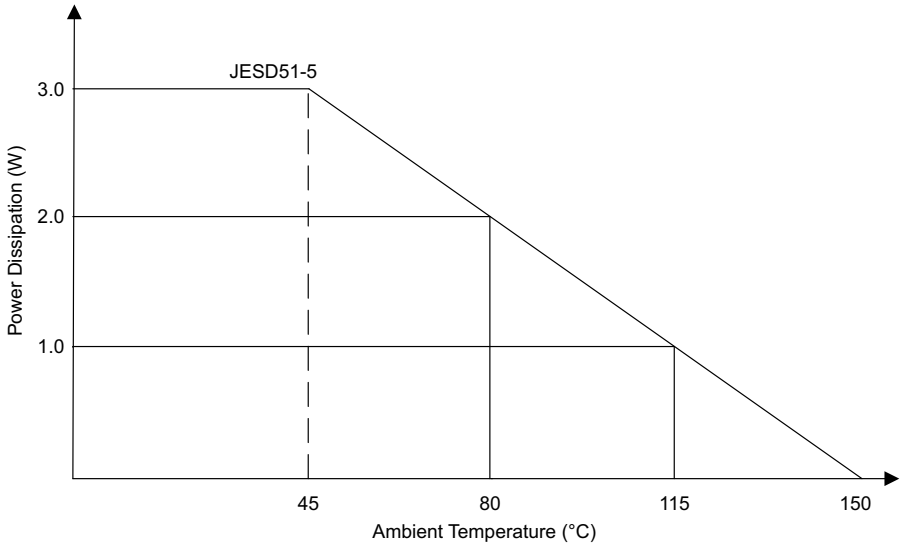


Figure 16. Power Dissipation Derating Profile, 24-Pin PWP Package With Thermal Pad

8.2.3 Application Curves

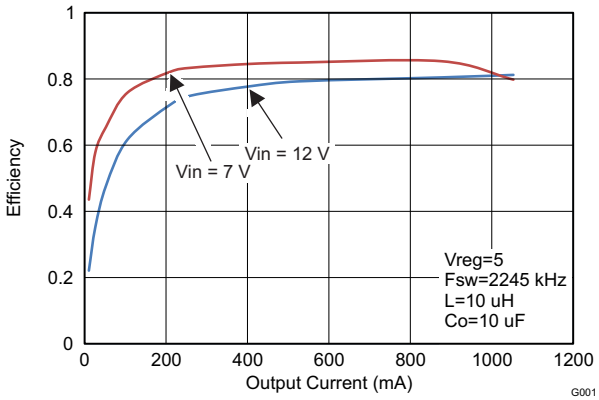


Figure 17. Efficiency vs Output Current on VREG

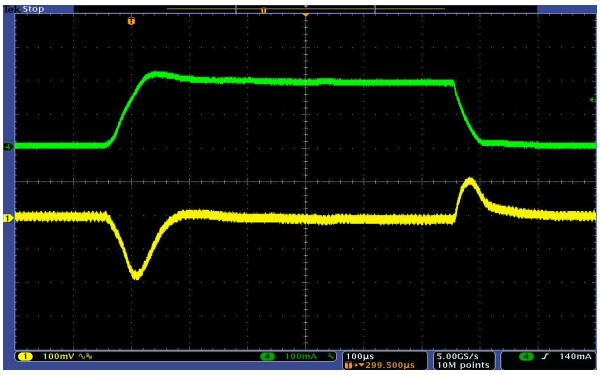


Figure 18. Load Transient Response, 10 mA to 200 mA

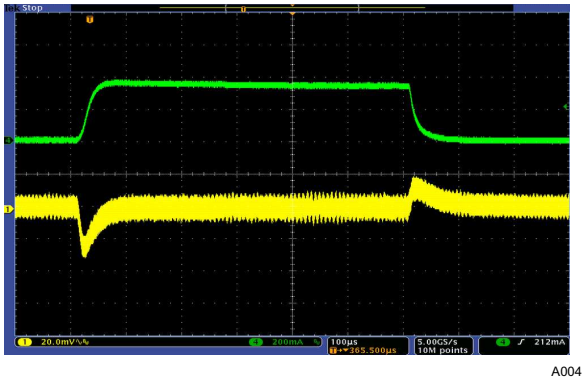


Figure 19. Load Transient Response, 10 mA to 350 mA

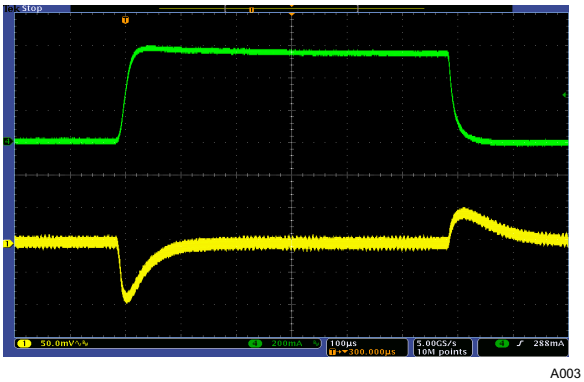


Figure 20. Load Transient Response, 10 mA to 550 mA

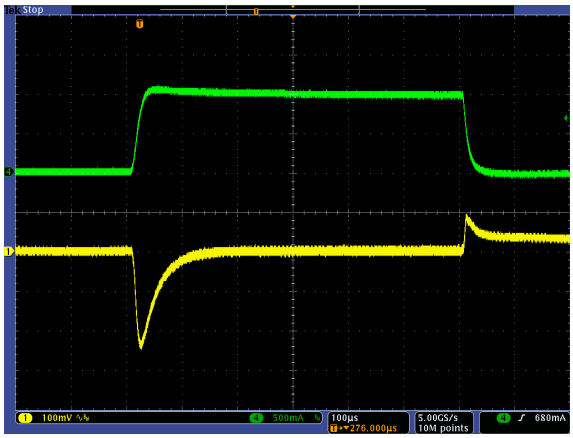


Figure 21. Load Transient Response, 10 mA to 1 A

9 Power Supply Recommendations

The TPS65300-Q1 device is designed to operate using an input supply voltage range from 5.6 V to 40 V.

10 Layout

10.1 Layout Guidelines

The following guidelines are recommended for the printed circuit board (PCB) layout of the TPS65300-Q1 device.

10.1.1 Inductor L

Use a low-EMI inductor with a ferrite-type shielded core. Other types of inductors may be used; however, they must have low-EMI characteristics and be located away from the low-power traces and components in the circuit.

10.1.2 Input Filter Capacitors C_I

Input ceramic filter capacitors should be located in close proximity to the VIN pin. Surface-mount capacitors are recommended to minimize lead length and reduce noise coupling.

10.1.3 Feedback

Route the feedback trace such that there is minimum interaction with any noise sources associated with the switching components. Recommended practice is to ensure placing the inductor away from the feedback trace to prevent a source of EMI noise.

10.1.4 Traces and Ground Plane

All power (high-current) traces should be thick and as short as possible. The inductor and output capacitors should be as close to each other as possible. This reduces EMI radiated by the power traces due to high switching currents.

In a two-sided PCB it is recommended to have ground planes on both sides of the PCB to help reduce noise and ground-loop errors. The ground connection for the input and output capacitors and IC ground should be connected to this ground plane.

In a multi-layer PCB, the ground plane is used to separate the power plane (where high switching currents and components are placed) from the signal plane (where the feedback trace and components are) for improved performance.

Also arrange the components such that the switching-current loops curl in the same direction. Place the high-current components such that during conduction the current path is in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles, helping to reduce radiated EMI.

10.2 Layout Example

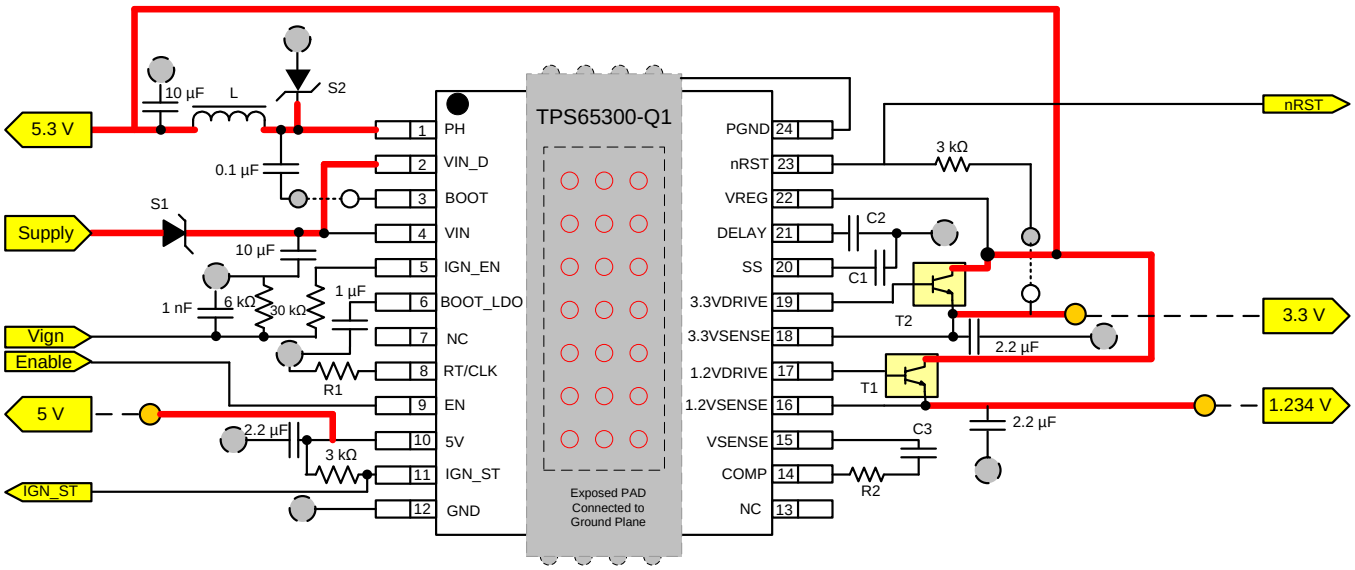


Figure 22. PCB Layout

11 器件和文档支持

11.1 器件支持

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 文档支持

11.2.1 相关文档

相关文档请参见以下部分：

《用户指南》，*TPS65300EVM*，文献编号：SLVU685

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

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All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65300QPWPRQ1	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS65300
TPS65300QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS65300
TPS65300QRHFRQ1	Active	Production	VQFN (RHF) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	65300Q1
TPS65300QRHFRQ1.A	Active	Production	VQFN (RHF) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	65300Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

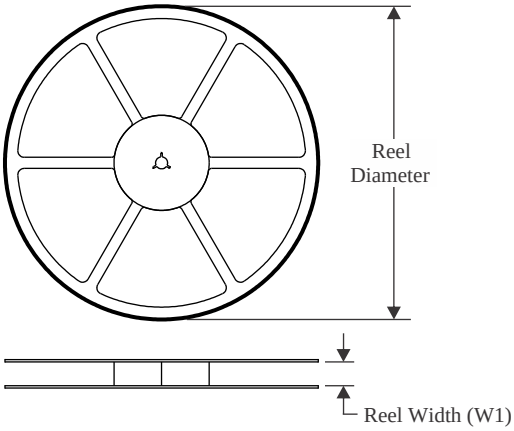
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

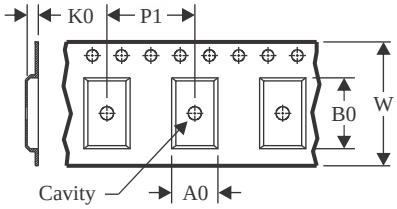
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

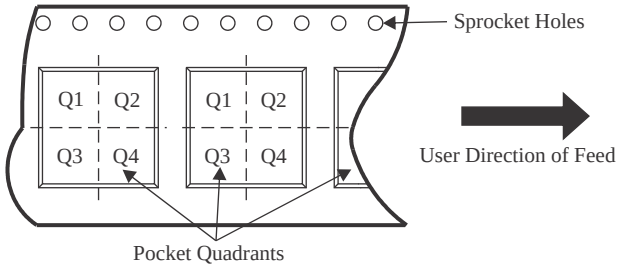


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

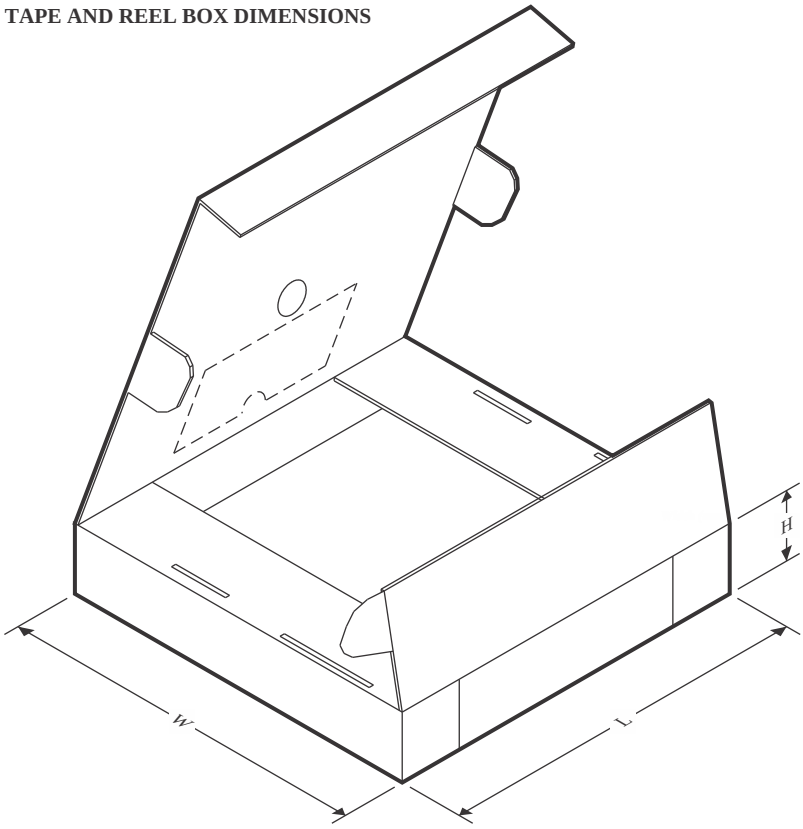
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65300QPWPRQ1	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS65300QRHFRQ1	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65300QPWPRQ1	HTSSOP	PWP	24	2000	350.0	350.0	43.0
TPS65300QRHFRQ1	VQFN	RHF	24	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

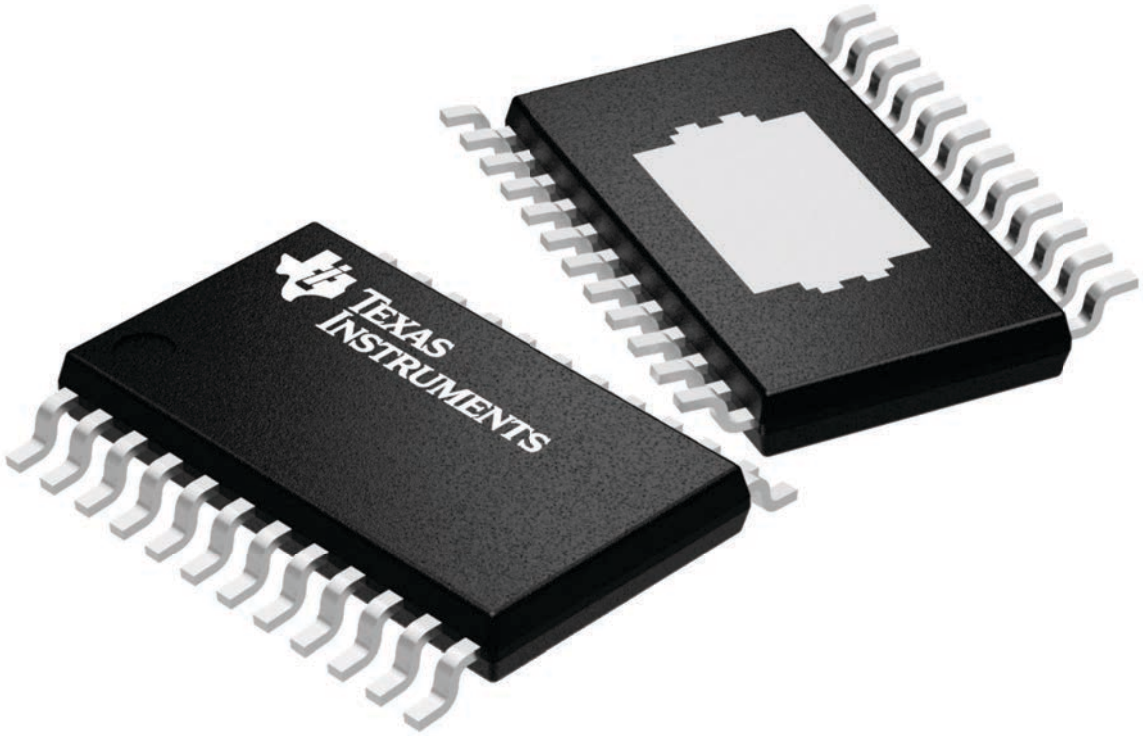
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



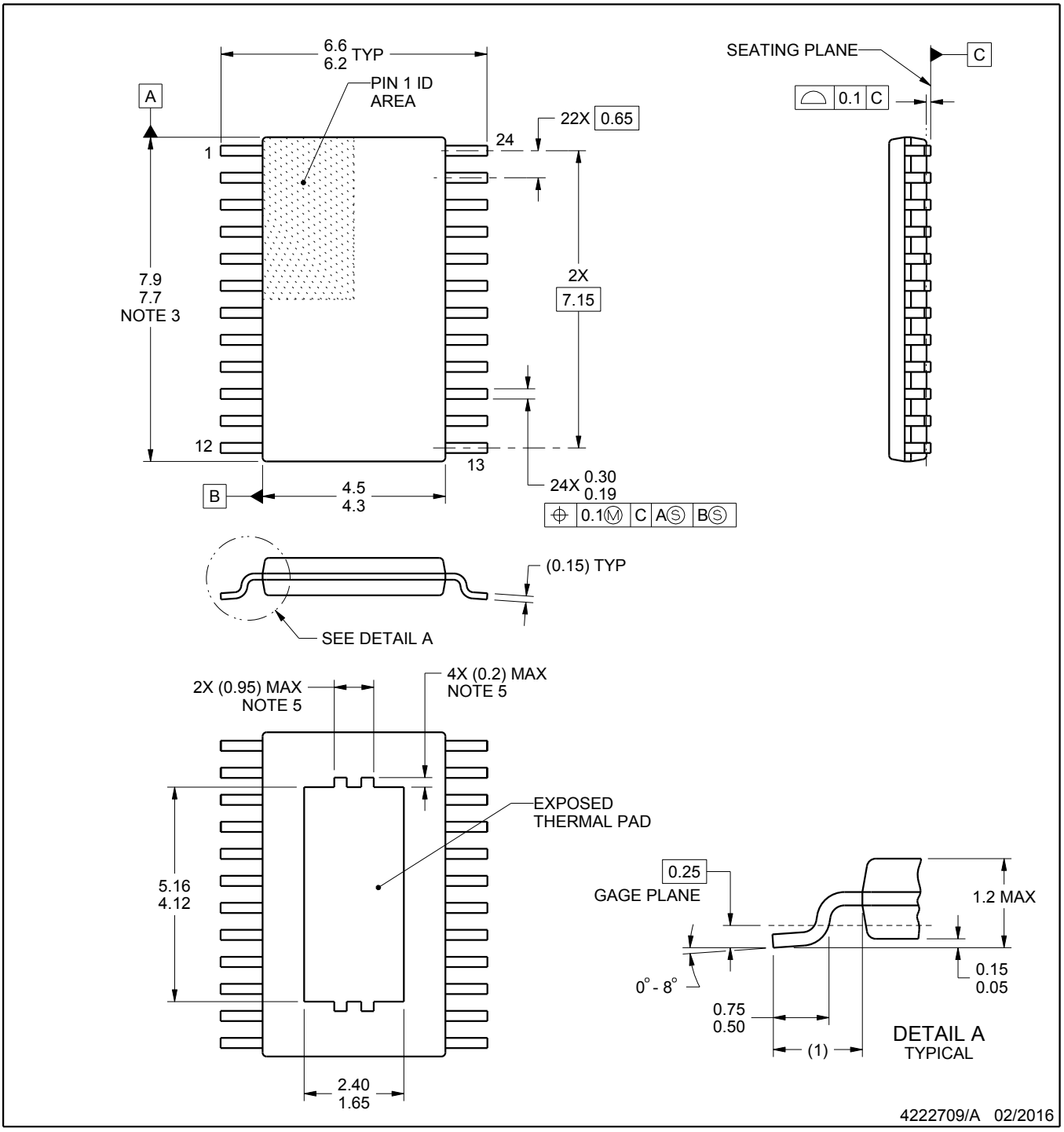
4224742/B

PACKAGE OUTLINE

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

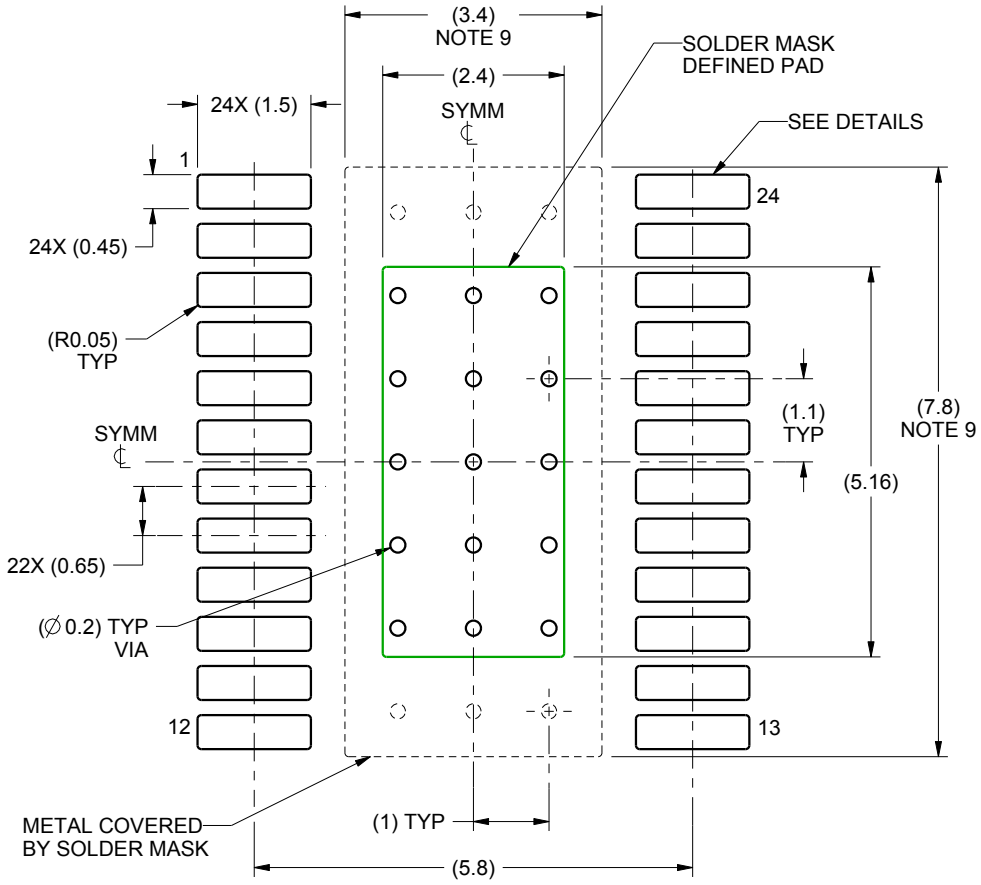
PLASTIC SMALL OUTLINE



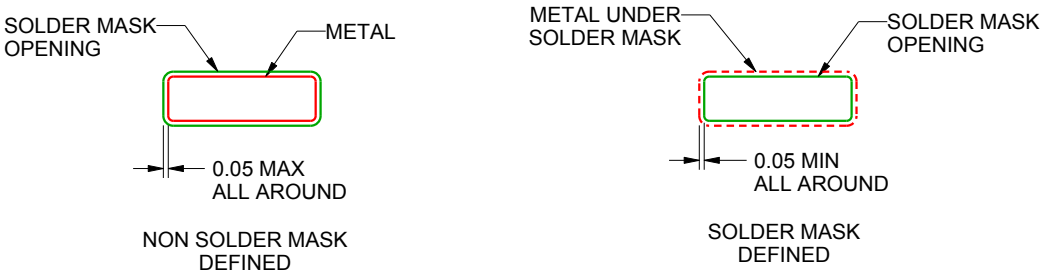
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.



LAND PATTERN EXAMPLE
SCALE:10X

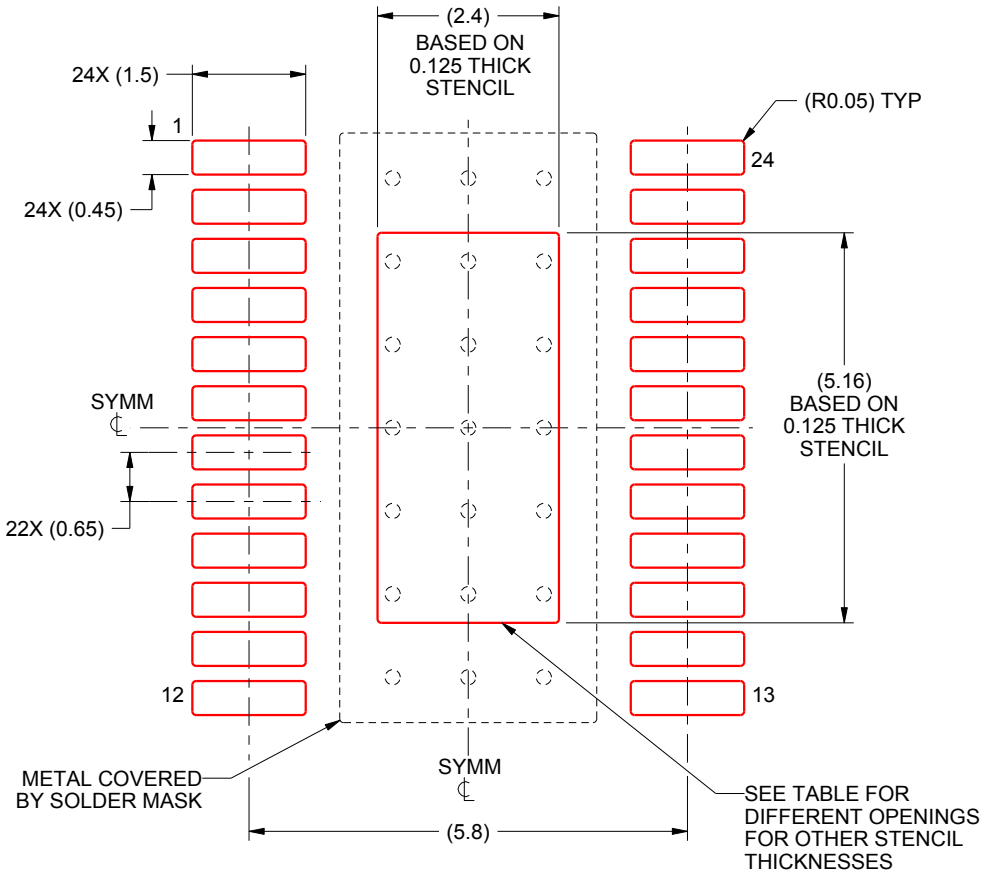


SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

4222709/A 02/2016

NOTES: (continued)

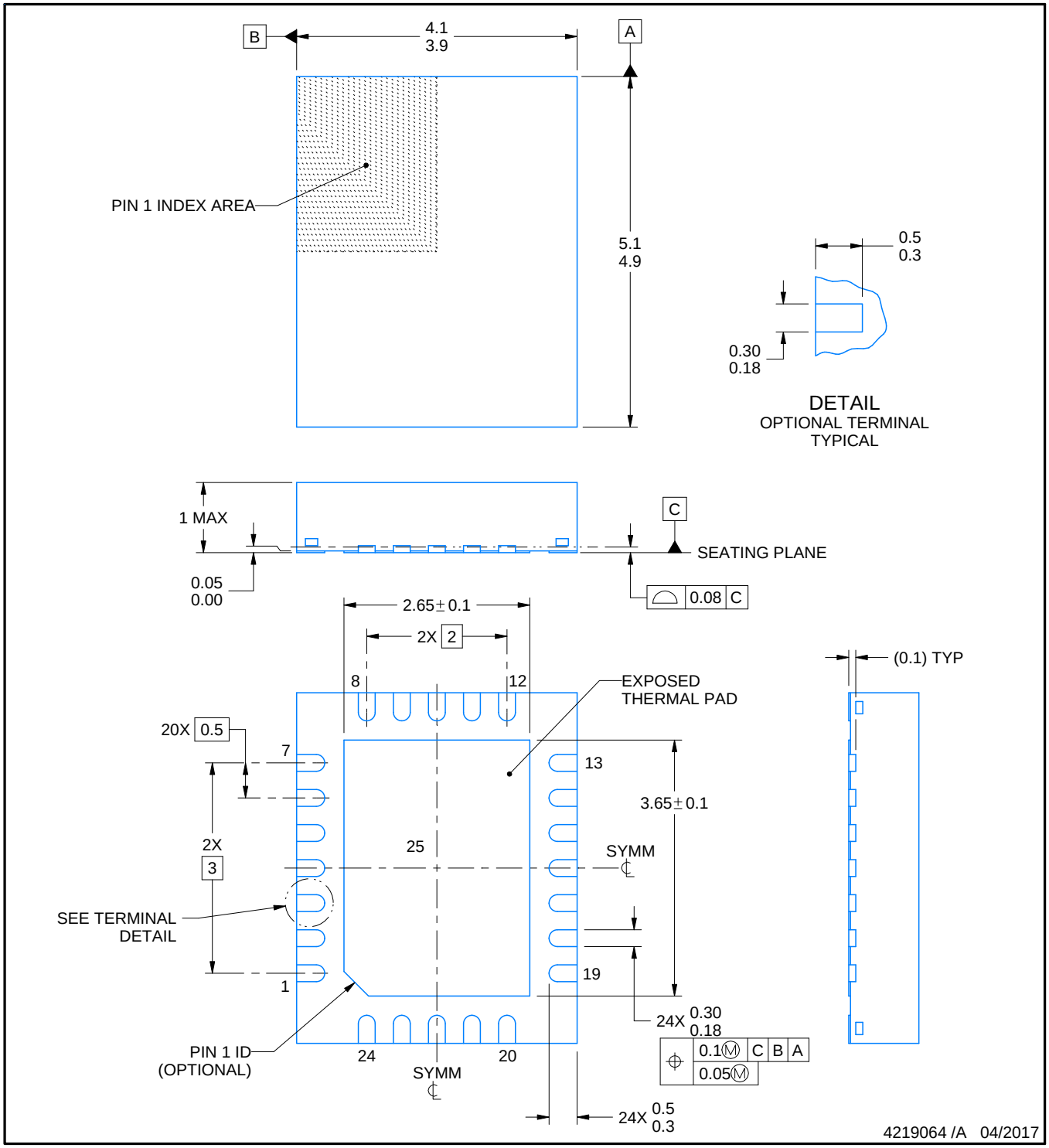
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RHF0024A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

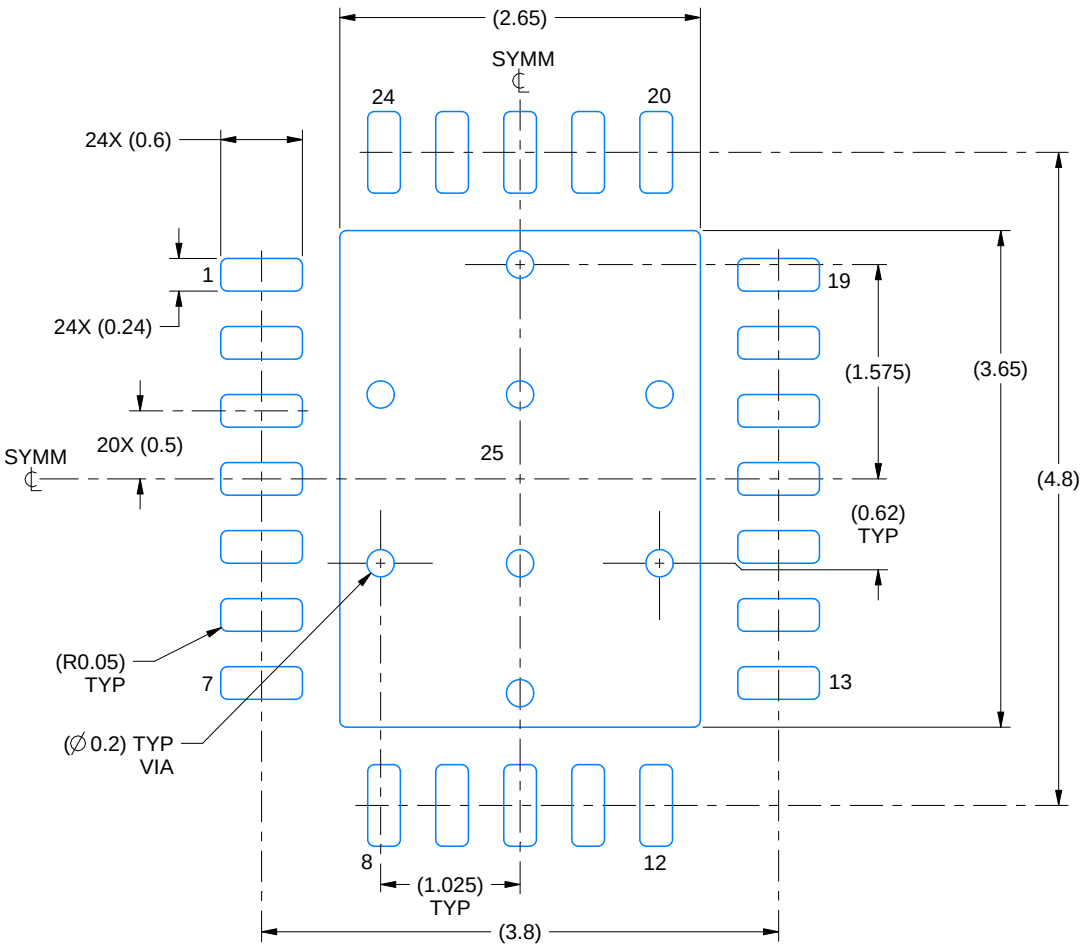
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

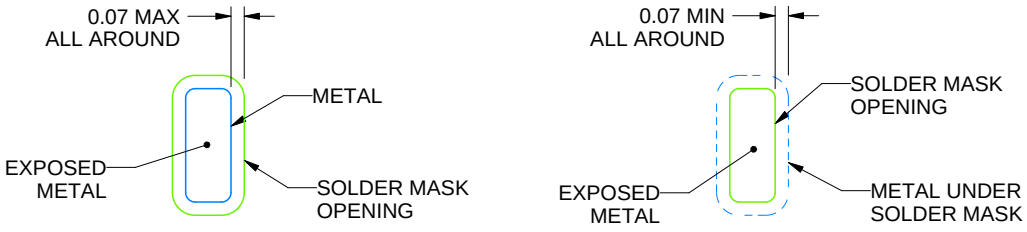
RHF0024A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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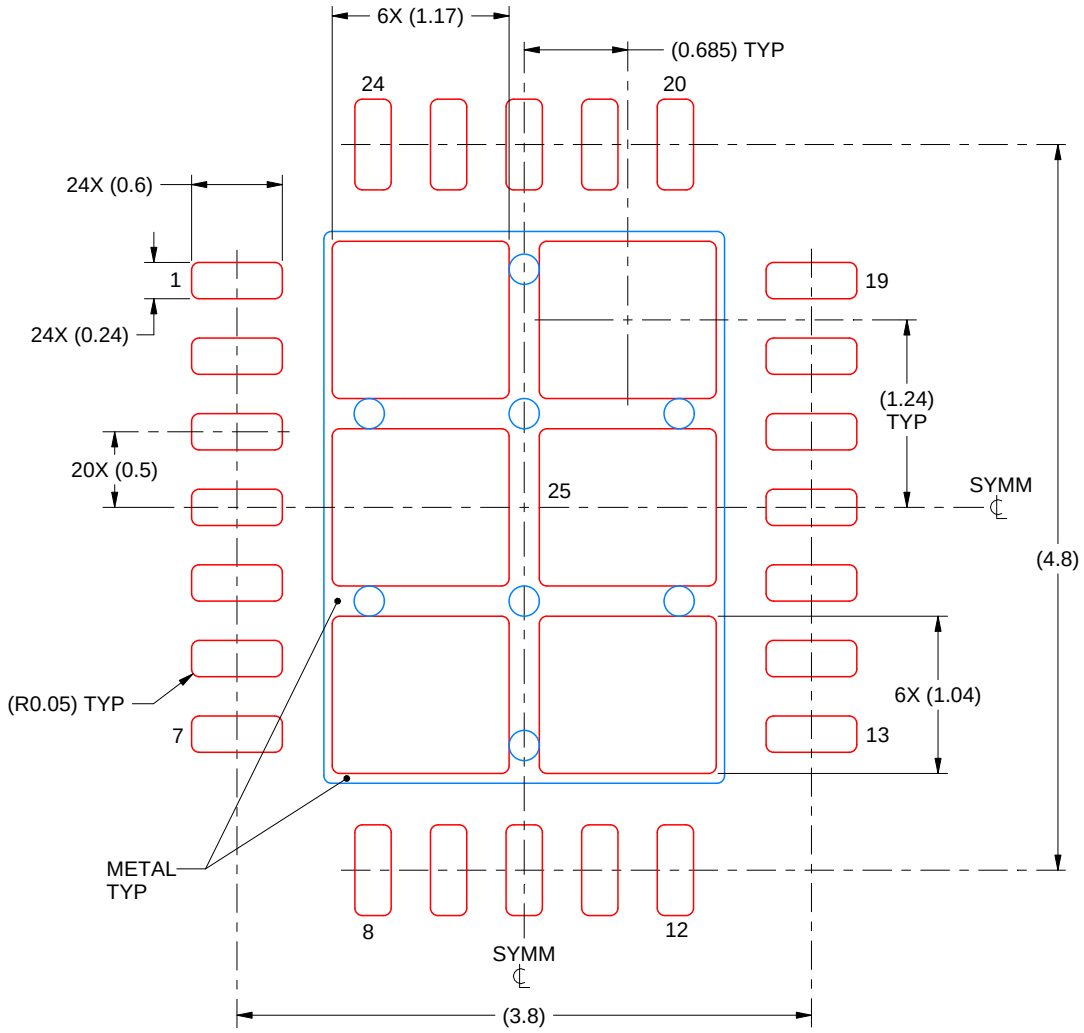
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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