TPS7A4201 28V 输入电压、50mA 稳压器

1 特性

- 宽输入电压范围：7V 至 28V
- 准确度：
  - 标称：1%
  - 整个线路、负载和温度范围内：2.5%
- 低静态电流：25μA
- 关断时的静态电流：4.1μA
- 最大输出电流：50mA
- CMOS 逻辑电平兼容的使能引脚
- 可调输出电压：约 1.175V 至 26V
- 与陶瓷电容搭配工作时保持稳定:
  - 输入电容：≥ 1μF
  - 输出电容：≥ 4.7μF
- 压降电压：290mV
- 内置电流限制和热关断保护
- 封装方式：高散热性能的微型小外形尺寸封装 (MSOP)-8 PowerPAD™
- 工作温度范围：-40°C 至 +125°C

2 应用

- 由工业用总线（具有高电压瞬态）供电的微处理器、微控制器
- 工业自动化
- 汽车
- LED 照明

3 说明

TPS7A4201 器件是一款能够耐受高电压的线性稳压器，不仅融合了耐热增强型封装 (MSOP-8) 的优势，还能够承受持续直流电压或最高可达 28V 的瞬态输入电压。

TPS7A4201 与任何高于 4.7μF 的输出电容以及高于 1μF 的输入电容搭配使用时均可保持稳定（过热和浪涌保护）。鉴于这款器件的封装 (MSOP-8) 小巧且可能使用的输出电容也较小，因此实现起来只需占用非常小的电路板空间。此外，TPS7A4201 还提供了一个与标准 CMOS 逻辑兼容的使能引脚 (EN)，用于使能低电流关断模式。

TPS7A4201 具有热关断和电流限制功能，以便在故障情况下保护系统。MSOP-8 封装的工作温度范围为 T_J = -40°C 至 +125°C。

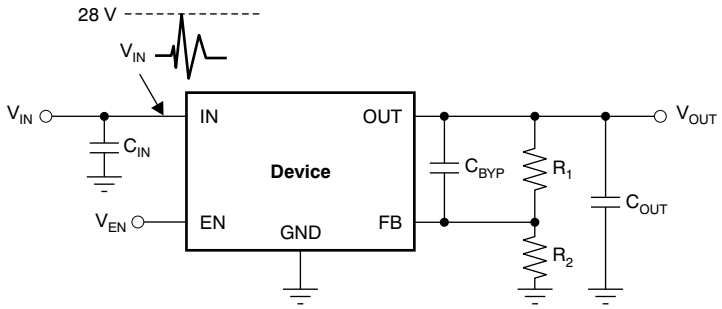
此外，TPS7A4201 器件非常适合在电信和工业 应用中利用中间电压轨生成低压电源；该器件不但能够提供一个充分稳压的电压轨，而且能够承受快速电压瞬变并在其间保持稳压状态。这些 功能 相当于一套更为简单且经济高效的电气浪涌保护电路，因此受到各类应用的青睐。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7A4201	MSOP PowerPAD (8)	3.00mm x 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用



目录

4 修订历史记录

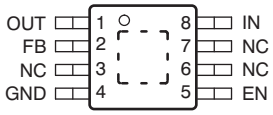
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (December 2011) to Revision A **Page**

- 已添加 *ESD 额定值表*，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分。 ... 1
- Changed maximum recommended operating condition values for VIN, VOUT, and VEN. ... 4
- Changed footnote 2 in *Electrical Characteristics* table ... 5
- Changed I_{LIM} parameter minimum specifications in *Electrical Characteristics* table ... 5

5 Pin Configuration and Functions

DGN Package
8-Pin MSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Regulator output. A capacitor greater than 4.7 µF must be tied from this pin to ground to assure stability.
FB	2	I	This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device.
NC	3	—	Not internally connected. This pin must either be left open or tied to GND.
	6		
	7		
GND	4	—	Ground
EN	5	I	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN\_HI}$ the regulator is enabled. If $V_{EN} \leq V_{EN\_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
IN	8	I	Input supply
PowerPAD	—	—	Solder to printed circuit board (PCB) to enhance thermal performance. **NOTE: The PowerPAD is internally connected to GND.** Although it can be left floating, it is highly recommended to connect the PowerPAD to the GND plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–0.3	+30	V
	OUT pin to GND pin	–0.3	+30	V
	OUT pin to IN pin	–30	+0.3	V
	FB pin to GND pin	–0.3	+2	V
	FB pin to IN pin	–30	+0.3	V
	EN pin to IN pin	–30	0.3	V
	EN pin to GND pin	–0.3	+30	V
Current	Peak output	Internally limited		
Temperature	Operating junction temperature, T_J	–40	+125	°C
	Storage, T_{stg}	–65	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VIN	7		28	V
VOUT	1.161		26	V
VEN	0		28	V
IOUT	0		50	mA

6.4 Thermal Information

THERMAL METRIC (1)		TPS7A4201 DGN (MSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 2.0 V or V_{IN} = 7.0 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		7.0		28.0	V
V_{REF}	Internal reference	T_J = +25°C, V_{FB} = V_{REF}, V_{IN} = 9 V, I_{OUT} = 25 mA	1.161	1.173	1.185	V
V_{OUT}	Output voltage range(1)	V_{IN} ≥ $V_{OUT(NOM)}$ + 2.0 V	V_{REF}		26	V
	Nominal accuracy	T_J = +25°C, V_{IN} = 9 V, I_{OUT} = 25 mA	–1.0		+1.0	$\%V_{OUT}$
	Overall accuracy	$V_{OUT(NOM)}$ + 2.0 V ≤ V_{IN} ≤ 24 V(2) 100 µA ≤ I_{OUT} ≤ 50 mA	–2.5		+2.5	$\%V_{OUT}$
$\Delta V_{O(\Delta VI)}$	Line regulation	7 V ≤ V_{IN} ≤ 28 V		0.03		$\%V_{OUT}$
$\Delta V_{O(\Delta VL)}$	Load regulation	100 µA ≤ I_{OUT} ≤ 50 mA		0.31		$\%V_{OUT}$
V_{DO}	Dropout voltage	V_{IN} = 17 V, $V_{OUT(NOM)}$ = 18 V, I_{OUT} = 20 mA		290		mV
		V_{IN} = 17 V, $V_{OUT(NOM)}$ = 18 V, I_{OUT} = 50 mA		0.78	1.3	V
I_{LIM}	Current limit	V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = 7.0 V, T_J ≤ +85°C	65	117	200	mA
		V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = 9.0 V	65	128	200	mA
I_{GND}	Ground current	7 V ≤ V_{IN} ≤ 28 V, I_{OUT} = 0 mA		25	65	µA
		I_{OUT} = 50 mA		25		µA
I_{SHDN}	Shutdown supply current	V_{EN} = +0.4 V		4.1	20	µA
I_{FB}	Feedback current(3)		–0.1	0.01	0.1	µA
I_{EN}	Enable current	7 V ≤ V_{IN} ≤ 28 V, V_{IN} = V_{EN}		0.02	1.0	µA
V_{EN_HI}	Enable high-level voltage		1.5		V_{IN}	V
V_{EN_LO}	Enable low- level voltage		0		0.4	V
V_{NOISE}	Output noise voltage	V_{IN} = 12 V, $V_{OUT(NOM)}$ = V_{REF}, C_{OUT} = 10 µF, BW = 10 Hz to 100 kHz		58		μV_{RMS}
		V_{IN} = 12 V, $V_{OUT(NOM)}$ = 5 V, C_{OUT} = 10 µF, C_{BYP}(4) = 10 nF, BW = 10 Hz to 100 kHz		73		μV_{RMS}
PSRR	Power-supply rejection ratio	V_{IN} = 12 V, $V_{OUT(NOM)}$ = 5 V, C_{OUT} = 10 µF, C_{BYP}(4) = 10 nF, f = 100 Hz		65		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+170		°C
		Reset, temperature decreasing		+150		°C
T_J	Operating junction temperature range		–40		+125	°C

(1) To ensure stability at no-load conditions, a current from the feedback resistive network greater than or equal to 10 µA is required.
(2) Maximum input voltage (V_{IN}) is limited to 24 V because of the package power dissipation limitations at full load [P ≈ (V_{IN} – V_{OUT}) × I_{OUT} = (24 V – V_{REF}) × 50 mA ≈ 1.14 V], given an ambient temperature of +50°C. The device is capable of sourcing steady-state load currents as high as 60 mA at higher input voltages without damage if the maximum operating junction temperature (T_J) is not exceeded. The Electrical Characteristics are not characterized for load current (I_{OUT}) exceeding 50 mA.
(3) I_{FB} > 0 flows out of the device.
(4) C_{BYP} refers to a bypass capacitor connected to the FB and OUT pins.

6.6 Dissipation Ratings

BOARD	PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$	DERATING FACTOR ABOVE T_A = +25°C	T_A ≤ +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
High-K(1)	DGN	55.9°C/W	8.47°C/W	16.6mW/°C	1.83W	1.08W	0.833W

(1) The JEDEC High-K (2s2p) board design used to derive this data was a 3-inch x 3-inch multilayer board with 2-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

6.7 Typical Characteristics

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 2.0 V or V_{IN} = 9.0 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

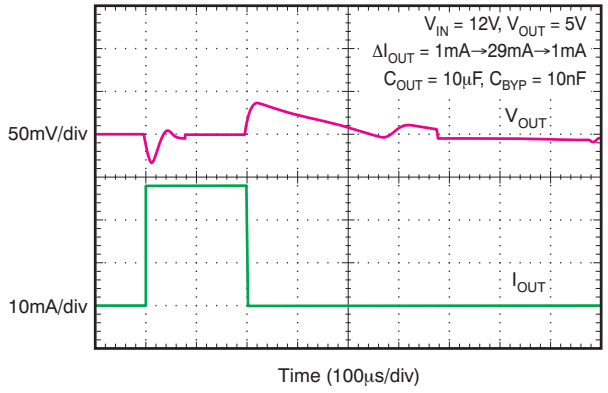


Figure 1. Load Transient Response

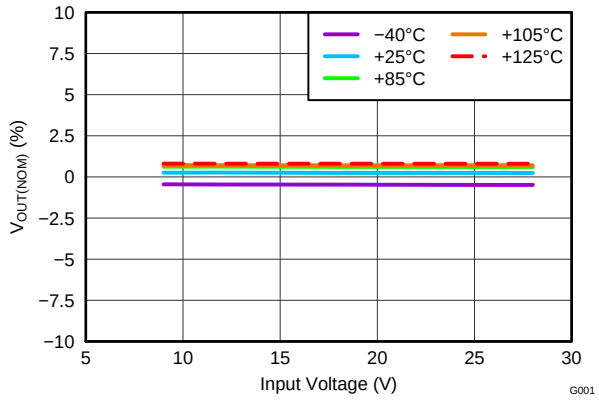


Figure 2. Line Regulation

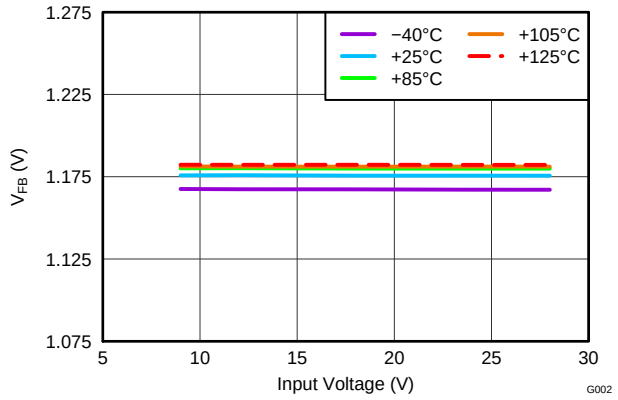


Figure 3. Feedback Voltage

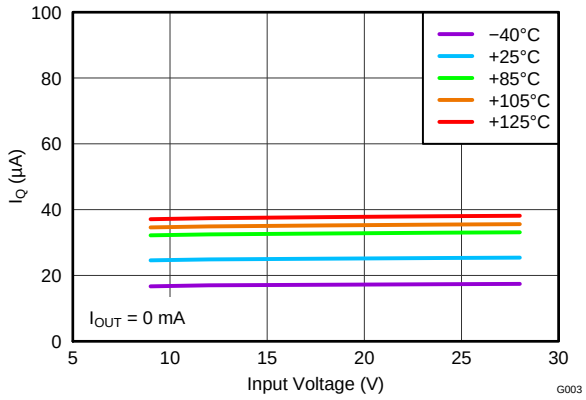


Figure 4. Quiescent Current vs Input Voltage

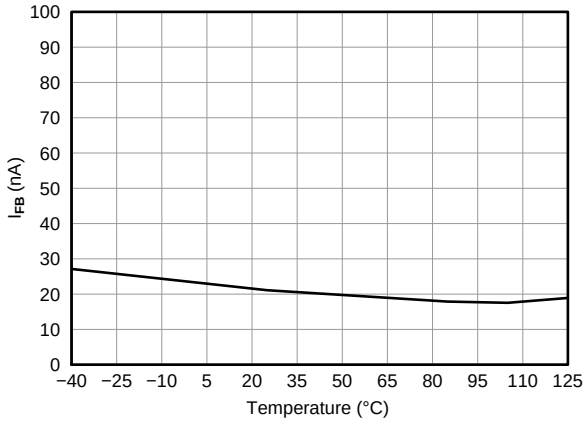


Figure 5. Feedback Current

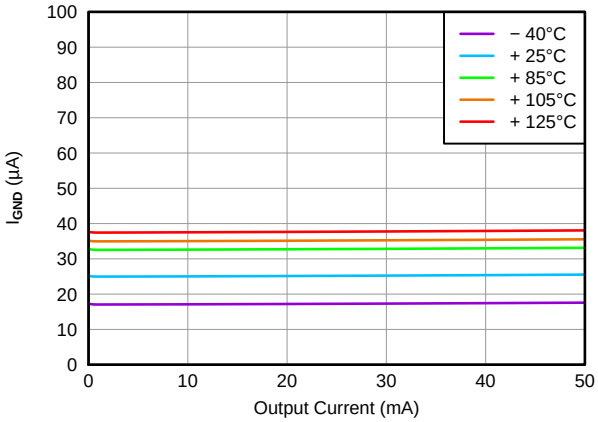


Figure 6. Ground Current

Typical Characteristics (continued)

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 2.0 V or V_{IN} = 9.0 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

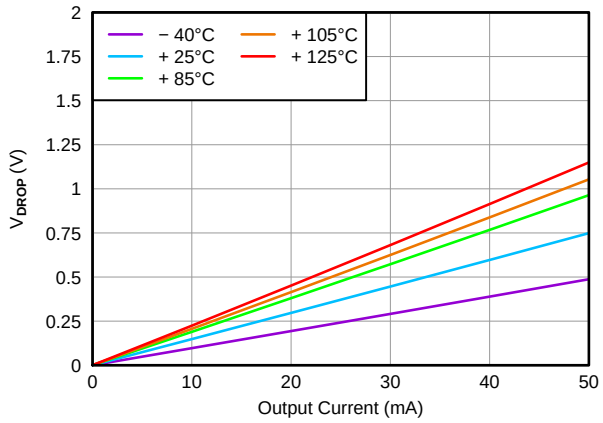


Figure 7. Dropout Voltage

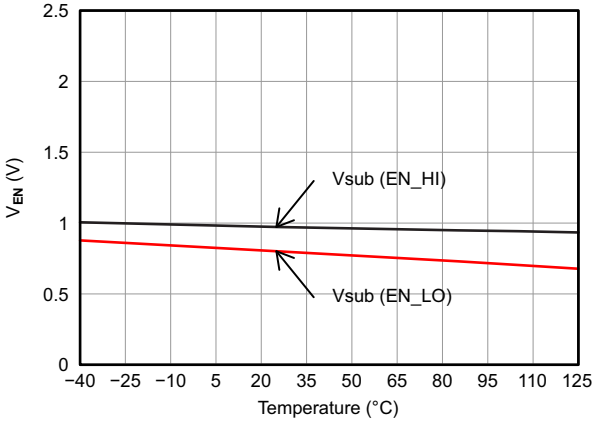


Figure 8. Enable Threshold Voltage

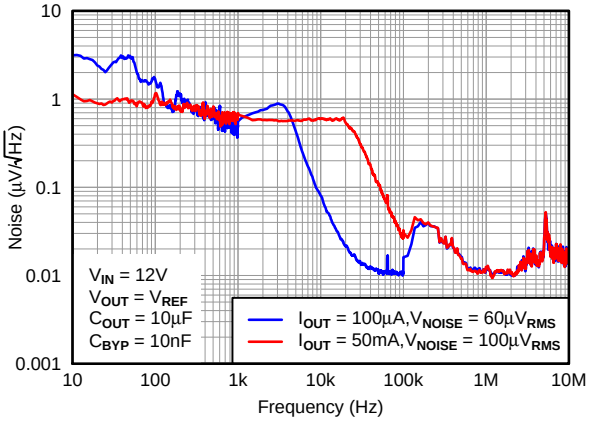


Figure 9. Output Spectral Noise Density

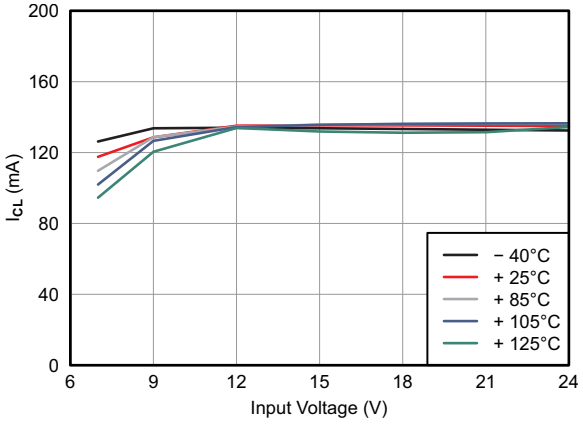


Figure 10. Current Limit

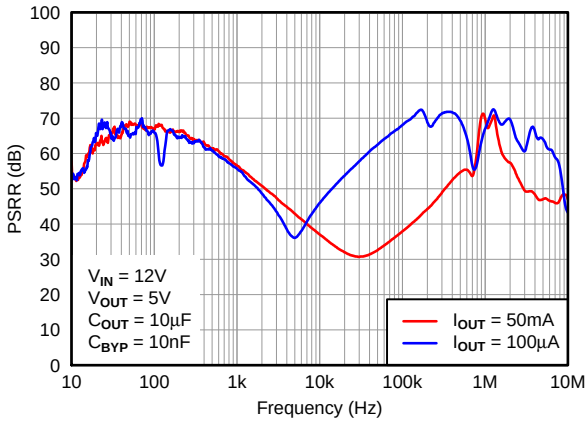


Figure 11. Power-Supply Rejection Ratio

7 Detailed Description

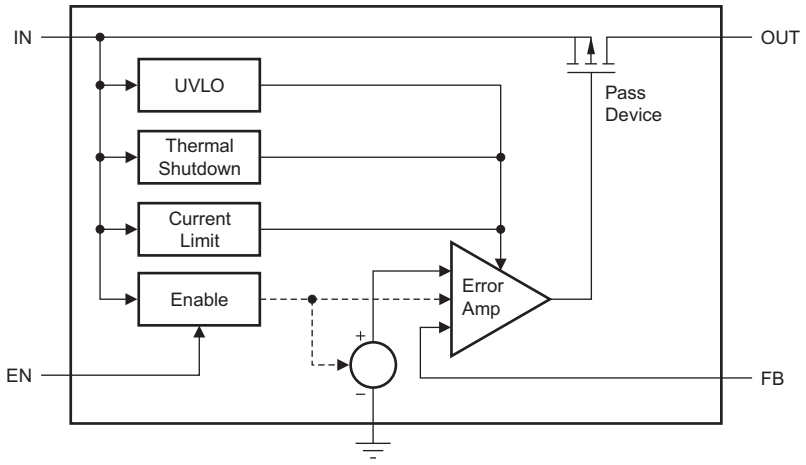
7.1 Overview

The TPS7A4201 belongs to a new generation of linear regulators that use an innovative BiCMOS process technology to achieve very high maximum input and output voltages.

This process not only allows the TPS7A4201 to maintain regulation during very fast voltage transients up to 28 V, but it also allows the TPS7A4201 to regulate from a continuous high-voltage input rail. Unlike other regulators created using bipolar technology, the TPS7A4201 ground current is also constant over its output current range, resulting in increased efficiency and lower power consumption.

These features, combined with a high thermal performance MSOP-8 PowerPAD package, make this device ideal for industrial and telecom applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable Pin Operation

The TPS7A4201 provides an enable pin (EN) feature that turns on the regulator when V_{EN} > 1.5 V.

7.3.2 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A4201 device has been designed to protect against overload conditions. The protection circuitry was not intended to replace proper heatsinking. Continuously running the TPS7A4201 device into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device (as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN\_HI}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN\_HI}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN\_LO}$	—	$T_J > 170°C$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adjustable Operation

The TPS7A4201 has an output voltage range of ~1.175 V to 26 V. The nominal output voltage of the device is set by two external resistors, as shown in Figure 12.

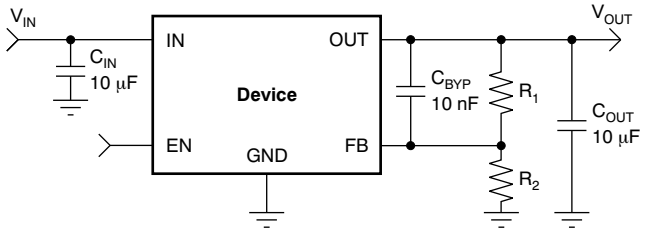


Figure 12. Adjustable Operation for Maximum AC Performance

R_1 and R_2 can be calculated for any output voltage range using the formula shown in Equation 1. To ensure stability under no-load conditions, this resistive network must provide a current greater than or equal to 10 µA.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right), \quad \text{where } \frac{V_{OUT}}{R_1 + R_2} \geq 10\ \mu A \tag{1}$$

If greater voltage accuracy is required, take into account the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

8.1.2 Transient Voltage Protection

One of the primary applications of the TPS7A4201 is to provide transient voltage protection to sensitive circuitry that may be damaged in the presence of high-voltage spikes.

This transient voltage protection can be more cost-effective and compact compared to topologies that use a transient voltage suppression (TVS) block.

8.2 Typical Application

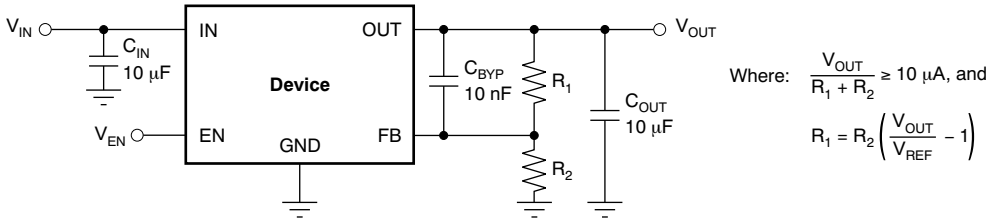


Figure 13. Example Circuit to Maximize Transient Performance

8.2.1 Design Requirements

For this design example, use the following parameters listed in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
V_{IN}	12 V
V_{OUT}	5 V (ideal), 4.981 V (actual)
I_{OUT}	28 mA
Accuracy	5 %
R1, R2	162 kΩ, 49.9 kΩ

8.2.2 Detailed Design Procedure

The maximum value of total feedback resistance can be calculated to be 500 kΩ. Equation 1 was used to calculate R1 and R2, and standard 1% resistors were selected to keep the accuracy within the 5% allocation. 10-uF ceramic input and output capacitors were selected, along with a 10-nF bypass capacitor for optimal AC performance.

8.2.2.1 Capacitor Recommendations

Low equivalent series resistance (ESR) capacitors should be used for the input, output, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved over-temperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

Note that high ESR capacitors may degrade PSRR.

8.2.2.2 Input and Output Capacitor Requirements

The TPS7A4101 high voltage linear regulator achieves stability with a minimum output capacitance of 4.7 µF and input capacitance of 1 µF; however, it is highly recommended to use 10-µF output and input capacitors to maximize ac performance.

8.2.2.3 Bypass Capacitor Requirements

Although a bypass capacitor (C_{BYP}) is not needed to achieve stability, it is highly recommended to use a 10-nF bypass capacitor to maximize ac performance (including line transient, noise and PSRR).

8.2.2.4 Maximum AC Performance

In order to maximize line transient, noise, and PSRR performance, it is recommended to include 10-µF (or higher) input and output capacitors, and a 10-nF bypass capacitor; see Figure 12. The solution shown delivers minimum noise levels of 58 μV_{RMS} and power-supply rejection levels above 36 dB from 10 Hz to 10 MHz.

8.2.2.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

Note that the presence of the C_{BYP} capacitor may greatly improve the TPS7A4201 line transient response, as noted in Figure 1.

8.2.3 Application Curves

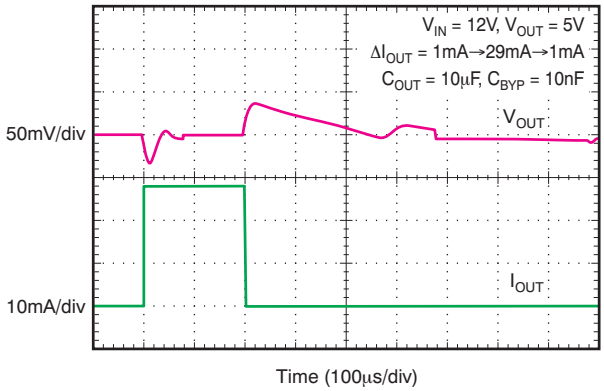


Figure 14. Load Transient Response

9 Power Supply Recommendations

The input supply for the LDO should not exceed its recommended operating conditions (7 V to 28 V). The input voltage should provide adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance. The input and output supplies should also be bypassed with 10-µF capacitors located near the input and output pins. There should be no other components located between these capacitors and the pins.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, C_{BYP}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for the TPS7A4201 evaluation board, available at www.ti.com.

10.2 Layout Example

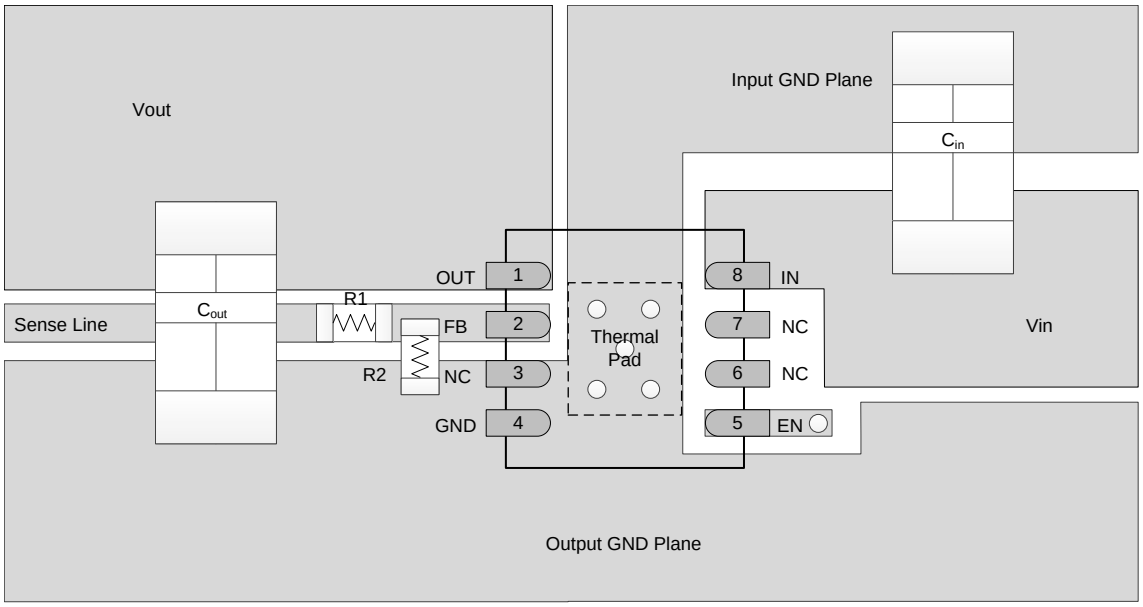


Figure 15. Recommended Layout Example

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle ON and OFF. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Thermal Considerations (接下页)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 45°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A4201 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A4201 device into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT})\ I_{OUT} \quad (2)$$

11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A4201DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SBC
TPS7A4201DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SBC
TPS7A4201DGNT	Active	Production	HVSSOP (DGN) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SBC
TPS7A4201DGNT.A	Active	Production	HVSSOP (DGN) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SBC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

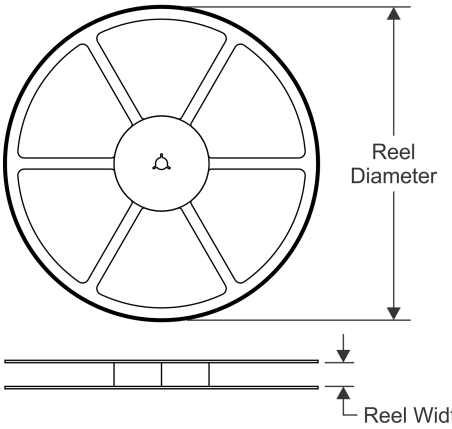
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

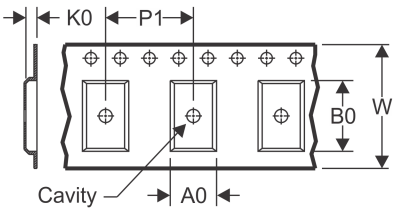
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

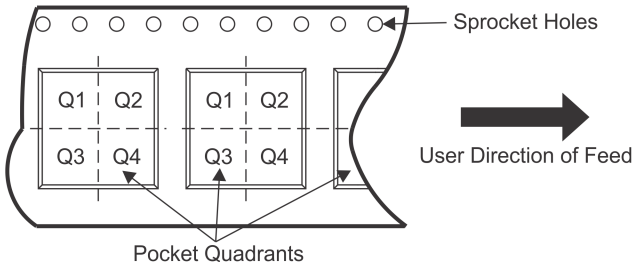


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

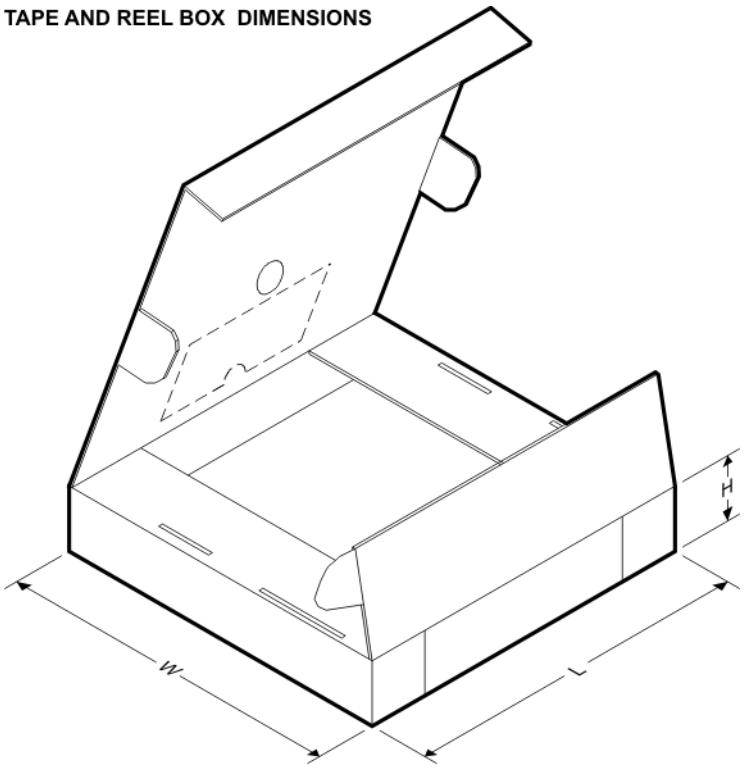
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4201DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A4201DGNT	HVSSOP	DGN	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4201DGNR	HVSSOP	DGN	8	2500	346.0	346.0	35.0
TPS7A4201DGNT	HVSSOP	DGN	8	250	200.0	183.0	25.0

GENERIC PACKAGE VIEW

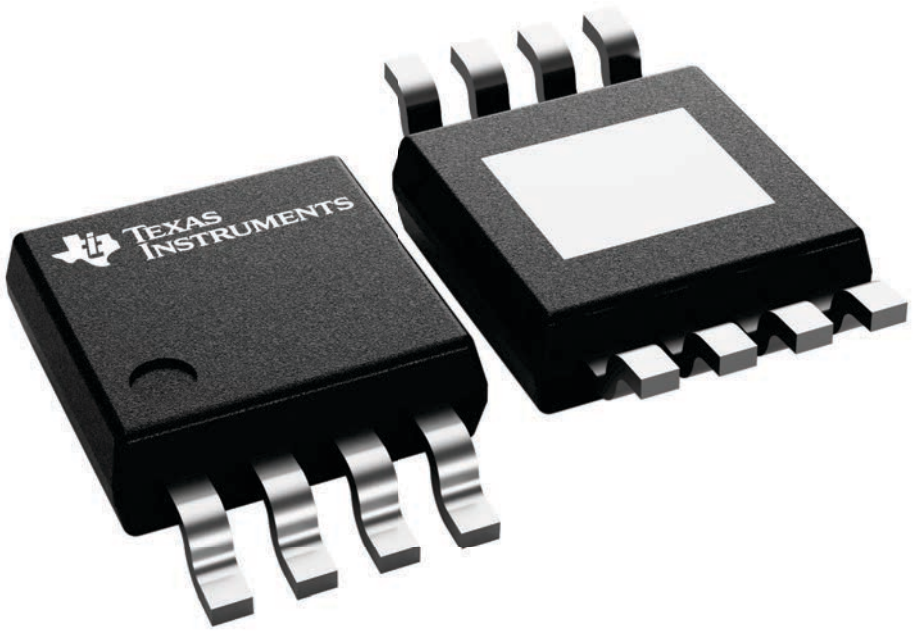
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

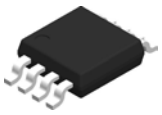
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

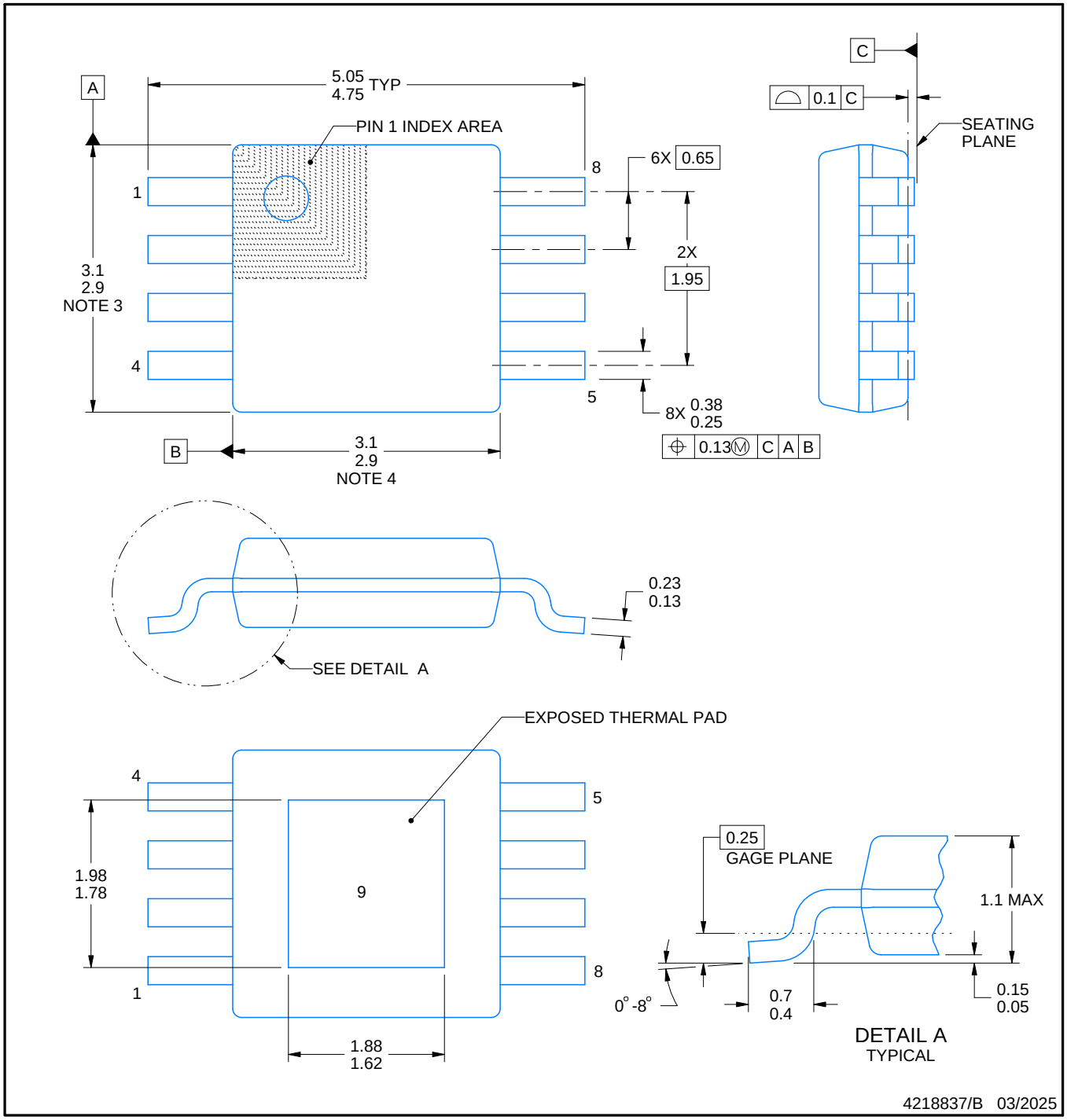
PACKAGE OUTLINE

DGN0008B



HVSSOP - 1.1 mm max height

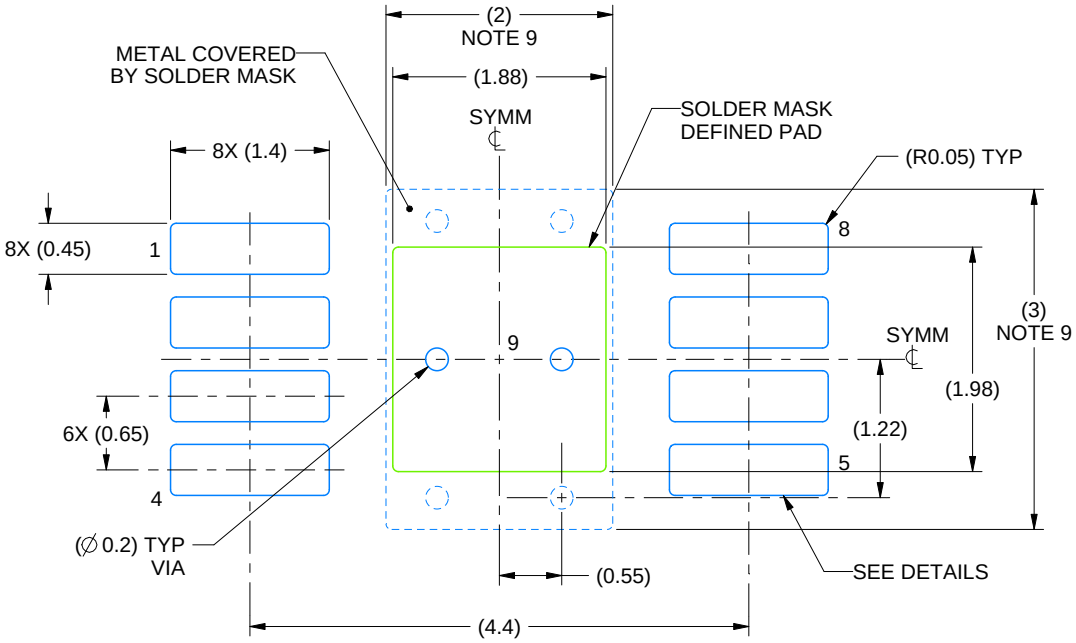
SMALL OUTLINE PACKAGE



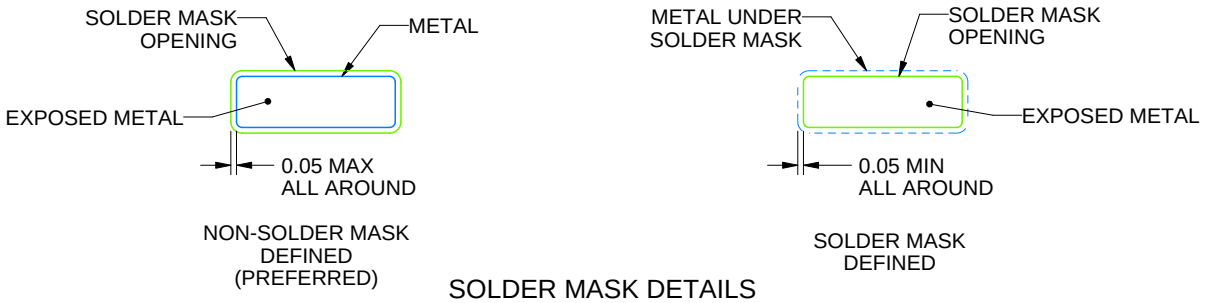
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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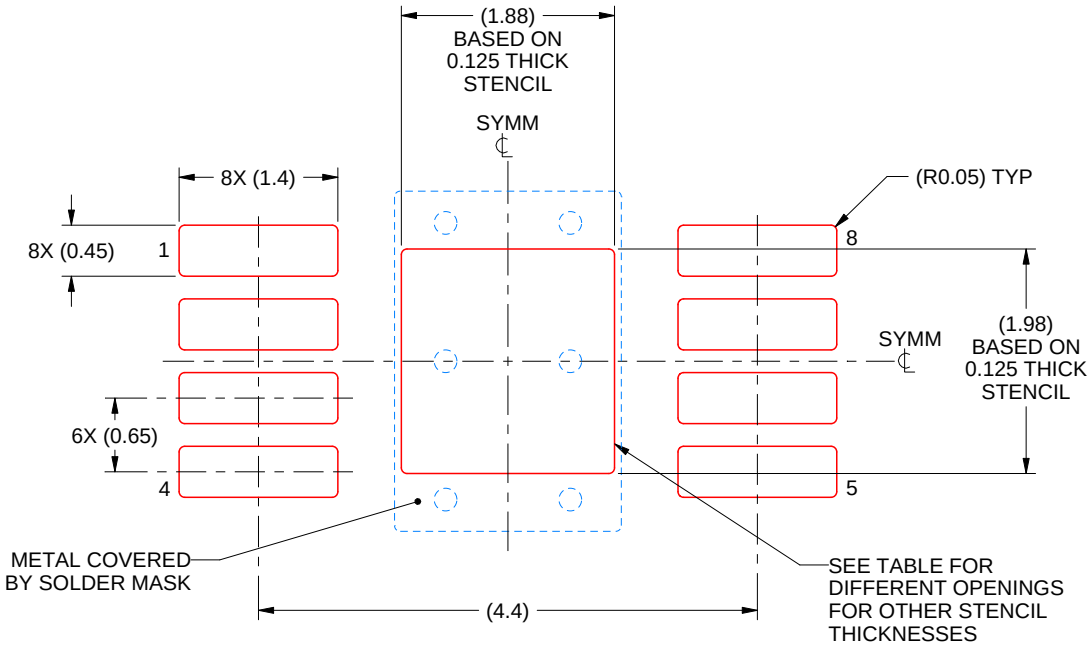
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.21
0.125	1.88 X 1.98 (SHOWN)
0.15	1.72 X 1.81
0.175	1.59 X 1.67

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月