XTR11x 4-20mA 电流环路变送器

1 特性

- 低静态电流：200μA
- 用于外部电路的 5V 稳压器
- 用于传感器激励的 V_{REF}：
  - XTR115：2.5V
  - XTR116：4.096V
- 低量程误差：0.05%
- 低非线性误差：0.003%
- 宽环路电源电压范围：7.5 V 至 36 V
- SO-8 封装

2 应用

- 2 线 4-20mA 电流环路
- 发送器
- 智能变送器
- 工业过程控制
- 测试系统
- 与 HART 调制解调器兼容
- 电流放大器
- 电压转电流放大器

3 说明

XTR115 和 XTR116 (XTR11x) 是精密电流输出转换器，设计用于通过业界通用电流环路传输模拟 4mA 至 20mA 信号。这些器件提供精确的电流调节和输出电流限制功能。

片上稳压器 (5V) 可用于为外部电路供电。精密片上 V_{REF}（XTR115 为 2.5V，XTR116 为 4.096V）可用于激励传感器或使其偏移。电流回路引脚 (I_{RET}) 可检测外部电路中使用的任何电流，以精确控制输出电流。

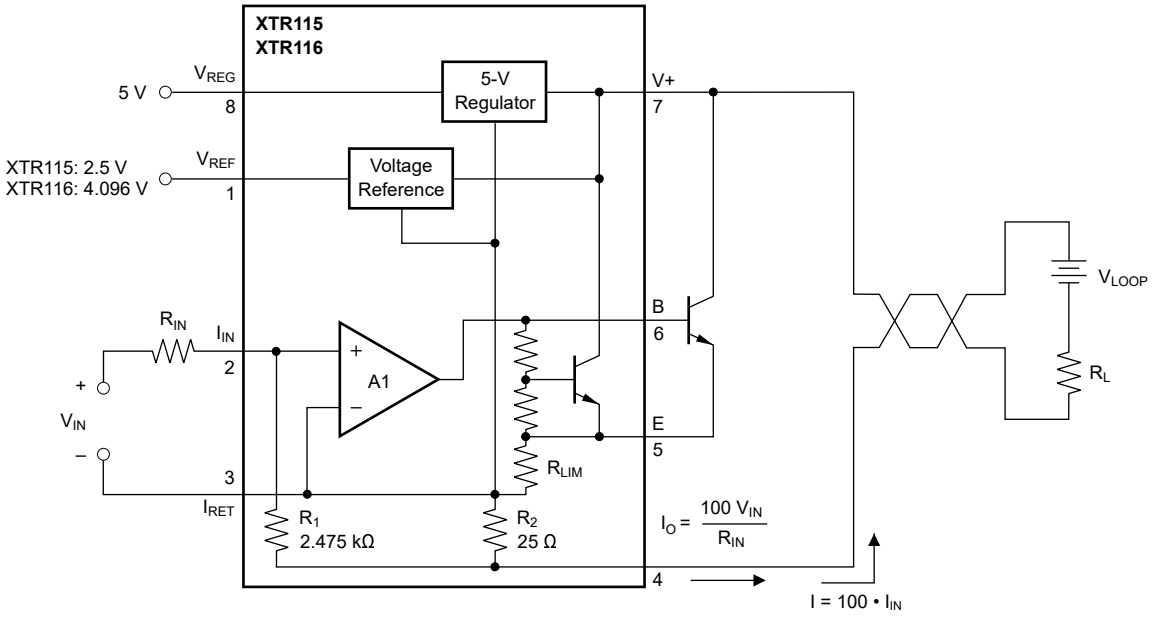
XTR11x 是使用 4mA 至 20mA 电流传输的智能传感器的基本构建块。

XTR11x 的工业级工作温度范围为 –40°C 至 +85°C。

器件信息

器件型号	片上 V_{REF}	封装(1)
XTR115	2.5V	D（SOIC，8）
XTR116	4.096V	

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (November 2003) to Revision B (March 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 添加了 *引脚功能*、*ESD 等级*、*热性能信息*、*建议运行条件* 和 *电气特性* 表以及 *详细说明*、*概述*、*功能方框图*、*特性说明*、*应用和实施*、*器件和文档支持* 和 *机械、封装和可订购信息* 部分	1
• Added *Pin Functions* table	3
• Changed operating temperature minimum value from –55°C to –40°C in *Absolute Maximum Ratings*	4
• Deleted thermal resistance, θ_{JA} specification of 150 °C/W from *Electrical Characteristics*; added a *Thermal Information* table, with $R_{\theta JA}$ = 128.2 °C/W and other detailed thermal parameters	4
• Changed span error test condition from: I_{IN} = 250 µA to 25 mA to: I_{OUT} = 250 µA to 25 mA in *Electrical Characteristics*	5
• Changed V_{REF} voltage accuracy vs load typical value from ±100 ppm/mA to ±200 ppm/mA in *Electrical Characteristics*	5
• Changed bias current vs temperature typical value from 150 pA/°C to 300 pA/°C in *Electrical Characteristics* .	5
• Changed *Basic Circuit Connections* application diagram	9
• Changed *External Transistor* applications information section to incorporate additional guidance regarding transistor power dissipation and thermal concerns	10
• Added *Circuit Stability* application information section	12

5 Pin Configuration and Functions

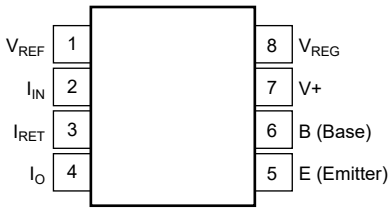


图 5-1. D Package, SOIC-8 (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V_{REF}	Output	Reference voltage output (2.5 V for XTR115, 4.096 V for XTR116)
2	I_{IN}	Input	Current input pin
3	I_{RET}	Input	Local ground return pin for V_{REG} and V_{REF}
4	I_O	Output	Regulated 4-mA to 20-mA current-loop output
5	E (Emitter)	Input	Emitter connection for external transistor
6	B (Base)	Output	Base connection for external transistor
7	V+	Power	Loop power supply
8	V_{REG}	Output	5-V regulator voltage output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V+	Power supply (referenced to I_O pin)		40	V
	Input voltage (referenced to I_{RET} pin)	0	V+	V
	Output current limit	Continuous		
	V_{REG}, short-circuit	Continuous		
	V_{REF}, short-circuit	Continuous		
T_A	Operating temperature	–40	125	°C
T_J	Junction temperature		165	°C
T_{stg}	Storage temperature	–55	125	°C
	Lead temperature (soldering, 10 s)		300	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+	Power supply voltage	7.5	24	36	V
T_A	Specified temperature	–40		85	°C

6.3 Thermal Information

THERMAL METRIC(1)		XTR11x D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	74.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.4 Electrical Characteristics

at T_A = 25°C, V+ = 24 V, R_{IN} = 20 kΩ, and TIP29C external transistor (unless otherwise noted)

PARAMETER		TEST CONDITIONS	XTR115U, XTR116U			XTR115UA, XTR116UA			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT									
I_O	Output current equation			$I_O = I_{IN} \times 100$			$I_O = I_{IN} \times 100$		
	Output current, linear range		0.25		25	0.25		25	mA
I_{LIM}	Overscale limit			32			32		mA
I_{MIN}	Underscale limit	I_{REG} = 0, I_{REF} = 0		0.2	0.25		0.2	0.25	mA
SPAN									
S	Span (current gain)			100			100		A/A
	Error(1)	I_{OUT} = 250 mA to 25 mA		±0.05	±0.2		±0.05	±0.4	%
	vs Temperature	T_A = –40°C to +85°C		±3	±20		±3	±20	ppm/°C
	Nonlinearity	I_{IN} = 250 mA to 25 mA		±0.003	±0.01		±0.003	±0.02	%
INPUT									
V_{OS}	Offset voltage (op amp)	I_{IN} = 40 mA		±100	±250		±100	±500	µV
	vs Temperature	T_A = –40°C to +85°C		±0.7	±3		±0.7	±6	µV/°C
	vs Supply voltage, V+	V+ = 7.5 V to 36 V		±0.1	±2		±0.1	±2	µV/V
I_B	Bias current			–35			–35		nA
	vs Temperature			300			300		pA/°C
e_n	Noise: 0.1 Hz to 10 Hz			0.6			0.6		µVp-p
DYNAMIC RESPONSE									
	Small signal bandwidth	C_{LOOP} = 0, R_L = 0		380			380		kHz
	Slew rate			3.2			3.2		mA/µs
V_{REF} (2)									
	XTR115			2.5			2.5		V
	XTR116			4.096			4.096		V
	Voltage accuracy	I_{REF} = 0		±0.05	±0.25		±0.05	±0.5	%
	vs Temperature	T_A = –40°C to +85°C		±20	±35		±20	±75	ppm/°C
	vs Supply voltage, V+	V+ = 7.5 V to 36 V		±1	±10		±1	±10	ppm/V
	vs Load	I_{REF} = 0 mA to 2.5 mA		±200			±200		ppm/mA
	Noise	0.1 Hz to 10 Hz		10			10		µVp-p
	Short-circuit current			16			16		mA
V_{REG} (2)									
	Voltage			5			5		V
	Voltage accuracy	I_{REG} = 0		±0.05	±0.1		±0.05	±0.1	V
	vs Temperature	T_A = –40°C to +85°C		±0.1			±0.1		mV/°C
	vs Supply voltage, V+	V+ = 7.5 V to 36 V		1			1		mV/V
	vs Output current			See *Typical Characteristics*			See *Typical Characteristics*		
	Short-circuit current			12			12		mA
POWER SUPPLY, V+									
	Quiescent current			200	250		200	250	µA
		T_A = –40°C to +85°C		240	300		240	300	µA

(1) Does not include initial error or TCR of R_{IN}.
(2) Voltage measured with respect to I_{RET} pin.

6.5 Typical Characteristics

At T_A = 25°C, V+ = 24 V, R_{IN} = 20 kΩ, and TIP29C external transistor (unless otherwise noted)

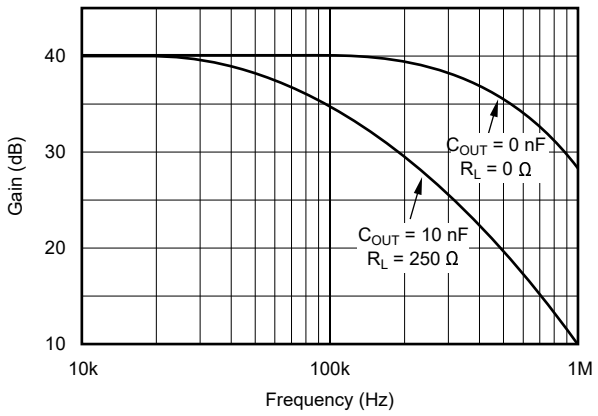


图 6-1. Current Gain vs Frequency

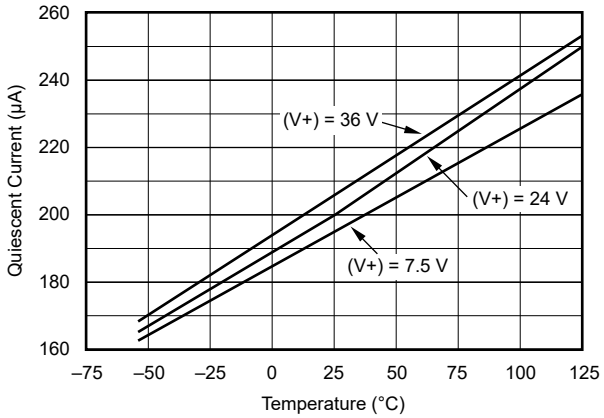


图 6-2. Quiescent Current vs Temperature

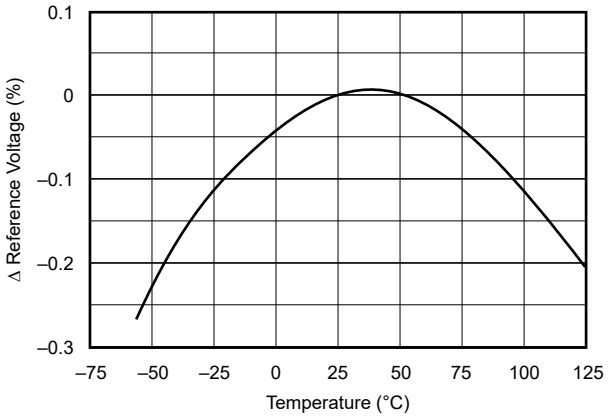


图 6-3. Reference Voltage vs Temperature

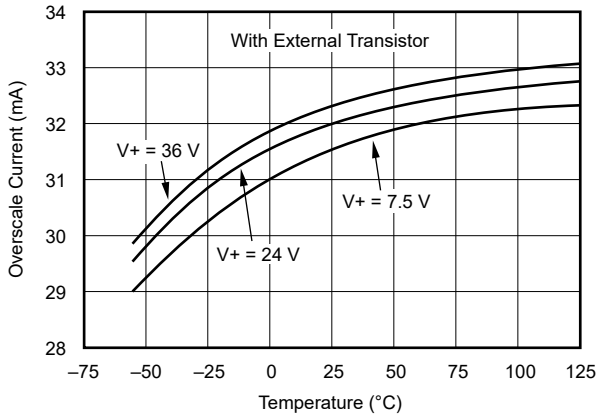


图 6-4. Overscale Current vs Temperature

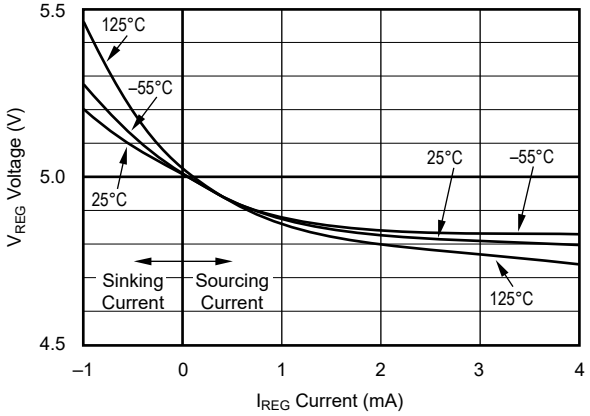


图 6-5. V_{REG} Voltage vs V_{REG} Current

7 Detailed Description

7.1 Overview

The XTR115 and XTR116 are precision current output converters designed to transmit analog 4-mA-to-20-mA signals over an industry standard current loop. The regulator and reference voltages power a sensor, such as a bridge as shown in 图 7-1. The sensor output, as a current signal I_{IN}, is gained up and transmitted over the loop to be read by a receiver.

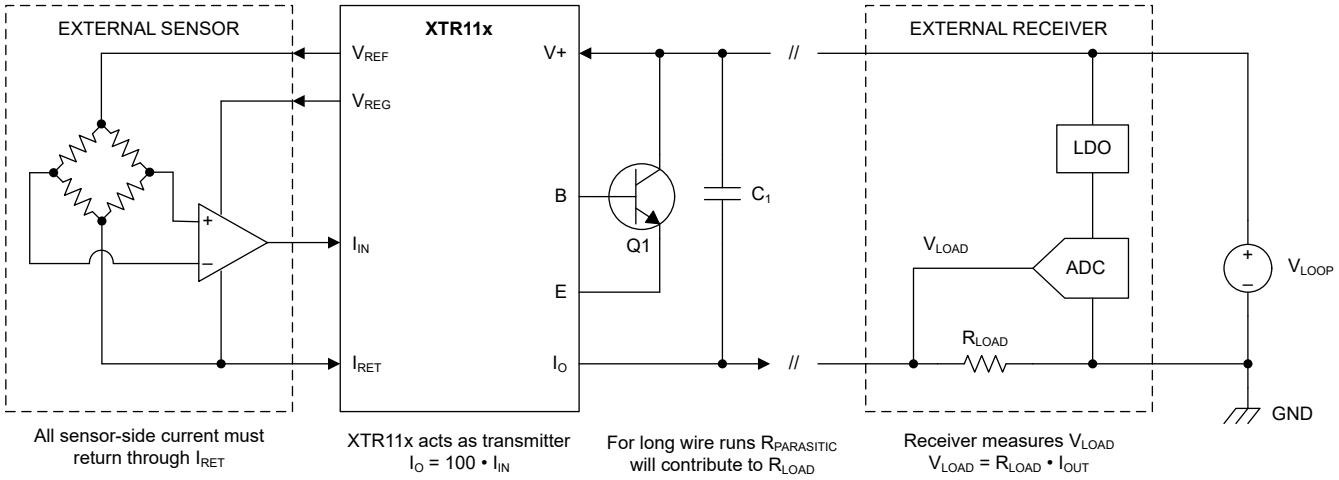
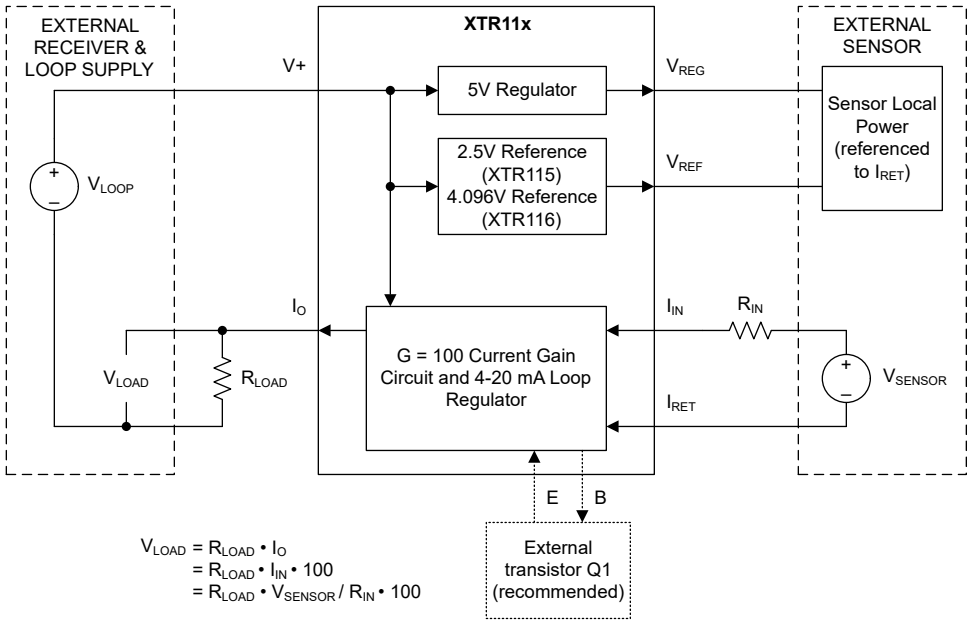


图 7-1. Typical Schematic

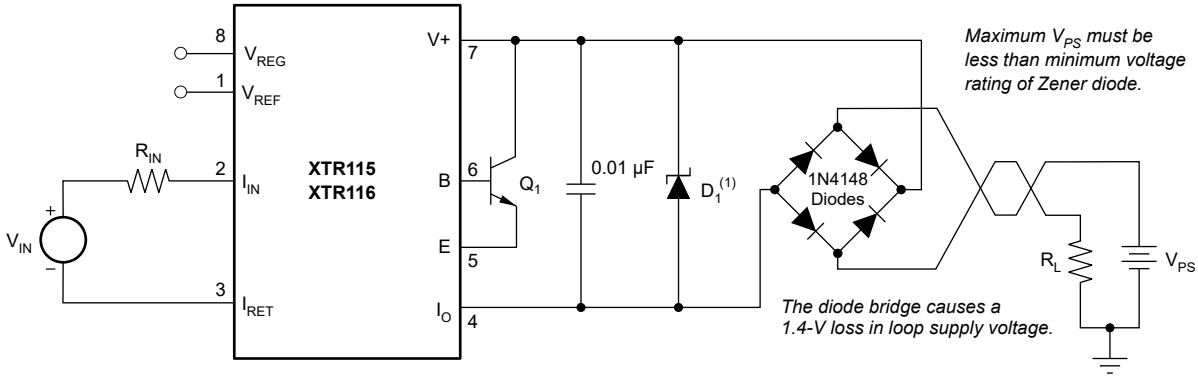
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reverse-Voltage Protection

The XTR11x low compliance voltage rating (7.5 V) permits the use of various voltage protection methods without compromising the operating range. 图 7-2 shows a diode bridge circuit that allows normal operation even when the voltage connection lines are reversed. The bridge causes a two-diode drop (approximately 1.4 V) loss in loop supply voltage. This loss results in a compliance voltage of approximately 9 V—satisfactory for most applications. A diode can be inserted in series with the loop supply voltage and the V+ pin to protect against reverse output connection lines with only a 0.7-V loss in loop supply voltage.



(1) Zener Diode 36 V: 1N4753A or Motorola P6KE39A. Use lower-voltage Zener diodes with loop power-supply voltages less than 30 V for increased protection; see 节 7.3.2.

图 7-2. Reverse Voltage Operation and Overvoltage Surge Protection

7.3.2 Overvoltage Surge Protection

Remote connections to current transmitters can sometimes be subjected to voltage surges. Best practice is to limit the maximum surge voltage applied to the XTR11x to as low as practical. Various Zener and surge clamping diodes are specially designed for this purpose. Select a clamp diode with as low a voltage rating as possible for best protection. For example, a 36-V protection diode provides proper transmitter operation at normal loop voltages, and also provides an appropriate level of protection against voltage surges. Characterization tests on several production lots showed no damage with loop supply voltages up to 65 V.

Most surge protection Zener diodes have a diode characteristic in the forward direction that conducts excessive current, possibly damaging receiving-side circuitry if the loop connections are reversed. If a surge protection diode is used, also use a series diode or diode bridge for protection against reversed connections.

8 Application and Implementation

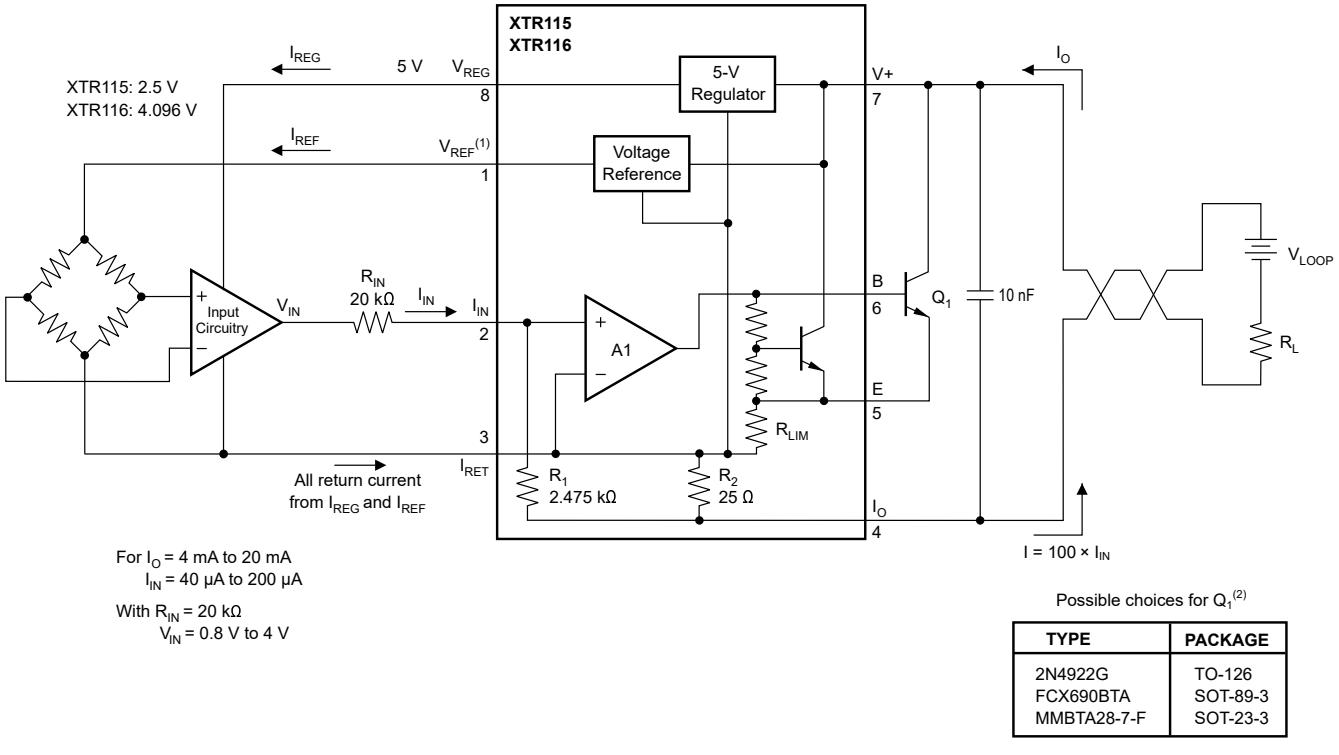
备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The XTR115 and XTR116 are identical devices except for the reference voltage output, pin 1. This voltage is available for external circuitry and is not used internally. Further discussions that apply to both devices refer to the XTR11x.

图 8-1 shows basic circuit connections with representative simplified input circuitry. The XTR11x is a two-wire current transmitter. The device input signal (pin 2) controls the output current. A portion of this current flows into the V+ power supply, pin 7. The remaining current flows in Q_1. External input circuitry connected to the XTR11x can be powered from VREG or VREF. Current drawn from these terminals must be returned to IRET, pin 3. This IRET pin is a *local ground* for input circuitry driving the XTR11x.



Possible choices for Q_1(2)

TYPE	PACKAGE
2N4922G	TO-126
FCX690BTA	SOT-89-3
MMBTA28-7-F	SOT-23-3

(1) Also see 图 8-4.
(2) See 节 8.1.1.

图 8-1. Basic Circuit Connections

The XTR11x is a current-input device with a gain of 100. A current flowing into pin 2 produces $I_O = 100 \cdot I_{IN}$. The input voltage at the I_{IN} pin is zero (referred to the I_{RET} pin). A voltage input is created with an external input resistor, as shown. Common full-scale input voltages range from 1 V and upward. Full-scale inputs greater than 0.5 V are recommended to minimize the effect of offset voltage and drift of A1.

8.1.1 External Transistor

The external transistor, Q_1, conducts the majority of the full-scale output current. Power dissipation in this transistor can approach 0.8 W with high loop voltage (40 V) and 20 mA of output current. The XTR11x is designed to use an external transistor to avoid on-chip, thermal-induced errors. Heat produced by Q_1 still causes ambient temperature changes that can affect the XTR11x. To minimize these effects, locate Q_1 away from sensitive analog circuitry, including the XTR11x. Mount Q_1 so that heat is conducted to the outside of the transducer housing and away from the XTR11x.

The XTR11x is designed to use virtually any NPN transistor with sufficient voltage, current, and power rating. Case style and thermal mounting considerations often influence the choice for any given application. Several possible choices are listed in 图 8-1. A MOSFET transistor does not improve the accuracy of the XTR11x and is not recommended. Although the XTR11x can be used without an additional external transistor, this configuration is not always practical at higher loop voltages and currents because of self-heating concerns.

8.1.2 Minimum Scale Current

The quiescent current of the XTR11x (typically 200 µA) is the lower limit of the device output current. Zero input current (I_{IN} = 0 A) produces an I_O equal to the quiescent current. Output current does not begin to increase until $I_{IN} > I_Q / 100$. Current drawn from V_{REF} or V_{REG} adds to this minimum output current. This means that more than 3.7 mA is available to power external circuitry while still allowing the output current to go below 4 mA.

8.1.3 Offsetting the Input

A low scale of 4 mA is produced by creating a 40-µA input current. This low-scale offset can be created with the proper value resistor from V_{REF} (as shown in 图 8-2, or by generating offset in the input drive circuitry.

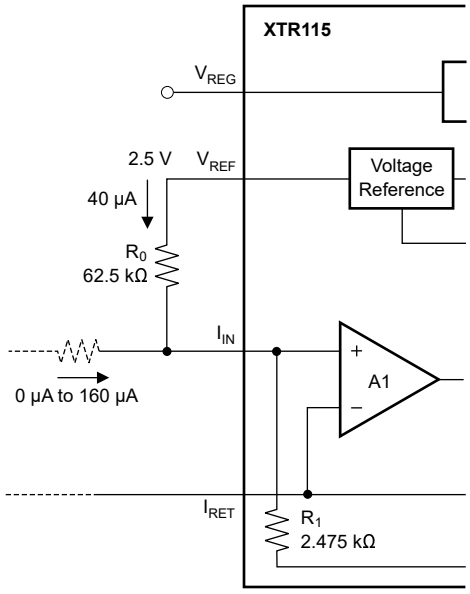


图 8-2. Creating Low-Scale Offset

8.1.4 Maximum Output Current

The XTR11x provide accurate, linear output up to 25 mA. Internal circuitry limits the output current to approximately 32 mA to protect the transmitter and loop power or measurement circuitry.

Extending the output current range of the XTR11x is possible by connecting an external resistor from pin 3 to pin 5 to change the current limit value.

CAUTION

All output current must flow through internal resistors; therefore, damage is possible with excessive current. Output currents greater than 45 mA can cause permanent damage.

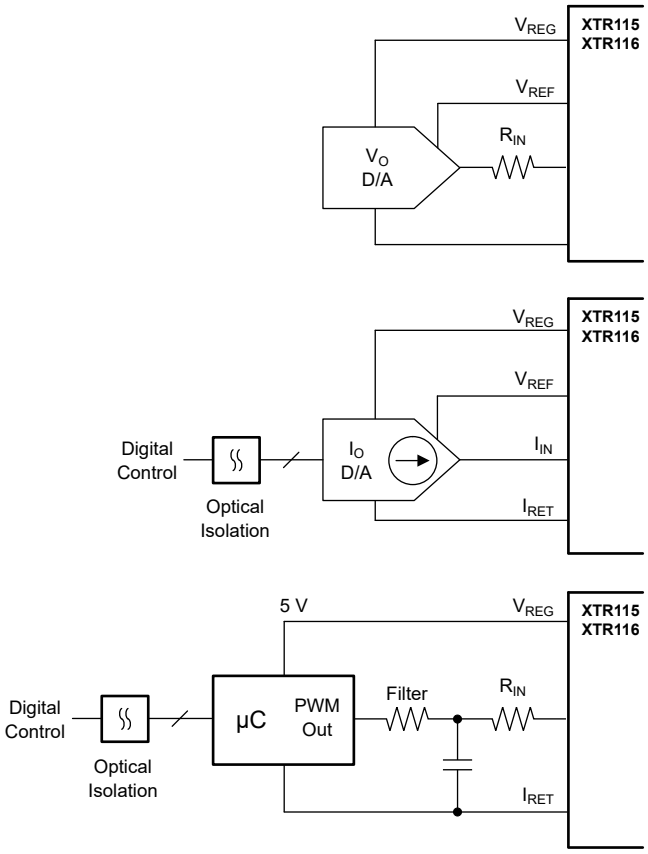


图 8-3. Digital Control Methods

8.1.5 Radio Frequency Interference

The long wire lengths of current loops invite radio frequency interference (RF). RF can be rectified by the input circuitry of the XTR11x or preceding circuitry. This RF generally appears as an unstable output current that varies with the position of loop supply or input wiring. Interference can also enter at the input pins. For integrated transmitter assemblies with short connection to the sensor, the interference more likely comes from the current-loop connections.

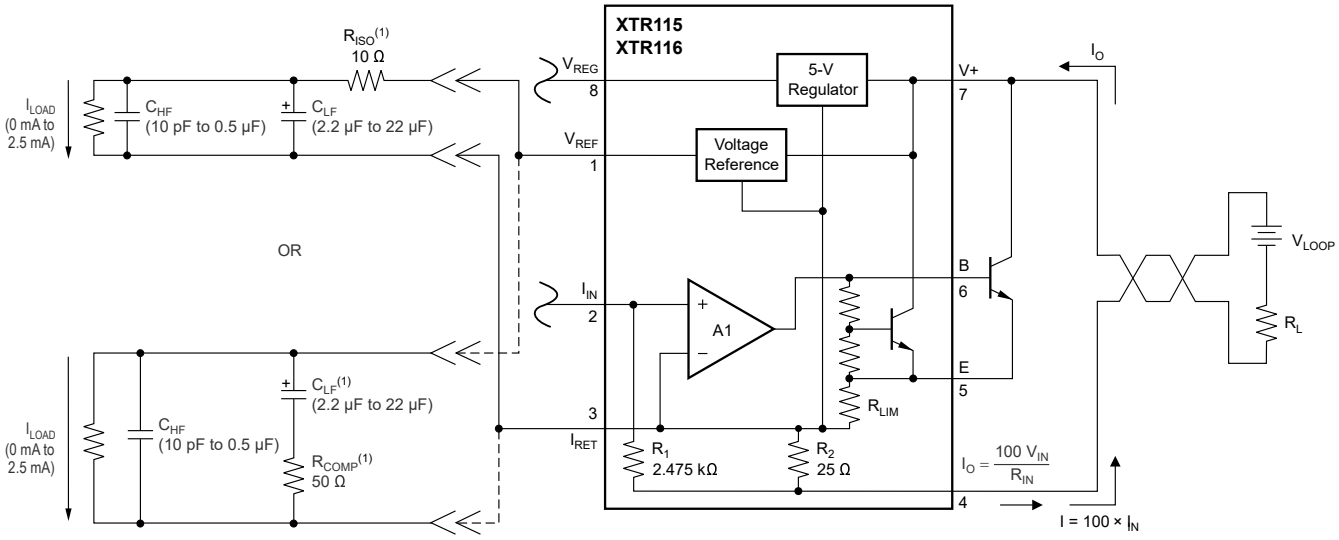
8.1.6 Circuit Stability

The 4-20 mA control-loop stability must be evaluated for any XTR11x design. A 10-nF decoupling capacitor between V+ and I_O is recommended for most applications. As this capacitance appears in parallel with the load resistance R_{LOAD} from a stability perspective, the capacitor and resistor form a filter corner that can limit the bandwidth of the system. Therefore, for HART applications, use a bypass capacitance of 2 nF to 3 nF instead.

For applications with EMI and EMC concerns, use a bypass capacitor with sufficiently low ESR to decouple any ripple voltage from the V_{LOOP} supply. Otherwise, the ripple voltage couples onto the 4-mA to 20-mA current source, and appears as noise across R_{LOAD} after the current-to-voltage conversion.

Additionally, stability concerns apply to the V_{REF} reference buffer when driving capacitive loads. 图 8-4 shows that two filtering capacitors are required, one C_{HF} of 10 pF to 0.5 µF and another C_{LF} of 2.2 µF to 22 µF. Either a series isolation resistance R_{ISO} or a snubber R_{COMP} is used, depending on application requirements.

If capacitive loading must be placed on the VREF pin, use one of the following compensation schemes to maintain stable operation. Values of capacitance must remain within the given ranges.



(1) Required compensation components.

图 8-4. Stable Operation With Capacitive Load on V_{REF}

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Special Function Amplifiers*: TI Precision Labs introduction video on Current Loop Transmitters
- Texas Instruments, *TIPD190* 2-wire, 4-20mA Transmitter, EMC/EMI Tested Reference Design with the XTR116

9.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTR115U	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	XTR 115U	
XTR115U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR 115U	Samples
XTR115UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR 115U A	Samples
XTR116U	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	XTR 116U	
XTR116U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR 116U	Samples
XTR116UA	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	XTR 116U A	
XTR116UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	XTR 116U A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

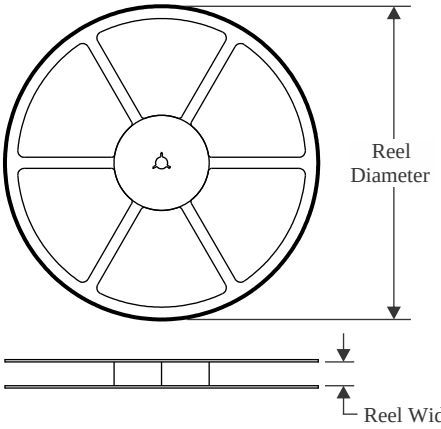
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

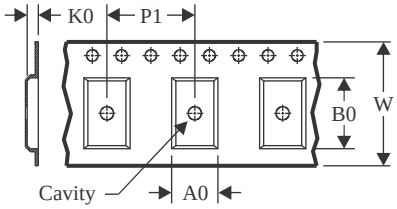
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

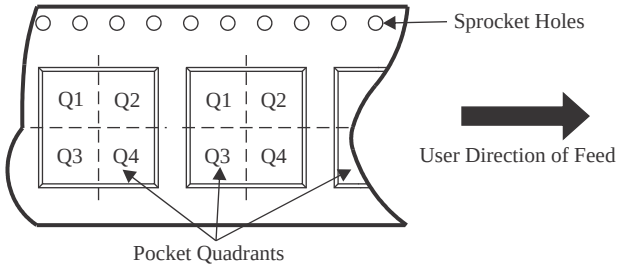


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

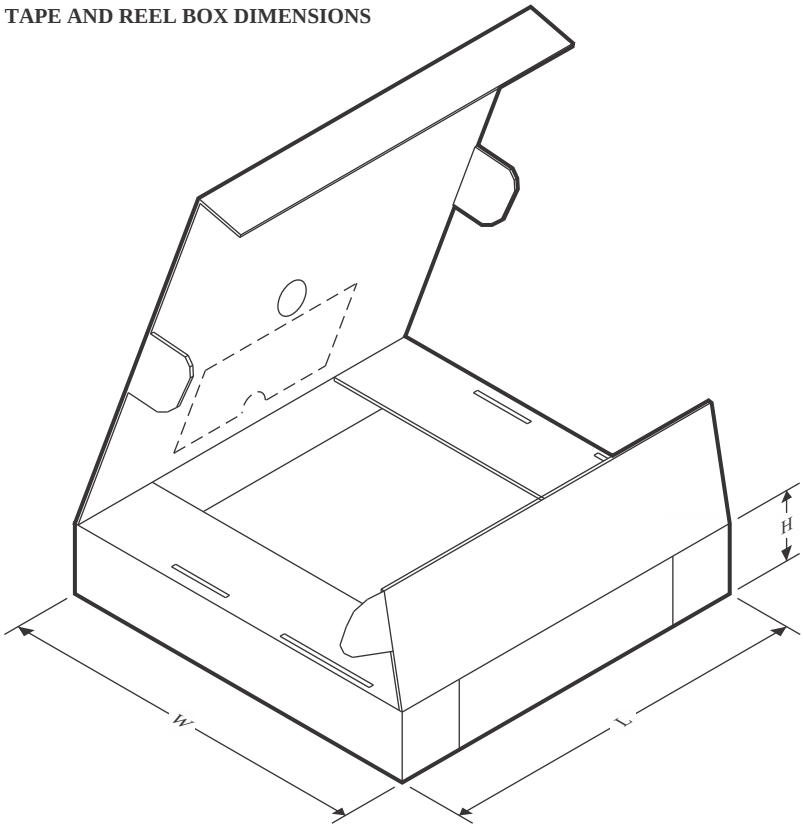
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

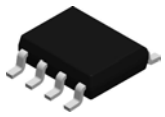
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR115U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR115U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR115UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR115UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR116U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR116U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR116UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
XTR116UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR115U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
XTR115U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
XTR115UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
XTR115UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
XTR116U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
XTR116U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
XTR116UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
XTR116UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0

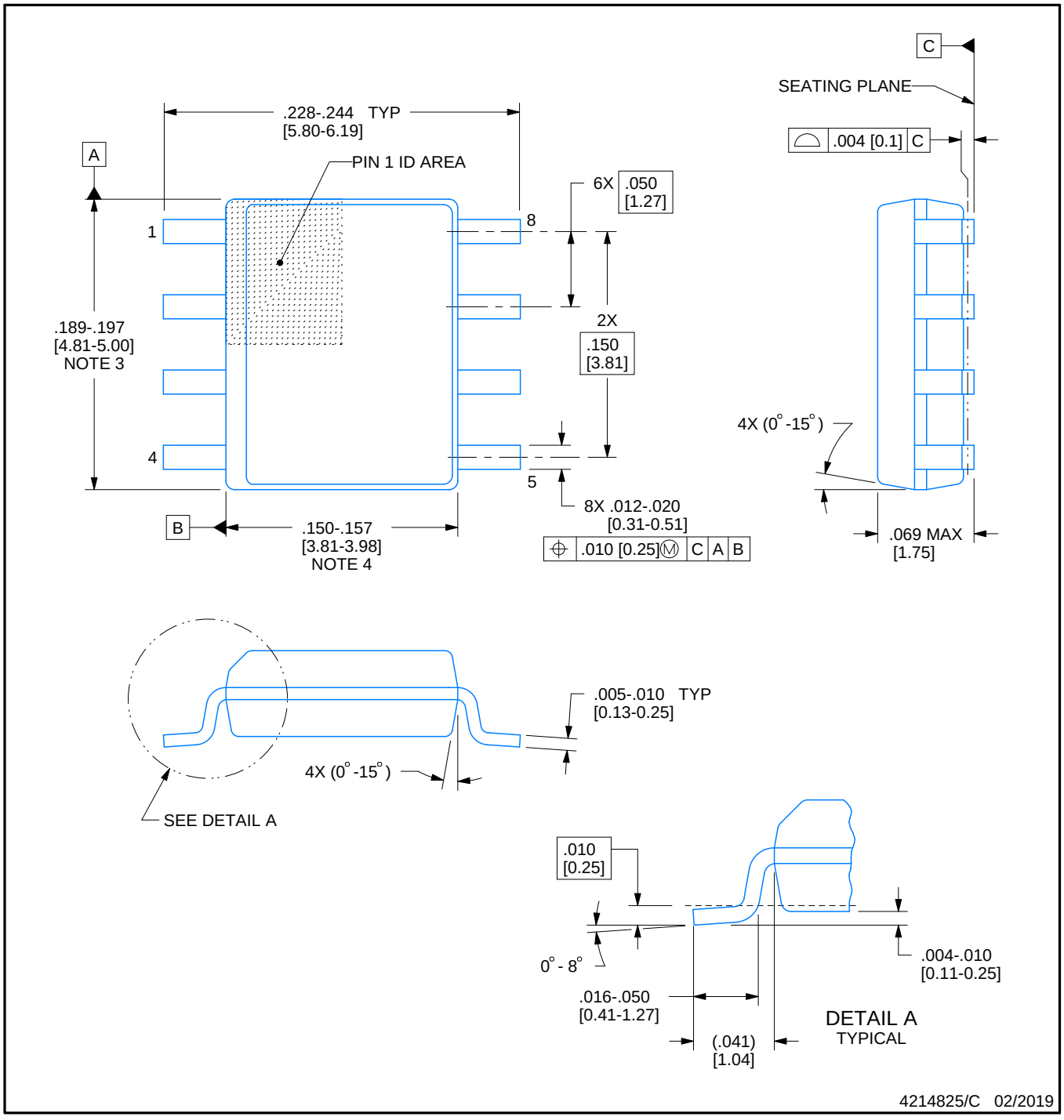


PACKAGE OUTLINE

D0008A

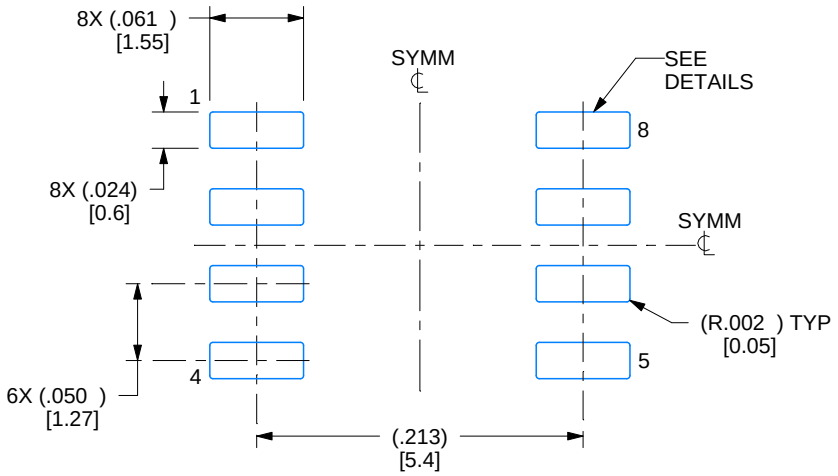
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

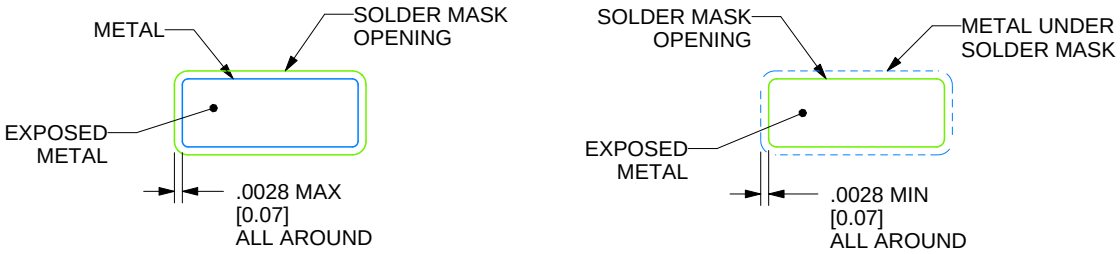


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

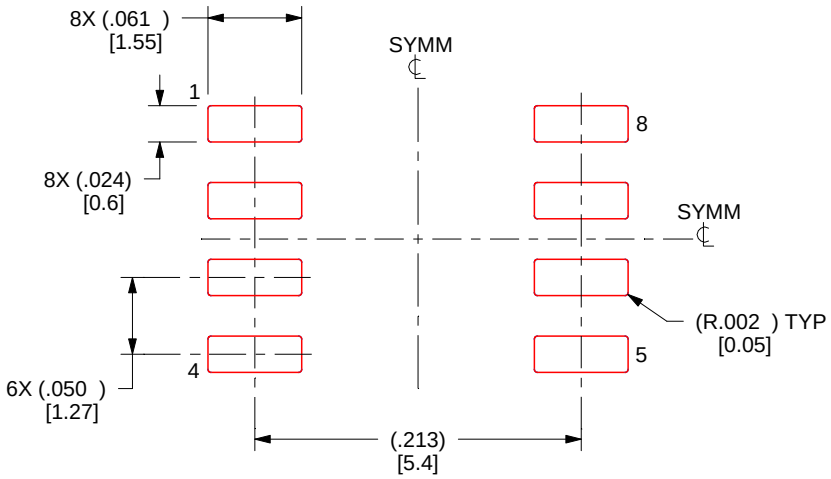
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265