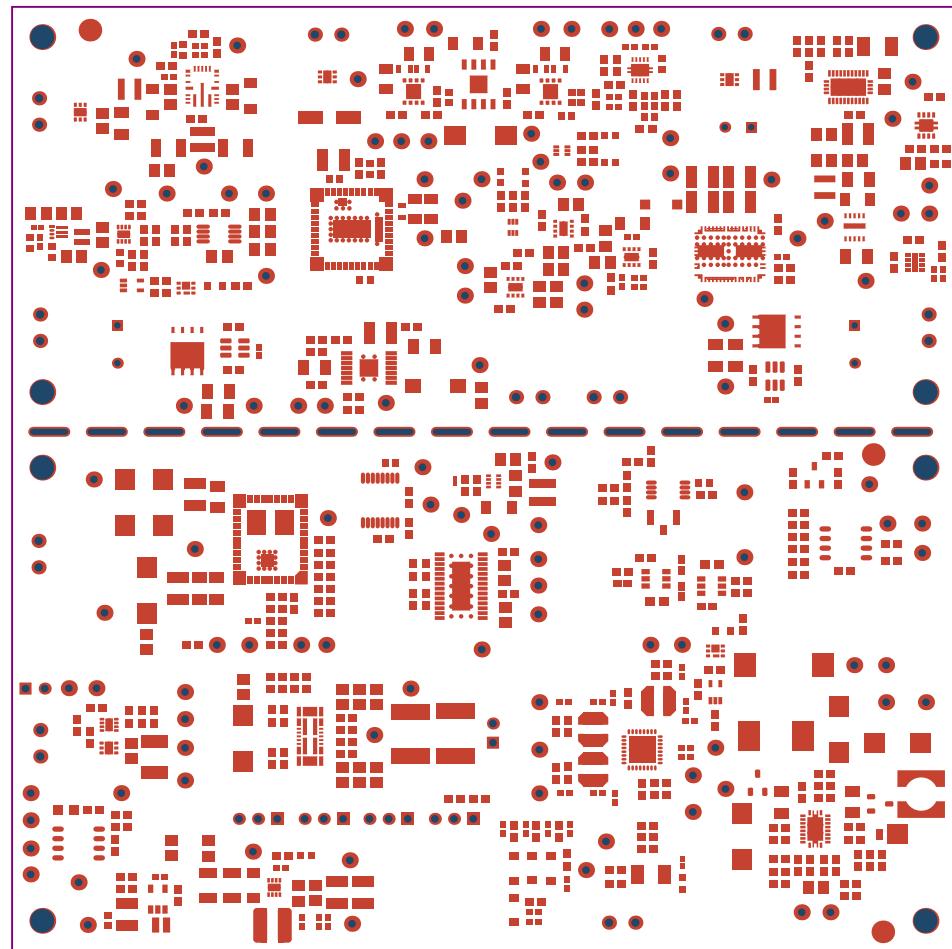
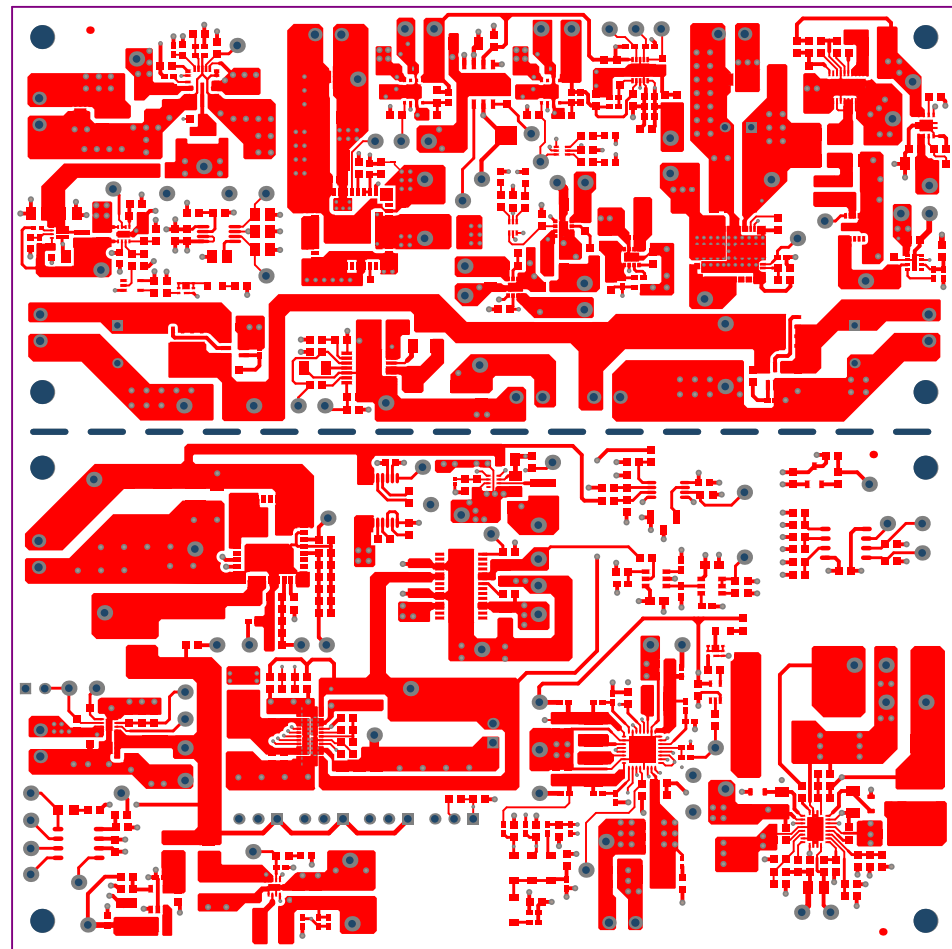


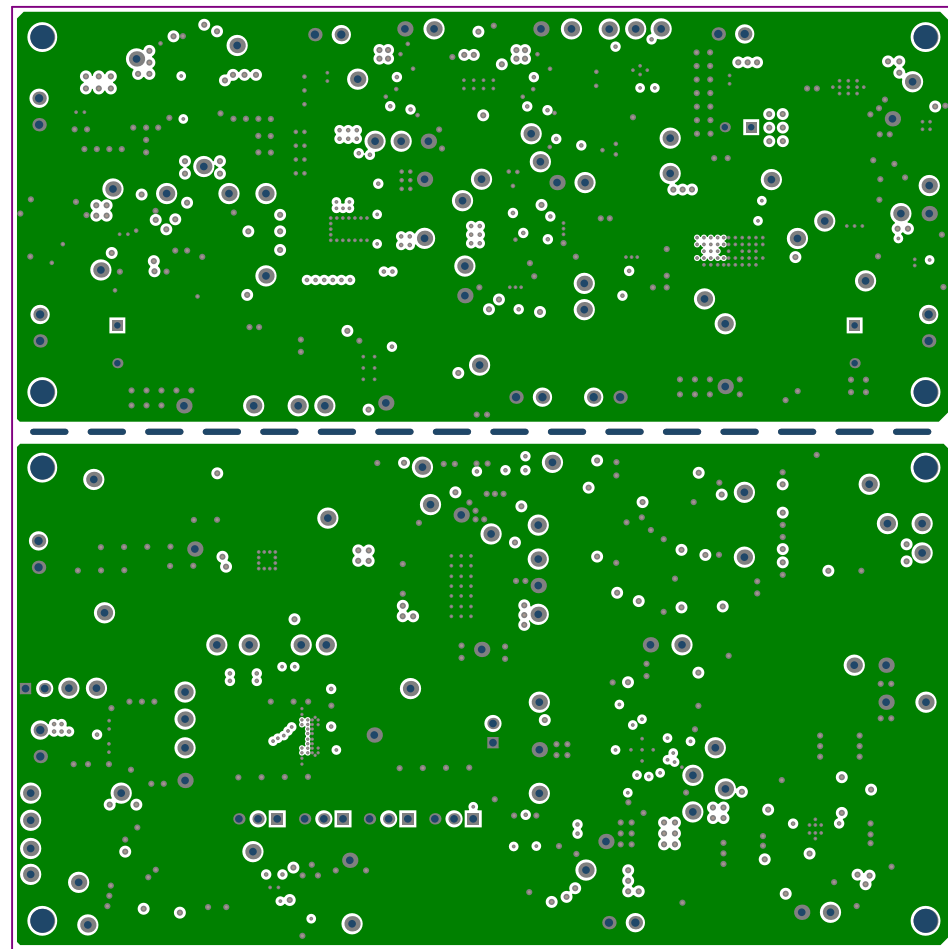
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010011-E1_Py_processor_Power	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Top Overlay	TID #: 010011		
PLOT NAME = Top Overlay	GENERATED : 10/18/2018 12:19:02 PM	TEXAS INSTRUMENTS	



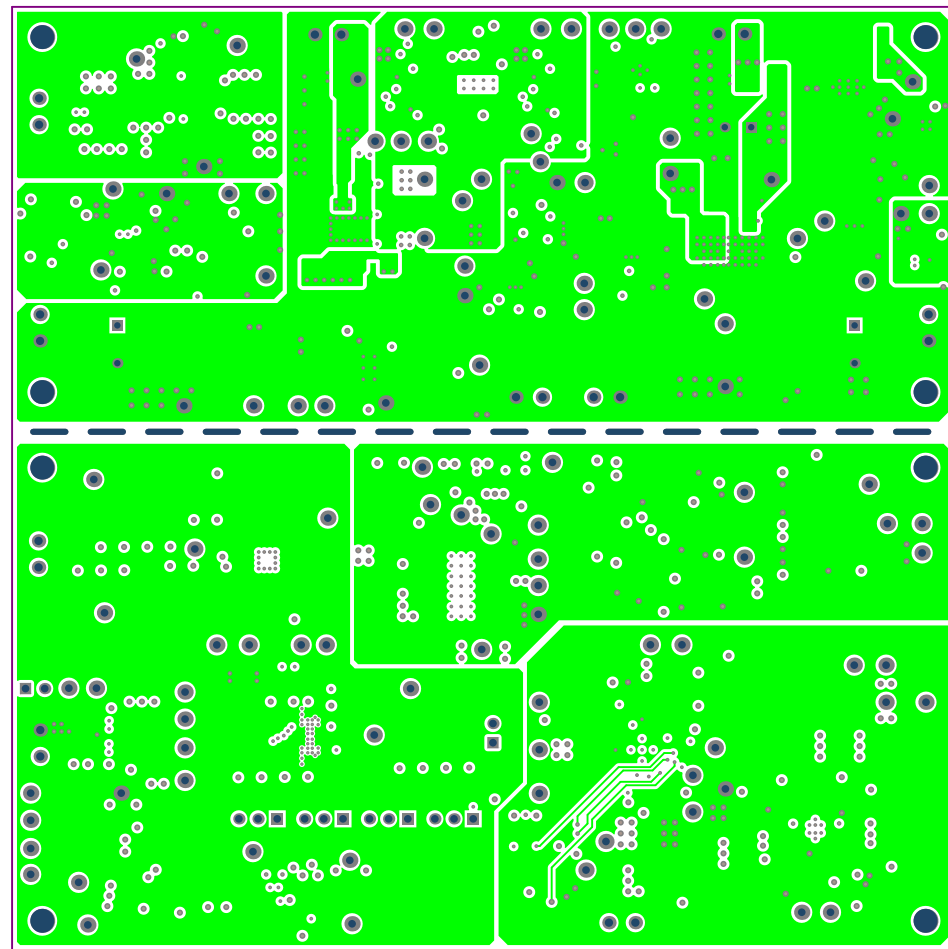
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDN-01001-E1_Processor_Power	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Top Solder	TID #: 010011		
PLOT NAME = Top Solder Mask	GENERATED : 10/18/2018 12:19:03 PM	TEXAS INSTRUMENTS	



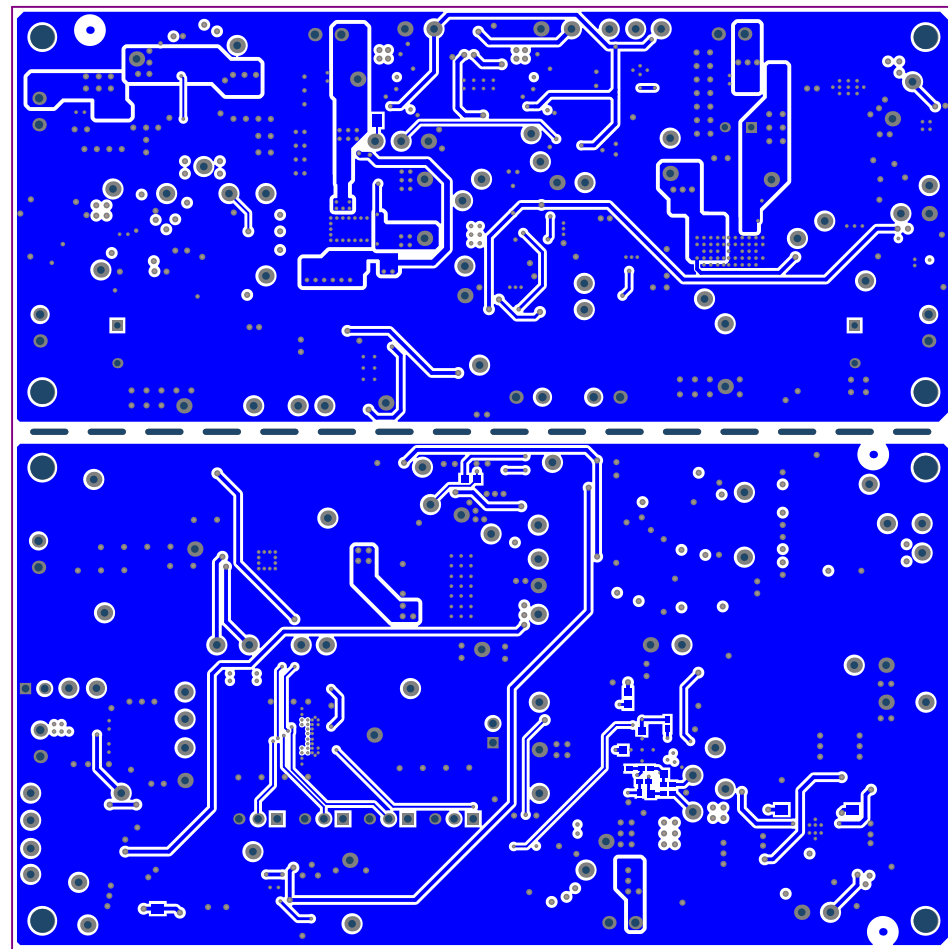
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDN-01001-E1_Processor_Power	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Top Layer	TID #: 010011		
PLOT NAME = Top Layer	GENERATED : 10/18/2018 12:19:03 PM		TEXAS INSTRUMENTS



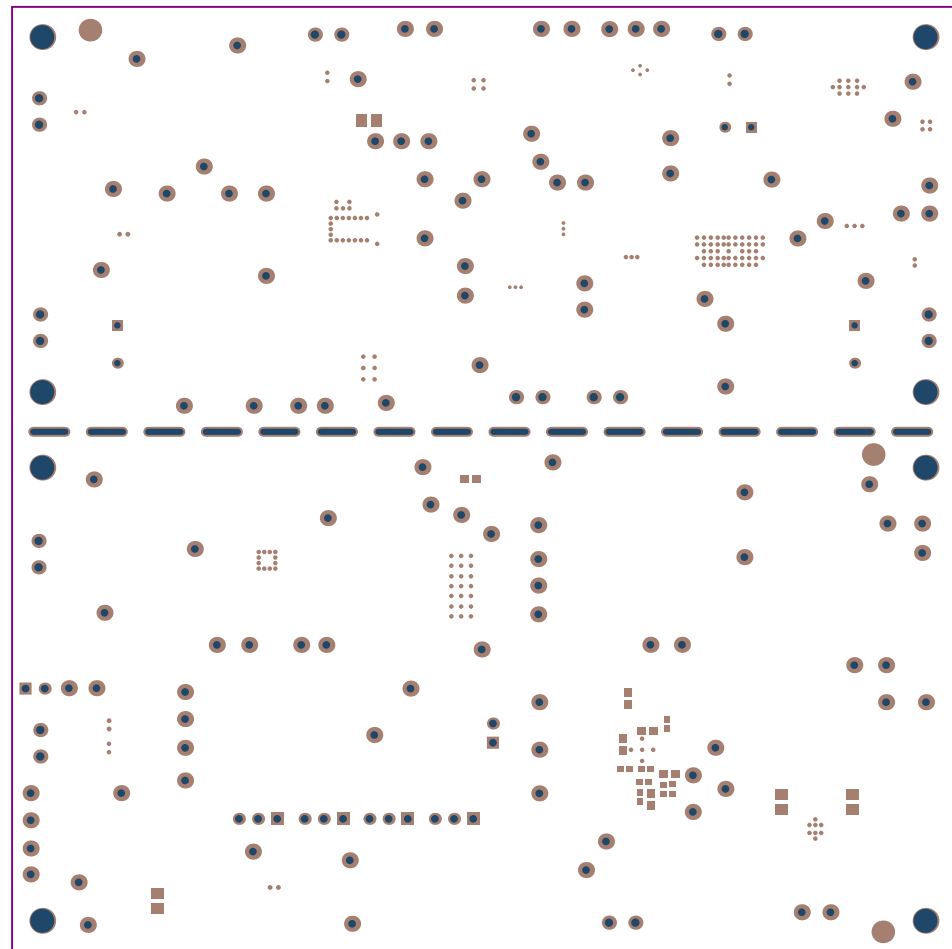
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDN-01001-E1_Processor_Power	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Gnd layer	TID #: 010011		
PLOT NAME = Signal Layer 1	GENERATED : 10/18/2018 12:19:04 PM	TEXAS INSTRUMENTS	



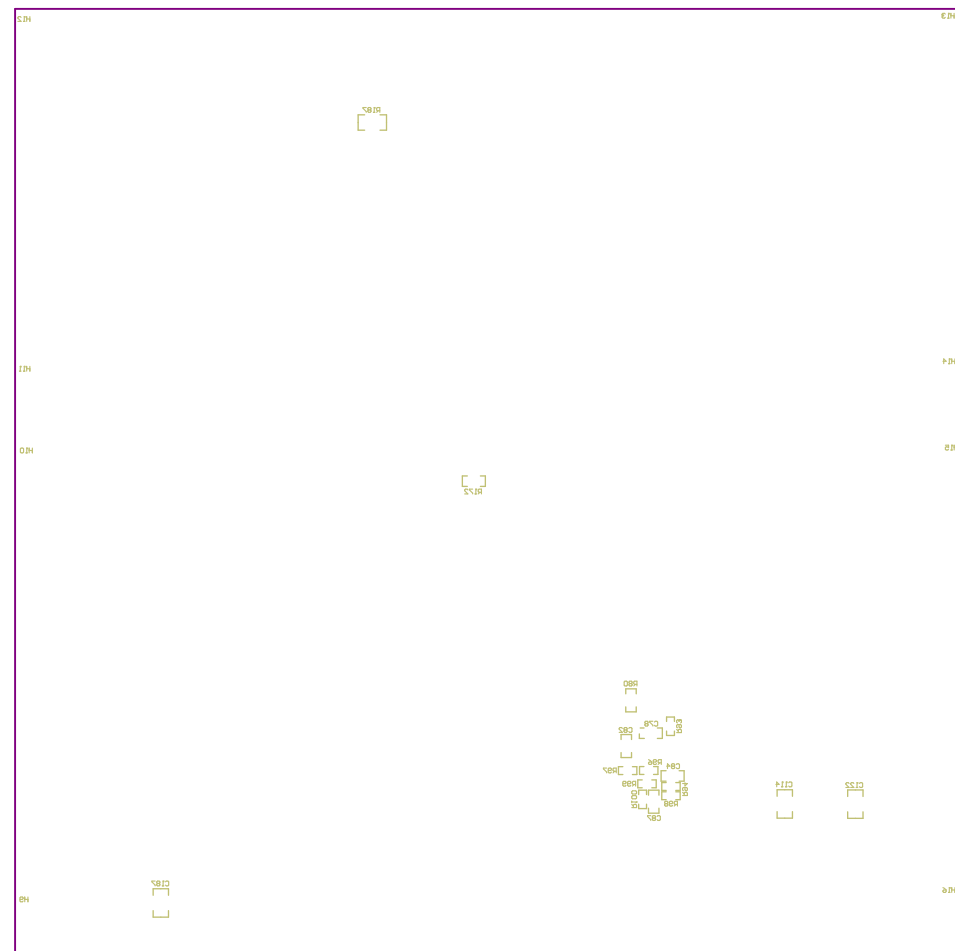
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDN-01001-E1_Processor_Power	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Gnd/Pwr layer	TID #: 010011		
PLOT NAME = Signal Layer 2	GENERATED : 10/18/2018 12:19:04 PM	TEXAS INSTRUMENTS	



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDN-01001-E1_Processor_Power	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Bottom Layer	TID #: 010011		
PLOT NAME = Bottom Layer	GENERATED : 10/18/2018 12:19:04 PM	TEXAS INSTRUMENTS	



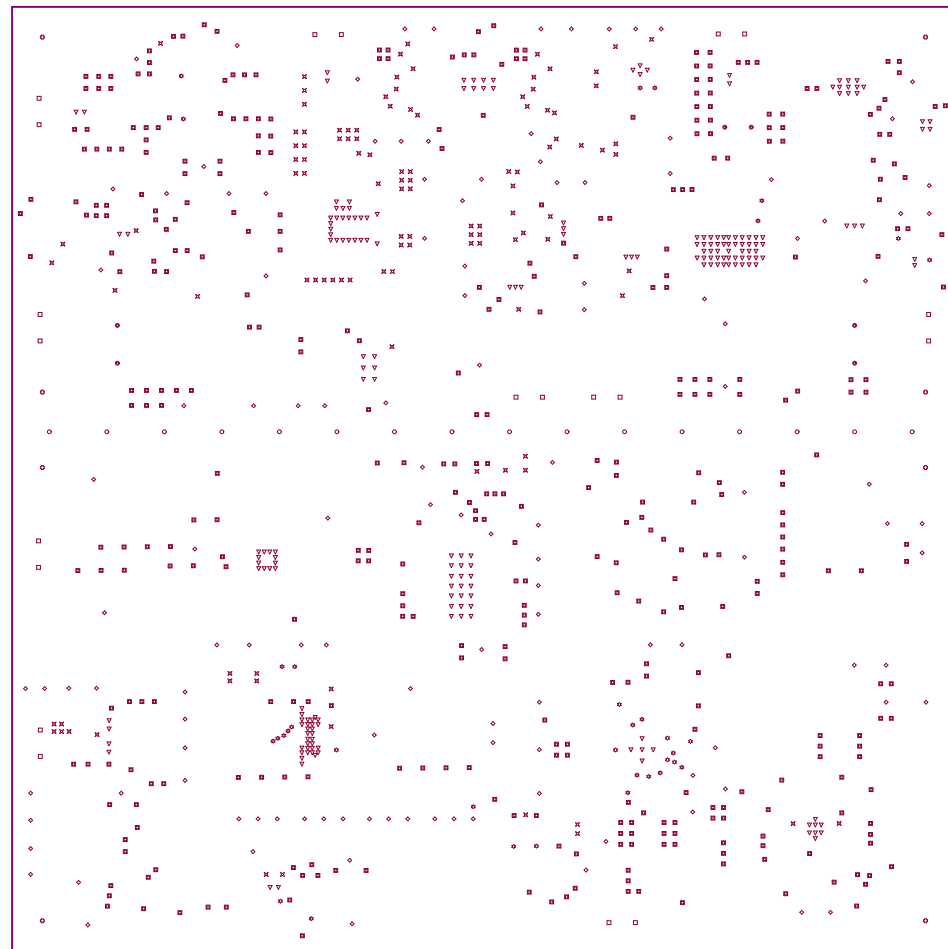
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDN-01001-E1_Processor_Power	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Bottom Solder	TID #: 010011		
PLOT NAME = Bottom Solder Mask	GENERATED : 10/18/2018 12:19:04 PM	TEXAS INSTRUMENTS	



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDN-01001-E1_Processor_Power	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Bottom Overlay	TID #: 010011		
PLOT NAME = Bottom Overlay	GENERATED : 10/18/2018 12:19:04 PM	TEXAS INSTRUMENTS	

Symbol	Count	Hole Size	Plated	Hole Type	Hole Length
▽	210	7.87mil (0.200mm)	PTH	Round	-
☆	35	8.00mil (0.203mm)	PTH	Round	-
✕	112	12.00mil (0.305mm)	PTH	Round	-
■	400	16.00mil (0.406mm)	PTH	Round	-
○	16	32.00mil (0.813mm)	NPTH	Slot	200.00mil (5.080mm)
⊙	6	33.47mil (0.850mm)	PTH	Round	-
◇	127	40.00mil (1.016mm)	PTH	Round	-
□	20	43.31mil (1.100mm)	PTH	Round	-
⊕	8	125.00mil (3.175mm)	NPTH	Round	-
	934 Total				

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout



Drill Table
 FOR 7.874MIL DRILL +0/-7.874MIL
 FOR 8MIL DRILL +0/-8MIL
 FOR 12MIL DRILL +0/-12MIL
 FOR 16MIL DRILL +0/-16MIL
 FOR PTH DRILL +/-3MIL
 FOR NPTH DRILL +/-2MIL

Note:-
7.874MIL Vias alone are not tented.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.30mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4 High Tg	16.00mil	4.2	
5	Gnd layer	Copper	1.42mil		
6	Dielectric 2	FR-4 High Tg	25.00mil	4.5	
7	Gnd/Pwr layer	Copper	1.42mil		
8	Dielectric 3	FR-4 High Tg	16.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.30mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)
125MM X 125MM

Number of Layers : 4
 MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 5.9 MIL
 MIN. VIA DRILL SIZE: 7.874 MIL

MINIMUM ANNULAR RING 4.925MIL EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 63 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

COPPER THICKNESS (FINISHED):
 OUTER: 1.4MIL (1oz) 2MIL (1.4oz) 2.8MIL (2oz)
 INNER SIGNAL: 1.4MIL (1oz) 2.8MIL (2oz) N/A

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL_FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR:
 GREEN BLUE OTHER _____

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRIM PER MECH LAYER 1
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS: VIA TENTING: YES NO
 MICROSECTION: YES IMPEDANCE CONTROL: YES NO
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK



PROJECT TITLE:
TIDA-010011-E1_Processor_Power

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-010011-E1_Processor_Power.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDN-010011-E1_Processor_Power	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Drill Drawing	TID #: 010011		
PLOT NAME = Drill Drawing	GENERATED : 10/18/2018 12:19:05 PM	TEXAS INSTRUMENTS	

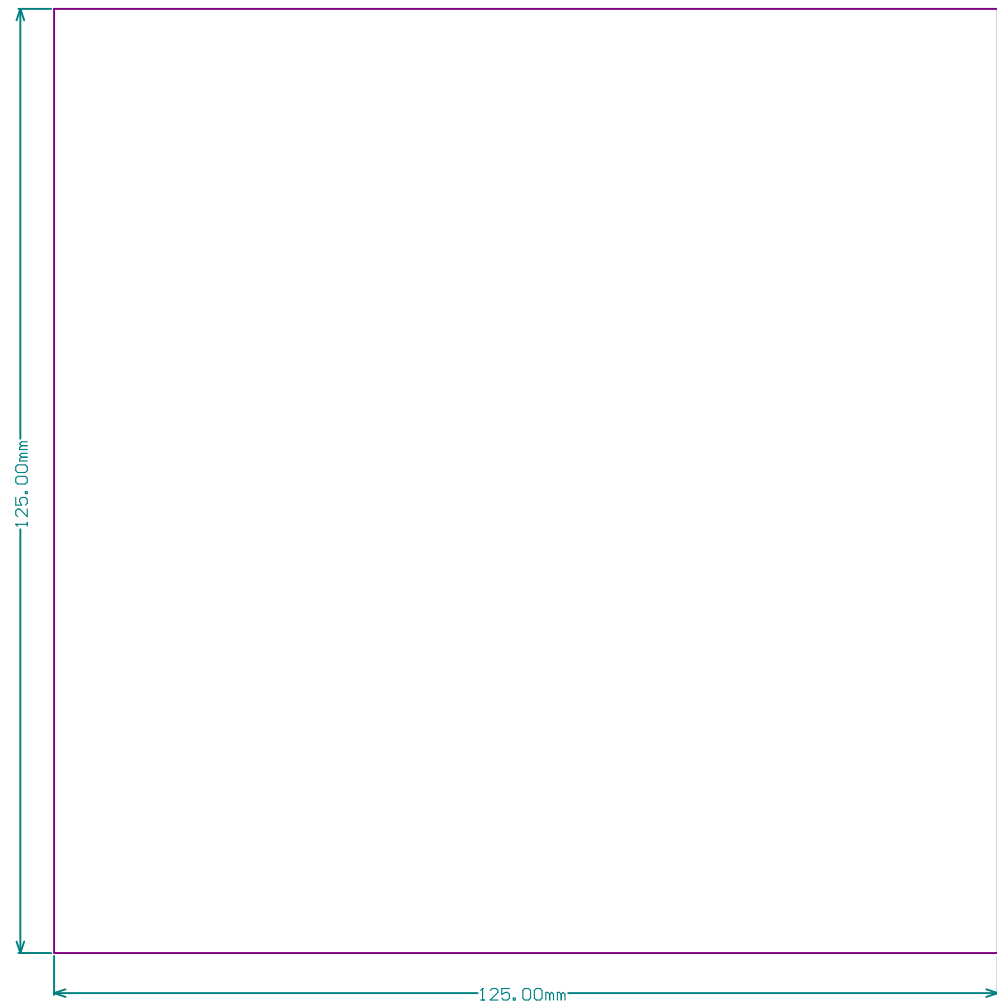
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ENGINEER:
Greenivasa

LAYOUT BY:
Avinash N

SCALE: 1.00

ALTIM DESIGNER VERSION:
17.1.9.592



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDN-01001-E1_Processor_Power	REV: E1	SUN REV: Not In VersionControl
LAYER NAME =	TID #: 010011		
PLOT NAME = Board Dimensions	GENERATED : 10/18/2018 12:19:06 PM	TEXAS INSTRUMENTS	

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