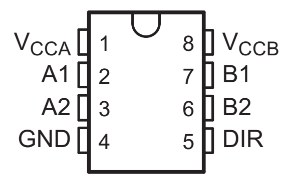
DUAL-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

Check for Samples: SN74AVC2T45-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range**
- **I/Os Are 4.6-V Tolerant**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Max Data Rates**
  - **500 Mbps (1.8-V to 3.3-V Translation)**
  - **320 Mbps (<1.8-V to 3.3-V Translation)**
  - **320 Mbps (Translate to 2.5 V or 1.8 V)**
  - **280 Mbps (Translate to 1.5 V)**
  - **240 Mbps (Translate to 1.2 V)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **8000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DCU PACKAGE
(TOP VIEW)



DESCRIPTION

This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVC2T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The SN74AVC2T45 is designed so that the DIR input is powered by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are in the high-impedance state.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	VSSOP – DCU	Reel of 3000	CAVC2T45TDCURQ1	SBUI

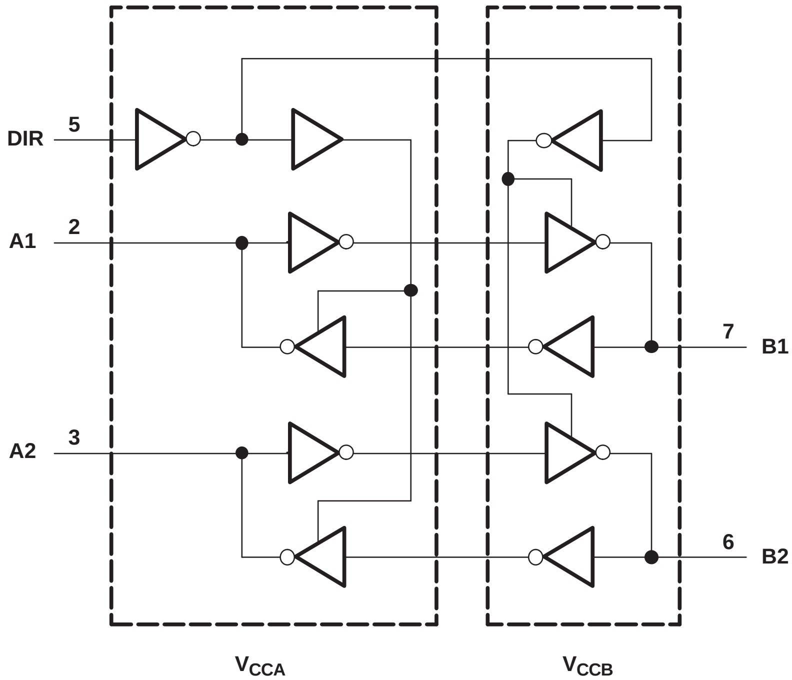
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE(1)
(EACH TRANSCEIVER)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range[2]	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state[2] [3]	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
θ_{JA}	Package thermal impedance[4]	DCU package		227	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current ratings are observed.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS[(1)(2)(3)(4)(5)]

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs[(4)]	1.2 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs[(4)]	1.2 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})[(5)]	1.2 V to 1.95 V		V_{CCA} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})[(5)]	1.2 V to 1.95 V			V_{CCA} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	105	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

ELECTRICAL CHARACTERISTICS(1)(2)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	–40°C to 105°C MIN	–40°C to 105°C MAX	UNIT
V_{OH}		I_{OH} = –100 μA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				V_{CCO} – 0.2 V		V
		I_{OH} = –3 mA		1.2 V	1.2 V		0.95				
		I_{OH} = –6 mA		1.4 V	1.4 V				1.05		
		I_{OH} = –8 mA		1.65 V	1.65 V				1.2		
		I_{OH} = –9 mA		2.3 V	2.3 V				1.75		
		I_{OH} = –12 mA		3 V	3 V				2.3		
V_{OL}		I_{OL} = 100 μA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V		0.25				
		I_{OL} = 6 mA		1.4 V	1.4 V					0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V					0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V					0.55	
		I_{OL} = 12 mA		3 V	3 V					0.7	
I_I	DIR	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	μA
I_{off}	A port	V_I or V_O = 0 to 3.6 V		0 V	0 to 3.6 V		±0.1	±1		±5	μA
	B port			0 to 3.6 V	0 V		±0.1	±1		±5	
I_{OZ}	B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND		0 V	3.6 V		±0.5	±2.5		±5	μA
	A port			3.6 V	0 V		±0.5	±2.5		±5	
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					10	μA
				0 V	3.6 V					–2	
				3.6 V	0 V					10	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					10	μA
				0 V	3.6 V					10	
				3.6 V	0 V					–2	
$I_{CCA} + I_{CCB}$ (see Table 1)		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					20	μA
C_I	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		2.5				pF
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V		6				pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V	V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	3.1	2.6	2.4	2.2	2.2	ns
t_{PHL}			3.1	2.6	2.4	2.2	2.2	
t_{PLH}	B	A	3.4	3.1	3	2.9	2.9	ns
t_{PHL}			3.4	3.1	3	2.9	2.9	
t_{PHZ}	DIR	A	5.2	5.2	5.1	5	4.8	ns
t_{PLZ}			5.2	5.2	5.1	5	4.8	
t_{PHZ}	DIR	B	5	4	3.8	2.8	3.2	ns
t_{PLZ}			5	4	3.8	2.8	3.2	
t_{PZH} (1)	DIR	A	8.4	7.1	6.8	5.7	6.1	ns
t_{PZL} (1)			8.4	7.1	6.8	5.7	6.1	
t_{PZH} (1)	DIR	B	8.3	7.8	7.5	7.2	7	ns
t_{PZL} (1)			8.3	7.8	7.5	7.2	7	

(1) The enable time is a calculated value, derived using the formula shown in the enable times section.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.8	0.7	5.6	0.5	4.8	0.4	3.9	0.3	3.7	ns
t_{PHL}			2.8	0.7	5.6	0.5	4.8	0.4	3.9	0.3	3.7	
t_{PLH}	B	A	2.7	0.8	5.6	0.7	5.4	0.6	5.1	0.5	4.9	ns
t_{PHL}			2.7	0.8	5.6	0.7	5.4	0.6	5.1	0.5	4.9	
t_{PHZ}	DIR	A	3.9	1.3	8.7	1.3	8	1.1	7.9	1.4	7.8	ns
t_{PLZ}			3.9	1.3	8.7	1.3	8	1.1	7.9	1.4	7.8	
t_{PHZ}	DIR	B	4.7	1.1	7.2	1.4	7.1	1.2	7.1	1.7	7.3	ns
t_{PLZ}			4.7	1.1	7.2	1.4	7.1	1.2	7.1	1.7	7.3	
t_{PZH} (1)	DIR	A	7.4		12.6		12.3		12		12	ns
t_{PZL} (1)			7.4		12.6		12.3		12		12	
t_{PZH} (1)	DIR	B	6.7		14.1		12.6		11.6		11.3	ns
t_{PZL} (1)			6.7		14.1		12.6		11.6		11.3	

(1) The enable time is a calculated value, derived using the formula shown in the enable times section.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.7	0.5	5.4	0.4	4.5	0.2	3.6	0.2	3.3	ns
t_{PHL}			2.7	0.5	5.4	0.4	4.5	0.2	3.6	0.2	3.3	
t_{PLH}	B	A	2.4	0.7	4.9	0.5	4.6	0.5	4.2	0.4	4	ns
t_{PHL}			2.4	0.7	4.9	0.5	4.6	0.5	4.2	0.4	4	
t_{PHZ}	DIR	A	3.7	1.3	8.3	0.7	7.1	1.4	5.5	1.1	5.4	ns
t_{PLZ}			3.7	1.3	8.3	0.7	7.1	1.4	5.5	1.1	5.4	
t_{PHZ}	DIR	B	4.4	1.3	6	1.3	6.1	0.8	5.9	1.5	6.1	ns
t_{PLZ}			4.4	1.3	6	1.3	6.1	0.8	5.9	1.5	6.1	
t_{PZH} (1)	DIR	A	6.8		10.7		10.5		9.9		9.9	ns
t_{PZL} (1)			6.8		10.7		10.5		9.9		9.9	
t_{PZH} (1)	DIR	B	6.4		13.5		11.4		8.9		8.5	ns
t_{PZL} (1)			6.4		13.5		11.4		8.9		8.5	

(1) The enable time is a calculated value, derived using the formula shown in the enable times section.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.6	0.4	5.1	0.2	4.2	0.2	3.2	0.2	2.8	ns
t_{PHL}			2.6	0.4	5.1	0.2	4.2	0.2	3.2	0.2	2.8	
t_{PLH}	B	A	2.1	0.6	4	0.5	3.6	0.4	3.2	0.3	3	ns
t_{PHL}			2.1	0.6	4	0.5	3.6	0.4	3.2	0.3	3	
t_{PHZ}	DIR	A	2.4	0.7	8.1	0.8	6.6	0.8	5.2	0.5	4.5	ns
t_{PLZ}			2.4	0.7	8.1	0.8	6.6	0.8	5.2	0.5	4.5	
t_{PHZ}	DIR	B	3.8	1	4.5	0.6	4.5	0.5	4.4	1.1	4.3	ns
t_{PLZ}			3.8	1	4.5	0.6	4.5	0.5	4.4	1.1	4.3	
t_{PZH} (1)	DIR	A	5.9		8.7		7.9		7.4		7.1	ns
t_{PZL} (1)			5.9		8.7		7.9		7.4		7.1	
t_{PZH} (1)	DIR	B	5		13		10.6		8.2		7.1	ns
t_{PZL} (1)			5		13		10.6		8.2		7.1	

(1) The enable time is a calculated value, derived using the formula shown in the enable times section.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.5	0.3	4.9	0.2	4	0.2	3	0.2	2.6	ns
t_{PHL}			2.5	0.3	4.9	0.2	4	0.2	3	0.2	2.6	
t_{PLH}	B	A	2.1	0.6	3.8	0.4	3.3	0.3	2.8	0.3	2.6	ns
t_{PHL}			2.1	0.6	3.8	0.4	3.3	0.3	2.8	0.3	2.6	
t_{PHZ}	DIR	A	2.9	1.1	8.2	1	6.7	1.3	4.9	1.2	4.2	ns
t_{PLZ}			2.9	1.1	8.2	1	6.7	1.3	4.9	1.2	4.2	
t_{PHZ}	DIR	B	3.4	0.5	6.8	0.3	5.8	0.3	4.8	1.1	4.4	ns
t_{PLZ}			3.4	0.5	6.8	0.3	5.8	0.3	4.8	1.1	4.4	
t_{PZH} (1)	DIR	A	5.5		10.4		8.9		7.4		6.8	ns
t_{PZL} (1)			5.5		10.4		8.9		7.4		6.8	
t_{PZH} (1)	DIR	B	5.4		12.9		10.5		7.7		6.6	ns
t_{PZL} (1)			5.4		12.9		10.5		7.7		6.6	

(1) The enable time is a calculated value, derived using the formula shown in the enable times section.

OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.2 V	V_{CCA} = V_{CCB} = 1.5 V	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns	3	3	3	3	4	pF
	B-port input, A-port output		12	13	13	14	15	
C_{pdB} (1)	A-port input, B-port output	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns	12	13	13	14	15	pF
	B-port input, A-port output		3	3	3	3	4	

(1) Power-dissipation capacitance per transceiver

Power-Up Considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

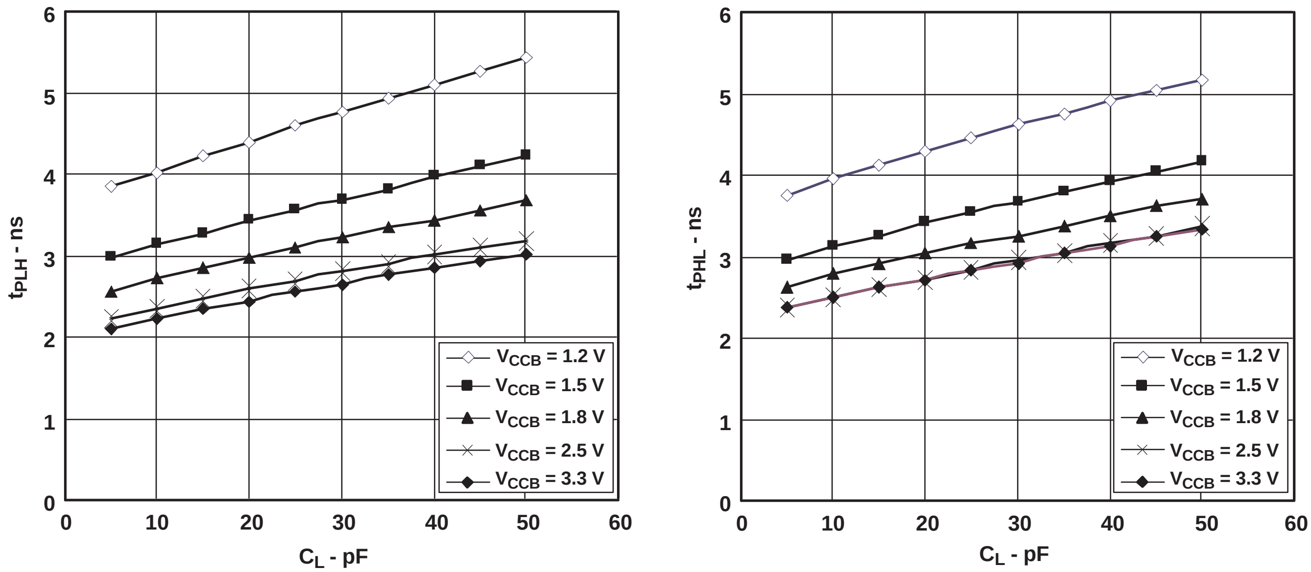
1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA}.
3. V_{CCB} can be ramped up along with or after V_{CCA}.

Table 1. Typical Total Static Power Consumption (I_{CCA} + I_{CCB})

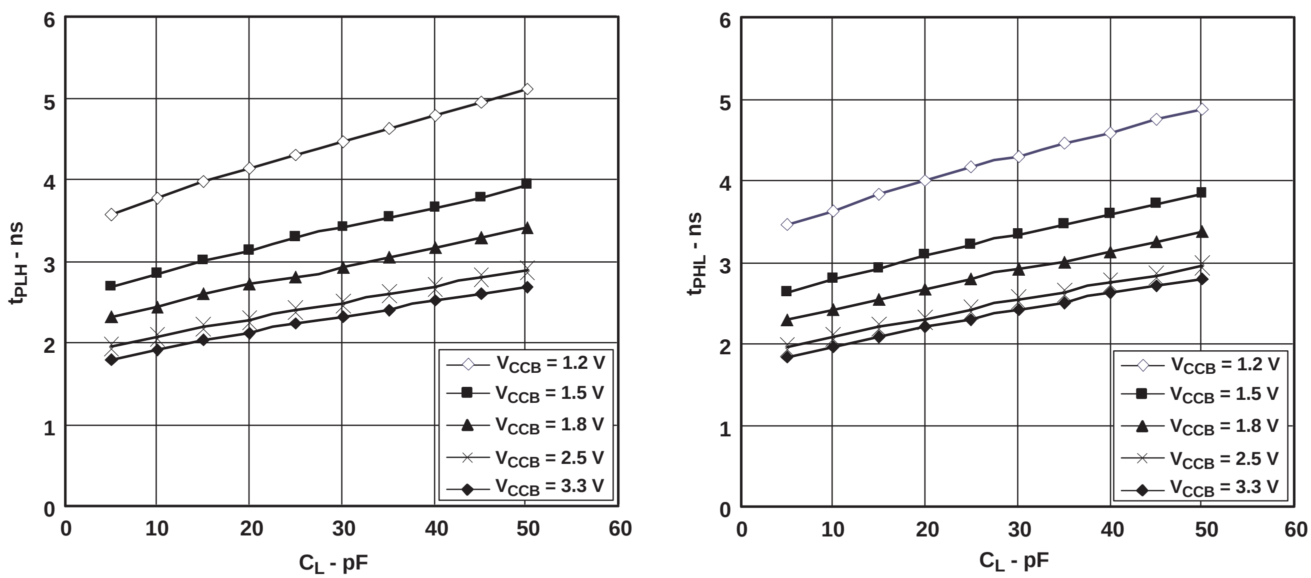
V_{CCB}	V_{CCA}						UNIT
	0 V	**1.2 V**	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5	μA
1.2 V	<0.5	<1	<1	<1	<1	1	
1.5 V	<0.5	<1	<1	<1	<1	1	
1.8 V	<0.5	<1	<1	<1	<1	<1	
2.5 V	<0.5	1	<1	<1	<1	<1	
3.3 V	<0.5	1	<1	<1	<1	<1	

TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, $T_A = 25°C$, $V_{CCA} = 1.2\ V$

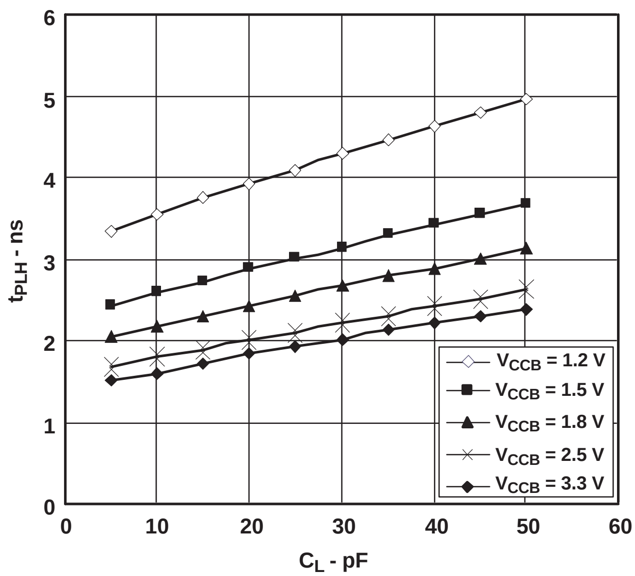


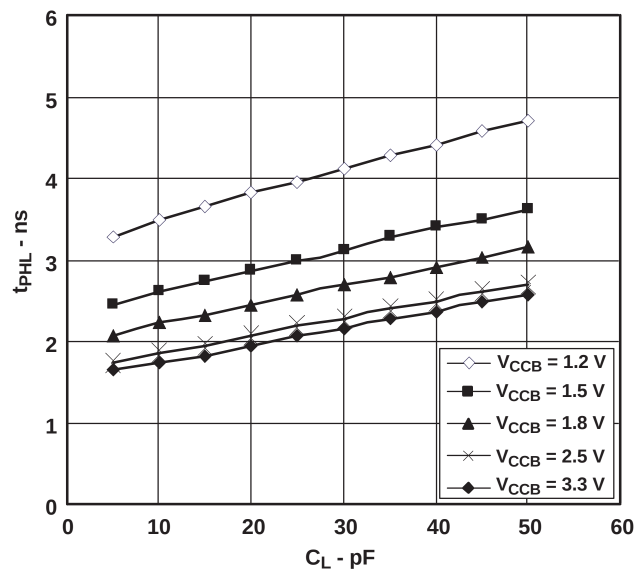
TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, $T_A = 25°C$, $V_{CCA} = 1.5\ V$



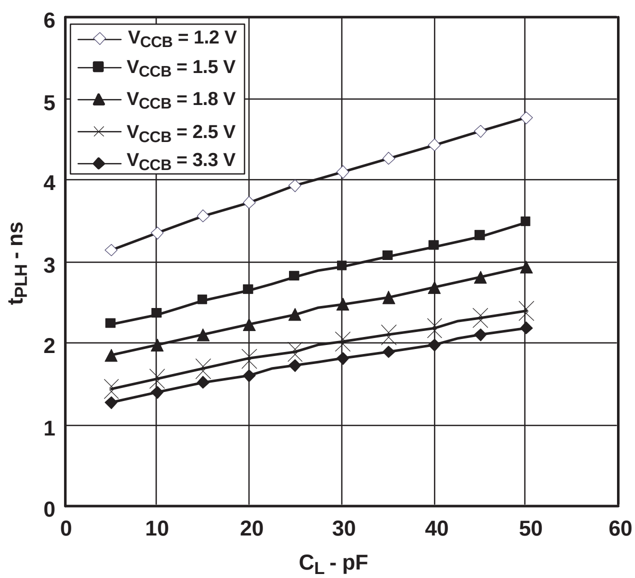
TYPICAL CHARACTERISTICS (continued)

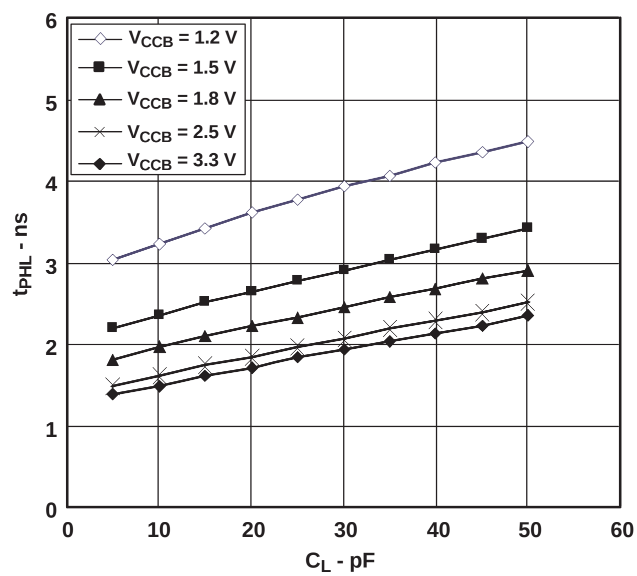
TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, T_A = 25°C, V_{CCA} = 1.8 V





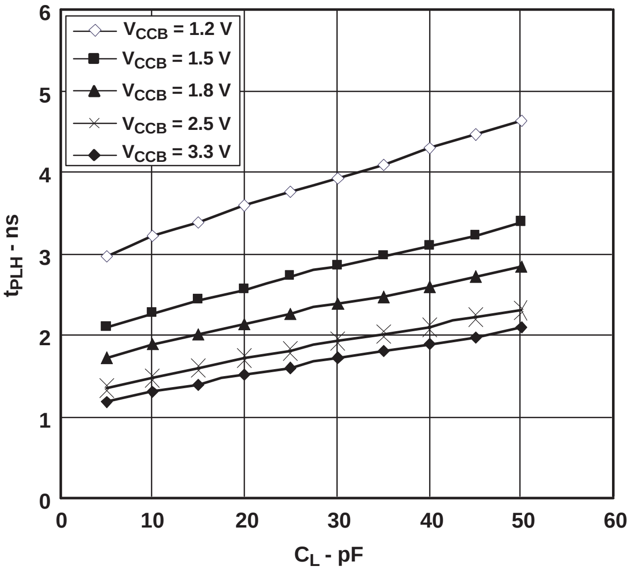
TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, T_A = 25°C, V_{CCA} = 2.5 V

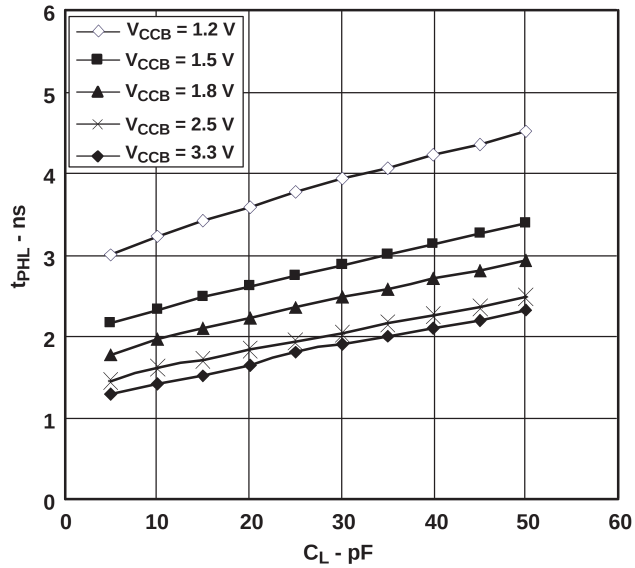




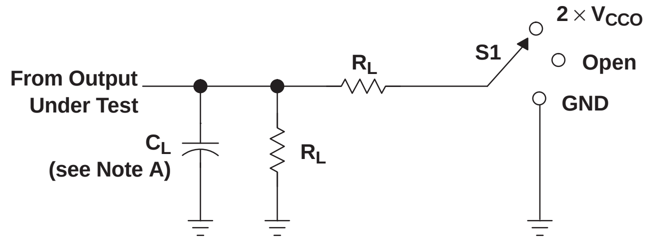
TYPICAL CHARACTERISTICS (continued)

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, $T_A = 25°C$, $V_{CCA} = 3.3\ V$





PARAMETER MEASUREMENT INFORMATION

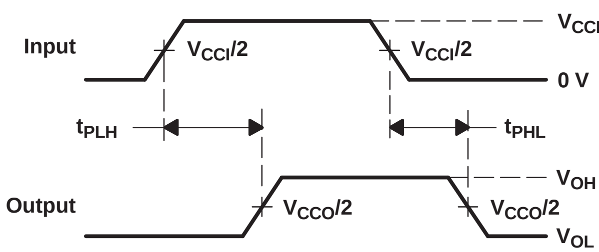


LOAD CIRCUIT

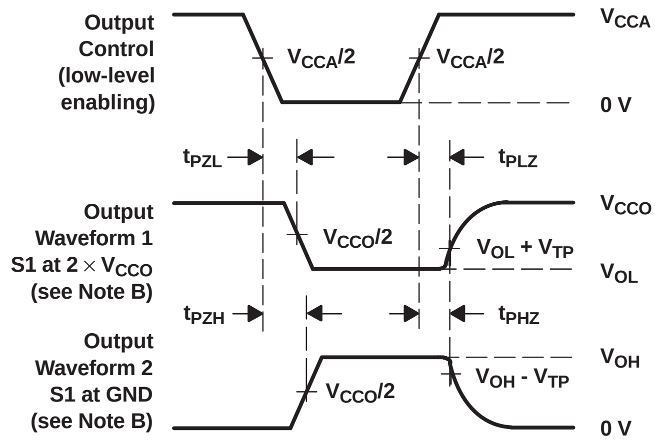
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

VOLTAGE WAVEFORMS
PULSE DURATION

V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



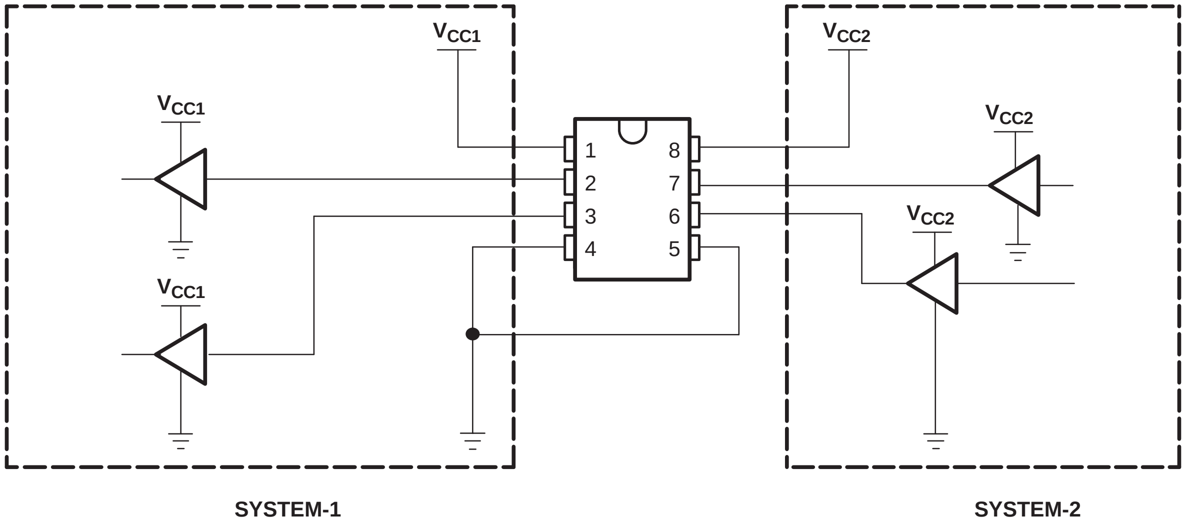
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Figure 2 is an example circuit of the SN74AVC2T45 used in a unidirectional logic level-shifting application.

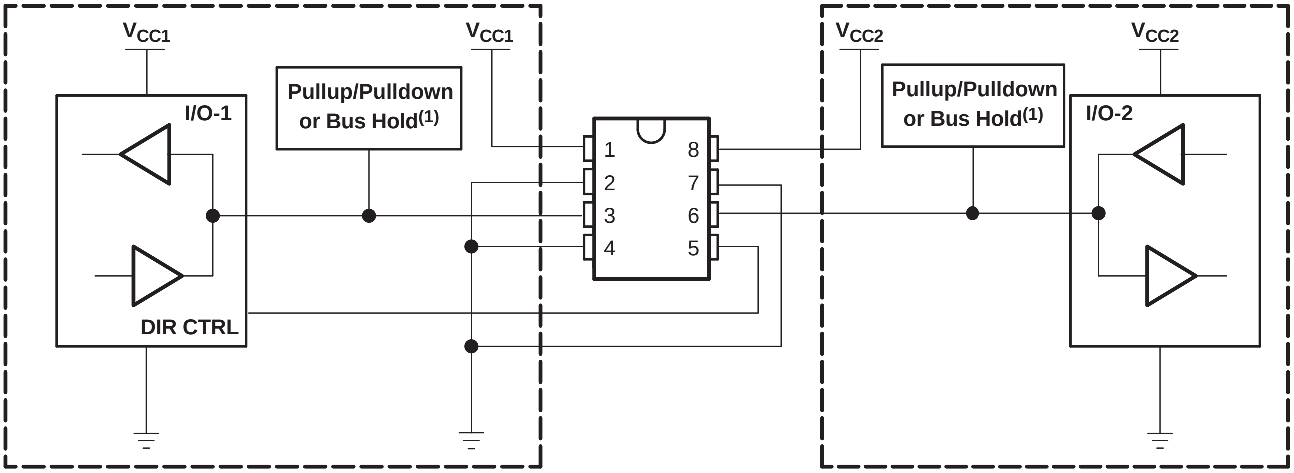


PIN	NAME	FUNCTION	DESCRIPTION
1	V_{CCA}	V_{CC1}	SYSTEM-1 supply voltage (1.2 V to 3.6 V)
2	A1	OUT1	Output level depends on V_{CC1} voltage.
3	A2	OUT2	Output level depends on V_{CC1} voltage.
4	GND	GND	Device GND
5	DIR	DIR	The GND (low-level) determines B-port to A-port direction.
6	B2	IN2	Input threshold value depends on V_{CC2} voltage.
7	B1	IN1	Input threshold value depends on V_{CC2} voltage.
8	V_{CCB}	V_{CC2}	SYSTEM-2 supply voltage (1.2 V to 3.6 V)

Figure 2. Unidirectional Logic Level-Shifting Application

APPLICATION INFORMATION

Figure 3 shows the SN74AVC2T45 used in a bidirectional logic level-shifting application. Since the SN74AVC2T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.



Following is a sequence that illustrates data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown.(1)
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown.(1)
4	L	In	Out	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, i.e., both pullup or both pulldown.

Figure 3. Bidirectional Logic Level-Shifting Application

Enable Times

Calculate the enable times for the SN74AVC2T45 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC2T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CAVC2T45TDCURQ1	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBUI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

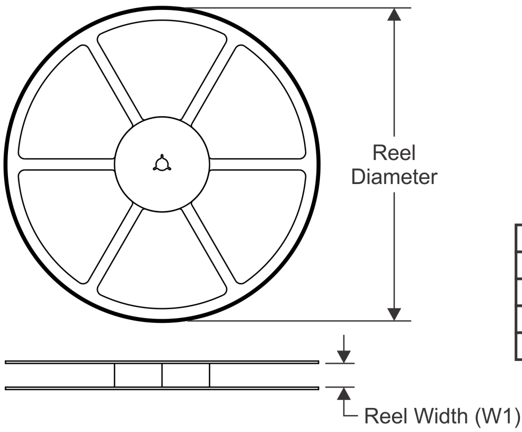
OTHER QUALIFIED VERSIONS OF SN74AVC2T45-Q1 :

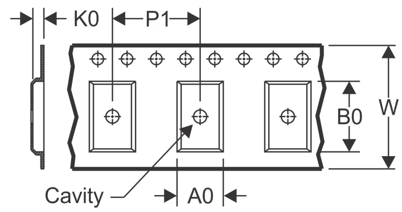
- Catalog: SN74AVC2T45

NOTE: Qualified Version Definitions:

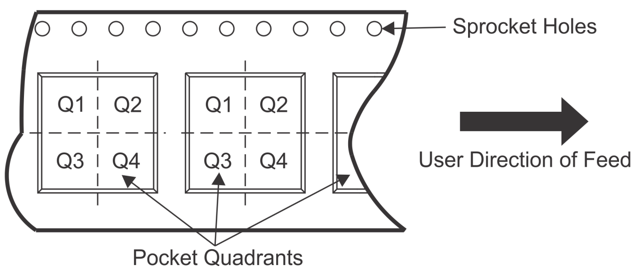
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





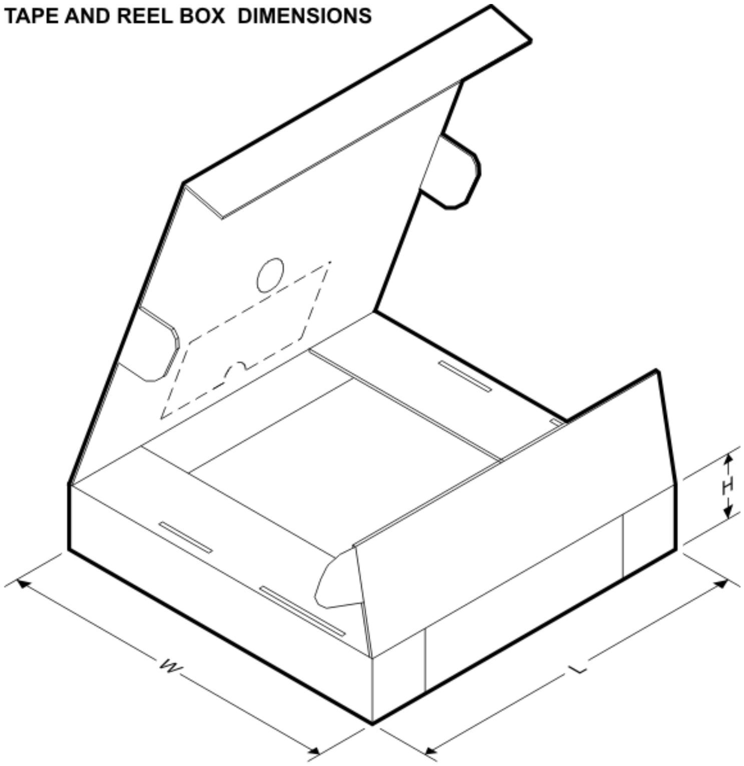
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

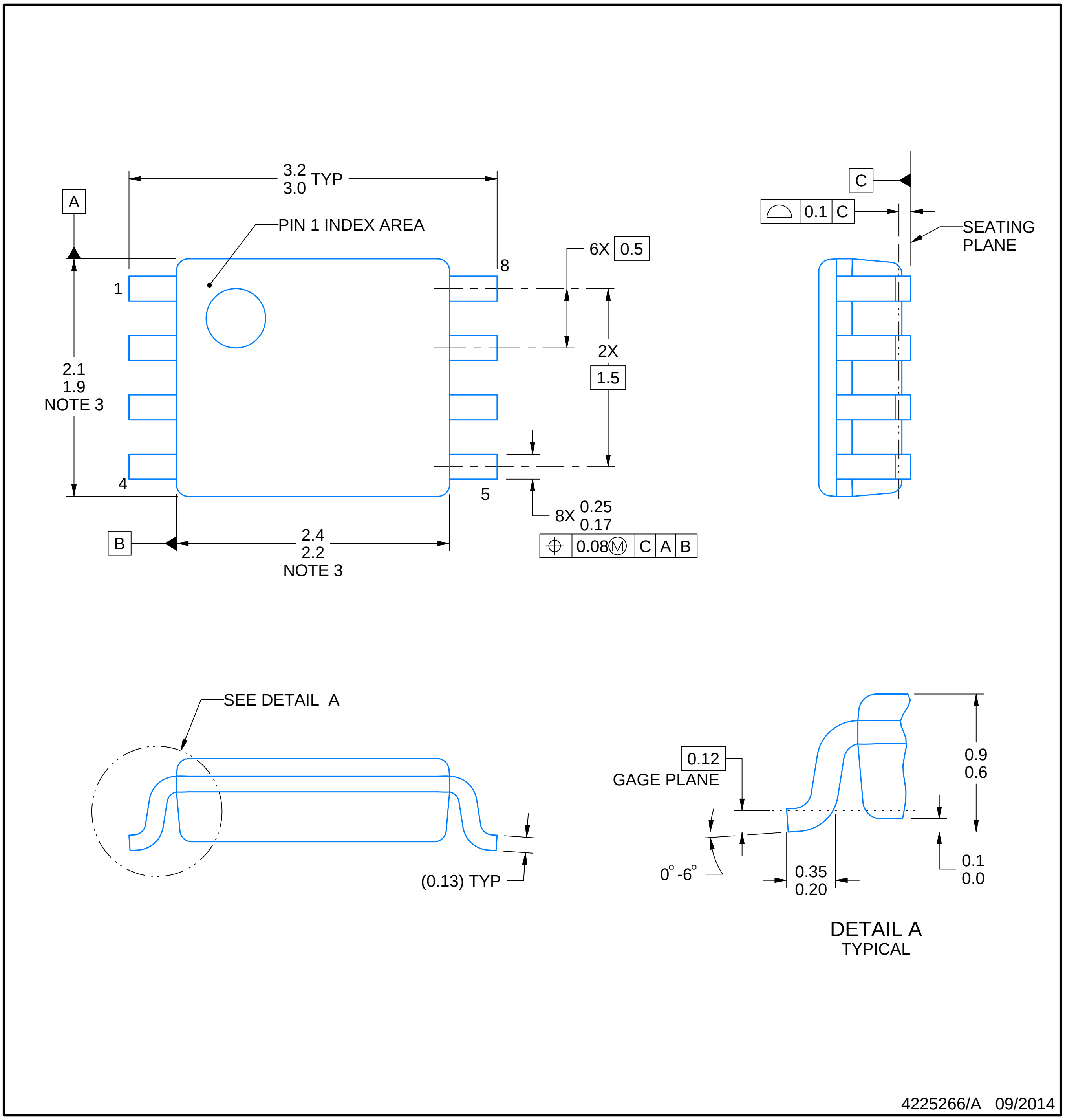
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAVC2T45TDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



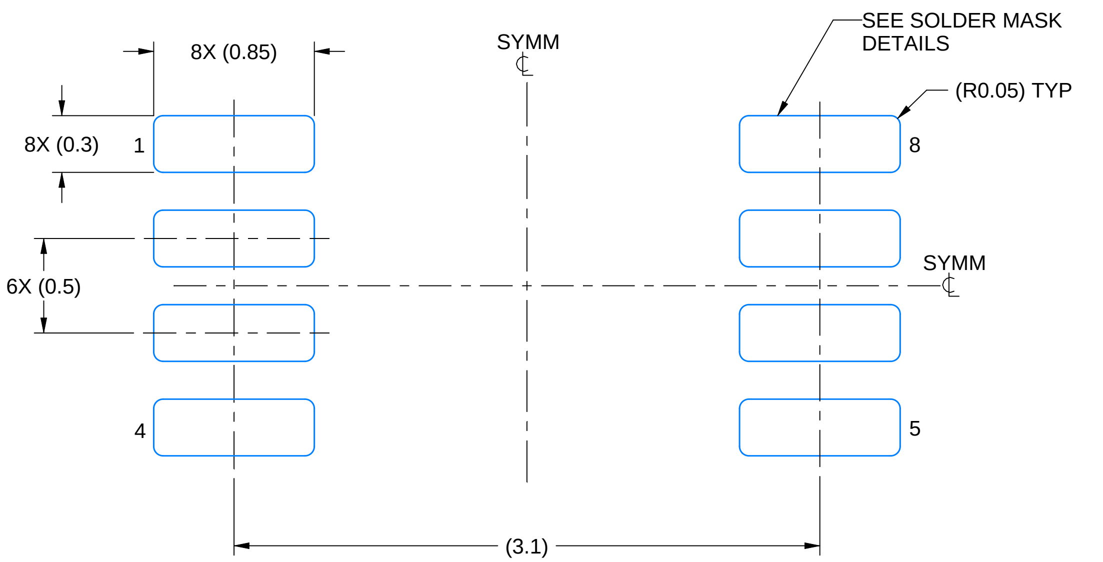
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAVC2T45TDCURQ1	VSSOP	DCU	8	3000	202.0	201.0	28.0

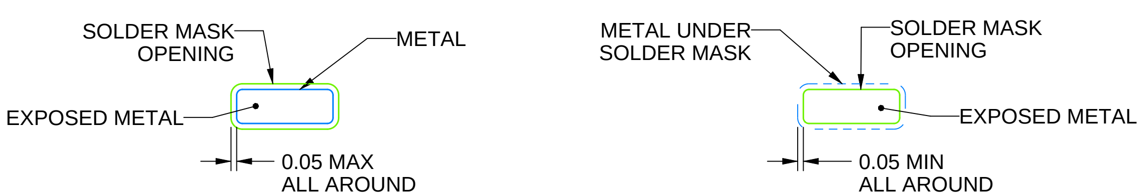


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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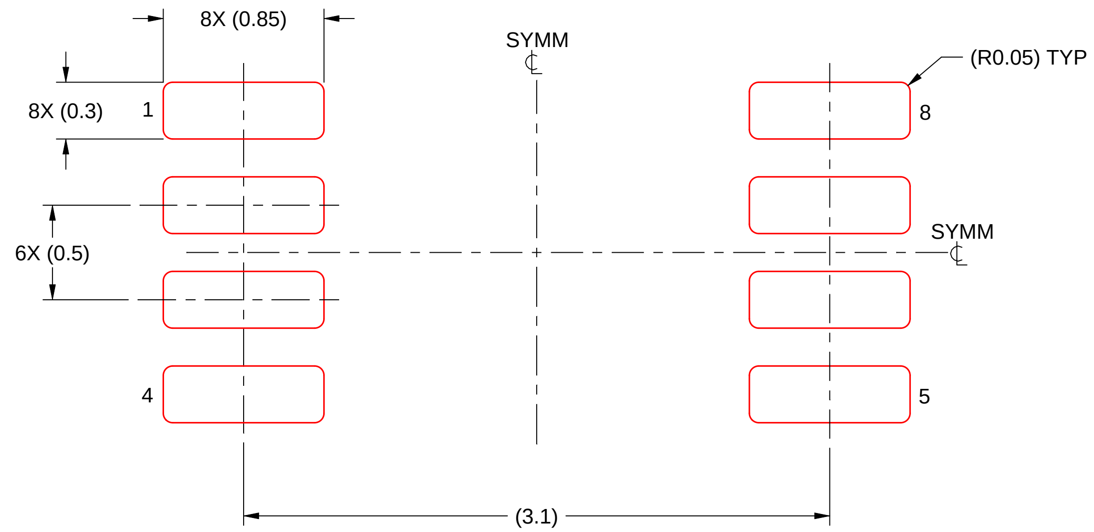
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.