SLAS648E – APRIL 2009 – REVISED MARCH 2011

- **Low Supply-Voltage Range, 1.8 V to 3.6 V**
- **Ultralow Power Consumption**
  Active Mode: 220 μA at 1 MHz, 2.2 V
  Standby Mode: 0.9 μA
  Off Mode (RAM Retention): 0.1 μA
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in Less Than 6 μs**
  - **Internal Very Low Power, Low-Frequency Oscillator**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **16-Bit Timer_A With Five Capture/Compare Registers**
- **Two Universal Serial Communication Interfaces (USCIs)**
  USCI_A0
  - **Enhanced UART Supporting Auto-Baudrate Detection**
  - **IrDA Encoder and Decoder**
  - **Synchronous SPI**

  USCI_B0
  - **I2C**
  - **Synchronous SPI**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **Integrated LCD Driver With Contrast Control for Up to 144 Segments**
- **Basic Timer With Real Time Clock Feature**
- **Brownout detector**
- **On-Chip Comparator for Analog Signal Compare Function or Slope A/D**
- **10-Bit 200-ksps Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, Autoscan, and Data Transfer Controller**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Bootstrap Loader**
- **On-Chip Emulation Module**
- **Family Members Include:**
  MSP430F4152: 16KB+256B Flash Memory 512B RAM
  MSP430F4132: 8KB+256B Flash Memory 512B RAM
- **Available in 64-Pin QFP Package and 48-Pin QFN Package (See Available Options)**
- **For Complete Module Descriptions, See The *MSP430x4xx Family User's Guide*, Literature Number SLAU056**

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generator that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 μs.

The MSP430F41x2 is a microcontroller configuration with two 16-bit timers, a basic timer with a real–time clock, a 10-bit A/D converter, a versatile analog comparator, two universal serial communication interfaces, up to 48 I/O pins, and a liquid crystal display driver.

Typical applications for this device include analog and digital sensor systems, remote controls, thermostats, digital timers, hand-held meters, etc.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS†

T_A	PACKAGED DEVICES‡	
	PLASTIC 64-PIN QFP (PM)	PLASTIC 48-PIN QFN (RGZ)
–40°C to 85°C	MSP430F4152IPM MSP430F4132IPM	MSP430F4152IRGZ MSP430F4132IRGZ

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

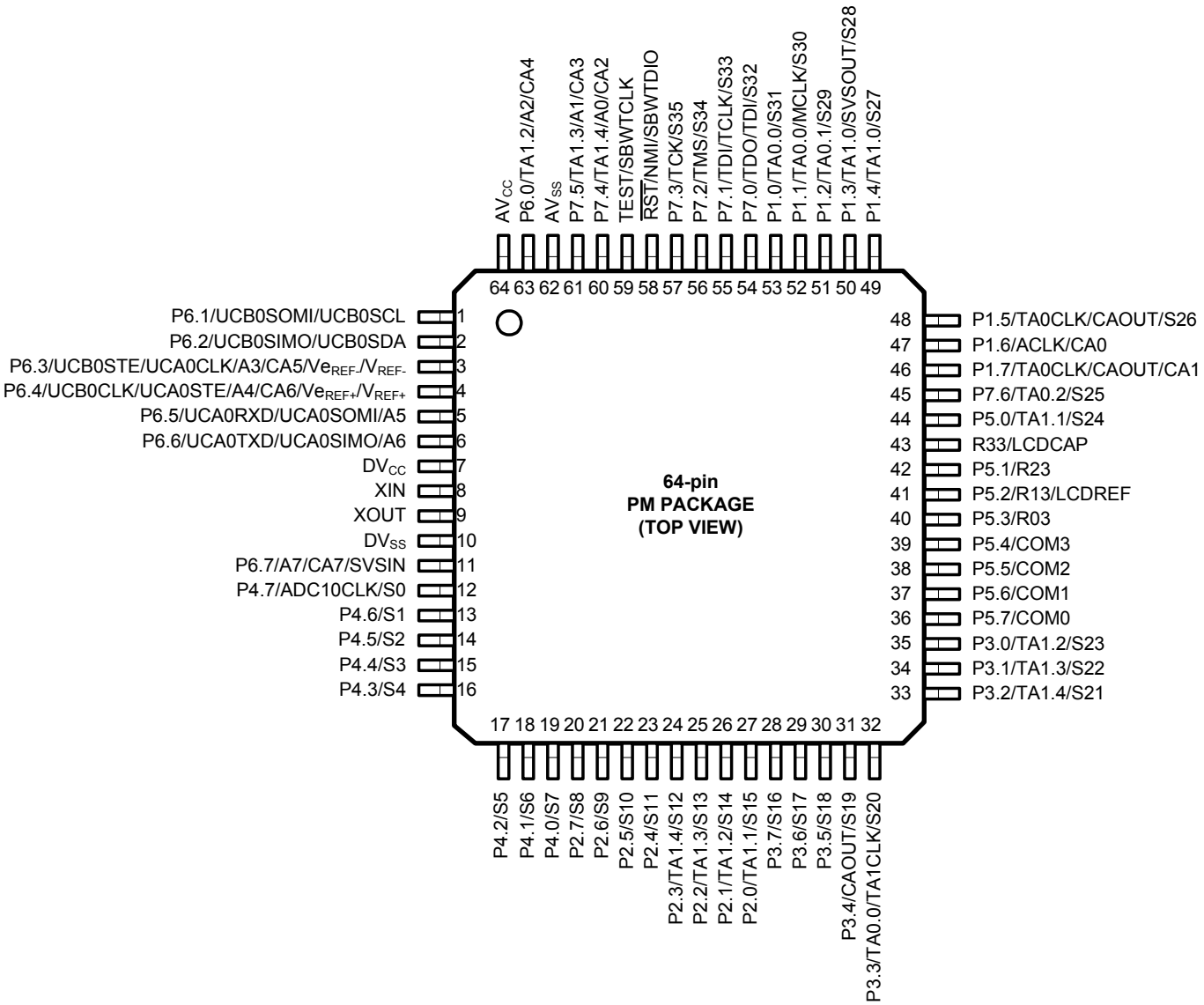
‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DEVELOPMENT TOOL SUPPORT

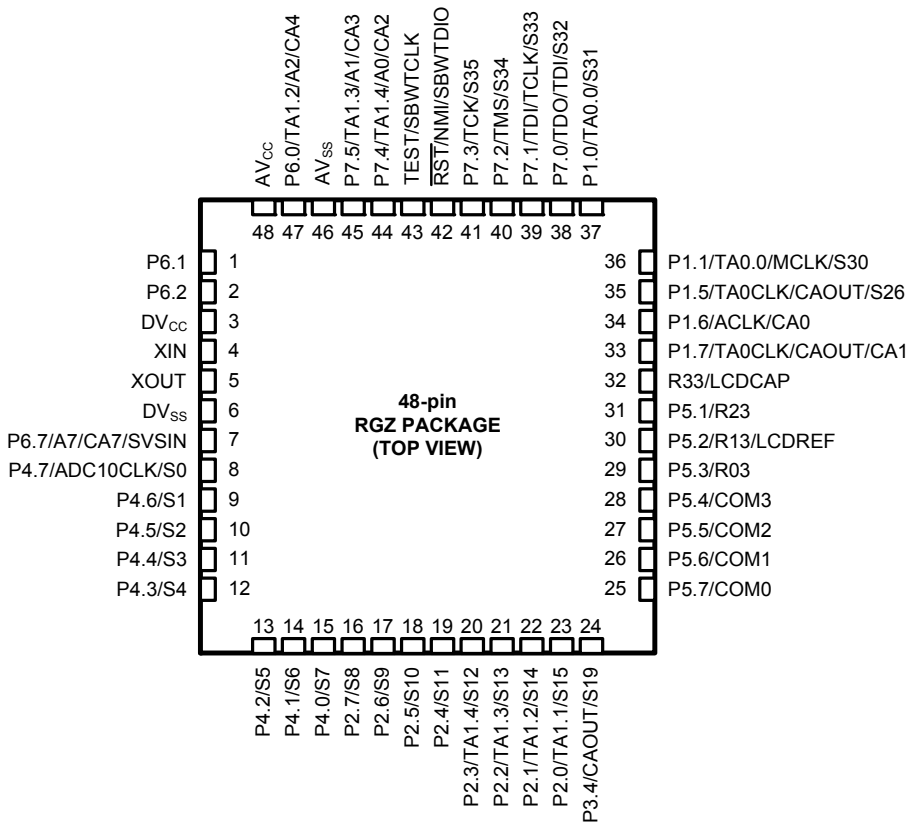
All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy to use development tools. Recommended hardware options include the following:

- Debugging and Programming Interface
  - MSP-FET430UIF (USB)
  - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP-FET430U64A (PM package)
- Production Programmer
  - MSP-GANG430

pin designation, MSP430F41x2IPM (QFP)

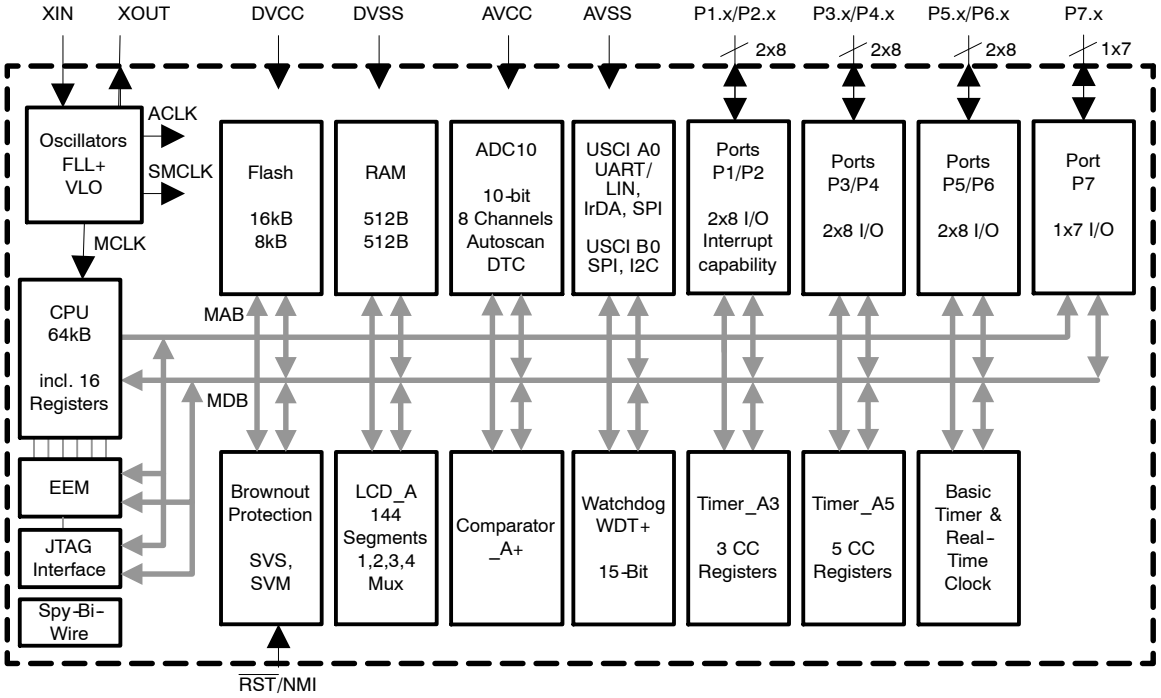


pin designation, MSP430F41x2IRGZ (QFN)†



† "Not available" pins in the 48-pin package should be initialized to output direction.

functional block diagram



NOTE: The USCI A0 and USCI B0 cannot be used in the 48-pin package options (RGZ).

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	64 PIN	48 PIN		
P1.0/TA0.0/S31	53	37	I/O	General-purpose digital I/O pin Timer0_A3, capture: CCI0A input, compare: Out0 output LCD segment output
P1.1/TA0.0/ MCLK/S30	52	36	I/O	General-purpose digital I/O pin Timer0_A3, capture: CCI0B input MCLK signal output LCD segment output
P1.2/TA0.1/S29	51	–	I/O	General-purpose digital I/O pin Timer0_A3, capture: CCI1A input, compare: Out1 output LCD segment output
P1.3/TA1.0/ SVSOUT/S28	50	–	I/O	General-purpose digital I/O pin Timer1_A5, capture: CCI0B input SVS comparator output LCD segment output
P1.4/TA1.0/S27	49	–	I/O	General-purpose digital I/O pin/ Timer1_A5, capture: CCI0A input, compare: Out0 output LCD segment output
P1.5/TA0CLK/ CAOUT/S26	48	35	I/O	General-purpose digital I/O pin Timer0_A3, clock signal TACLK input Comparator_A output LCD segment output
P1.6/ACLK/CA0	47	34	I/O	General-purpose digital I/O pin Comparator_A input 0 ACLK signal output
P1.7/TA0CLK CAOUT/CA1	46	33	I/O	General-purpose digital I/O pin Timer0_A3, clock signal TACLK input Comparator_A output Comparator_A input 1
P2.0/TA1.1/S15	27	23	I/O	General-purpose digital I/O pin Timer1_A5, compare: Out1 Output LCD segment output
P2.1/TA1.2/S14	26	22	I/O	General-purpose digital I/O pin Timer1_A5, compare: Out2 Output LCD segment output
P2.2/TA1.3/S13	25	21	I/O	General-purpose digital I/O pin Timer1_A5, compare: Out3 Output LCD segment output
P2.3/TA1.4/S12	24	20	I/O	General-purpose digital I/O pin Timer1_A5, compare: Out4 output LCD segment output
P2.4/S11	23	19	I/O	General-purpose digital I/O pin LCD segment output
P2.5/S10	22	18	I/O	General-purpose digital I/O pin LCD segment output
P2.6/S9	21	17	I/O	General-purpose digital I/O pin LCD segment output
P2.7/S8	20	16	I/O	General-purpose digital I/O pin LCD segment output

Terminal Functions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	64 PIN	48 PIN		
P3.0/TA1.2/S23	35	–	I/O	General-purpose digital I/O pin Timer1_A5, capture: CCI2A input, compare: Out2 output LCD segment output
P3.1/TA1.3/S22	34	–	I/O	General-purpose digital I/O pin Timer1_A5, capture: CCI3A input, compare: Out3 output LCD segment output
P3.2/TA1.4/S21	33	–	I/O	General-purpose digital I/O pin Timer1_A5, capture: CCI4A input, compare: Out4 output LCD segment output
P3.3/TA0.0/ TA1CLK/S20	32	–	I/O	General-purpose digital I/O pin Timer0_A3, compare: Out0 output Timer1_A5, clock signal TACLK input LCD segment output
P3.4/CAOUT/S19	31	24	I/O	General-purpose digital I/O pin Comparator_A output LCD segment output
P3.5/S18	30	–	I/O	General-purpose digital I/O pin LCD segment output
P3.6/S17	29	–	I/O	General-purpose digital I/O pin LCD segment output
P3.7/S16	28	–	I/O	General-purpose digital I/O pin LCD segment output
P4.0/S7	19	15	I/O	General-purpose digital I/O pin LCD segment output
P4.1/S6	18	14	I/O	General-purpose digital I/O pin LCD segment output
P4.2/S5	17	13	I/O	General-purpose digital I/O pin LCD segment output
P4.3/S4	16	12	I/O	General-purpose digital I/O pin LCD segment output
P4.4/S3	15	11	I/O	General-purpose digital I/O pin LCD segment output
P4.5/S2	14	10	I/O	General-purpose digital I/O pin LCD segment output
P4.6/S1	13	9	I/O	General-purpose digital I/O pin LCD segment output
P4.7/ADC10CLK/ S0	12	8	I/O	General-purpose digital I/O pin ADC10, conversion clock LCD segment output
P5.0/TA1.1/S24	44	–	I/O	General-purpose digital I/O pin Timer1_A5, capture: CCI1A input, compare: Out1 output LCD segment output
LCDCAP/R33	43	32	I/O	Capacitor connection for LCD charge pump input port of the most positive analog LCD level (V4)
P5.1/R23	42	31	I/O	General-purpose digital I/O pin input port of the second most positive analog LCD level (V3)
P5.2/LCDREF/ R13	41	30	I/O	General-purpose digital I/O pin External LCD reference voltage input input port of the third most positive analog LCD level (V3 or V2)

Terminal Functions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	64 PIN	48 PIN		
P5.3/R03	40	29	I/O	General-purpose digital I/O pin input port of the fourth most positive analog LCD level (V1)
P5.4/COM3	39	28	I/O	General-purpose digital I/O pin common output, COM0–3 are used for LCD backplanes
P5.5/COM2	38	27	I/O	General-purpose digital I/O pin common output, COM0–3 are used for LCD backplanes
P5.6/COM1	37	26	I/O	General-purpose digital I/O pin common output, COM0–3 are used for LCD backplanes
P5.7/COM0	36	25	I/O	General-purpose digital I/O pin common output, COM0–3 are used for LCD backplanes
P6.0/TA1.2/A2†/ CA4	63	47	I/O	General-purpose digital I/O pin Timer1_A5, compare: Out2 output ADC10 analog input A2† Comparator_A input 4
P6.1/ UCB0SOMI†/ UCB0SCL†	1	1	I/O	General-purpose digital I/O pin USCI B0 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode†
P6.2/ UCB0SIMO†/ UCB0SDA†	2	2	I/O	General-purpose digital I/O pin USCI B0 slave in/master out in SPI mode, SDA I^2C data in I^2C mode†
P6.3/UCB0STE/ UCA0CLK/A3/ CA5/V_{eref-}/V_{ref-}	3	–	I/O	General-purpose digital I/O pin USCI B0 slave transmit enable/USCI A0 clock input/output ADC10 analog input A3 / negative reference Comparator_A input 5
P6.4/UCB0CLK/ UCA0STE/A4/ CA6/V_{eref+}/V_{ref+}	4	–	I/O	General-purpose digital I/O pin USCI B0 clock input/output, USCI A0 slave transmit enable ADC10 analog input A4/ positive reference Comparator_A input 6
P6.5/UCA0RXD/ UCA0SOMI/A5	5	–	I/O	General-purpose digital I/O pin USCI A0 receive data input in UART mode, slave data out/master in in SPI mode ADC10 analog input A5
P6.6/UCA0TXD/ UCA0SIMO/A6	6	–	I/O	General-purpose digital I/O pin USCI A0 transmit data output in UART mode, slave data in/master out SPI mode ADC10 analog input A6
P6.7/A7/CA7/ SVSIN	11	7	I/O	General-purpose digital I/O pin ADC10 analog input A7 Comparator_A input 7 SVS input
P7.0/TDO/TDI/ S32	54	38	I/O	General-purpose digital I/O pin JTAG test data output terminal or test data input in programming an test LCD segment output
P7.1/TDI/TCLK/ S33	55	39	I/O	General-purpose digital I/O pin JTAG test data input or test clock input in programming an test LCD segment output
P7.2/TMS/S34	56	40	I/O	General-purpose digital I/O pin JTAG test mode select, input terminal for device programming and test LCD segment output

† 64-pin package devices only

Terminal Functions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	64 PIN	48 PIN		
P7.3/TCK/S35	57	41	I/O	General-purpose digital I/O pin Test clock input for device programming and test LCD segment output
P7.4/TA1.4/ A0/CA2	60	44	I/O	General-purpose digital I/O pin Timer1_A5, capture: CCI4B input, compare: Out4 output ADC10 analog input A0 Comparator_A input 2
P7.5/TA1.3/ A1/CA3	61	45	I/O	General-purpose digital I/O pin Timer1_A5, capture: CCI3B input, compare: Out3 output ADC10 analog input A1 Comparator_A input 3
P7.6/TA0.2/S25	45	–	I/O	General-purpose digital I/O pin Timer0_A3, capture: CCI2A input, compare: Out2 output LCD segment output
AV_{CC}	64	48		Analog supply voltage, positive terminal
AV_{SS}	62	46		Analog supply voltage, negative terminal
DV_{CC}	7	3		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS}	10	6		Digital supply voltage, negative terminal. Supplies all digital parts.
XOUT	9	5	O	Output port for crystal oscillator XT1. Standard or watch crystals can be connected.
XIN	8	4	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
$\overline{RST}$/NMI/ SBWTDIO	58	42	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/SBWTCLK	59	43	I	Selects test mode for JTAG pins on Port7. The device protection fuse is connected to TEST.
Thermal Pad	NA	NA	NA	QFN package pad (RGZ package only). Connection to DV_{SS} is recommended.

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; Table 2 shows the address modes.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 ---> R5
Single operands, destination only	e.g., CALL R8	PC -->(TOS), R8--> PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 —> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) —> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) —> M(TONI)
Absolute	●	●	MOV & MEM, & TCDAT		M(MEM) —> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) —> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) —> R11 R10 + 2 —> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 —> M(TONI)

NOTE: S = source, D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - FLL+ loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - FLL+ loop control is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0xFFFF to 0xFFC0. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

If the reset vector (located at address 0xFFFE) contains 0xFFFF (e.g., flash is not programmed), the CPU goes into LPM4 immediately after power-up.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Flash Memory PC Out-of-Range (see Note 4)	PORIFG RSTIFG WDTIFG KEYV (see Note 1)	Reset	0xFFFE	15, highest
NMI Oscillator Fault Flash Memory Access Violation	NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1, 2, and 4)	(Non)maskable (Non)maskable (Non)maskable	0xFFFC	14
Timer_A5	TA1CCR0 CCIFG0 (see Note 2)	Maskable	0xFFFA	13
Timer_A5	TA1CCR1 to TACCR4 CCIFGs, and TAIFG (see Notes 1 and 2)	Maskable	0xFFF8	12
Comparator_A+	CAIFG	Maskable	0xFFF6	11
Watchdog Timer+	WDTIFG	Maskable	0xFFF4	10
USCI_A0/B0 Receive	UCA0RXIFG (see Note 1), UCB0RXIFG (SPI mode), or UCB0STAT UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG (I2C mode) (see Note 1)	Maskable	0xFFF2	9
USCI_A0/B0 Transmit	UCA0TXIFG (see Note 1), UCB0TXIFG (SPI mode), or UCB0RXIFG and UCB0TXIFG (I2C mode) (see Note 1)	Maskable	0xFFF0	8
ADC10	ADC10IFG (see Note 2)	Maskable	0xFFEE	7
Timer_A3	TACCR0 CCIFG0 (see Note 2)	Maskable	0xFFEC	6
Timer_A3	TACCR1 CCIFG1 and TACCR2 CCIFG2, TAIFG (see Notes 1 and 2)	Maskable	0xFFEA	5
I/O Port P1 (Eight Flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	Maskable	0xFFE8	4
			0xFFE6	3
			0xFFE4	2
I/O Port P2 (Eight Flags)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	Maskable	0xFFE2	1
Basic Timer1/RTC	BTIFG	Maskable	0xFFE0	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh). (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
4. Access and key violations, KEYV and ACCVIFG.

special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.
OFIE	Oscillator fault enable
NMIIE	(Non)maskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h	BTIE				UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
	rw-0				rw-0	rw-0	rw-0	rw-0

UCA0RXIE	USCI_A0 receive interrupt enable
UCA0TXIE	USCI_A0 transmit interrupt enable
UCB0RXIE	USCI_B0 receive interrupt enable
UCB0TXIE	USCI_B0 transmit interrupt enable
BTIE	Basic timer interrupt enable

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.

OFIFG Flag set on oscillator fault

RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power-up.

PORIFG Power-on interrupt flag. Set on V_{CC} power–up.

NMIIFG Set via $\overline{RST}$/NMI-pin

Address	7	6	5	4	3	2	1	0
03h	BTIFG				UCB0 TXIFG	UCB0 RXIFG	UCA0 TXIFG	UCA0 RXIFG
	rw-0				rw-1	rw-0	rw-1	rw-0

UCA0RXIFG USCI_A0 receive interrupt flag

UCA0TXIFG USCI_A0 transmit interrupt flag

UCB0RXIFG USCI_B0 receive interrupt flag

UCB0TXIFG USCI_B0 transmit interrupt flag

BTIFG Basic Timer1 interrupt flag

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is Reset or set by PUC.
	rw-(0,1):	Bit can be read and written. It is Reset or set by POR.
		SFR bit is not present in device

memory organization

		MSP430F4152	MSP430F4132
Memory Main: interrupt vector Main: code memory	Size Flash Flash	16KB 0FFFFh – 0FFE0h 0FFFFh – 0C000h	8KB 0FFFFh – 0FFE0h 0FFFFh – 0E000h
Information memory	Size Flash	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h
Boot memory	Size ROM	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h
RAM	Size	512B 03FFh – 0200h	512B 03FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

bootstrap loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Memory Programming User's Guide*, literature number SLAU265.

BSL FUNCTION	PM PACKAGE PINS	RGZ PACKAGE PINS
Data transmit	53 – P1.0	37 – P1.0
Data receive	52 – P1.1	36 – P1.1

flash memory (Flash)

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n.
  Segments A to D are also called *information memory.*

peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x4xx Family User's Guide*, literature number SLAU056.

oscillator and system clock

The clock system in the MSP430F41x2 is supported by the FLL+ module that includes support for a 32768-Hz watch crystal oscillator, an internal very low-power low–frequency oscillator, an internal digitally-controlled oscillator (DCO), and an 8-MHz high-frequency crystal oscillator (XT1). The FLL+ clock module is designed to meet the requirements of both low system cost and low power consumption. The FLL+ features a digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high-frequency crystal, or a very low-power LF oscillator
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8

brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must insure the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

digital I/O

There are seven 8-bit I/O ports implemented—ports P1 through P7. Port P7 is a 7-bit I/O port.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

watchdog timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

Basic Timer1 and Real-Time Clock (RTC)

The Basic Timer1 has two independent 8-bit timers which can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 is extended to provide an integrated real-time clock (RTC). An internal calendar compensates for month with less than 31 days and includes leap year correction.

LCD_A driver with regulated charge pump

The LCD_A driver generates the segment and common signals required to drive an LCD display. The LCD_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2–MUX, 3–MUX, and 4–MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage via an integrated charge pump. Furthermore it is possible to control the level of the LCD voltage and thus contrast in software.

Timer0_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_A3 SIGNAL CONNECTIONS

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PM	RGZ					PM	RGZ
48 – P1.5 46 – P1.7	35 – P1.5 33 – P1.7	TA0CLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
48 – P1.5	35 – P1.5	$\overline{\text{TA0CLK}}$	$\overline{\text{TACLK}}$				
53 – P1.0	37 – P1.0	TA0.0	CCI0A	CCR0	TA0	53 – P1.0	37 – P1.0
52 – P1.1	36 – P1.1	TA0.0	CCI0B			32 – P3.3	–
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
51 – P1.2	–	TA0.1	CCI1A	CCR1	TA1	51 – P1.2	
		CAOUT (internal)	CCI1B			ADC10 (internal)	ADC10 (internal)
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
45 – P7.6	–	TA0.2	CCI2A	CCR2	TA2	45 – P7.6	–
		ACLK (internal)	CCI2B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				

Timer1_A5

Timer_A5 is a 16-bit timer/counter with five capture/compare registers. Timer_A5 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A5 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_A5 SIGNAL CONNECTIONS							
INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PM	RGZ					PM	RGZ
32 – P3.3	–	TA1CLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
32 – P3.3	–	$\overline{\text{TA1CLK}}$	$\overline{\text{TACLK}}$				
49 – P1.4	–	TA1.0	CCI0A	CCR0	TA0	49 – P1.4	–
50 – P1.3	–	TA1.0	CCI0B			ADC10 (internal)	ADC10 (internal)
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
44 – P5.0	–	TA1.1	CCI1A	CCR1	TA1	44 – P5.0	–
		CAOUT (internal)	CCI1B			27 – P2.0	23 – P2.0
		DV_{SS}	GND			ADC10 (internal)	ADC10 (internal)
		DV_{CC}	V_{CC}				
35 – P3.0	–	TA1.2	CCI2A	CCR2	TA2	35 – P3.0	–
		ACLK (internal)	CCI2B			26 – P2.1	22 – P2.1
		DV_{SS}	GND			63 – P6.0	47 – P6.0
		DV_{CC}	V_{CC}				
34 – P3.1	–	TA1.3	CCI3A	CCR3	TA3	34 – P3.1	–
61 – P7.5	45 – P7.5	TA1.3	CCI3B			25 – P2.2	21 – P2.2
		DV_{SS}	GND			61 – P7.5	45 – P7.5
		DV_{CC}	V_{CC}				
33 – P3.2	–	TA1.4	CCI4A	CCR4	TA4	33 – P3.2	–
60 – P7.4	44 – P7.4	TA1.4	CCI4B			24 – P2.3	20 – P2.3
		DV_{SS}	GND			60 – P7.4	44 – P7.4
		DV_{CC}	V_{CC}				

universal serial communication interface (USCI) (USCI_A0, USCI_B0)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I2C and asynchronous communication protocols like UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

USCI_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

USCI_B0 provides support for SPI (3 or 4 pin) and I2C.

Comparator_A+

The primary function of the comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

ADC10

The ADC10 module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and data transfer controller (DTC) for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog timer control	WDTCTL	0120h
Timer0_A3	Capture/compare register 2	TA0CCR2	0176h
	Capture/compare register 1	TA0CCR1	0174h
	Capture/compare register 0	TA0CCR0	0172h
	Timer_A register	TA0R	0170h
	Capture/compare control 2	TA0CCTL2	0166h
	Capture/compare control 1	TA0CCTL1	0164h
	Capture/compare control 0	TA0CCTL0	0162h
	Timer_A control	TA0CTL	0160h
	Timer_A interrupt vector	TA0IV	012Eh
Timer1_A5	Capture/compare register 4	TA1CCR4	019A
	Capture/compare register 3	TA1CCR3	0198
	Capture/compare register 2	TA1CCR2	0196h
	Capture/compare register 1	TA1CCR1	0194h
	Capture/compare register 0	TA1CCR0	0192h
	Timer_A register	TA1R	0190h
	Capture/compare control 4	TA1CCTL4	018A
	Capture/compare control 3	TA1CCTL3	0188
	Capture/compare control 2	TA1CCTL2	0186h
	Capture/compare control 1	TA1CCTL1	0184h
	Capture/compare control 0	TA1CCTL0	0182h
	Timer_A control	TA1CTL	0180h
	Timer_A interrupt vector	TA1IV	011Eh
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
ADC10	ADC data transfer start address	ADC10SA	01BCh
	ADC memory	ADC10MEM	01B4h
	ADC control register 1	ADC10CTL1	01B2h
	ADC control register 0	ADC10CTL0	01B0h
	ADC analog enable 0	ADC10AE0	004Ah
	ADC analog enable 1	ADC10AE1	004Bh
	ADC data transfer control register 1	ADC10DTC1	0049h
	ADC data transfer control register 0	ADC10DTC0	0048h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
LCD_A	LCD Voltage Control 1	LCDAVCTL1	0AFh
	LCD Voltage Control 0	LCDAVCTL0	0AEh
	LCD Voltage Port Control 1	LCDAPCTL1	0ADh
	LCD Voltage Port Control 0	LCDAPCTL0	0ACh
	LCD memory 20	LCDM20	0A4h
	:	:	:
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	:	:	:
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDACTL	090h
USCI A0/B0	USCI A0 auto baud rate control	UCA0ABCTL	0x005D
	USCI A0 transmit buffer	UCA0TXBUF	0x0067
	USCI A0 receive buffer	UCA0RXBUF	0x0066
	USCI A0 status	UCA0STAT	0x0065
	USCI A0 modulation control	UCA0MCTL	0x0064
	USCI A0 baud rate control 1	UCA0BR1	0x0063
	USCI A0 baud rate control 0	UCA0BR0	0x0062
	USCI A0 control 1	UCA0CTL1	0x0061
	USCI A0 control 0	UCA0CTL0	0x0060
	USCI A0 IrDA receive control	UCA0IRRCTL	0x005F
	USCI A0 IrDA transmit control	UCA0IRTCTL	0x005E
	USCI B0 transmit buffer	UCB0TXBUF	0x006F
	USCI B0 receive buffer	UCB0RXBUF	0x006E
	USCI B0 status	UCB0STAT	0x006D
	USCI B0 I2C Interrupt enable	UCB0CIE	0x006C
	USCI B0 baud rate control 1	UCB0BR1	0x006B
	USCI B0 baud rate control 0	UCB0BR0	0x006A
	USCI B0 control 1	UCB0CTL1	0x0069
	USCI B0 control 0	UCB0CTL0	0x0068
	USCI B0 I2C slave address	UCB0SA	0x011A
	USCI B0 I2C own address	UCB0OA	0x0118
Comparator_A+	Comparator_A port disable	CAPD	05Bh
	Comparator_A control2	CACTL2	05Ah
	Comparator_A control1	CACTL1	059h
Brownout, SVS	SVS control register (Reset by brownout signal)	SVSCTL	056h
FLL+ Clock	FLL+ Control 2	FLL_CTL2	055h
	FLL+ Control 1	FLL_CTL1	054h
	FLL+ Control 0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
RTC (Basic Timer1)	Real Time Clock Year High Byte	RTCYEARH	04Fh
	Real Time Clock Year Low Byte	RTCYEARL	04Eh
	Real Time Clock Month	RTCMON	04Dh
	Real Time Clock Day of Month	RTCDAY	04Ch
	Basic Timer1 Counter	BTCNT2	047h
	Basic Timer1 Counter	BTCNT1	046h
	Real Time Counter 4	RTCNT4	045h
	(Real Time Clock Day of Week)	(RTCDOW)	
	Real Time Counter 3	RTCNT3	044h
	(Real Time Clock Hour)	(RTCHOUR)	
	Real Time Counter 2	RTCNT2	043h
	(Real Time Clock Minute)	(RTCMIN)	
	Real Time Counter 1	RTCNT1	042h
	(Real Time Clock Second)	(RTCSEC)	
	Real Time Clock Control	RTCCTL	041h
	Basic Timer1 Control	BTCTL	040h
Port P7	Port P7 selection	P7SEL	03Bh
	Port P7 direction	P7DIR	03Ah
	Port P7 output	P7OUT	039h
	Port P7 input	P7IN	038h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Port P1	Port P1 selection register	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special functions	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS} . . . . . –0.3 V to 4.1 V
Voltage applied to any pin (see Note 1) . . . . . –0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature, T_{stg}: Unprogrammed device . . . . . –55°C to 150°C
Programmed device . . . . . –55°C to 85°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage during program execution, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})			1.8		3.6	V
Supply voltage during flash memory programming, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})			2.2		3.6	V
Supply voltage, V_{SS} (AV_{SS} = DV_{SS} = V_{SS})			0		0	V
Operating free-air temperature range, T_A			–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 1)	LF selected, XTS_FLL = 0	Watch crystal		32.768		kHz
	XT1 selected, XTS_FLL = 1	Ceramic resonator	0.45		6	MHz
	XT1 selected, XTS_FLL = 1	Crystal	1		6	MHz
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	dc		4.15	MHz
		V_{CC} = 3.0 V	dc		8	

NOTES: 1. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

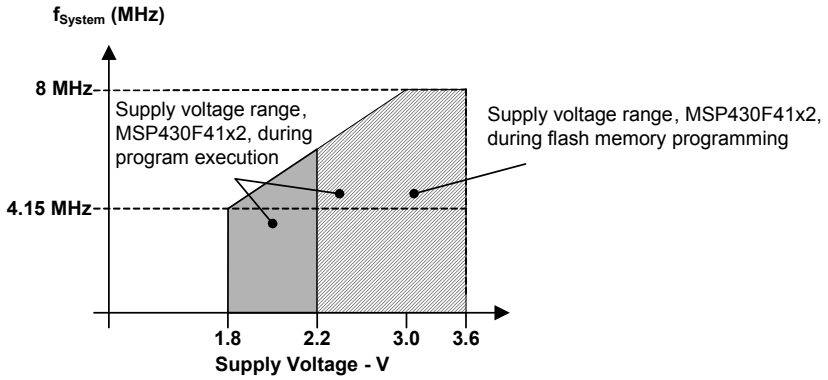


Figure 1. Frequency vs Supply Voltage

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current

PARAMETER		T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(AM)}$	Active mode (see Note 1), $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32768 Hz, XTS=0, SELM=(0,1)	–40°C to 85°C	2.2 V		220	295	µA
			3 V		350	398	
$I_{(LPM0)}$	Low-power mode 0 (LPM0) (see Note 1)	–40°C to 85°C	2.2 V		33	60	µA
			3 V		50	92	
$I_{(LPM2)}$	Low-power mode 2 (LPM2), f(MCLK) = f (SMCLK) = 0 MHz, f(ACLK) = 32768 Hz, SCG0 = 0 (see Note 2)	–40°C to 85°C	2.2 V		6	13	µA
			3 V		7	15	
$I_{(LPM3)}$	Low-power mode 3 (LPM3), $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32768 Hz, SCG0 = 1, Basic Timer1 enabled , ACLK selected, LCD_A enabled, LCDCPEN = 0, (static mode, $f_{LCD} = f_{(ACLK)}/32$) (see Notes 2 and 3)	–40°C	2.2 V		0.85	1.4	µA
		25°C			0.90	1.2	
		60°C			1.15	1.4	
		85°C			2.15	3.0	
		–40°C	3 V		1.0	1.5	
		25°C			1.1	1.5	
		60°C			1.4	1.9	
		85°C			2.5	3.5	
$I_{(LPM3)}$	Low-power mode 3 (LPM3), $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32768 Hz, SCG0 = 1, Basic Timer1 enabled , ACLK selected, LCD_A enabled, LCDCPEN = 0, (4-mux mode, $f_{LCD} = f_{(ACLK)}/32$) (see Notes 2 and 3)	–40°C	2.2 V		1.8	3.3	µA
		25°C			2.1	3.2	
		85°C			3.6	5.0	
		–40°C	3 V		2.1	3.6	
		25°C			2.3	3.6	
		85°C			4.1	5.5	
$I_{(LPM4)}$	Low-power mode 4 (LPM4), $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1 (see Note 2)	–40°C	2.2 V		0.1	0.5	µA
		25°C			0.1	0.5	
		60°C			0.35	0.9	
		85°C			1.1	2.5	
		–40°C	3 V		0.1	0.8	
		25°C			0.1	0.8	
		60°C			0.8	1.2	
		85°C			1.9	3.5	

NOTES: 1. Timer_A is clocked by $f_{(DCOCLK)}$ = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
2. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
3. The LPM3 currents are characterized with a Micro Crystal CC4V–T1A (9 pF) crystal and OSCCAPx = 01h.

typical characteristics – LPM4 current

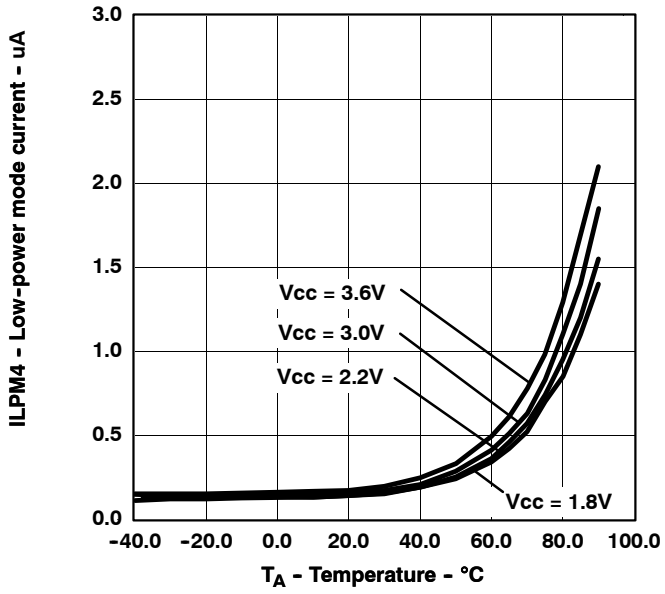


Figure 2. I_{LPM4} – LPM4 Current vs Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – ports P1, P2, P3, P4, P5, P6, and P7, $\overline{RST}$/NMI, JTAG (TCK, TMS, TDI/TCLK, TDO/TDI)

PARAMETER		V_{CC}	MIN	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	2.2 V	1.1	1.55	V
		3 V	1.5	1.98	
V_{IT-}	Negative-going input threshold voltage	2.2 V	0.4	0.9	V
		3 V	0.9	1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	2.2 V	0.3	1.1	V
		3 V	0.5	1	

inputs Px.y, TAx

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag (see Note 1)	2.2 V	62		ns
			3 V	50		
$t_{(cap)}$	Timer_A capture timing	TA0, TA1, TA2	2.2 V	62		ns
			3 V	50		
$f_{(TAext)}$	Timer_A clock frequency externally applied to pin	TACLK, INCLK: $t_{(H)} = t_{(L)}$	2.2 V		8	MHz
			3 V		10	
$f_{(TAint)}$	Timer_A, clock frequency	SMCLK or ACLK signal selected	2.2 V		8	MHz
			3 V		10	

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.

leakage current – ports P1, P2, P3, P4, P5, P6, and P7 (see Note 1)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	Leakage current	Port Px	$V_{(Px.y)}$ (see Note 2)	2.2 V/3 V		±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – ports P1, P2, P3, P4, P5, P6, and P7

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 2.2 V	(see Note 1)	V_{CC}–0.25	V_{CC}	V
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 2.2 V	(see Note 2)	V_{CC}–0.6	V_{CC}	
		$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 3 V	(see Note 1)	V_{CC}–0.25	V_{CC}	
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 3 V	(see Note 2)	V_{CC}–0.6	V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V	(see Note 1)	V_{SS}	V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V	(see Note 2)	V_{SS}	V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V	(see Note 1)	V_{SS}	V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V	(see Note 2)	V_{SS}	V_{SS}+0.6	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(Px.y)}$	(x = 1, 2, 3, 4, 5, 6, 7, 0 ≤ y ≤ 7)	C_L = 20 pF, I_L = ±1.5 mA	V_{CC} = 2.2 V / 3 V	dc		f_{System}	MHz
$f_{(MCLK)}$	P1.1/TA0.0/MCLK/S30	C_L = 20 pF				f_{System}	MHz
$t_{(Xdc)}$	Duty cycle of output frequency	P1.1/TA0.0/MCLK/S30, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(MCLK)} = f_{(XT1)}$	40%		60%	
			$f_{(MCLK)} = f_{(DCOCLK)}$	50%– 15 ns	50%	50%+ 15 ns	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – ports Px (continued)

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

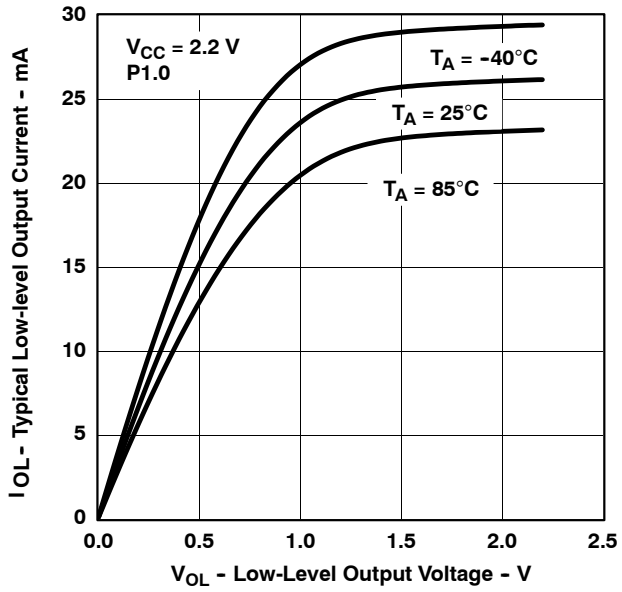


Figure 3

TYPICAL LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

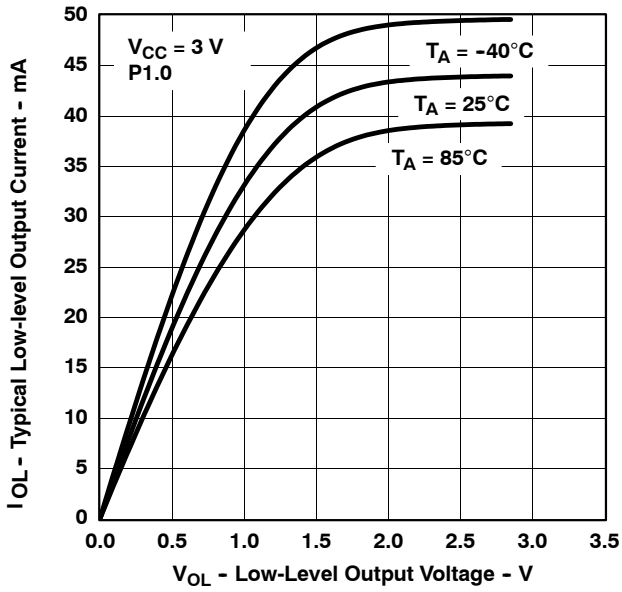


Figure 4

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

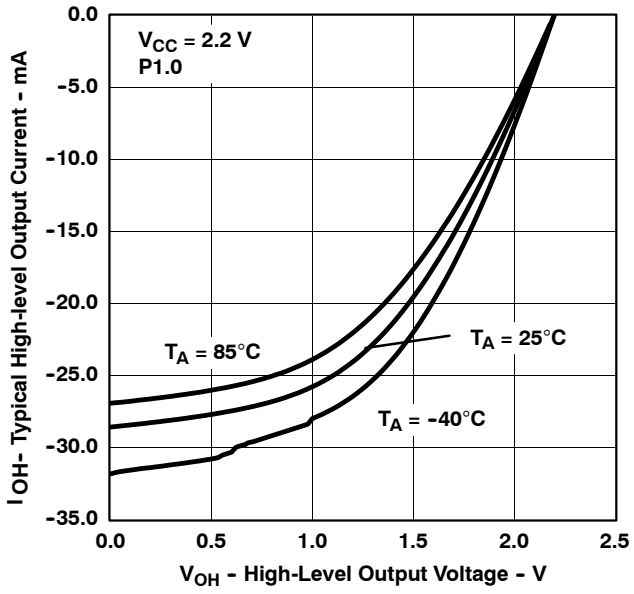


Figure 5

TYPICAL HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

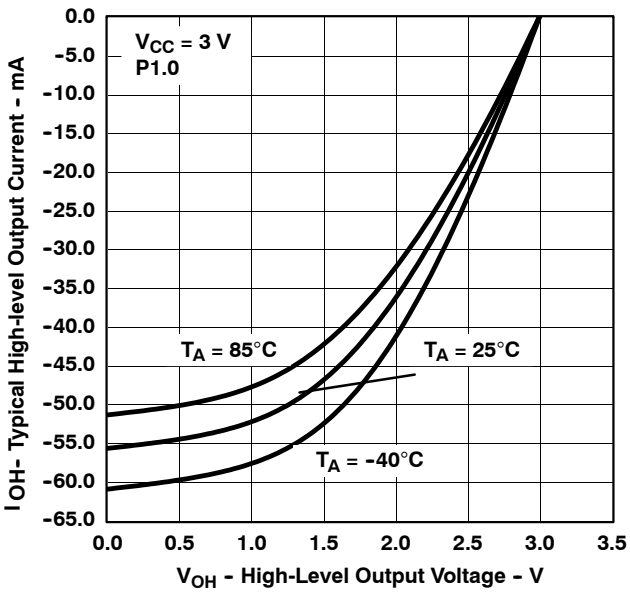


Figure 6

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

wake-up LPM3

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V/3 V		6	µs
		f = 2 MHz			6	
		f = 3 MHz			6	

POR/brownout reset (BOR) (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout (see Note 2)				2000	µs
$V_{CC(start)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 7)		0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 7)			1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 7)				mV
$t_{(reset)}$		Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			µs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8V.

2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout.

typical characteristics

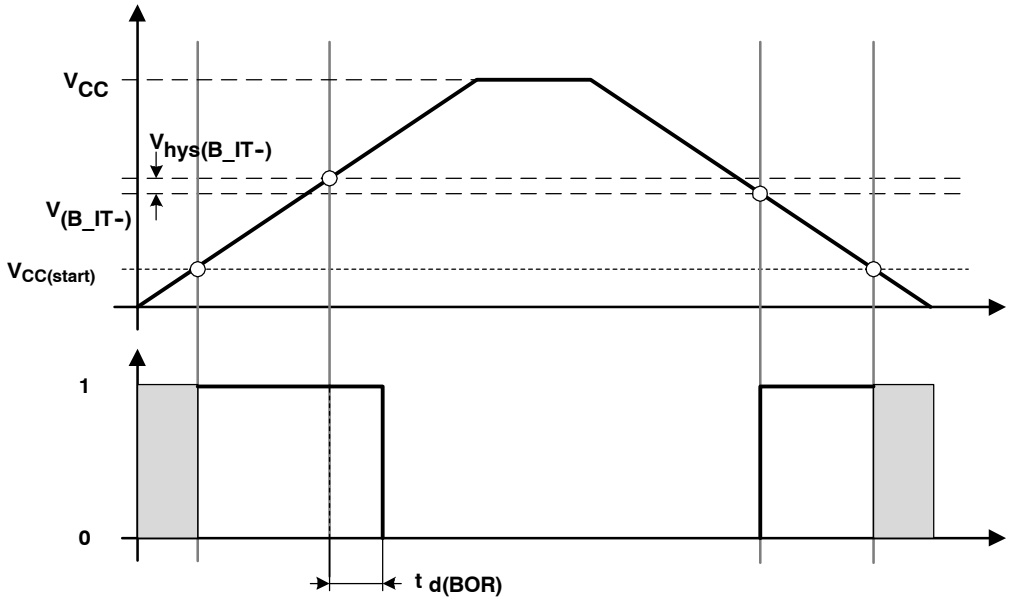


Figure 7. POR/Brownout Reset (BOR) vs Supply Voltage

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

typical characteristics (continued)

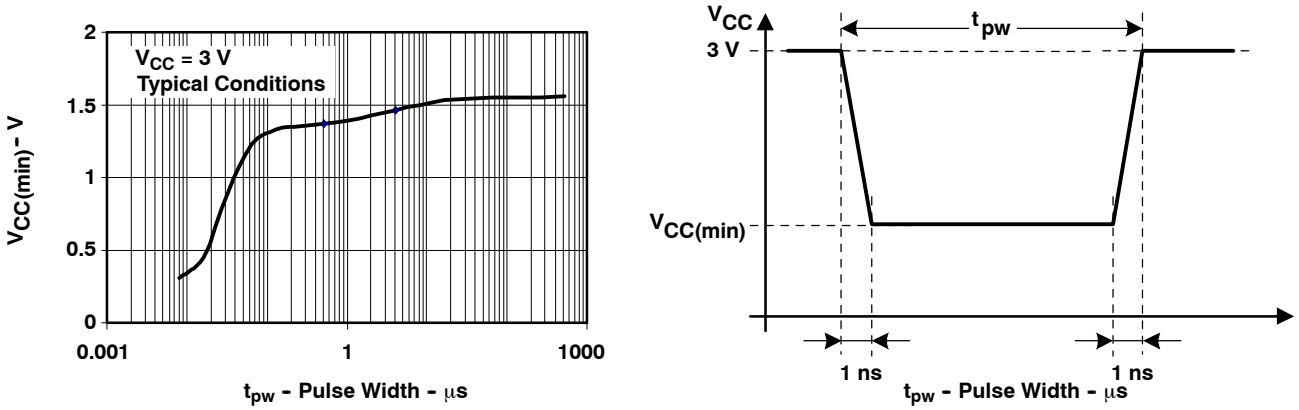


Figure 8. $V_{(CC)min}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

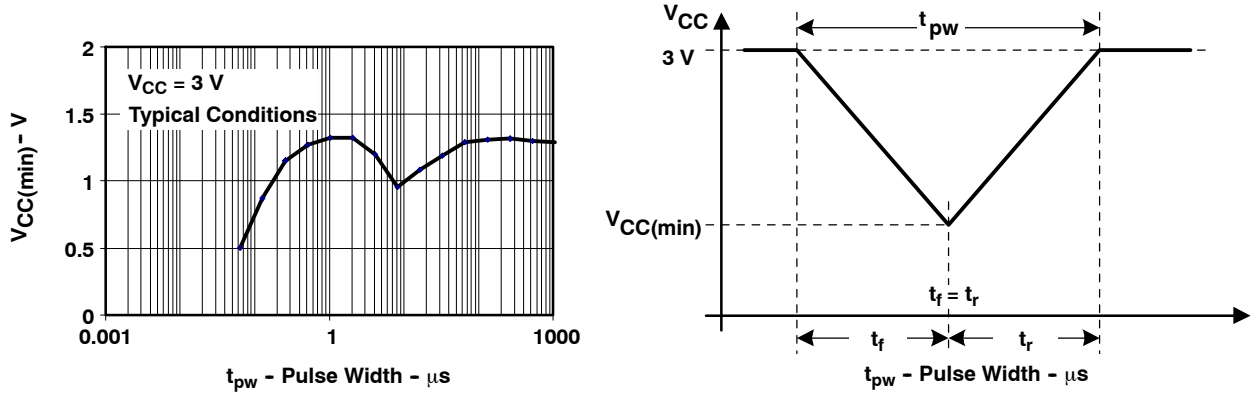


Figure 9. $V_{CC(min)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

SVS (supply voltage supervisor/monitor)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	$dV_{CC}/dt > 30$ V/ms (see Figure 10)		5		150	µs
	$dV_{CC}/dt \le 30$ V/ms				2000	µs
$t_{d(SVSon)}$	SVS_{ON}, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V			150	300	µs
t_{settle}	VLD ≠ 0‡				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \le 3$ V/s (see Figure 10)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 10)	VLD = 1	70	120	210	mV
		VLD = 2 to 14	$V_{(SVS\_IT-)} \times 0.001$		$V_{(SVS\_IT-)} \times 0.016$	
	$V_{CC}/dt \le 3$ V/s (see Figure 10), External voltage applied on A7	VLD = 15	4.4		20	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \le 3$ V/s (see Figure 10 and Figure 11)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61†	
		VLD = 13	3.24	3.5	3.76†	
		VLD = 14	3.43	3.7†	3.99†	
	$V_{CC}/dt \le 3$ V/s (see Figure 10 and Figure 11), External voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (see Note 1)	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	µA

† The recommended operating voltage range is limited to 3.6 V.

‡ t_{settle} is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.

NOTE 1: The current consumption of the SVS module is not included in the I_{CC} current consumption data.

typical characteristics

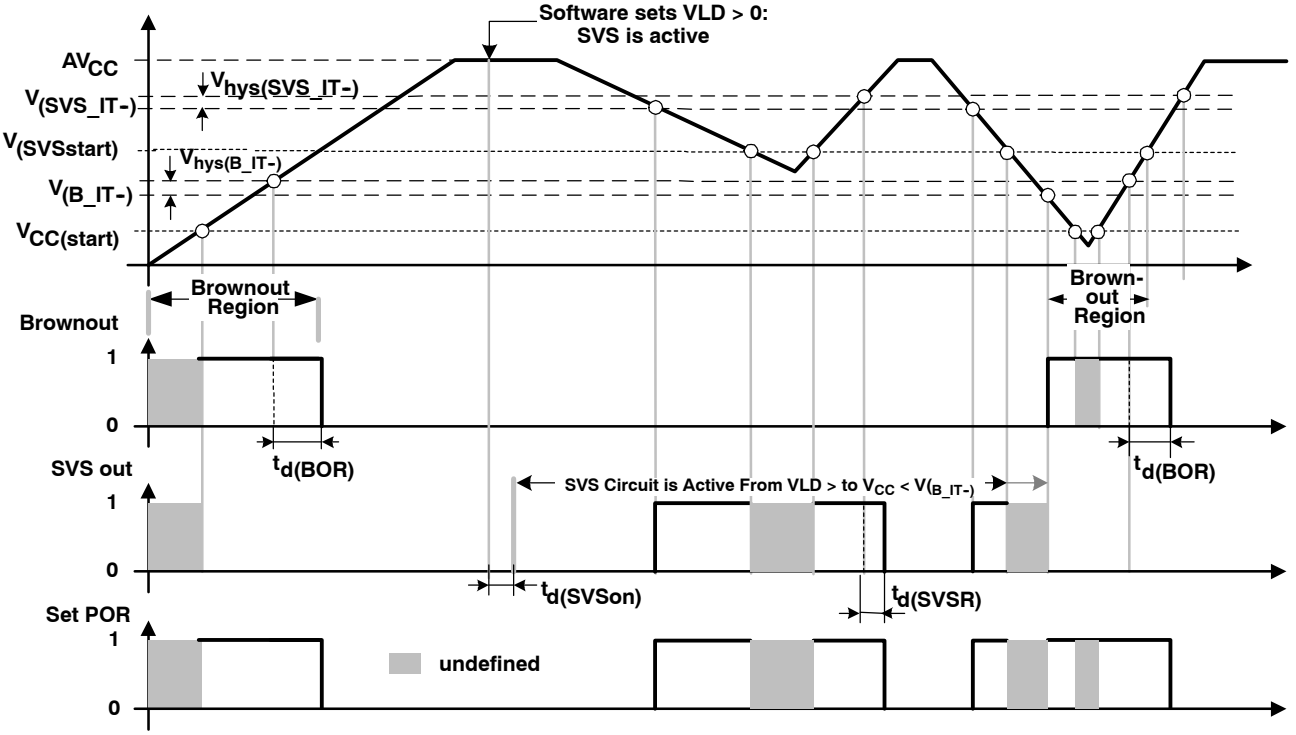


Figure 10. SVS Reset (SVSR) vs Supply Voltage

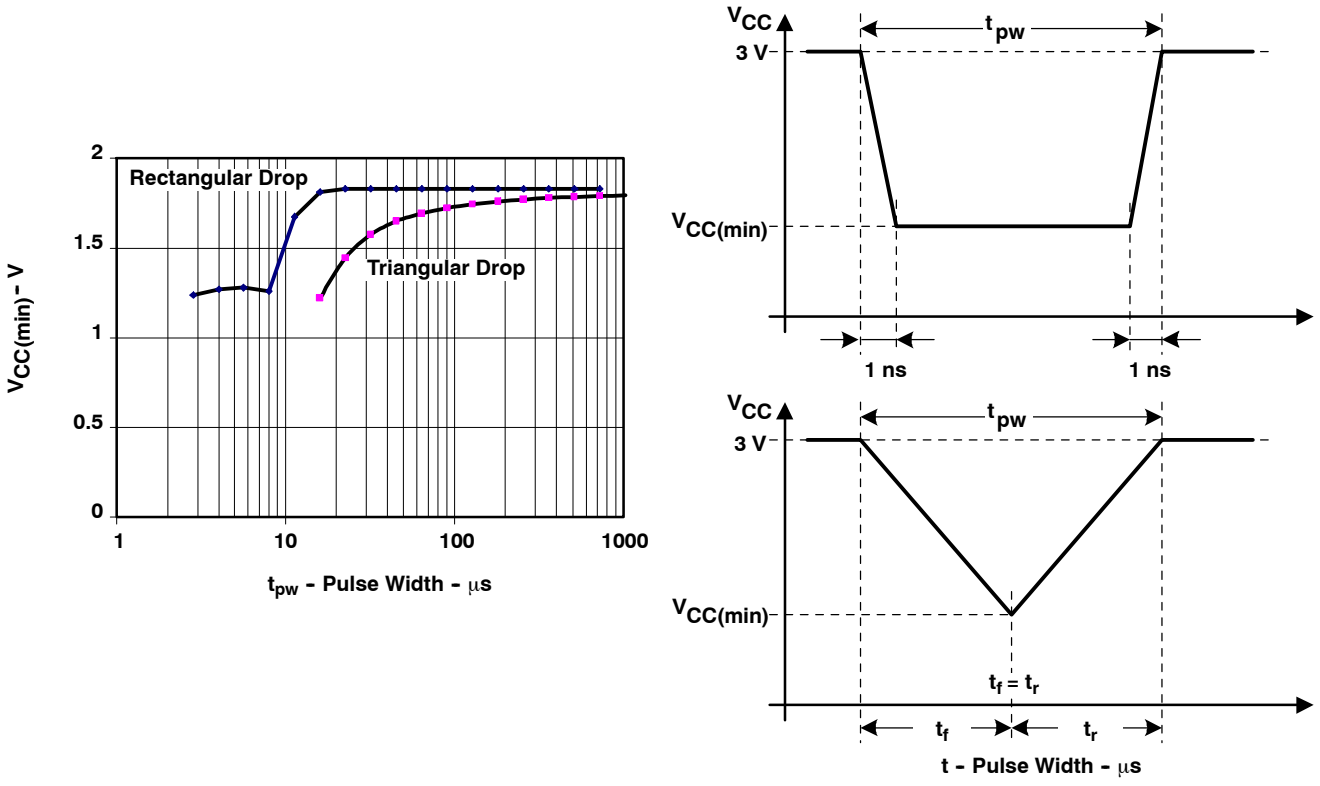


Figure 11. $V_{CC(min)}$: Square Voltage Drop and Triangle Voltage Drop to Generate an SVS Signal (VLD = 1)

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

DCO

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$ = 01E0h, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0	2.2 V/3 V		1		MHz
$f_{(DCO2)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1	2.2 V	0.3	0.65	1.25	MHz
		3 V	0.3	0.7	1.3	
$f_{(DCO27)}$	FN_8 = FN_4 = FN_3 = FN_2 = 0, DCOPLUS = 1 (see Note 1)	2.2 V	2.5	5.6	10.5	MHz
		3 V	2.7	6.1	11.3	
$f_{(DCO2)}$	FN_8 = FN_4 = FN_3 = 0, FN_2 = 1, DCOPLUS = 1	2.2 V	0.7	1.3	2.3	MHz
		3 V	0.8	1.5	2.5	
$f_{(DCO27)}$	FN_8 = FN_4 = FN_3 = 0, FN_2 = 1, DCOPLUS = 1 (see Note 1)	2.2 V	5.7	10.8	18	MHz
		3 V	6.5	12.1	20	
$f_{(DCO2)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1	2.2 V	1.2	2	3	MHz
		3 V	1.3	2.2	3.5	
$f_{(DCO27)}$	FN_8 = FN_4 = 0, FN_3 = 1, FN_2 = x, DCOPLUS = 1 (see Note 1)	2.2 V	9	15.5	25	MHz
		3 V	10.3	17.9	28.5	
$f_{(DCO2)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	1.8	2.8	4.2	MHz
		3 V	2.1	3.4	5.2	
$f_{(DCO27)}$	FN_8 = 0, FN_4 = 1, FN_3 = FN_2 = x, DCOPLUS = 1 (see Note 1)	2.2 V	13.5	21.5	33	MHz
		3 V	16	26.6	41	
$f_{(DCO2)}$	FN_8 = 1, FN_4 = FN_3 = FN_2 = x, DCOPLUS = 1	2.2 V	2.8	4.2	6.2	MHz
		3 V	4.2	6.3	9.2	
$f_{(DCO27)}$	FN_8 = 1,FN_4 = FN_3 = FN_2 = x, DCOPLUS = 1 (see Note 1)	2.2 V	21	32	46	MHz
		3 V	30	46	70	
S_n	Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$, (see Figure 13 for taps 21 to 27)	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01E0h, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0	2.2 V	–0.2	–0.4	-0.6	%/°C
		3 V	–0.2	–0.4	-0.6	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01E0h, FN_8 = FN_4 = FN_3 = FN_2 = 0, D = 2, DCOPLUS = 0		0	5	15	%/V

NOTES: 1. Do not exceed the maximum system frequency.

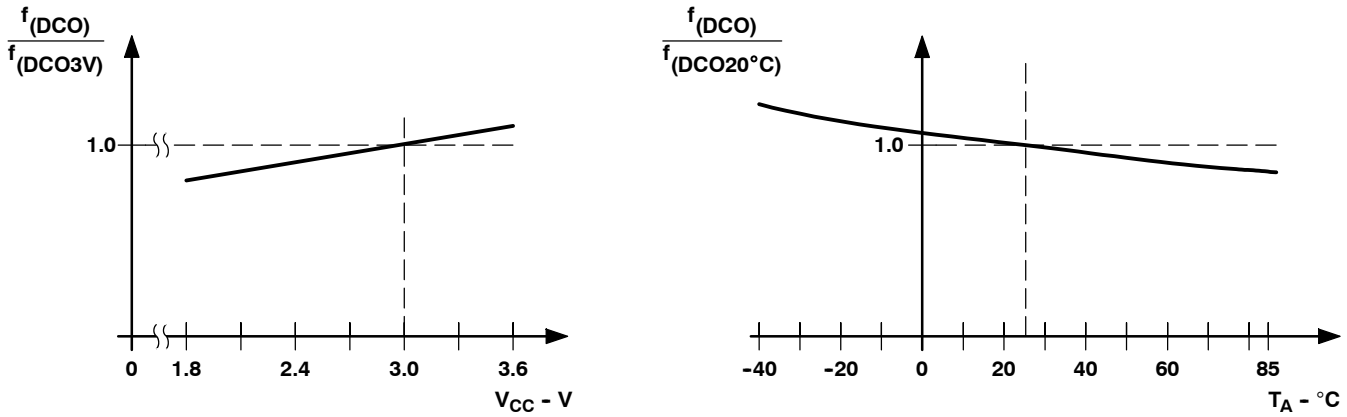


Figure 12. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

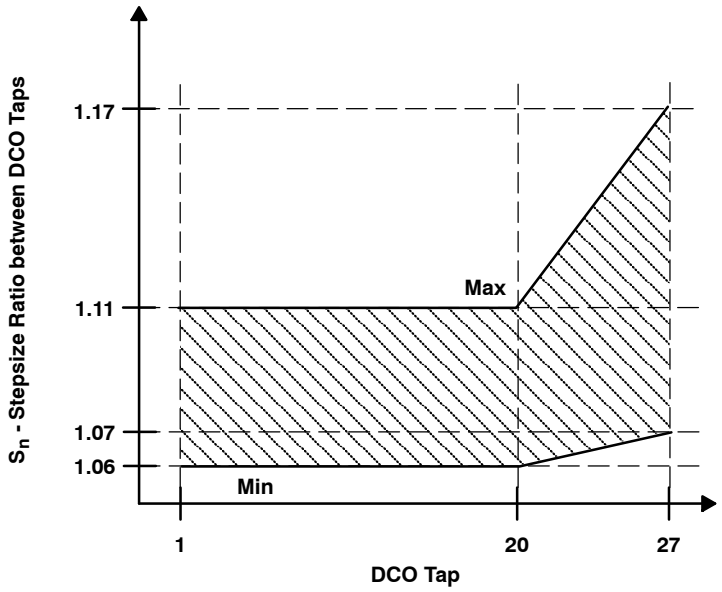


Figure 13. DCO Tap Step Size

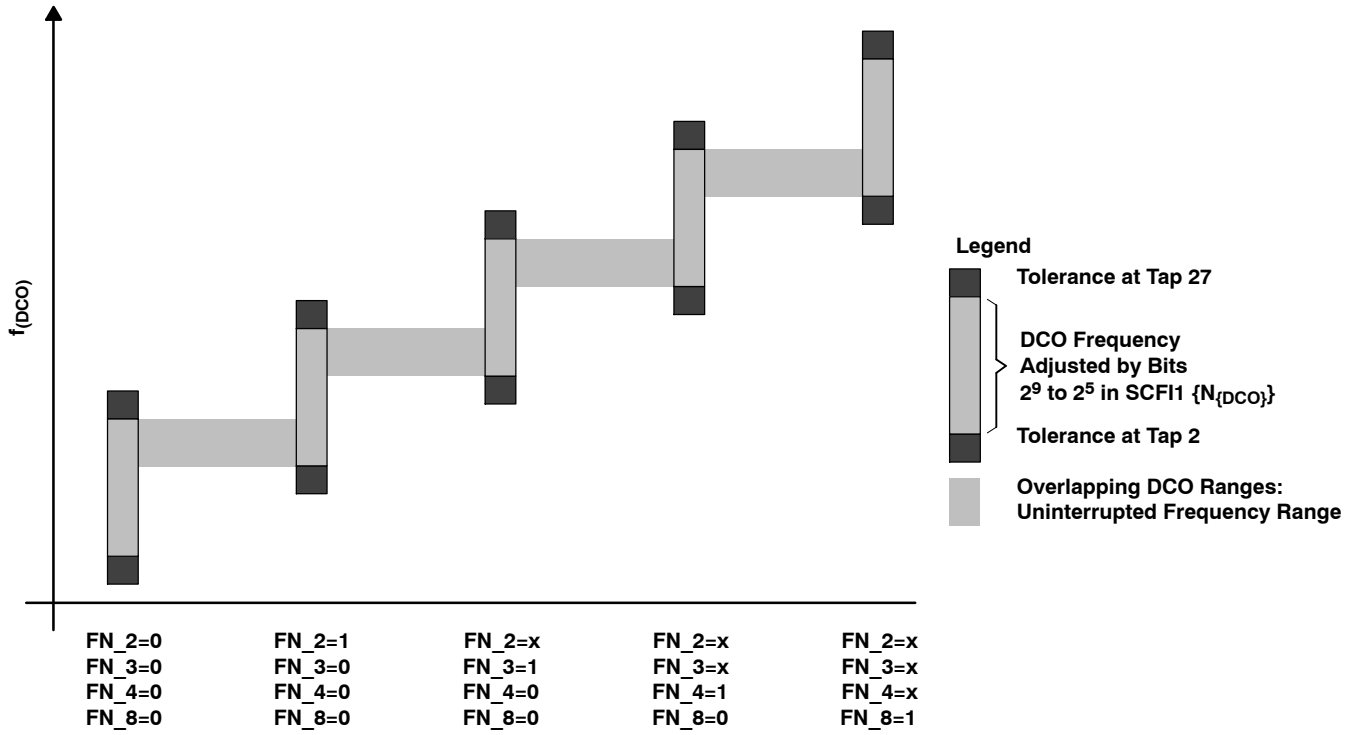


Figure 14. Five Overlapping DCO Ranges Controlled by FN_x Bits

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

crystal oscillator, LFXT1, low-frequency modes (see Note 4)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 kHz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 kHz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode (see Note 1)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
Duty cycle	LF mode	XTS = 0, Measured at P1.6/ACLK, $f_{LFXT1,LF}$ = 32768Hz	2.2 V/3 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode (see Note 3)	XTS = 0, XCAPx = 0. LFXT1Sx = 3 (see Note 2)	2.2 V/3 V	10		10000	Hz

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Measured with logic level input frequency but also applies to operation with crystals.
3. Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.
4. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
   - Keep the trace between the device and the crystal as short as possible.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

crystal oscillator, LFXT1, high frequency modes

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{LFXT1}	LFXT1 oscillator crystal frequency	Ceramic resonator	1.8 V to 3.6 V	0.45		6	MHz
		Crystal resonator	1.8 V to 3.6 V	1		6	
$C_{L,eff}$	Integrated effective load capacitance, HF mode (see Note 1)	See Note 2			1		pF
Duty cycle		Measured at P1.6/ACLK	2.2 V/3 V	40	50	60	%

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

internal very low power, low-frequency oscillator (VLO)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	T_A = –40°C to 85°C	2.2 V/3 V	4	12	20	kHz
df_{VLO}/dT	VLO frequency temperature drift	See Note	2.2 V/3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	See Note 2	1.8V to 3.6V		4		%/V

NOTES: 1. Calculated using the box method:
I Version: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C))/MIN(–40°C to 85°C)/(85°C – (–40°C))
2. Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V))/MIN(1.8 V to 3.6 V)/(3.6 V – 1.8 V)

RAM

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
VRAMh	See Note 1	CPU halted	1.6		V

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

LCD_A

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(LCD)}$	Supply voltage range	Charge pump enabled (LCDCPEN = 1, VLCDx > 0000)		2.2		3.6	V
C_{LCD}	Capacitor on LCDCAP (see Note 1)	Charge pump enabled (LCDCPEN = 1, VLCDx > 0000)		4.7			μF
$I_{CC(LCD)}$	Average supply current (see Note 2)	$V_{LCD(typ)}$=3V, LCDCPEN = 1, VLCDx= 1000, all segments on f_{LCD}= f_{ACLK}/32 no LCD connected (see Note 3) T_A = 25°C	2.2 V		3.8		μA
f_{LCD}	LCD frequency					1.1	kHz
V_{LCD}	LCD voltage	VLCDx = 0000			V_{CC}		V
V_{LCD}	LCD voltage	VLCDx = 0001			2.60		V
V_{LCD}	LCD voltage	VLCDx = 0010			2.66		V
V_{LCD}	LCD voltage	VLCDx = 0011			2.72		V
V_{LCD}	LCD voltage	VLCDx = 0100			2.78		V
V_{LCD}	LCD voltage	VLCDx = 0101			2.84		V
V_{LCD}	LCD voltage	VLCDx = 0110			2.90		V
V_{LCD}	LCD voltage	VLCDx = 0111			2.96		V
V_{LCD}	LCD voltage	VLCDx = 1000			3.02		V
V_{LCD}	LCD voltage	VLCDx = 1001			3.08		V
V_{LCD}	LCD voltage	VLCDx = 1010			3.14		V
V_{LCD}	LCD voltage	VLCDx = 1011			3.20		V
V_{LCD}	LCD voltage	VLCDx = 1100			3.26		V
V_{LCD}	LCD voltage	VLCDx = 1101			3.32		V
V_{LCD}	LCD voltage	VLCDx = 1110			3.38		V
V_{LCD}	LCD voltage	VLCDx = 1111			3.44	3.60	V
R_{LCD}	LCD driver output impedance	V_{LCD} = 3 V, LCDCPEN = 1, VLCDx = 1000, I_{LOAD} = ±10 μA	2.2 V			10	kΩ

NOTES: 1. Enabling the internal charge pump with an external capacitor smaller than the minimum specified might damage the device.
2. Refer to the supply current specifications $I_{(LPM3)}$ for additional current specifications with the LCD_A module active.
3. Connecting an actual display will increase the current consumption depending on the size of the LCD.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Comparator_A+ (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(CC)}$		CAON = 1, CARSEL = 0, CAREF = 0	2.2 V		25	40	μA
			3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P1.6/CA0 and P1.7/CA1	2.2 V		30	50	μA
			3 V		45	80	
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P1.6/CA0 and P1.7/CA1	2.2 V / 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5 } V_{CC} \text{ node}}{V_{CC}}$	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P1.6/CA0 and P1.7/CA1	2.2V / 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	See Figure 15 and Figure 16	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P1.6/CA0 and P1.7/CA1, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
V_{IC}	Common-mode input voltage range	CAON = 1	2.2 V / 3 V	0		V_{CC}–1	V
V_p–V_S	Offset voltage	See Note 2	2.2 V / 3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON = 1	2.2 V / 3 V	0	0.7	1.4	mV
$t_{(response\ LH\ and\ HL)}$ (see Note 3)		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	2.2 V	80	165	300	ns
			3 V	70	120	240	
		T_A = 25°C Overdrive 10 mV, with filter: CAF = 1	2.2 V	1.4	1.9	2.8	μs
			3 V	0.9	1.5	2.2	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.
3. The response time is measured at P1.6/CA0 with an input voltage step and the Comparator_A already enabled (CAON=1). If CAON is set at the same time, a settling time of up to 300ns is added to the response time.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

typical characteristics

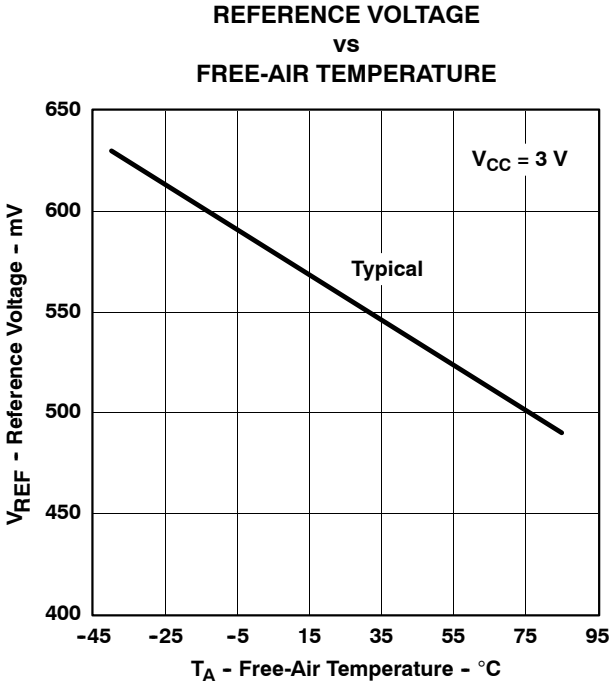


Figure 15. $V_{(RefVT)}$ vs Temperature

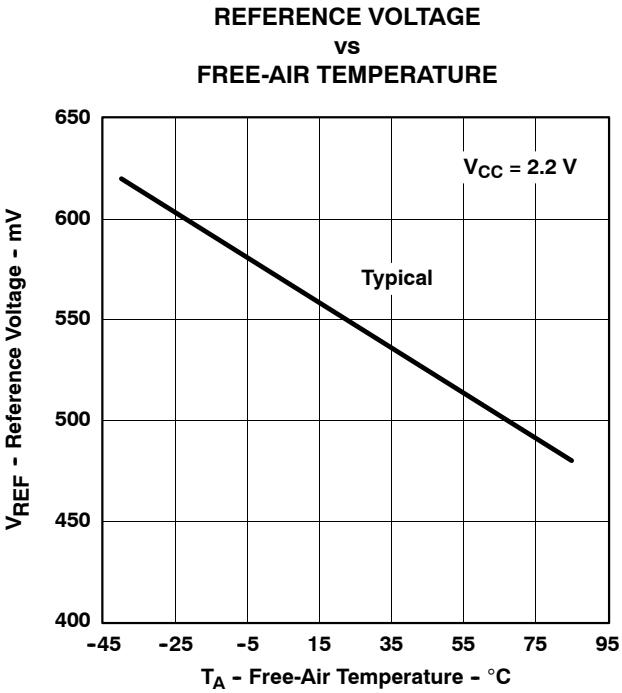


Figure 16. $V_{(RefVT)}$ vs Temperature

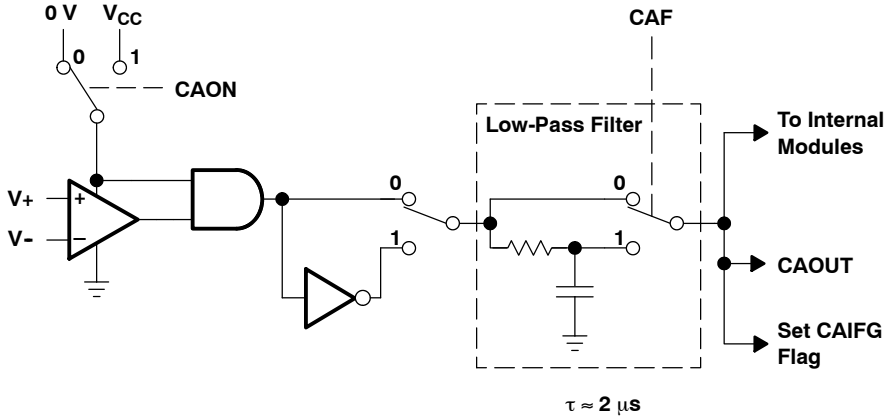


Figure 17. Block Diagram of Comparator_A Module

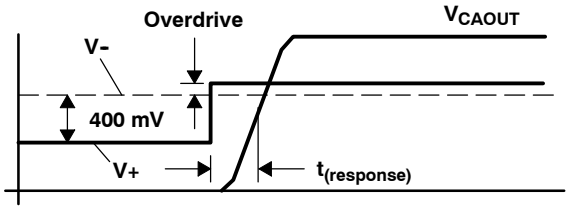


Figure 18. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, power supply and input range conditions (see Note)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Analog supply voltage range	V_{SS} = 0 V		2.2		3.6	V
V_{Ax}	Analog input voltage range (see Note 2)	All Ax terminals, Analog inputs selected in ADC10AE register		0		V_{CC}	V
I_{ADC10}	ADC10 supply current (see Note 3)	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0 ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	2.2 V		0.52	1.05	mA
			3 V		0.6	1.2	
I_{REF+}	Reference supply current, reference buffer disabled (see Note 4)	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	2.2 V/3 V		0.25	0.4	mA
		$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0	3 V				mA
$I_{REFB,0}$	Reference buffer supply current with ADC10SR = 0 (see Note 4)	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0	2.2 V/3 V		1.1	1.4	mA
			2.2 V/3 V			1.8	mA
$I_{REFB,1}$	Reference buffer supply current with ADC10SR = 1 (see Note 4)	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 1	2.2 V/3 V		0.5	0.7	mA
			2.2 V/3 V			0.8	mA
C_I	Input capacitance	Only one terminal Ax selected at a time				27	pF
R_I	Input MUX ON resistance	$0V \le V_{Ax} \le V_{CC}$	2.2 V/3 V			2000	Ω

NOTES: 1. The leakage current is defined in the leakage current table with Px.x/Ax parameter.
2. The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
3. The internal reference supply current is not included in current consumption parameter I_{ADC10}.
4. The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, built-in voltage reference

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC,REF+}$	Positive built-in reference analog supply voltage range	$I_{VREF+} \le 1$ mA, REF2_5V = 0			2.2			V
		$I_{VREF+} \le 0.5$ mA, REF2_5V = 1			2.8			
		$I_{VREF+} \le 1$ mA, REF2_5V = 1			2.9			
V_{REF+}	Positive built-in reference voltage	$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 0		2.2 V/ 3 V	1.41	1.5	1.59	V
		$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 1		3 V	2.35	2.5	2.65	V
$I_{LD,VREF+}$	Maximum V_{REF+} load current			2.2 V			±0.5	mA
				3 V			±1	
	V_{REF+} load regulation	I_{VREF+} = 500 μA ± 100 μA, Analog input voltage $V_{Ax} \approx 0.75$ V, REF2_5V = 0		2.2 V/ 3 V			±2	LSB
		I_{VREF+} = 500 μA ± 100 μA, Analog input voltage $V_{Ax} \approx 1.25$ V, REF2_5V = 1		3 V			±2	LSB
	V_{REF+} load regulation response time	I_{VREF+} = 100 μA→900 μA, $V_{Ax} \approx 0.5 \times V_{REF+}$, Error of conversion result ≤ 1 LSB	ADC10SR = 0	3 V			400	ns
			ADC10SR = 1	3V			2000	
C_{VREF+}	Max. capacitance at pin V_{REF+} (see Note 1)	$I_{VREF+} \le$ ±1 mA, REFON = 1, REFOUT = 1		2.2 V/ 3 V			100	pF
TC_{REF+}	Temperature coefficient	I_{VREF+} = const. with 0 mA ≤ $I_{VREF+} \le 1$ mA (see Note 3)		2.2 V/ 3 V			±100	ppm/°C
t_{REFON}	Settling time of internal reference voltage (see Note 2)	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 → 1		3.6 V			30	μs
$t_{REFBURST}$	Settling time of reference buffer (see Note 2)	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 1, REFBURST = 1	ADC10SR = 0	2.2 V			1	μs
			ADC10SR = 1	2.2 V			2.5	
		I_{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1	ADC10SR = 0	3 V			2	
			ADC10SR = 1	3 V			4.5	

NOTES: 1. The capacitance applied to the internal buffer operational amplifier, if switched to terminal P6.4/UCB0CLK/UCA0STE/A4/CA6/V_{eref+}/V_{ref+} (REFOUT = 1), must be limited; the reference buffer may become unstable, otherwise.
2. The condition is that the error in a conversion started after t_{REFON} or t_{RefBuf} is less than ±0.5 LSB.
3. Calculated using the box method: ((MAX(V_{REF}(T)) – MIN(V_{REF}(T))) / MIN(V_{REF}(T)) / (T_{MAX} – T_{MIN})

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, external reference (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference input voltage range (see Note 2)	$V_{eREF+} > V_{eREF-}$, SREF1 = 1, SREF0 = 0		1.4		V_{CC}	V
		$V_{eREF-} \le V_{eREF+} \le (V_{CC} - 0.15\ V)$ SREF1 = 1, SREF0 = 1 (see Note 3)		1.4		3.0	
V_{eREF-}	Negative external reference input voltage range (see Note 4)	$V_{eREF+} > V_{eREF-}$		0		1.2	V
ΔV_{eREF}	Differential external reference input voltage range $\Delta V_{eREF} = V_{eREF+} - V_{eREF-}$	$V_{eREF+} > V_{eREF-}$ (see Note 5)		1.4		V_{CC}	V
I_{VeREF+}	Static input current into V_{eREF+}	$0V \le V_{eREF+} \le V_{CC}$, SREF1 = 1, SREF0 = 0	2.2 V/3 V			±1	µA
		$0V \le V_{eREF+} \le (V_{CC} - 0.15\ V) \le 3\ V$, SREF1 = 1, SREF0 = 1 (see Note 3)	2.2 V/3 V			0	
I_{VeREF-}	Static input current into V_{eREF-}	$0V \le V_{eREF-} \le V_{CC}$	2.2 V/3 V			±1	µA

NOTES:
1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
4. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
5. The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, timing parameters

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$	ADC10 input clock frequency	For specified performance of ADC10 linearity parameters	ADC10SR = 0	2.2 V/3 V	0.45		6.3	MHz
			ADC10SR = 1	2.2 V/3 V	0.45		1.5	
$f_{ADC10OSC}$	ADC10 built-in oscillator frequency	ADC10DIVx = 0, ADC10SSELx = 0 $f_{ADC10CLK} = f_{ADC10OSC}$		2.2 V/3 V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0 $f_{ADC10CLK} = f_{ADC10OSC}$		2.2 V/3 V	2.06		3.51	µs
		$f_{ADC10CLK}$ from ACLK, MCLK or SMCLK: ADC10SSELx ≠ 0			13× ADC10DIV× $1/f_{ADC10CLK}$			µs
$t_{ADC10ON}$	Turn on settling time of the ADC	See Note 1					100	ns

NOTE 1: The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signals are already settled.

10-bit ADC, linearity parameters

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error		2.2 V/3 V			±1	LSB
E_D	Differential linearity error		2.2 V/3 V			±1	LSB
E_O	Offset error	Source impedance R_S < 100 Ω	2.2 V/3 V			±1	LSB
E_G	Gain error	SREFx = 010, Unbuffered external reference, V_{eREF+} = 1.5 V	2.2 V		±1.1	±2	LSB
		SREFx = 010, Unbuffered external reference, V_{eREF+} = 2.5 V	3 V		±1.1	±2	LSB
		SREFx = 011, Buffered external reference (see Note 2), V_{eREF+} = 1.5 V	2.2 V		±1.1	±4	LSB
		SREFx = 011, Buffered external reference (see Note 2), V_{eREF+} = 2.5 V	3 V		±1.1	±3	LSB
E_T	Total unadjusted error	SREFx = 010, Unbuffered external reference, V_{eREF+} = 1.5 V	2.2 V		±2	±5	LSB
		SREFx = 010, Unbuffered external reference, V_{eREF+} = 2.5 V	3 V		±2	±5	LSB
		SREFx = 011, Buffered external reference (see Note 2), V_{eREF+} = 1.5 V	2.2 V		±2	±7	LSB
		SREFx = 011, Buffered external reference (see Note 2), V_{eREF+} = 2.5 V	3 V		±2	±6	LSB

NOTE 1: The reference buffer's offset adds to the gain and total unadjusted error.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, temperature sensor and built-in V_{MID}

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Temperature sensor supply current (see Note)	REFON = 0, INCHx = 0Ah, ADC10ON = 1, T_A = 25°C	2.2 V		40	120	μA
			3 V		60	160	
TC_{SENSOR}		ADC10ON = 1, INCHx = 0Ah (see Note 2)	2.2 V/3 V		3.55		mV/°C
$V_{Offset,Sensor}$	Sensor offset voltage	ADC10ON = 1, INCHx = 0Ah (see Note 2)		–100		100	mV
V_{Sensor}	Sensor output voltage (see Note 3)	Temperature sensor voltage at T_A = 85°C	2.2 V/3 V	1195	1295	1395	mV
		Temperature sensor voltage at T_A = 25°C	2.2 V/3 V	985	1085	1185	mV
		Temperature sensor voltage at T_A = 0°C	2.2 V/3 V	895	995	1095	
$t_{Sensor(sample)}$	Sample time required if channel 10 is selected (see Note 4)	ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V/3 V	30			μs
I_{VMID}	Current into divider at channel11 (see Note 5)	ADC10ON = 1, INCHx = 0Bh	2.2 V			NA	μA
			3 V			NA	
V_{MID}	V_{CC} divider at channel 11	ADC10ON = 1, INCHx = 0Bh, V_{MID} is ≈0.5 x V_{CC}	2.2 V	1.06	1.1	1.14	V
			3 V	1.46	1.5	1.54	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (see Note 6)	ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

NOTES:
1. The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1), or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
2. The following formula can be used to calculate the temperature sensor output voltage:
   $V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV] or
   $V_{Sensor,typ} = TC_{Sensor}$ T [°C] + $V_{Sensor}(T_A = 0°C)$ [mV]
3. Results based on characterization and/or production test, not TC_{Sensor} or $V_{Offset,sensor}$.
4. The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
5. No additional current is needed. The V_{MID} is used during sampling.
6. The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

Timer0_A3, Timer1_A5

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK, External: TACLK, INCLK, Duty cycle = 50% ±10%	2.2 V		8	MHz
			3 V		10	
$t_{TA,cap}$	Timer_A, capture timing	TA0, TA1, TA2	2.2 V/3 V	20		ns

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (UART mode)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$f_{max,BITCLK}$	Maximum BITCLK clock frequency (equals baudrate in MBaud) (see Note 1)		2.2V /3 V	2			MHz
t_{τ}	UART receive deglitch time (see Note 2)		2.2 V	50	150		ns
			3 V	50	100		

NOTES: 1. The DCO wake-up time must be considered in LPM3/4 for baudrates above 1 MHz.
2. Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed.

USCI (SPI master mode) (see Figure 19 and Figure 20)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ± 10%			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		2.2 V	110		ns
			3 V	75		
$t_{HD,MI}$	SOMI input data hold time		2.2 V	0		ns
			3 V	0		
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V		30	ns
			3 V		20	

NOTE: $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ refer to the SPI parameters of the attached slave.

USCI (SPI slave mode) (see Figure 21 and Figure 22)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time STE low to clock		2.2 V/3 V		50		ns
$t_{STE,LAG}$	STE lag time Last clock to STE high		2.2 V/3 V	10			ns
$t_{STE,ACC}$	STE access time STE low to SOMI data out		2.2 V/3 V		50		ns
$t_{STE,DIS}$	STE disable time STE high to SOMI high impedance		2.2 V/3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			
$t_{HD,SI}$	SIMO input data hold time		2.2 V	10			ns
			3 V	10			
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		75	110	ns
			3 V		50	75	

NOTE: $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ refer to the SPI parameters of the attached master.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

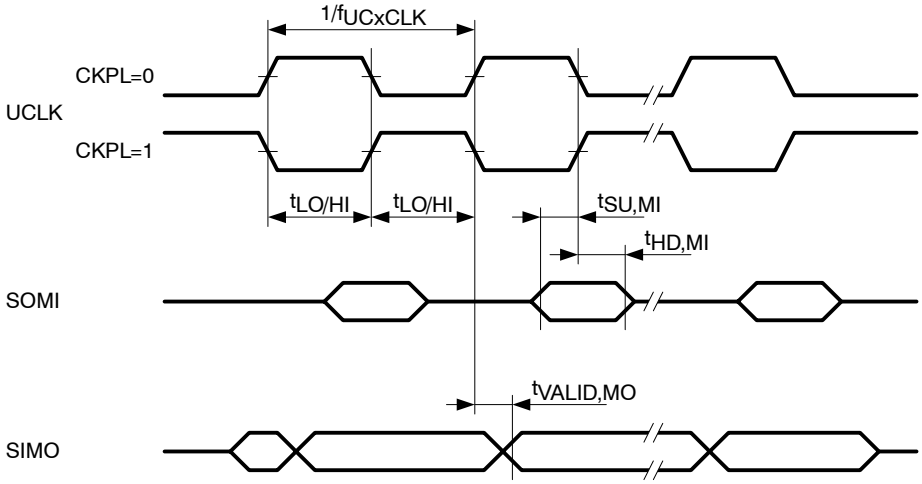


Figure 19. SPI Master Mode, CKPH = 0

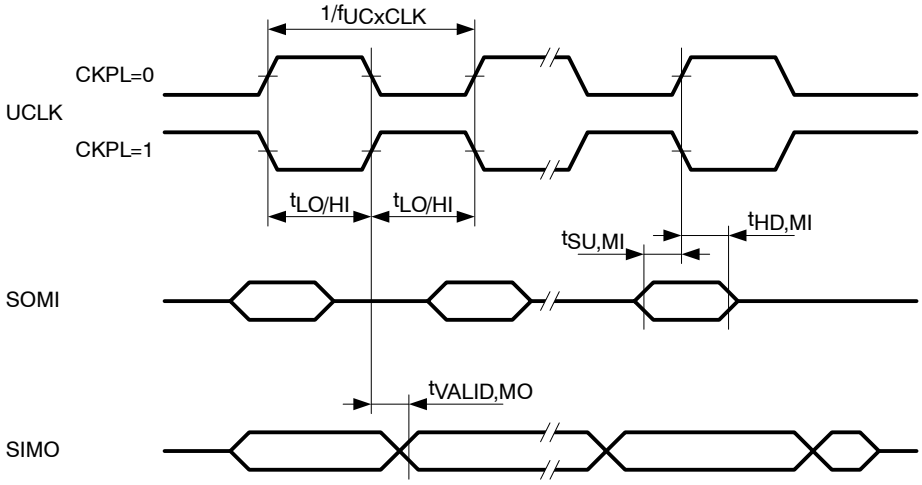


Figure 20. SPI Master Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

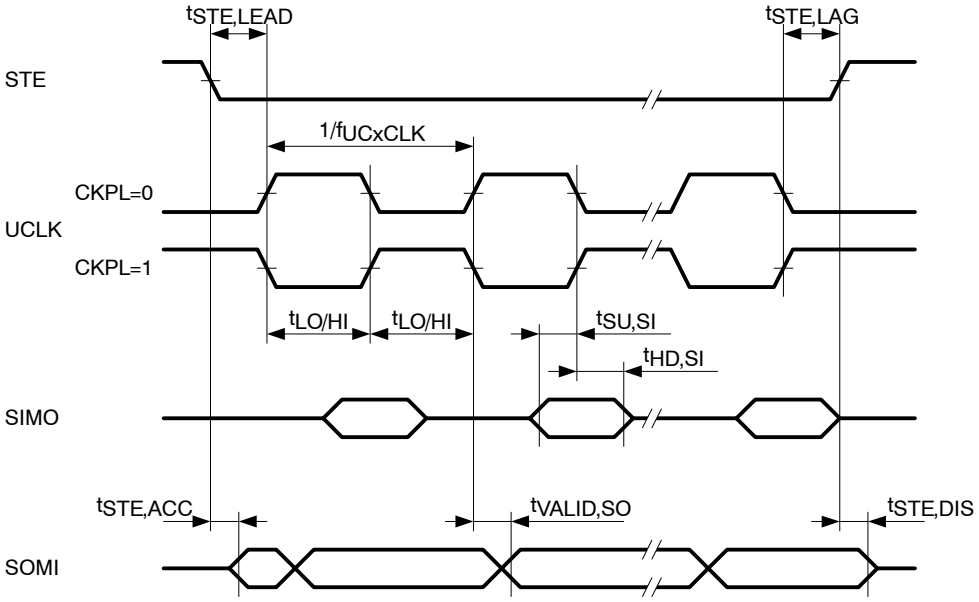


Figure 21. SPI Slave Mode, CKPH = 0

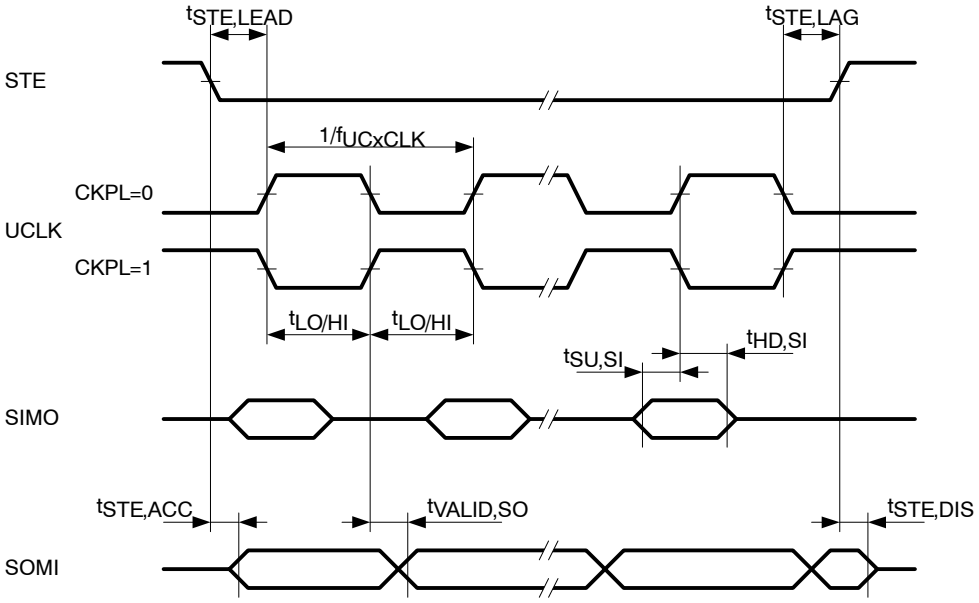


Figure 22. SPI Slave Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (I2C mode) (see Figure 23)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V/3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \le 100kHz$	2.2 V/3 V	4.0			us
		$f_{SCL} > 100kHz$	2.2 V/3 V	0.6			us
$t_{SU,STA}$	Setup time for a repeated START	$f_{SCL} \le 100kHz$	2.2 V/3 V	4.7			us
		$f_{SCL} > 100kHz$	2.2 V/3 V	0.6			us
$t_{HD,DAT}$	Data hold time		2.2 V/3 V	0			ns
$t_{SU,DAT}$	Data set-up time		2.2 V/3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		2.2 V/3 V	4.0			us
t_{SP}	Pulse width of spikes suppressed by input filter		2.2 V	50	150	600	ns
			3 V	50	100	600	ns

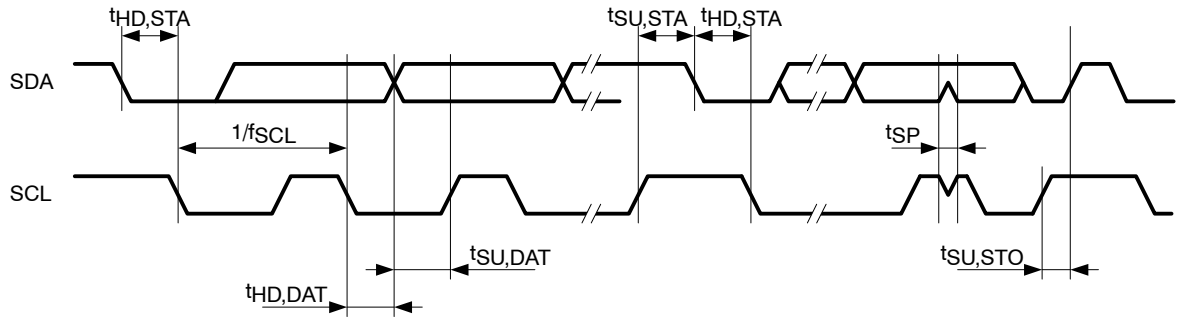


Figure 23. I2C Mode Timing

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

flash memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.2		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.5V/3.6V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase		2.5V/3.6V		3	7	mA
t_{CPT}	Cumulative program time	see Note 1	2.5V/3.6V			10	ms
$t_{CMErase}$	Cumulative mass erase time	see Note 2	2.5V/3.6V	200			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 3			35		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				30		
$t_{Block, 1-63}$	Block program time for each additional byte or word				21		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				5297		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1 ms (= 5297x1 / f_{FTG}, max = 5297 x 1 / 476 kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles is required.)
3. These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1 / f_{FTG}).

JTAG and Spy-Bi-Wire interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency		2.2 V/3 V	0		8	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse length		2.2 V/3 V	0.025		15	us
$t_{SBW,En}$	Spy-Bi-Wire enable time, TEST high to acceptance of first clock edge (see Note 1)		2.2 V/3 V			1	us
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time		2.2 V/3 V	15		100	us
f_{TCK}	TCK input frequency (see Note 2)		2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pulldown resistance on TEST		2.2 V/3 V	25	60	90	kΩ

NOTES: 1. Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
2. f_{TCK} may be restricted to meet the timing requirements of the module selected.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

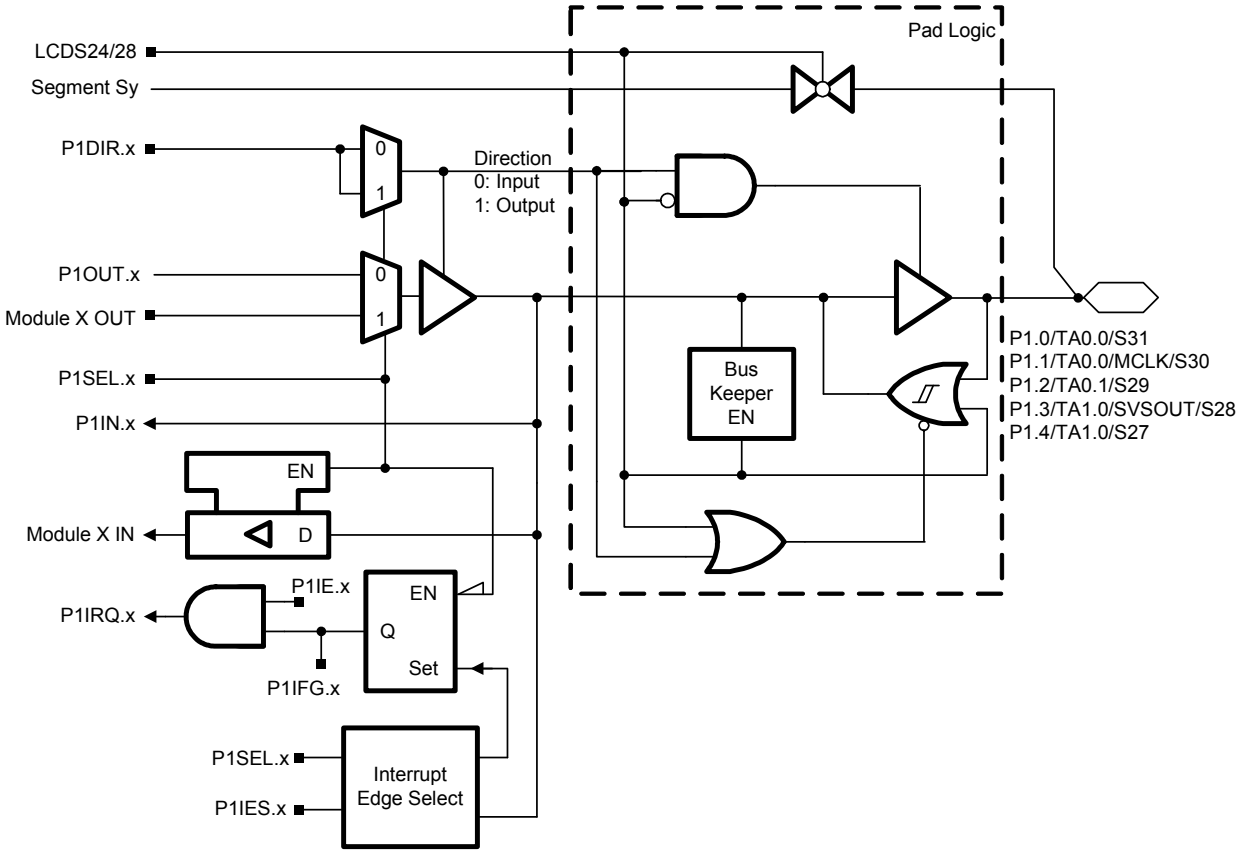
JTAG fuse (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5		V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow			6	7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow				100	mA
t_{FB}	Time to blow fuse				1	ms

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

APPLICATION INFORMATION

Port P1 pin schematic: P1.0 to P1.4, input/output with Schmitt trigger



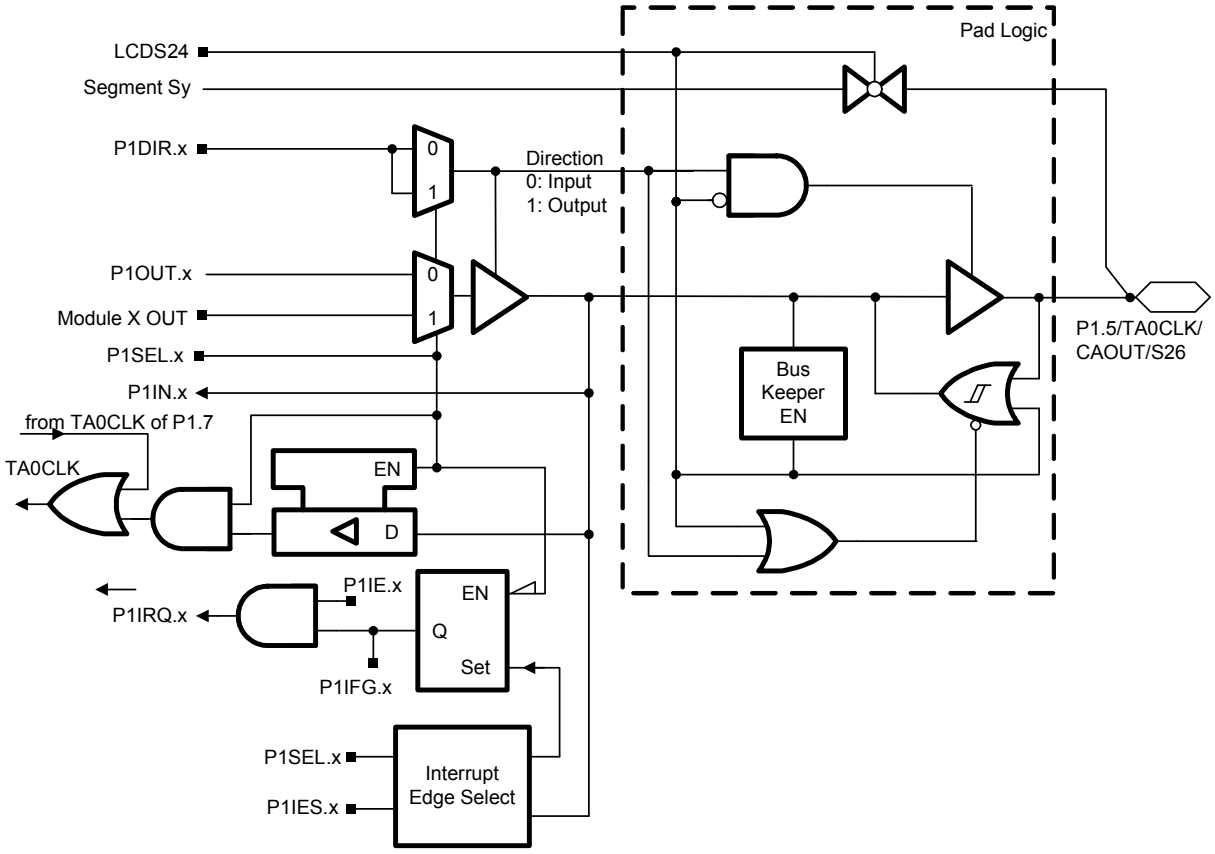
Port P1 (P1.0 to P1.4) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	LCDS24 LCDS28
P1.0/TA0.0/S31	0	P1.x (I/O)	I: 0, O: 1	0	0
		Timer0_A3.CCI0A	0	1	0
		Timer0_A3.TA0	1	1	0
		S31	x	x	1 (LCDS28)
P1.1/TA0.0/MCLK/S30	1	P1.x (I/O)	I: 0, O: 1	0	0
		Timer0_A3.CCI0B	0	1	0
		MCLK	1	1	0
		S30	x	x	1 (LCDS28)
P1.2/TA0.1/S29	2	P1.x (I/O)	I: 0, O: 1	0	0
		Timer0_A3.CCI1A	0	1	0
		Timer0_A3.TA1	1	1	0
		S29	x	x	1 (LCDS28)
P1.3/TA1.0/SVSOUT/S28	3	P1.x (I/O)	I: 0, O: 1	0	0
		Timer1_A5.CCI0B	0	1	0
		SVSOUT	1	1	0
		S28	x	x	1 (LCDS28)
P1.4/TA1.0/S27	4	P1.x (I/O)	I: 0, O: 1	0	0
		Timer1_A5.CCI0A	0	1	0
		Timer1_A5.TA0	1	1	0
		S27	x	x	1 (LCDS24)

NOTES: 1. x: Don’t care

APPLICATION INFORMATION

Port P1 pin schematic: P1.5, input/output with Schmitt trigger



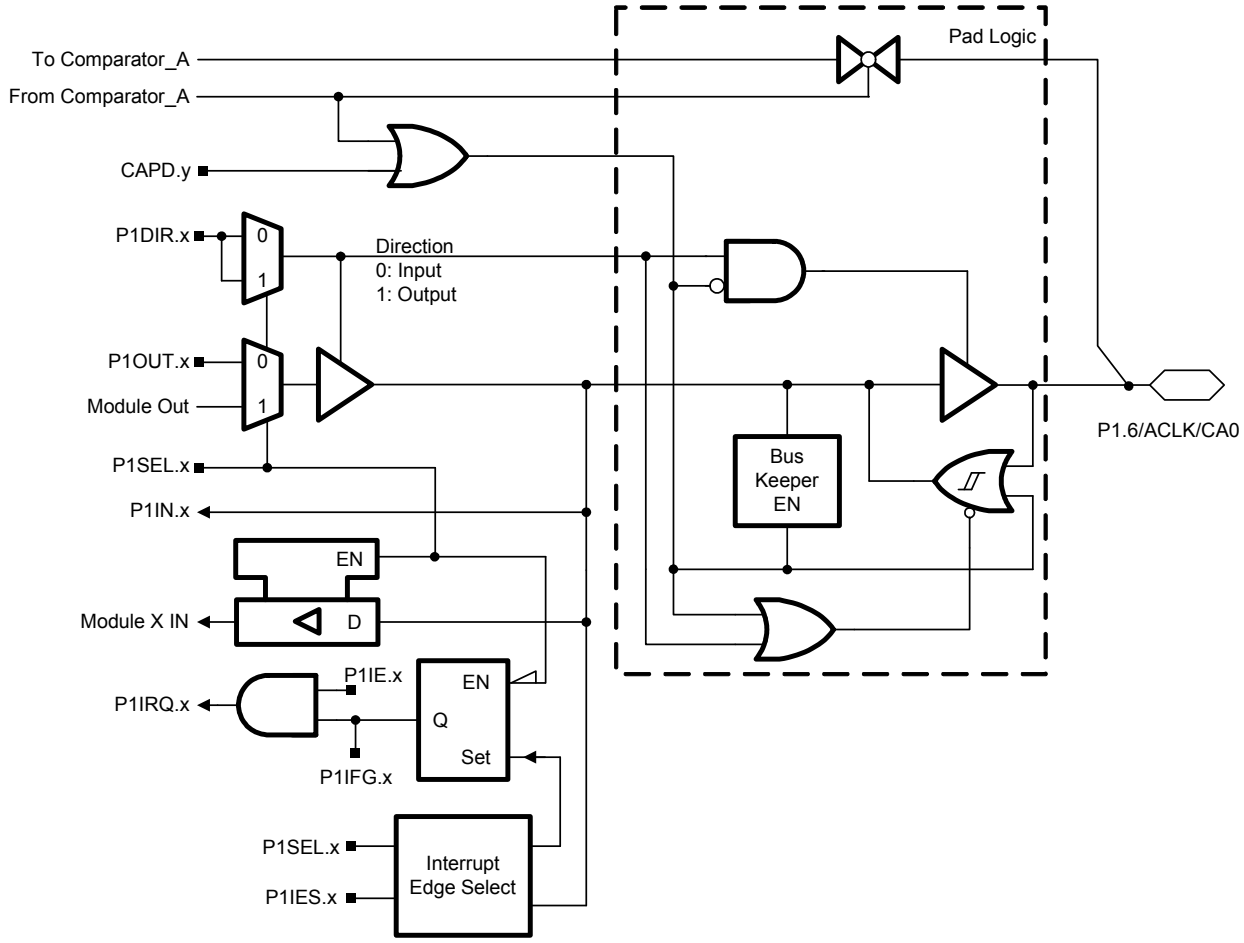
Port P1 (P1.5) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	LCDS24 LCDS28
P1.5/TA0CLK/CAOUT/S26	5	P1.x (I/O)	I: 0, O: 1	0	0
		Timer0_A3.TACLK	0	1	0
		CAOUT	1	1	0
		S26	x	x	1 (LCDS24)

NOTES: 1. x: Don't care
2. The input TA0CLK of P1.5 and P1.7 are logically ORed. Therefore only one of them should be enabled at a time to feed in TA0CLK.

APPLICATION INFORMATION

Port P1 pin schematic: P1.6, input/output with Schmitt trigger



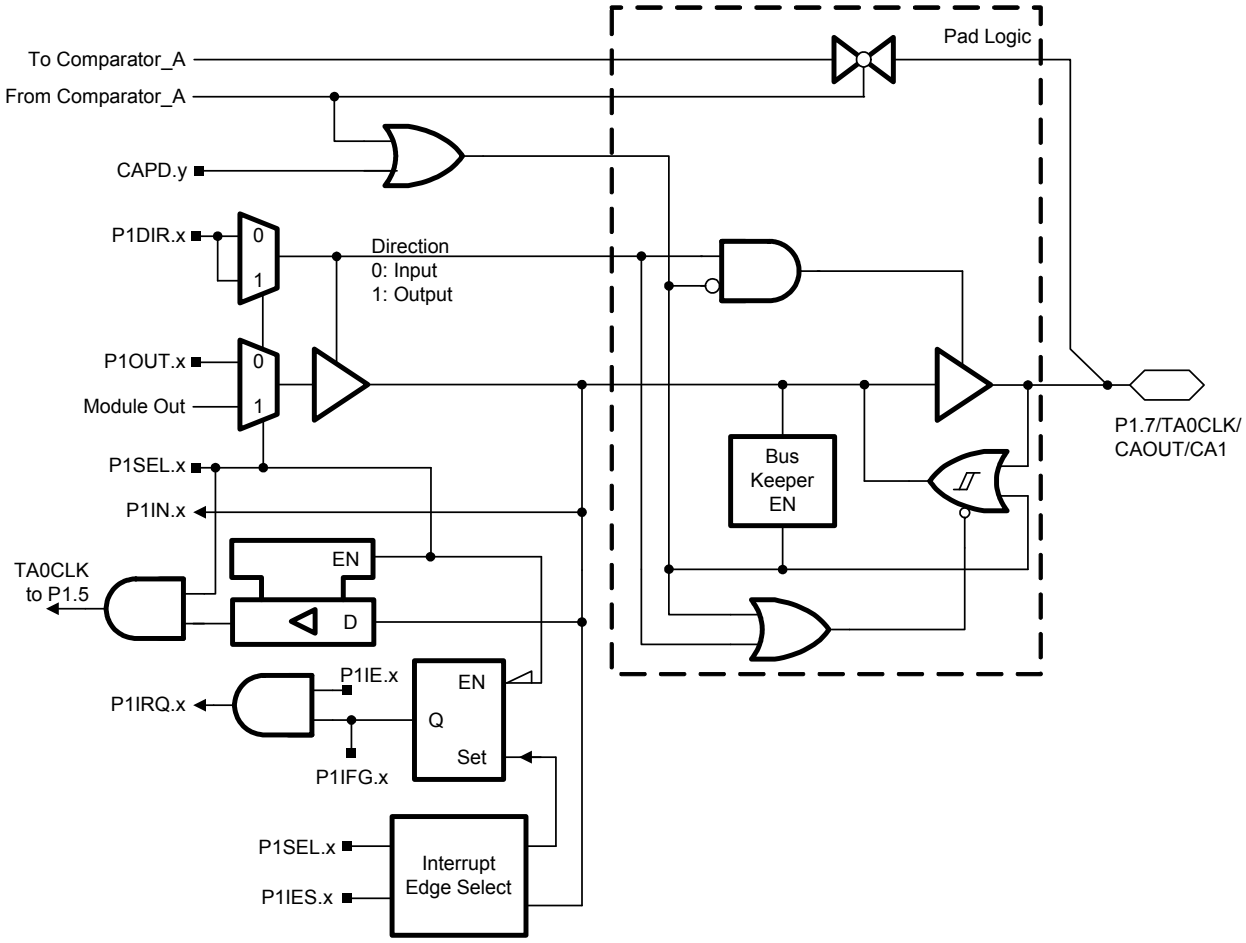
Port P1 (P1.6) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			CAPD	P1DIR.x	P1SEL.x
P1.6/ACLK/CA0	6	P1.x (I/O)	0	I: 0, O: 1	0
		ACLK	0	1	1
		CA0	1 (CAPD.0)	x	x

NOTES: 1. x: Don't care

APPLICATION INFORMATION

Port P1 pin schematic: P1.7, input/output with Schmitt trigger



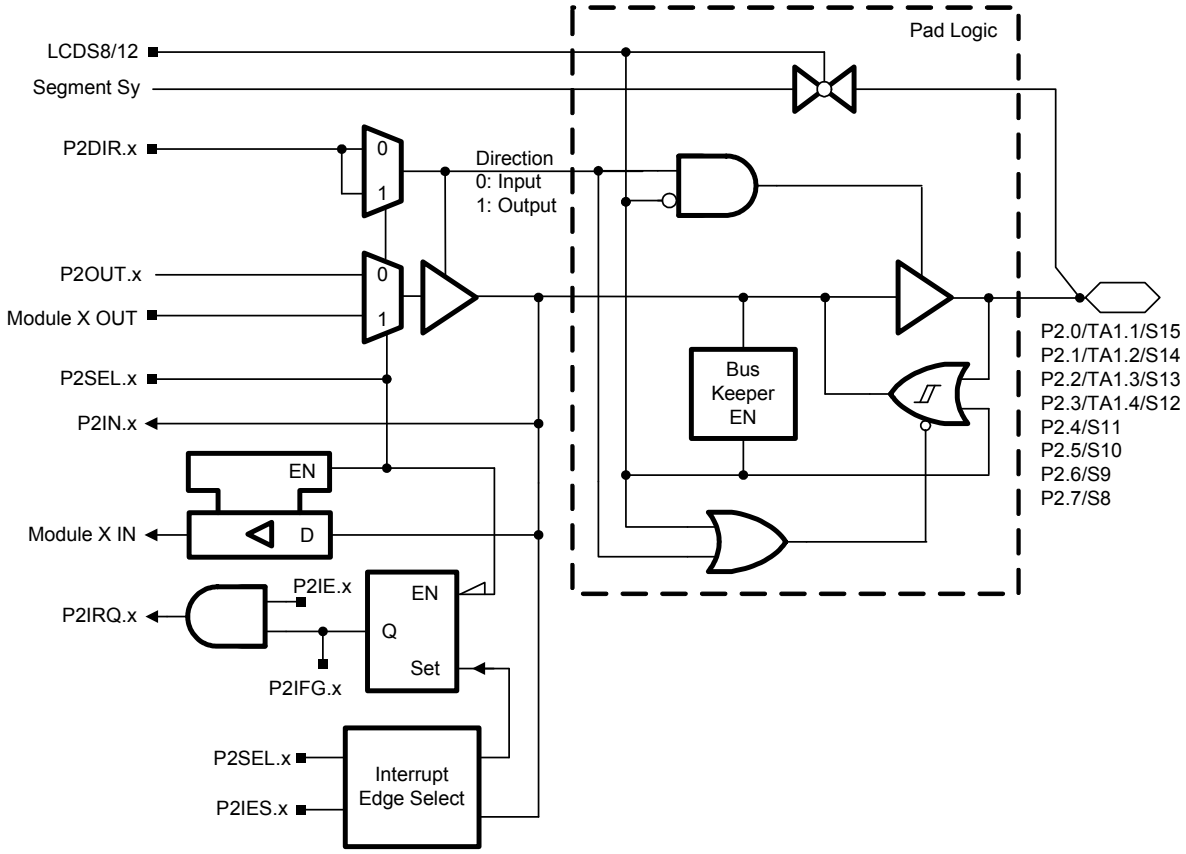
Port P1 (P1.7) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			CAPD	P1DIR.x	P1SEL.x
P1.7/TA0CLK/CAOUT/CA1	7	P1.x (I/O)	0	I: 0, O: 1	0
		Timer0_A3.TACLK	0	0	1
		CAOUT	0	1	1
		CA1	1 (CAPD.1)	x	x

NOTES: 1. x: Don't care
2. The input TA0CLK of P1.5 and P1.7 are combined by a logical OR. Therefore, only one of them should be enabled at a time to feed in TA0CLK.

APPLICATION INFORMATION

Port P2 pin schematic: P2.0 to P2.7 input/output with Schmitt trigger



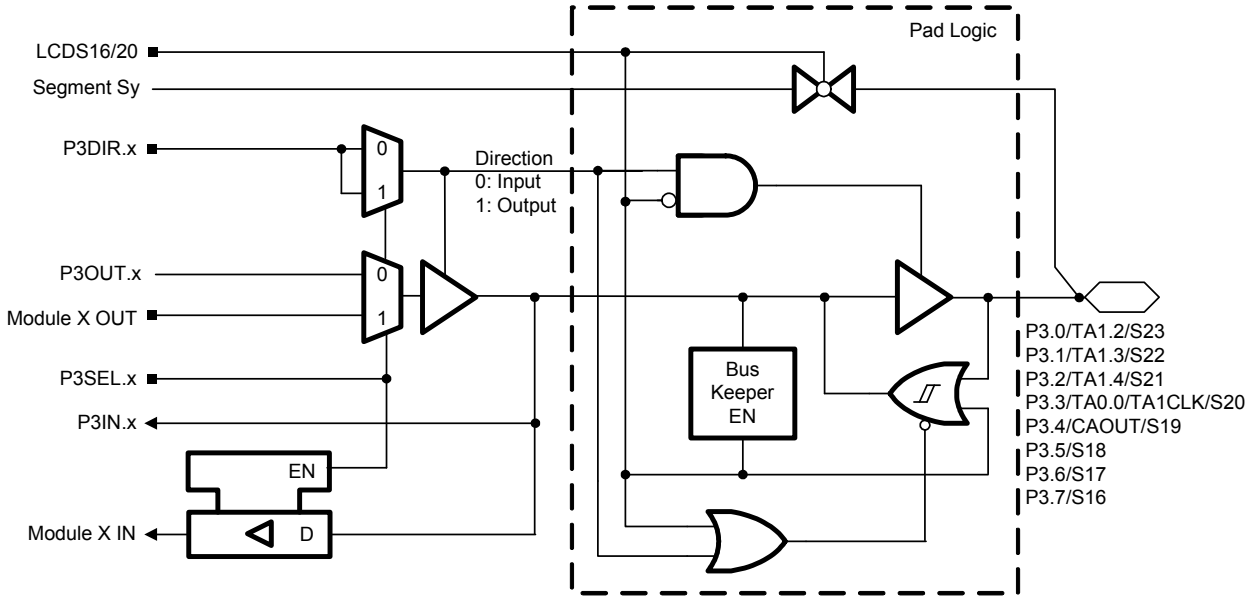
Port P2 (P2.0 to P2.7) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.x	LCDS8 LCDS12
P2.0/TA1.1/S15	0	P2.x (I/O)	I: 0, O: 1	0	0
		Timer1_A5.TA1	1	1	0
		S15	x	x	1 (LCDS12)
P2.1/TA1.2/S14	1	P2.x (I/O)	I: 0, O: 1	0	0
		Timer1_A5.TA2	1	1	0
		S14	x	x	1 (LCDS12)
P2.2/TA1.3/S13	2	P2.x (I/O)	I: 0, O: 1	0	0
		Timer1_A5.TA3	1	1	0
		S13	x	x	1 (LCDS12)
P2.3/TA1.4/S12	3	P2.x (I/O)	I: 0, O: 1	0	0
		Timer1_A5.TA4	1	1	0
		S12	x	x	1 (LCDS12)
P2.4/S11	4	P2.x (I/O)	I: 0, O: 1	0	0
		S11	x	x	1 (LCDS8)
P2.5/S10	5	P2.x (I/O)	I: 0, O: 1	0	0
		S10	x	x	1 (LCDS8)
P2.6/S9	6	P2.x (I/O)	I: 0, O: 1	0	0
		S9	x	x	1 (LCDS8)
P2.7/S8	7	P2.x (I/O)	I: 0, O: 1	0	0
		S8	x	x	1 (LCDS8)

NOTES: 1. x: Don’t care

APPLICATION INFORMATION

Port P3 pin schematic: P3.0 to P3.7 input/output with Schmitt trigger



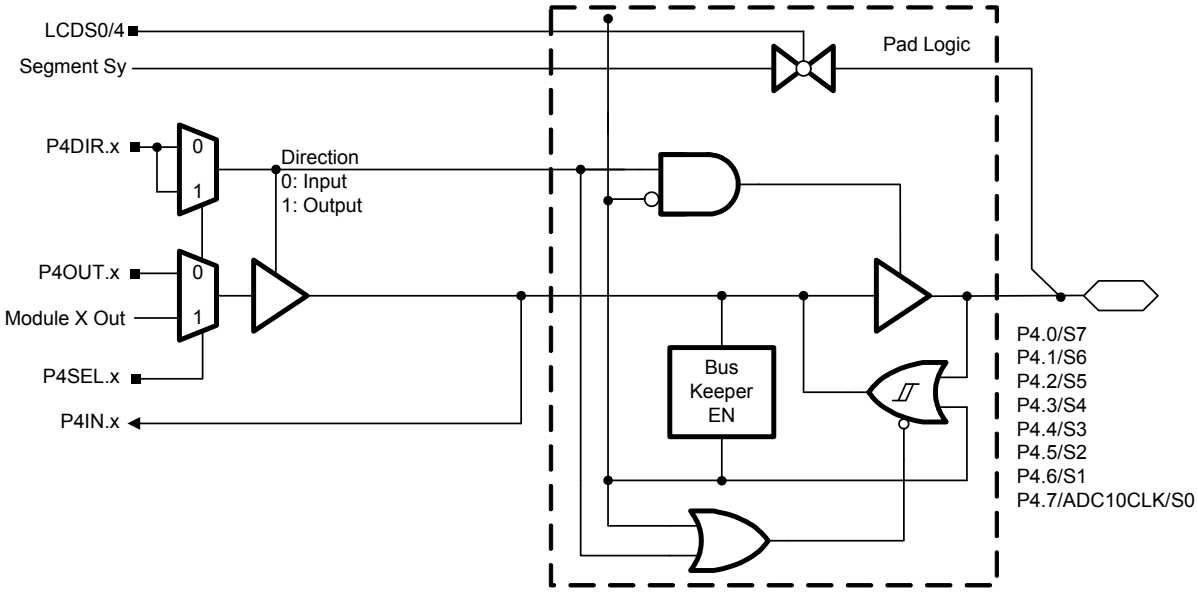
Port P3 (P3.0 to P3.7) pin functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P3DIR.x	P3SEL.x	LCDS16 LCDS20
P3.0/TA1.2/S23	0	P3.x (I/O)	I: 0, O: 1	0	0
		Timer1_A5.CCI2A	0	1	0
		Timer1_A5.TA2	1	1	0
		S23	x	x	1 (LCDS20)
P3.1/TA1.3/S22	1	P3.x (I/O)	I: 0, O: 1	0	0
		Timer1_A5.CCI3A	0	1	0
		Timer1_A5.TA3	1	1	0
		S22	x	x	1 (LCDS20)
P3.2/TA1.4/S21	2	P3.x (I/O)	I: 0, O: 1	0	0
		Timer1_A5.CCI4A	0	1	0
		Timer1_A5.TA4	1	1	0
		S21	x	x	1 (LCDS20)
P3.3/TA0.0/TA1CLK/S20	3	P3.x (I/O)	I: 0, O: 1	0	0
		Timer1_A5.TACLK	0	1	0
		Timer0_A3.TA0	1	1	0
		S20	x	x	1 (LCDS20)
P3.4/CAOUT/S19	4	P3.x (I/O)	I: 0, O: 1	0	0
		CAOUT	1	1	0
		S19	x	x	1 (LCDS16)
P3.5/S18	5	P3.x (I/O)	I: 0, O: 1	0	0
		S18	x	x	1 (LCDS16)
P3.6/S17	6	P3.x (I/O)	I: 0, O: 1	0	0
		S17	x	x	1 (LCDS16)
P3.7/S16	7	P3.x (I/O)	I: 0, O: 1	0	0
		S16	x	x	1 (LCDS16)

NOTES: 1. x: Don’t care

APPLICATION INFORMATION

Port P4 pin schematic: P4.0 to P4.7 input/output with Schmitt trigger



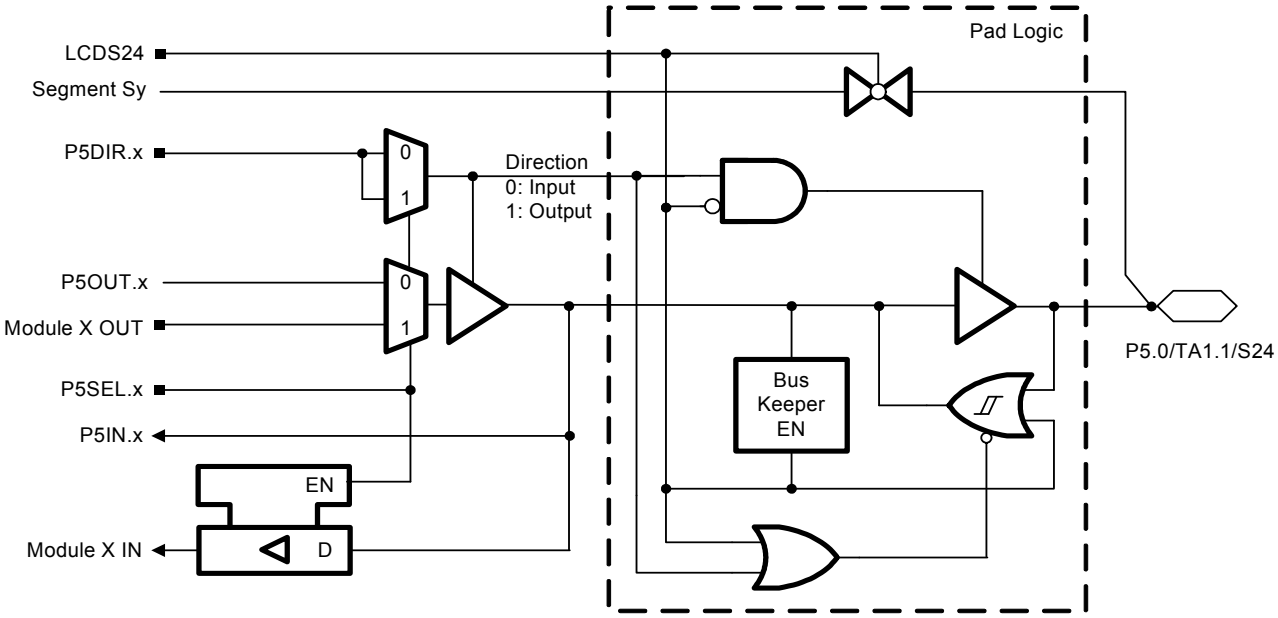
Port P4 (P4.0 to P4.7) pin functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P4DIR.x	P4SEL.x	LCDS4 LCDS0
P4.0/S7	0	P4.x (I/O)	I: 0, O: 1	0	0
		S7	x	x	1 (LCDS4)
P4.1/S6	1	P4.x (I/O)	I: 0, O: 1	0	0
		S6	x	x	1 (LCDS4)
P4.2/S5	2	P4.x (I/O)	I: 0, O: 1	0	0
		S5	x	x	1 (LCDS4)
P4.3/S4	3	P4.x (I/O)	I: 0, O: 1	0	0
		S4	x	x	1 (LCDS4)
P4.4/S3	4	P4.x (I/O)	I: 0, O: 1	0	0
		S3	x	x	1 (LCDS0)
P4.5/S2	5	P4.x (I/O)	I: 0, O: 1	0	0
		S2	x	x	1 (LCDS0)
P4.6/S1	6	P4.x (I/O)	I: 0, O: 1	0	0
		S1	x	x	1 (LCDS0)
P4.7/ADC10CLK/S0	7	P4.x (I/O)	I: 0, O: 1	0	0
		ADC10CLK	1	1	0
		S0	x	x	1 (LCDS0)

NOTES: 1. x: Don't care

APPLICATION INFORMATION

Port P5 pin schematic: P5.0, input/output with Schmitt trigger



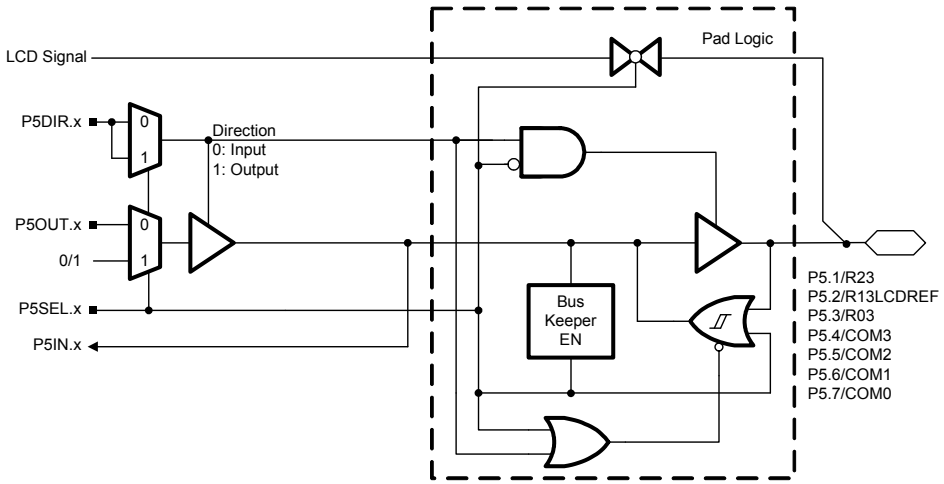
Port P5 (P5.0) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P5DIR.x	P5SEL.x	LCDS24
P5.0/TA1.1/S24	0	P5.x (I/O)	I: 0, O: 1	0	0
		Timer1_A5.CCI1A	0	1	0
		Timer1_A5.TA1	1	1	0
		S24	x	x	1

NOTES: 1. x: Don't care

APPLICATION INFORMATION

Port P5 pin schematic: P5.1 to P5.7, input/output with Schmitt trigger



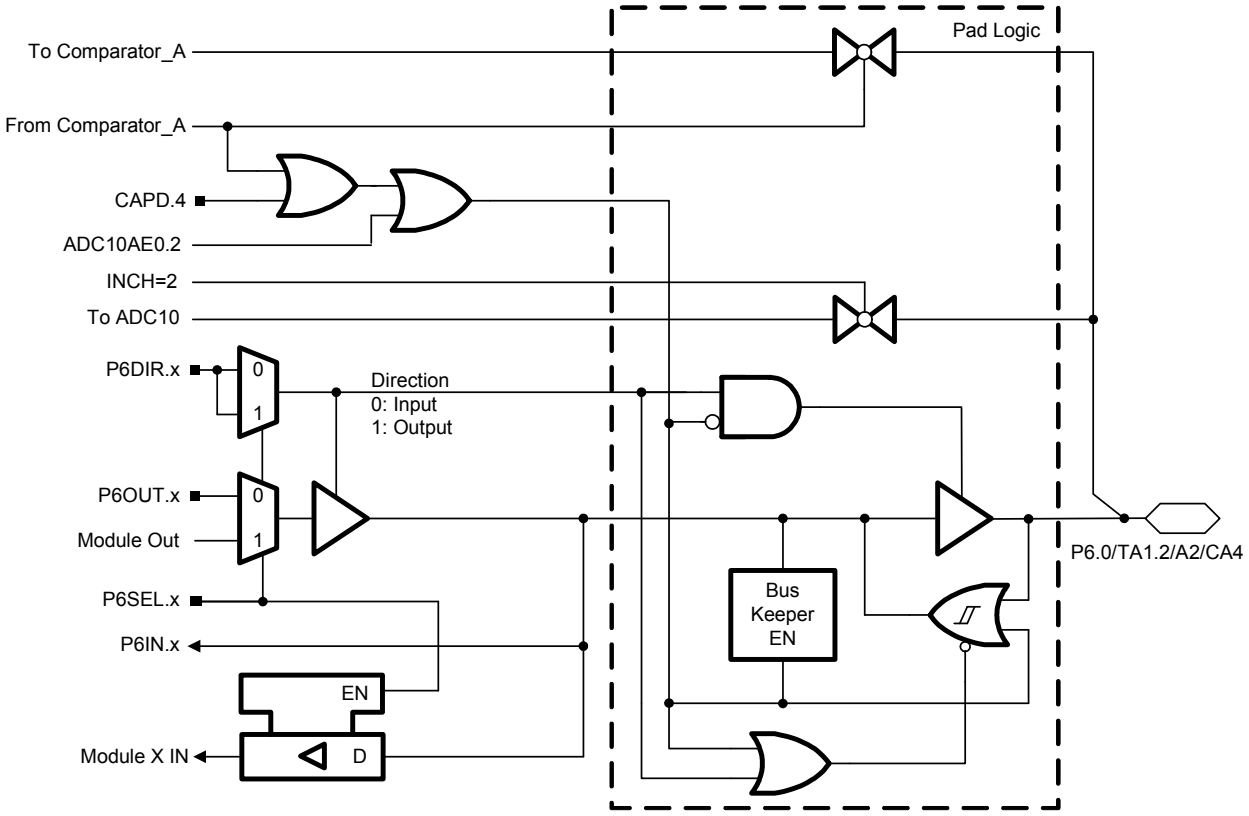
Port P5 (P5.1 to P5.7) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.x	P5SEL.x
P5.1/R23	1	P5.x (I/O)	I: 0, O: 1	0
		R23	x	1
P5.2/LCDREF/R13	2	P5.x (I/O)	I: 0, O: 1	0
		R13 or LCDREF	x	1
P5.3/R03	3	P5.x (I/O)	I: 0, O: 1	0
		R03	x	1
P5.4/COM3	4	P5.x (I/O)	I: 0, O: 1	0
		COM3	x	1
P5.5/COM2	5	P5.x (I/O)	I: 0, O: 1	0
		COM2	x	1
P5.6/COM1	6	P5.x (I/O)	I: 0, O: 1	0
		COM1	x	1
P5.7/COM0	7	P5.x (I/O)	I: 0, O: 1	0
		COM0	x	1

NOTES: 1. x: Don't care

APPLICATION INFORMATION

Port P6 pin schematic: P6.0, input/output with Schmitt trigger



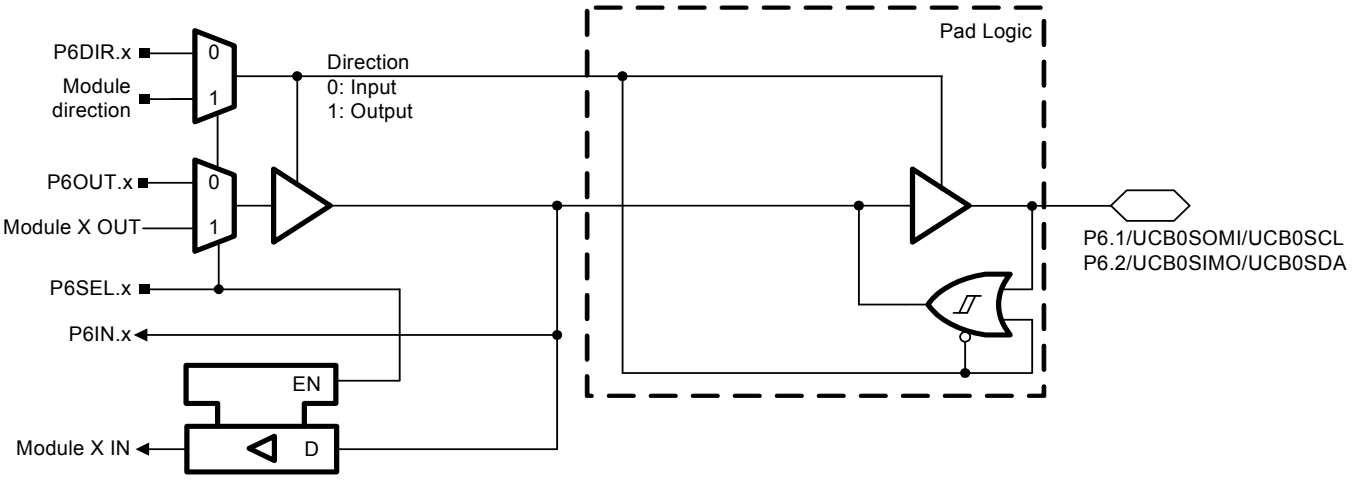
Port P6 (P6.0) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD	ADC10AE0.y	P6DIR.x	P6SEL.x
P6.0/TA1.2/A2/CA4	0	P6.x (I/O)	0	0	I: 0, O: 1	0
		Timer1_A5.TA2	0	0	1	1
		A2	x	1 (y=2)	x	x
		CA4	1 (CAPD.4)	x	x	x

NOTES: 1. x: Don't care

APPLICATION INFORMATION

Port P6 pin schematic: P6.1 and P6.2, inpututput with Schmitt trigger



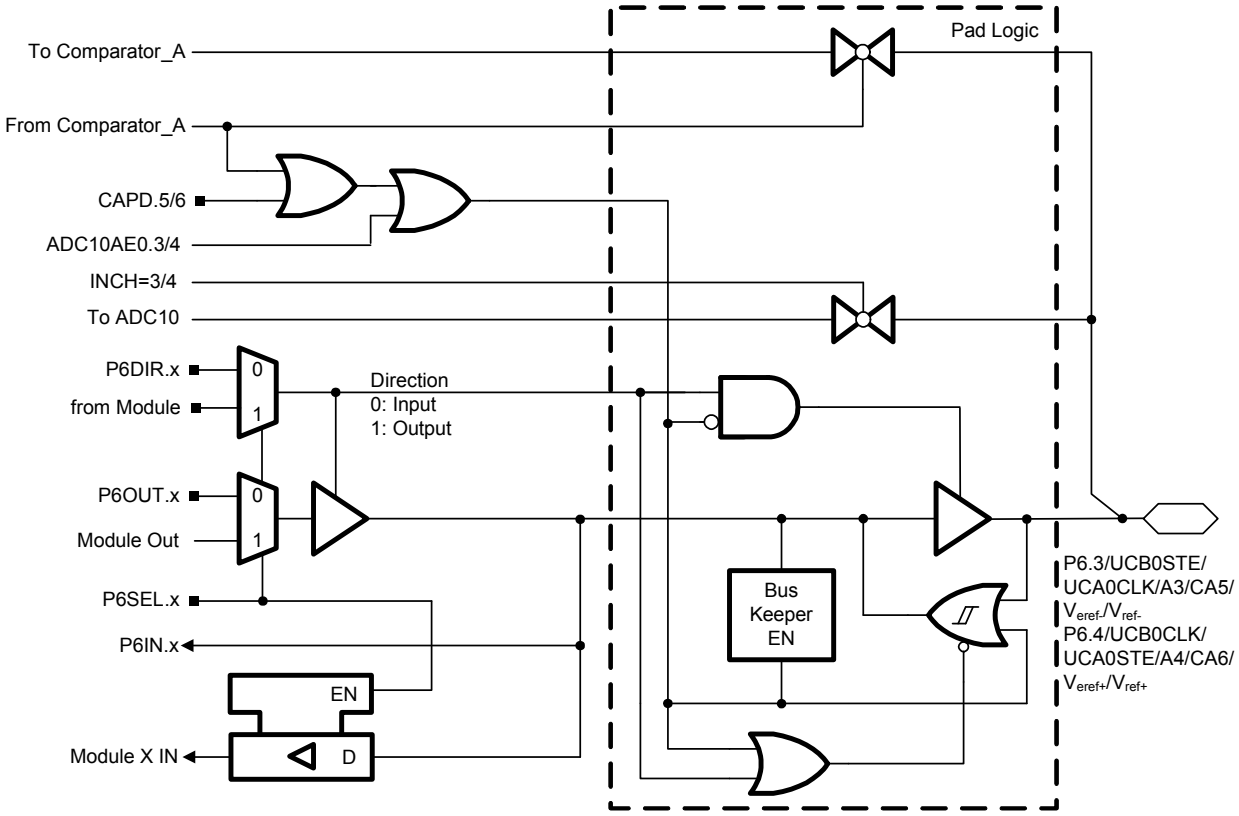
Port P6 (P6.1 and P6.2) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.1/UCB0SOMI/UCB0SCL	1	P6.x (I/O)	I: 0, O: 1	0
		UCB0SOMI/UCB0SCL (see Note 2)	x	1
P6.2/UCB0SIMO/UCB0SDA	2	P6.x (I/O)	I: 0, O: 1	0
		UCB0SIMO/UCB0SDA (see Note 2)	x	1

NOTES: 1. x: Don't care
2. The pin direction is controlled by the USCI module.

APPLICATION INFORMATION

Port P6 pin schematic: P6.3 and P6.4, input/output with Schmitt trigger



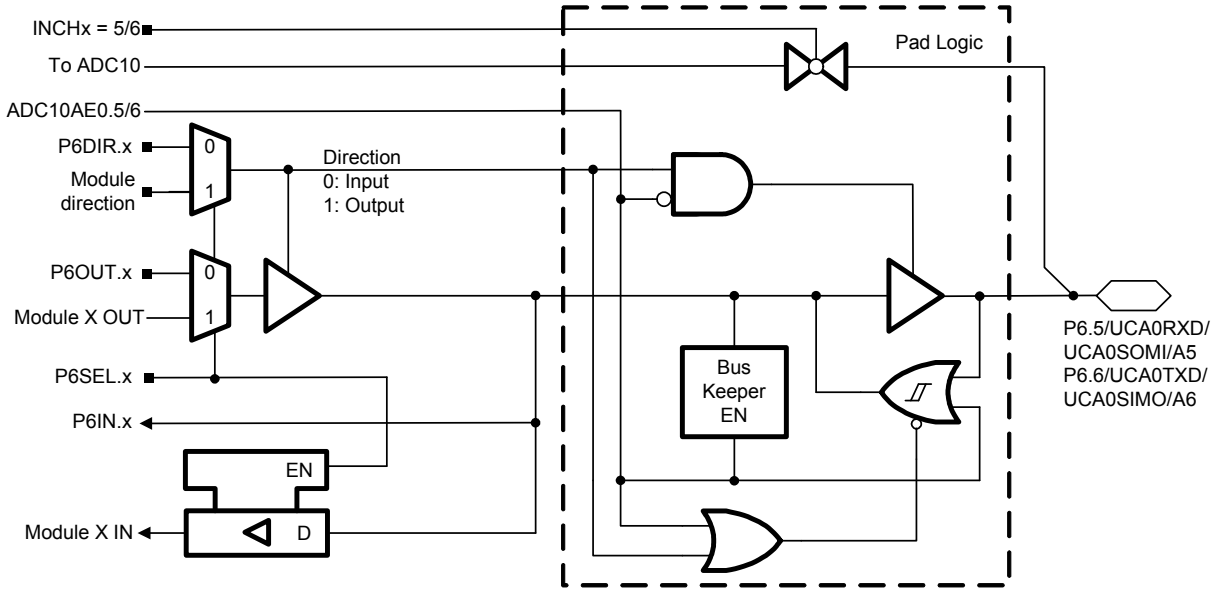
Port P6 (P6.3 and P6.4) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD	ADC10AE0.y	P6DIR.x	P6SEL.x
P6.3/UCB0STE/ UCA0CLK/A3/CA5/ /V_{eref-}/V_{ref-}	3	P6.x (I/O)	0	0	I: 0, O: 1	0
		UCB0STE/UCA0CLK (see Note 2)	0	0	x	1
		A3/V_{eref-}/V_{ref-}	x	1 (y=3)	x	x
		CA5	1 (CAPD.5)	x	x	x
P6.4/UCB0CLK/ UCA0STE/A4/CA6/ /V_{eref+}/V_{ref+}	4	P6.x (I/O)	0	0	I: 0, O: 1	0
		UCB0CLK/UCA0STE (see Note 2)	0	0	x	1
		A4/V_{eref+}/V_{ref+}	x	1 (y=4)	x	x
		CA6	1 (CAPD.6)	x	x	x

NOTES: 1. x: Don't care
2. The pin direction is controlled by the USCI module.

APPLICATION INFORMATION

Port P6 pin schematic: P6.5 and P6.6, input/output with Schmitt trigger



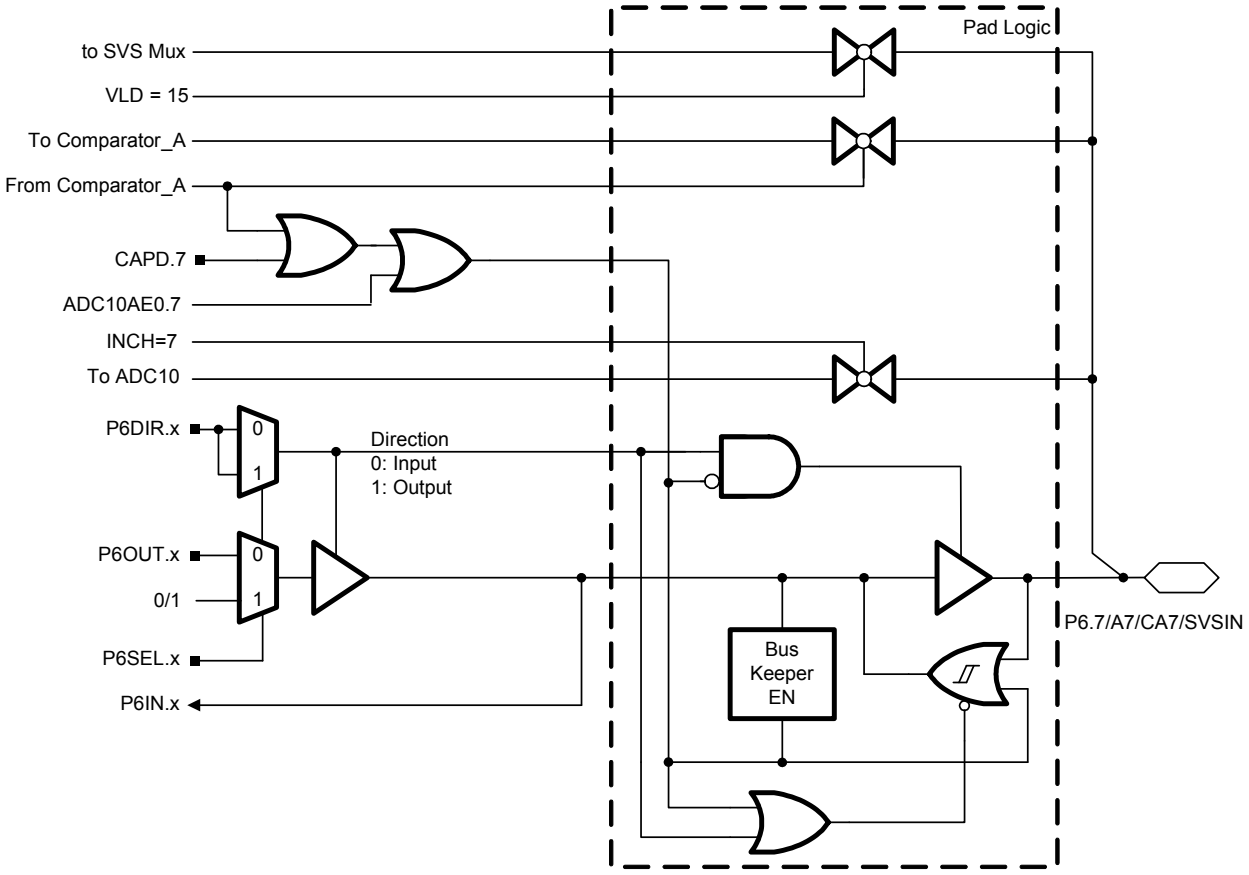
Port P6 (P6.5 and P6.6) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			ADC10AE0.y	P6DIR.x	P6SEL.x
P6.5/UCA0RXD/ UCA0SOMI/A5	5	P6.x (I/O)	0	I: 0, O: 1	0
		UCA0RXD/UCA0SOMI (see Note 2)	0	x	1
		A5	1 (y=5)	x	x
P6.6/UCA0TXD/ UCA0SIMO/A6	6	P6.x (I/O)	0	I: 0, O: 1	0
		UCA0TXD/UCA0SIMO (see Note 2)	0	x	1
		A6	1 (y=6)	x	x

NOTES: 1. x: Don't care
2. The pin direction is controlled by the USCI module.

APPLICATION INFORMATION

Port P6 pin schematic: P6.7, input/output with Schmitt trigger



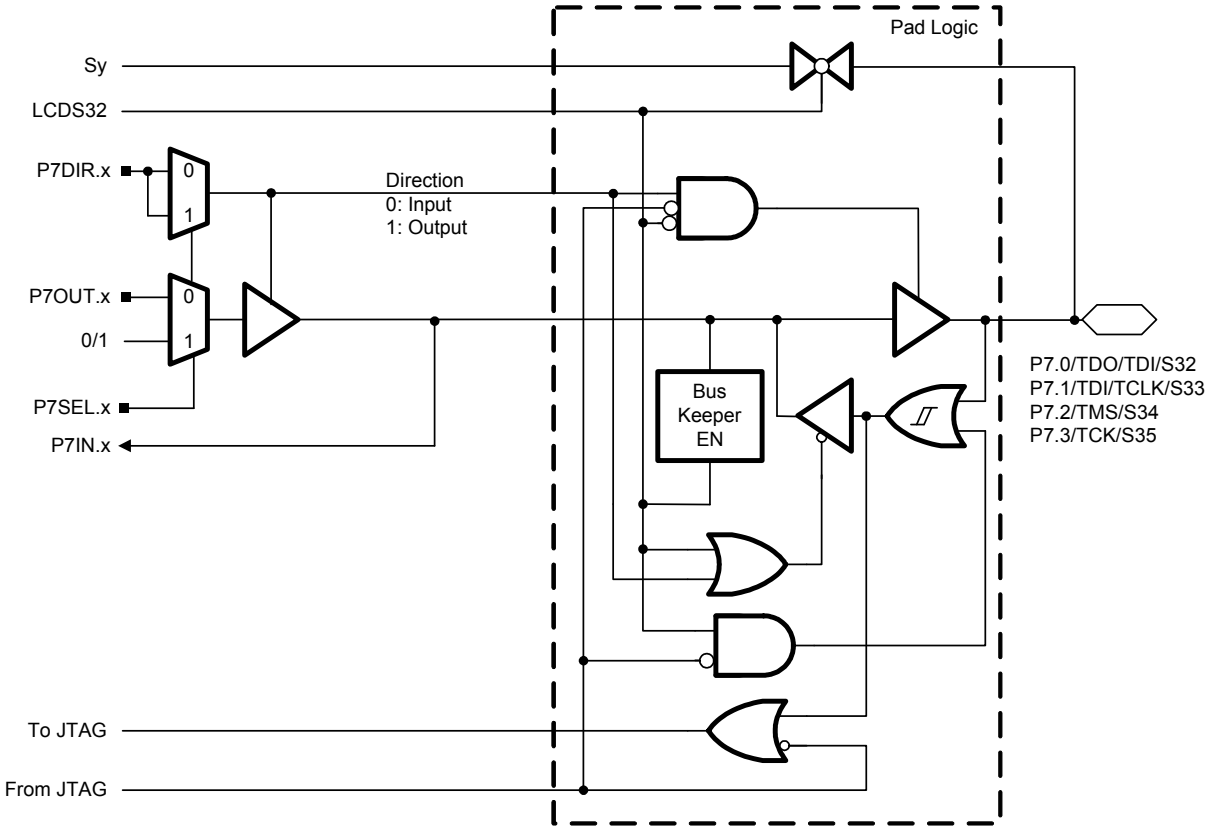
Port P6 (P6.7) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			VLDx = 15	CAPD	ADC10AE0	P6DIR.x	P6SEL.x
P6.7/A7/CA7/SVSIN	7	P7.x (I/O)	0	0	0	I: 0, O: 1	0
		A7	0	x	1 (y = 7)	x	x
		CA7	0	1 (CAPD.7)	x	x	x
		SVSIN	1	0	0	x	x

NOTES: 1. x: Don't care

/APPLICATION INFORMATION

Port P7 pin schematic: P7.0 to P7.3, input/output with Schmitt trigger



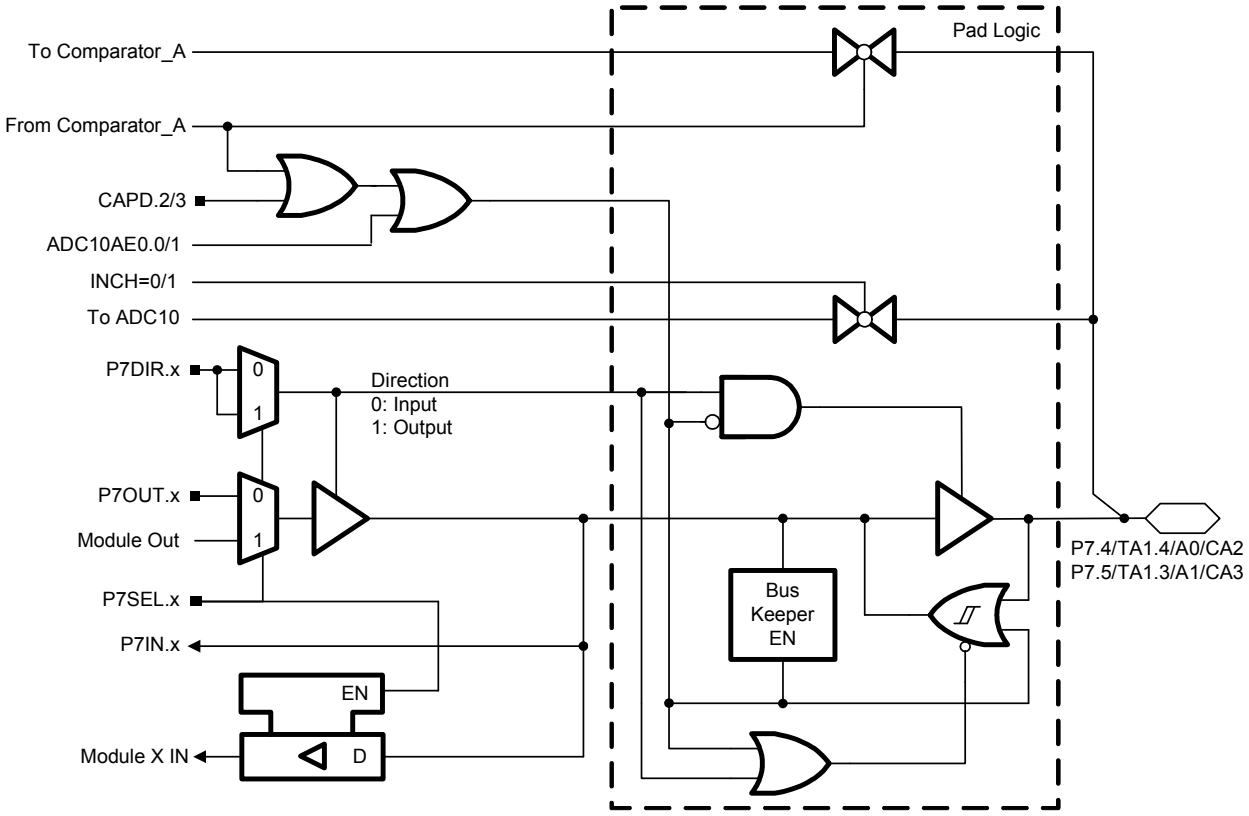
Port P7 (P7.0 to P7.3) pin functions

PIN NAME (P7.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			JTAG Mode	P7DIR.x	P7SEL.x	LCDS32
P7.0/TDO/TDI/S32	0	P7.x (I/O)	0	I: 0, O: 1	0	0
		TDO/TDI (see Note 1)	1	x	x	x
		S32	0	x	x	1
P7.1/TDI/TCLK/S33	1	P7.x (I/O)	0	I: 0, O: 1	0	0
		TDI/TCLK (see Note 1)	1	x	x	x
		S33	0	x	x	1
P7.2/TMS/S34	2	P7.x (I/O)	0	I: 0, O: 1	0	0
		TMS (see Note 1)	1	x	x	x
		S34	0	x	x	1
P7.3/TCK/S35	3	P7.3 (I/O)	0	I: 0, O: 1	0	0
		TCK (see Note 1)	1	x	x	x
		S35	0	x	x	1

NOTES: 1. In JTAG Mode the internal pullup/pulldown resistors are disabled.
2. X: Don't care.

APPLICATION INFORMATION

Port P7 pin schematic: P7.4 and P7.5, input/output with Schmitt trigger



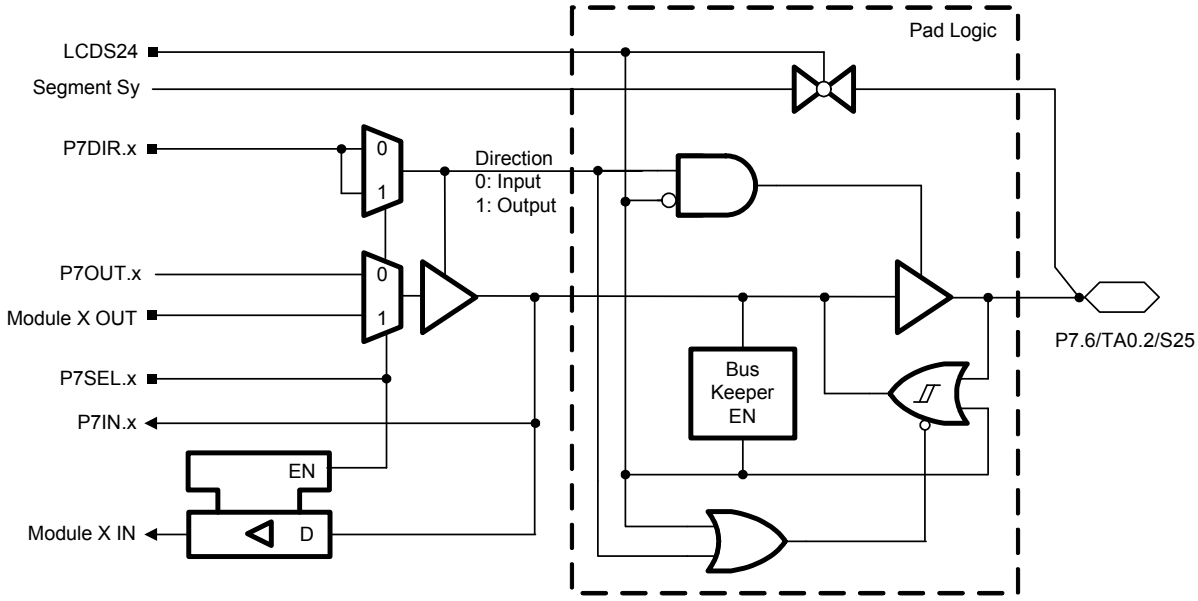
Port P7 (P7.4 and P7.5) pin functions

PIN NAME (P7.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD	ADC10AE0.y	P7DIR.x	P7SEL.x
P7.4/TA1.4/A0/CA2	4	P7.x (I/O)	0	0	I: 0, O: 1	0
		Timer1_A5.TA4	0	0	1	1
		Timer1_A5.CCI4B	0	0	0	1
		A0	x	1 (y=0)	x	x
		CA2	1 (CAPD.2)	x	x	x
P7.5/TA1.3/A1/CA3	5	P7.x (I/O)	0	0	I: 0, O: 1	0
		Timer1_A5.TA3	0	0	1	1
		Timer1_A5.CCI3B	0	0	0	1
		A1	x	1 (y=1)	x	x
		CA3	1 (CAPD.3)	x	x	x

NOTES: 1. x: Don't care

APPLICATION INFORMATION

Port P7 pin schematic: P7.6, input/output with Schmitt trigger



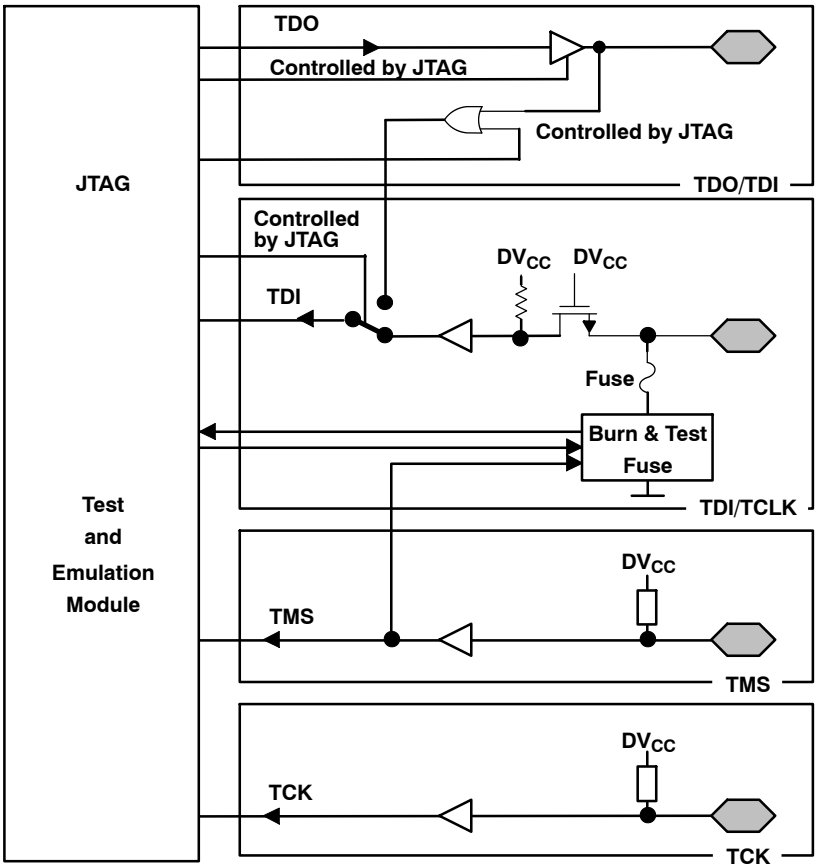
Port P7 (P7.6) pin functions

PIN NAME (P7.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P7DIR.x	P7SEL.x	LCDS24
P7.6/TA0.2/S25	6	P7.x (I/O)	I: 0, O: 1	0	0
		Timer0_A3.CCI2A	0	1	0
		Timer0_A3.TA2	1	1	0
		S25	x	x	1

NOTES: 1. x: Don't care

APPLICATION INFORMATION

JTAG pins: TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt trigger



During Programming Activity and During Blowing of the Fuse, Pin TDO/TDI Is Used to Apply the Test Input Data for JTAG Circuitry

JTAG fuse check mode

For details on the JTAG fuse check mode, see the *MSP430 Memory Programming User's Guide* (SLAU265) chapter "Fuse Check and Reset of the JTAG State Machine (TAP Controller)".

Data Sheet Revision History

LITERATURE NUMBER	SUMMARY
SLAS648	Production Data release
SLAS648A	Changed TDI/TCLK to TEST in Note 1 of “absolute maximum ratings” table (page 23) Changed lower limit of Storage temperature, Programmed device from –40°C to –55°C in “absolute maximum ratings” table (page 23)
SLAS648B	Corrected Timer_A3 Signal Connections and Timer_A5 Signal Connections tables (pages 17, 18) Removed bullet indicating that Segment A contains calibration data (page 15)
SLAS648C	Added note to functional block diagram (page 5)
SLAS648D	In “absolute maximum ratings” table, changed LFXT1 crystal frequency, $f_{(LFXT1)}$ MIN from 450 to 0.45 MHz (with ceramic resonator) and from 1000 to 1 MHz (with crystal) (page 23) In “crystal oscillator, LFXT1, high frequency modes” table, changed f_{LFXT1} MAX from 8 to 6 MHz for both ceramic and crystal resonator (page 36)$t_{d(SVSon)}$
SLAS648E	Changed limits on $t_{d(SVSon)}$ parameter (page 31)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSP430F4132IPM	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4132
MSP430F4132IPM.A	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4132
MSP430F4132IPMR	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4132
MSP430F4132IPMR.A	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4132
MSP430F4132IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F4132
MSP430F4132IRGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F4132
MSP430F4132IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F4132
MSP430F4132IRGZT.A	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F4132
MSP430F4152IPM	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4152
MSP430F4152IPM.A	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4152
MSP430F4152IPMR	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4152
MSP430F4152IPMR.A	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4152
MSP430F4152IPMRG4	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4152
MSP430F4152IPMRG4.A	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F4152
MSP430F4152IRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F4152
MSP430F4152IRGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F4152
MSP430F4152IRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F4152
MSP430F4152IRGZT.A	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F4152

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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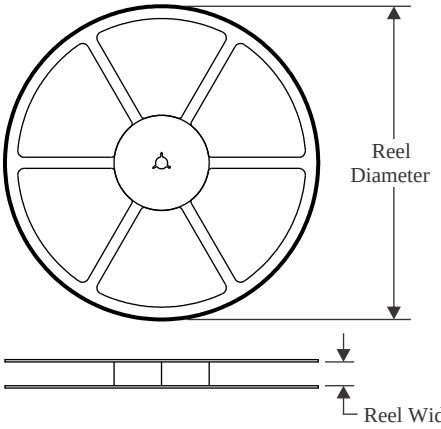
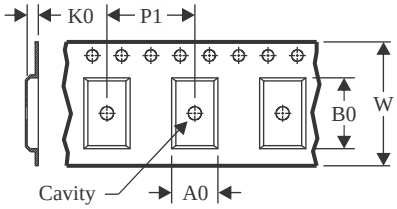
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

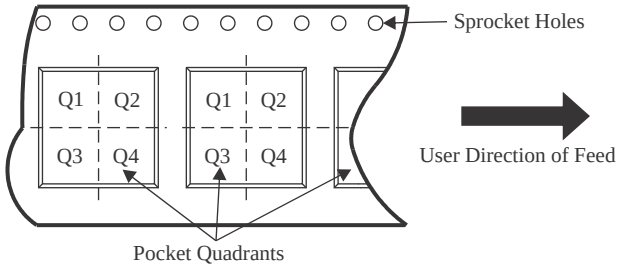


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

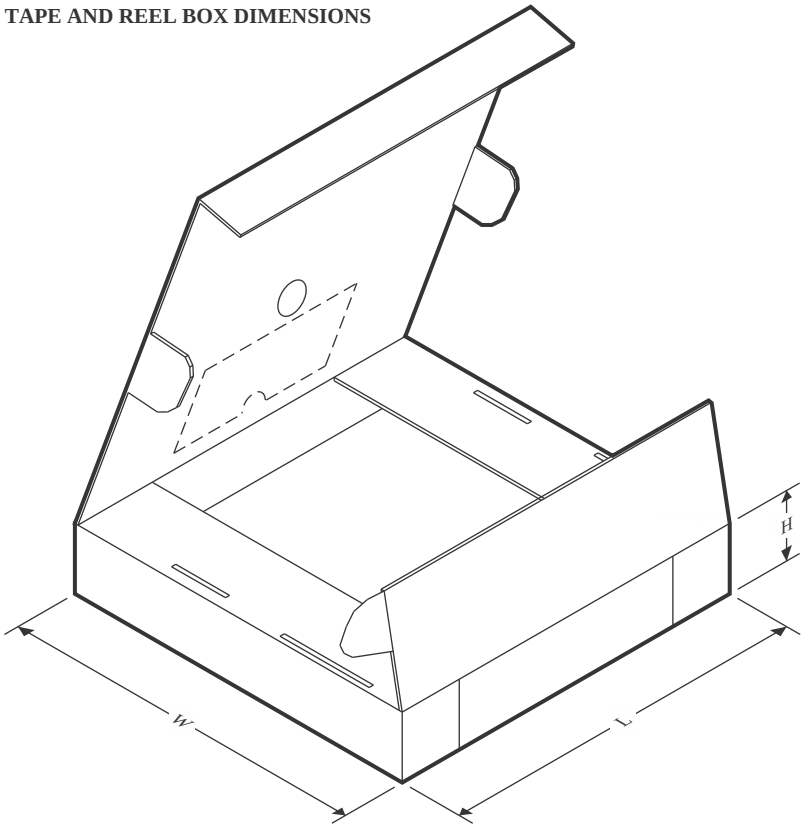
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F4132IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F4132IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F4132IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F4152IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F4152IPMRG4	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F4152IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
MSP430F4152IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

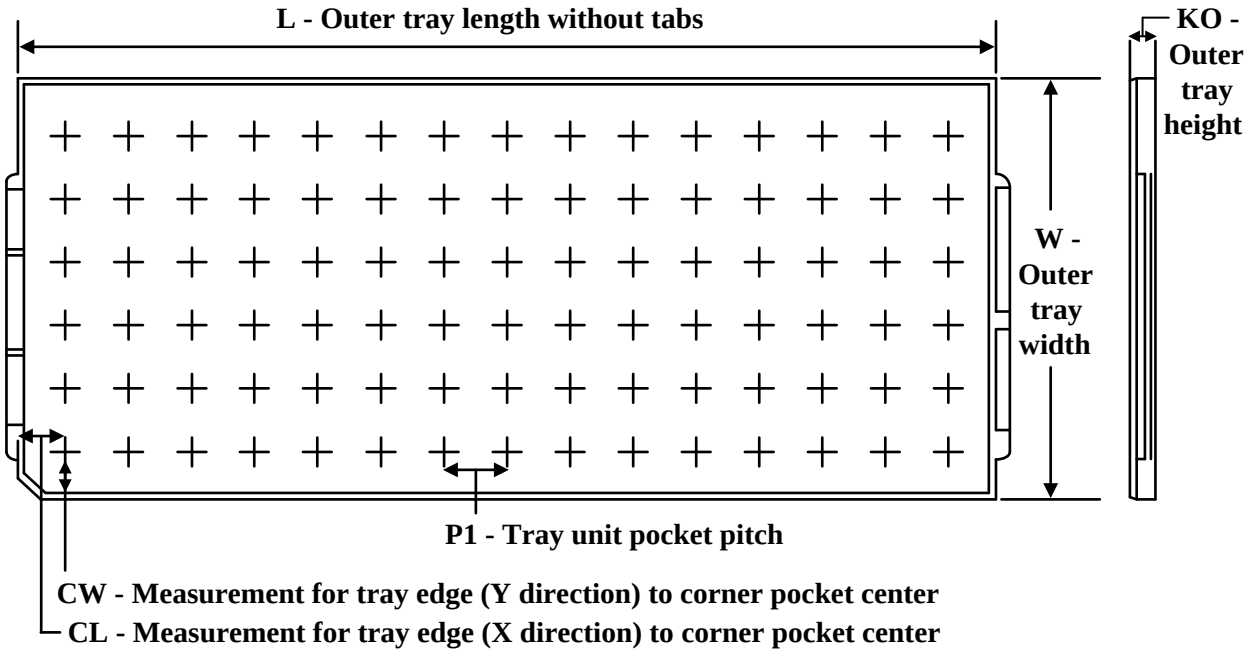
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F4132IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F4132IRGZR	VQFN	RGZ	48	2500	353.0	353.0	32.0
MSP430F4132IRGZT	VQFN	RGZ	48	250	213.0	191.0	35.0
MSP430F4152IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F4152IPMRG4	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F4152IRGZR	VQFN	RGZ	48	2500	353.0	353.0	32.0
MSP430F4152IRGZT	VQFN	RGZ	48	250	213.0	191.0	35.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
MSP430F4132IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F4132IPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F4132IPM.A	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F4132IPM.A	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F4152IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F4152IPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F4152IPM.A	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F4152IPM.A	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

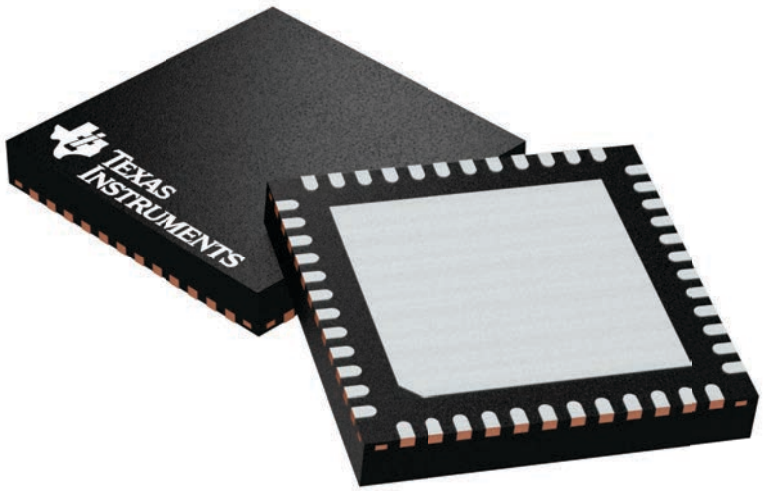
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

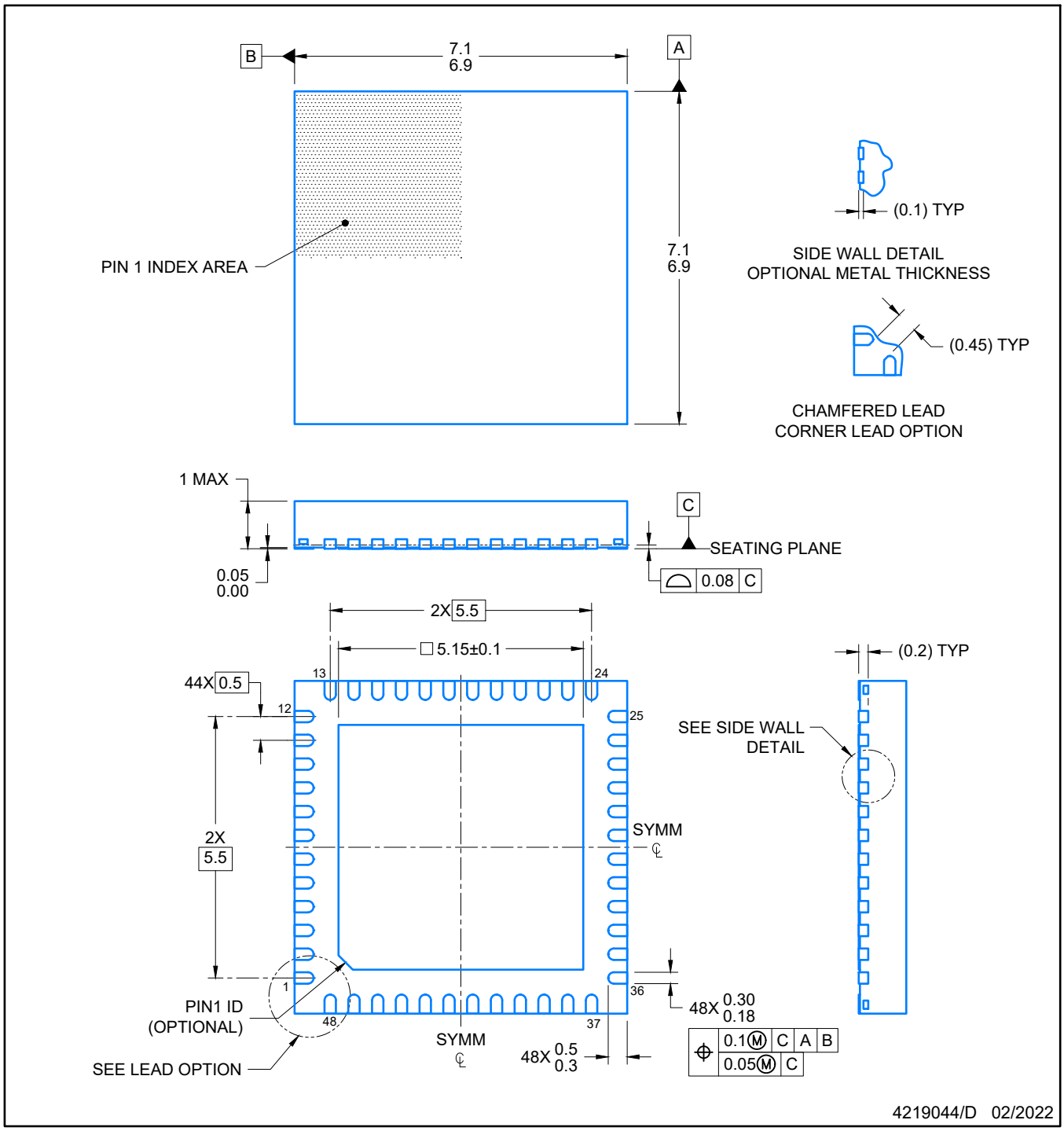
PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

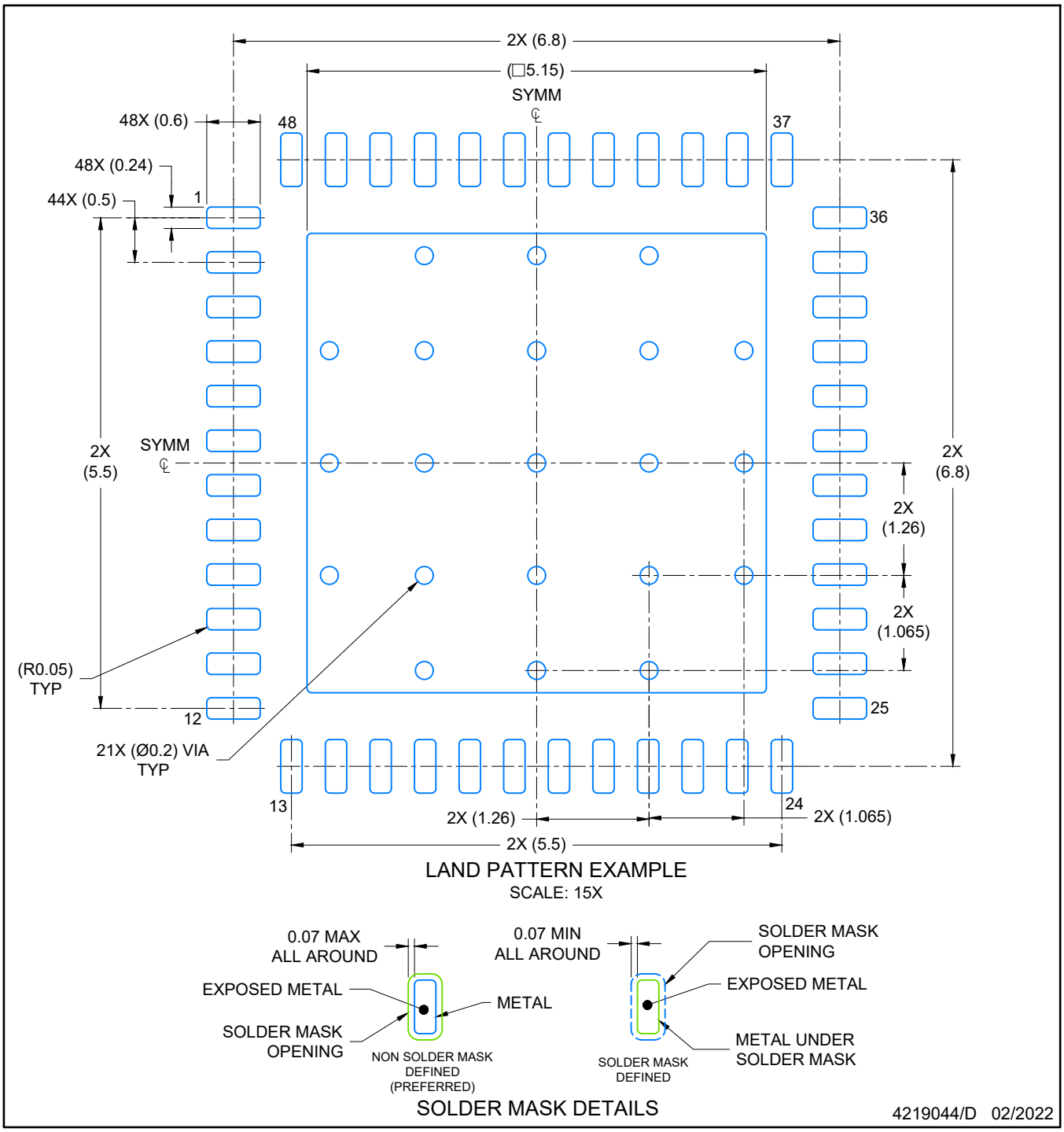
4224671/A

PLASTIC QUADFLAT PACK- NO LEAD



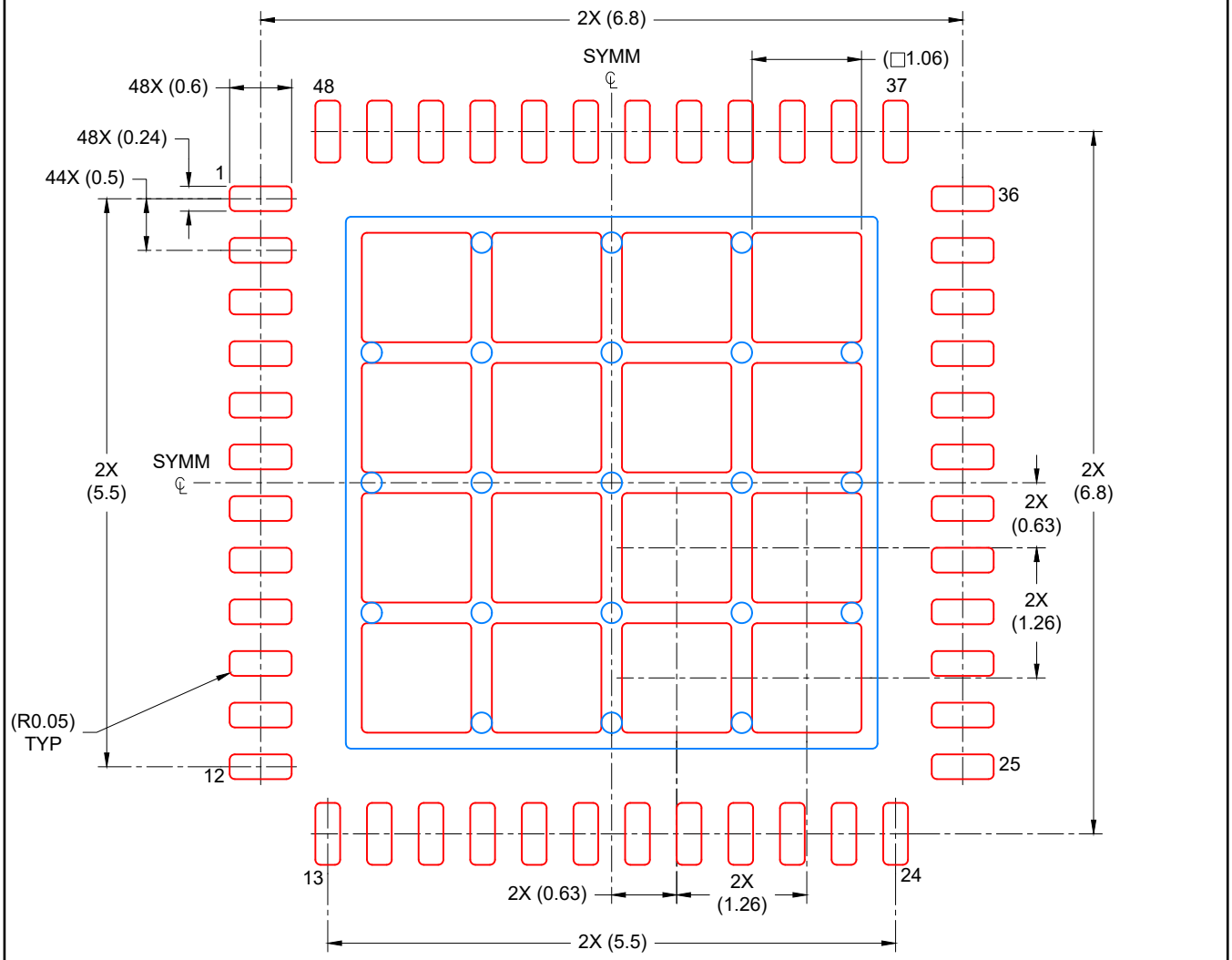
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/D 02/2022

NOTES: (continued)

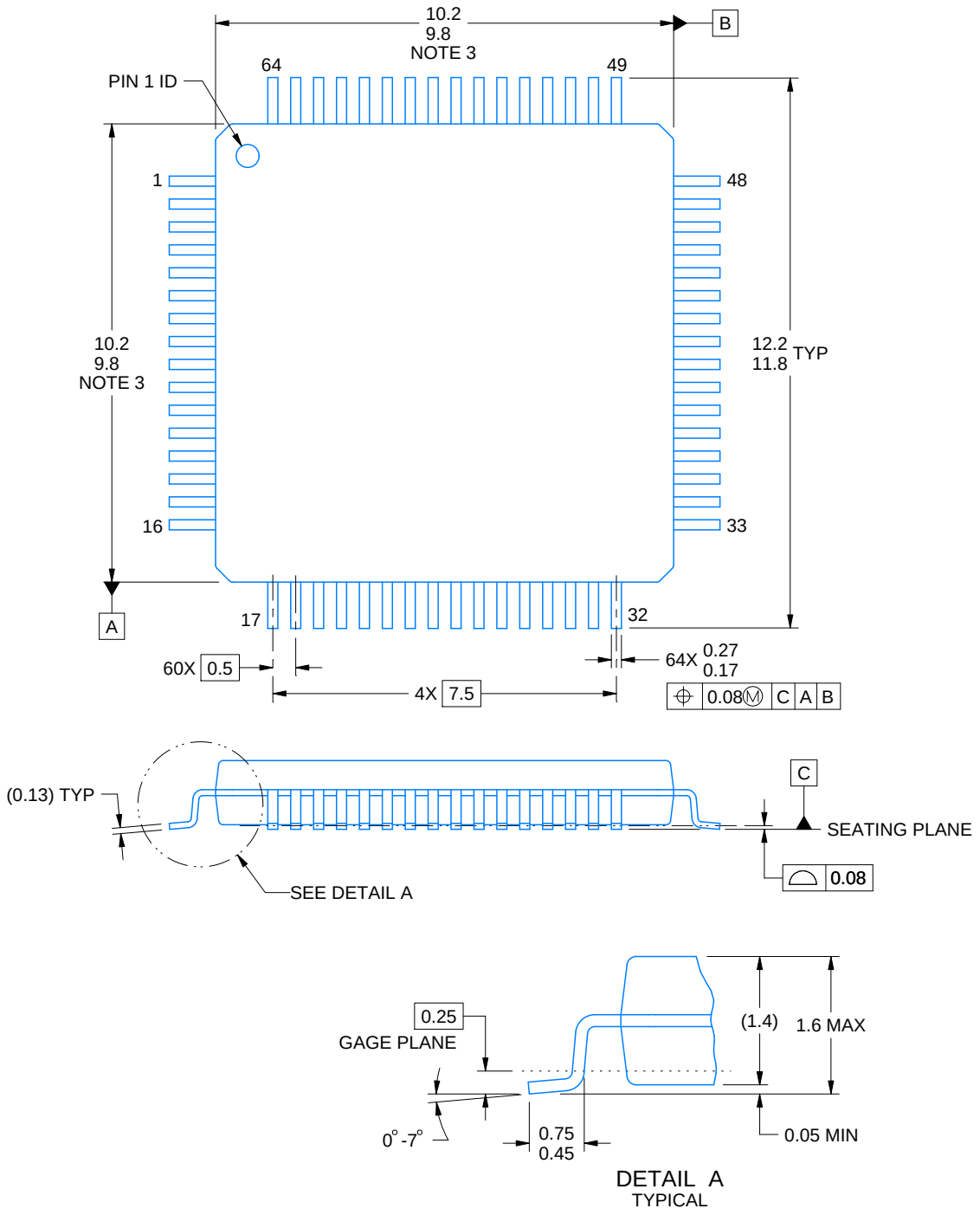
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

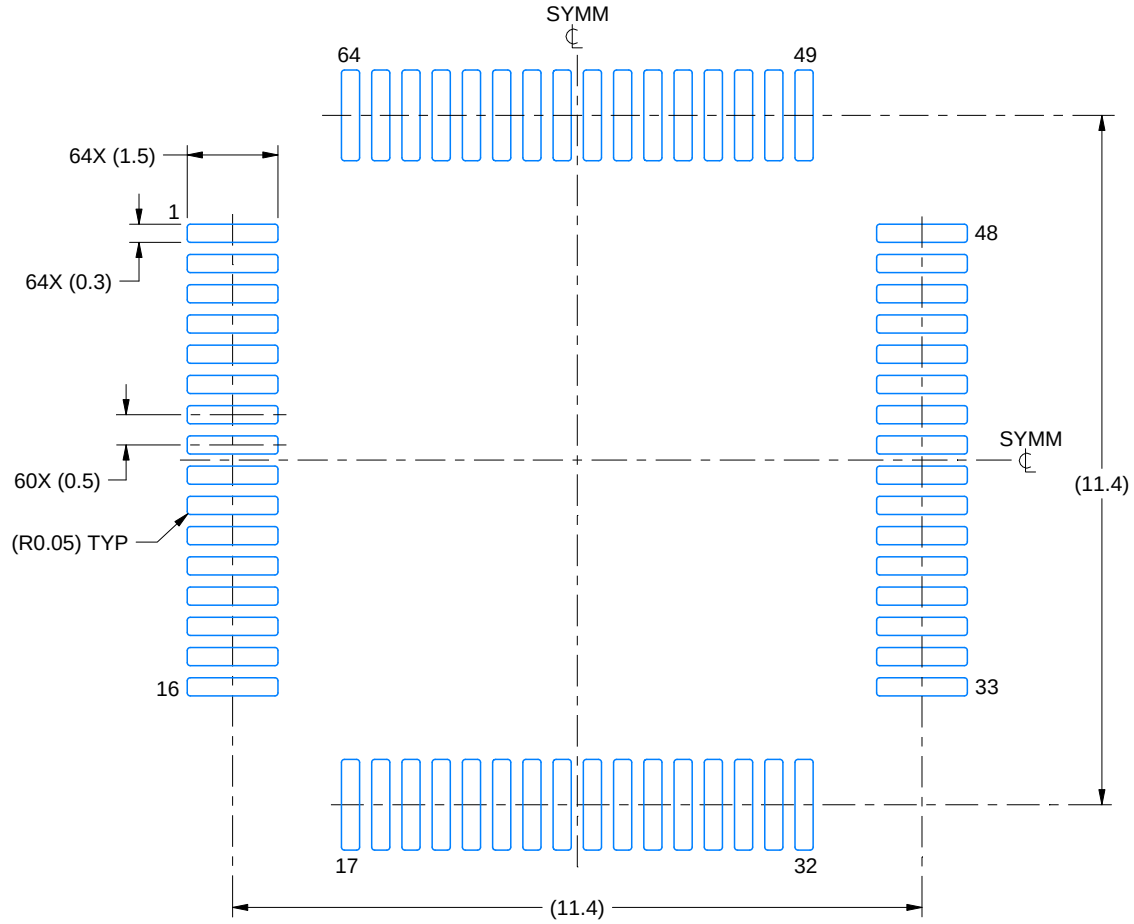
PLASTIC QUAD FLATPACK



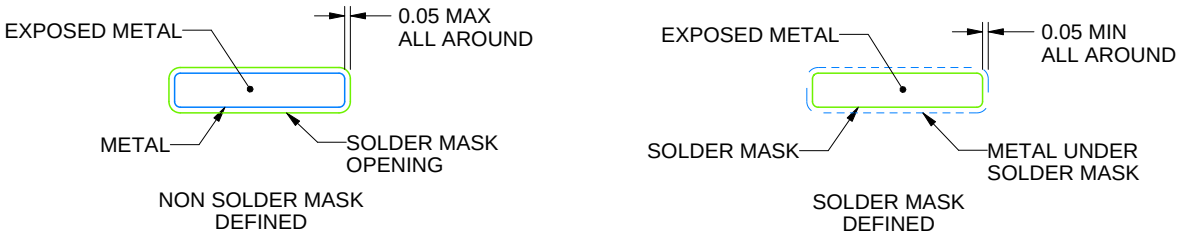
4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

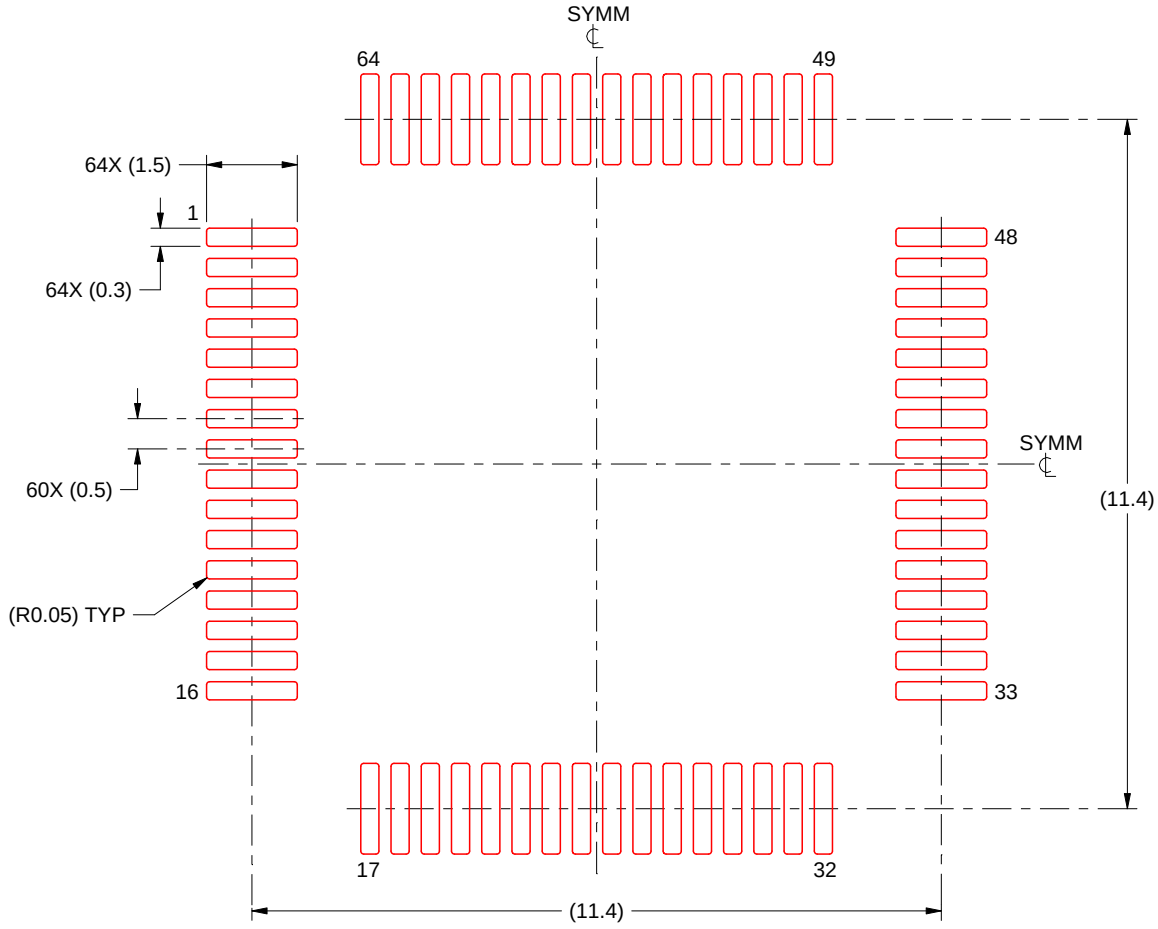


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025