Application Report
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# bq27541 to bq27541-v200 Change List

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**ABSTRACT**

This document describes the design changes from the bq27541 (firmware version 1.12) to bq27541-v200 (firmware version 2.00). For ordering information and data sheet, see the Texas Instruments Web site at http://www.power.ti.com.

## Change Details

This firmware release fixes the known bugs in the bq27541 with firmware v1.12 and upgrades it to bq27541-v200 with firmware v2.00. It also added new features and Impedance Track™ enhancements to improve performance. The latest ordering information and data sheet are available on the TI web site. The latest version of the evaluation software is required to be able to use the new commands and read/write to all the new data flash configuration locations.

| ID | bq27541-v200 | bq27541 | Comment |
|---|---|---|---|
| 1 | New life-time data logging feature. See the data sheet for new data flash added. | No life-time data logging feature | New feature |
| 2 | Configurable ADC Ground Select between Vss and SRP. This feature addresses board level layout issues and provides configurability. Default is set to Vss | ADC reference is hardwired to SRP. | New feature |
| 3 | New 8-byte serial number in data flash. See the data sheet Section 5 for details | No serial number feature | New feature |
| 4 | Voltage at charge termination now saved and is used in DOD at EOC calculation. | Voltage at charge termination is not saved | New feature |
| 5 | Add OCVTaken flag. Flag is cleared at entry to relax and set at first OCV in relax. | No OCVTaken flag to indicate OCV measurements | New feature. |
| 6 | Add new data commands:<br>a) Internal_Temp()<br>b) StateOfHealth()<br>c) PassedCharge()<br>d) DOD0()<br>e) PackConfig()<br>See data sheet for command details. | These commands are unavailable. | New features |
| 7 | Add new data flash parameter DF Config Version and Control() subcommand DF_VERSION to report value. This feature enables customer to track data flash versions. | No DF_VERSION subcommand and DF Config Version data flash. | New feature |
| 8 | SE Pin state is based on HIBERNATE mode. New Pack Configuration register bit SE_EN is added to enable function. See data sheet for system shutdown enable operations. | SE Pin function cannot be disabled | New feature. |
| 9 | Temperature Compensation to improve reference voltage drift with temperature to improve voltage measurement accuracy | No temperature compensation for voltage drift. | Measurement enhancement |
| 10 | New data flash parameters for Ra computation:<br>a) Ra Filter,<br>b) Ra Max Delta<br>c) Max Res Factor<br>d) Min Res Factor<br>New Pack Configuration Register bit ResFactorStep (bit 6) to enable or disable of Ra steps up/down to max/min Res Factor before disabling Ra updates.<br>This feature eliminates unexpected fluctuation in the updated Ra values to avoid data corruption due to extreme data | No Ra filtering function. Ra value can change abruptly. | Impedance Track™ enhancement |

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| 11 | New data flash filtering parameters to limit Avg I/P Last Run to DesignCapacity/Max Sim Rate and DesignCapacity/Min Sim Rate :<br>a) Max Sim Rate<br>b) Min Sim Rate | No Sim Rate configuration to limit Avg I/P simulation. | Impedance Track™ enhancement |
| 12 | New data flash filtering parameter DeltaV Max Delta to limit change of DeltaV. | Delta V value change is not limited. | Impedance Track™ enhancement |
| 13 | New data flash filtering parameter Qmax Max Delta % to limit change of Qmax during update as a percentage to Design Capacity. | Qmax change is not limited. | Impedance Track™ enhancement |
| 14 | Allow extrapolation of Ra of next grid on exit of discharge if the terminated voltage is reached. | No extrapolation of Ra allowed unless grid point is reached | Impedance Track™ enhancement |
| 15 | Qstart/RM/FCC are updated under the following additional conditions:<br>a) Start of charge<br>b) Temperature change > DODatEOC Delta T<br>c) Charge termination<br>d) At rest during each 1-hr DOD0 update interval | Qstart/RM/FCC is not updated during these conditions. | Impedance Track™ enhancement |
| 16 | When overdischarged below termination voltage, internal True Remaining Capacity continues to count negative and RM remains 0. RM remains 0 until internal True Remaining Capacity is charged to positive value.<br>When overcharged above FCC, internal True Remaining Capacity continues to count and RM remains equal to FCC. RM starts to count down when internal True Remaining Capacity becomes less than FCC. This feature improves remaining capacity calculation. | When overdischarged, RM starts to count up immediately when charging begins. This causes overestimation of capacity.<br>When overcharged, RM starts to count down immediately when discharge begins. This causes underestimation of capacity. | Impedance Track™ enhancement |
| 17 | Use two exponent Rb tables for enhanced cold temperature modeling to improve cold temperature accuracy | Single Rb exponent is used for full temperature range. | Impedance Track™ enhancement |
| 18 | Improve IR Compensation to simulate OCV under load up to C/5 | C/20 is the maximum OCV under load allowed for IR compensation | Impedance Track™ enhancement |
| 19 | New data flash parameters T rise and T Time Constant for thermal Modeling. Thermal modeling is used to model for self-heating. | No thermal modeling | Impedance Track™ enhancement |
| 20 | New Transient modeling to model loading change. | No transient modeling | Impedance Track™ enhancement |
| 21 | Fix HW_VER Command to show correct hardware "B4" | HW_VER command shows "00" | Bug fix |
| 22 | CHG_INH and XCHG bits are set based on temperature settings in data flash only. | CHG_INH and XCHG bits are set based on temperature settings in data flash and FC flag is set | Bug fix |
| 23 | PREV_MAC command limits command to < 0x0020 | PREV_MAC command limits command to < 0x000b | Bug fix |
| 24 | Do not update Qmax if RUP_DIS bit set | Qmax is updated regardless of RUP_DIS bit | Bug fix |
| 25 | When loading requirement is not met during discharge grid point, previous resistance data is preserved for the skipped point. | When loading requirement is not met during discharge grid point, resistance is interpolated for the skipped point. | Bug fix |
| 26 | On an exit from discharge in which min DoD has been passed, only allow the extrapolation of R values for the grid points during a learning cycle. | Extrapolation is allowed on any cycle. | Bug fix |
| 27 | Add a check to force SOC to 0 if RM and FCC are ≤ 0. | SOC is 100 when RM & FCC are ≤ 0. | Bug fix |
| 28 | Enable use of secure memory key for authentication by setting data flash key to all zeros. | Secure memory key cannot be enabled. | Bug fix |
| 29 | AtRateTTE reports 65535 when AtRate is set to 0. | AtRateTTE reports are incorrect when AtRate is set to 0. | Bug fix |



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