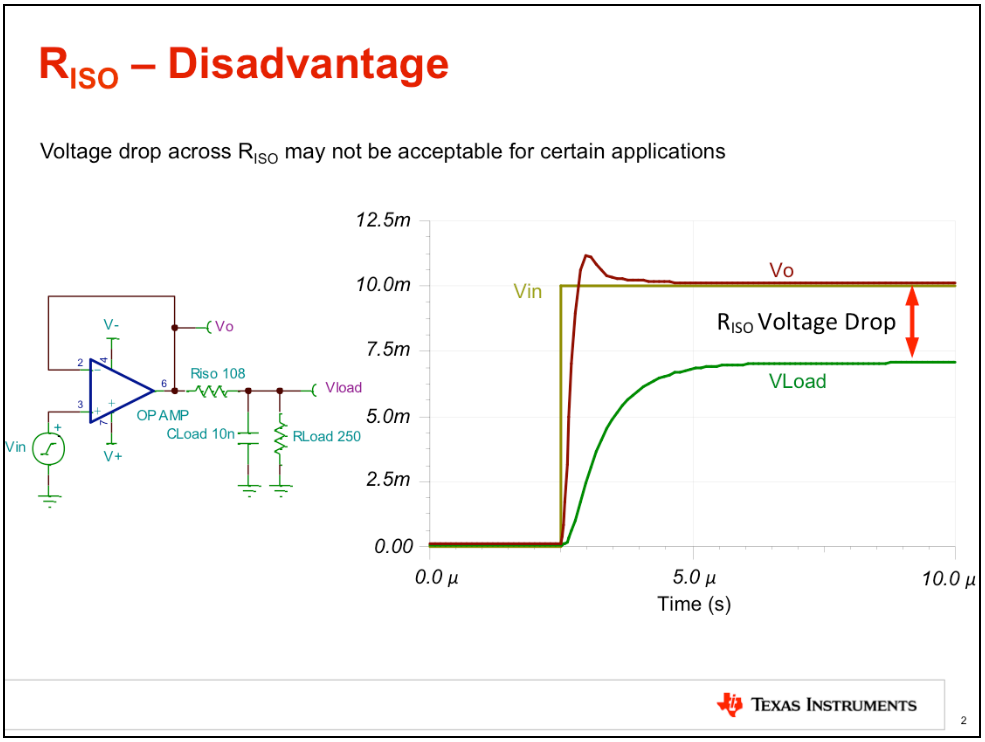
Hello, and welcome to part six of the TI Precision Labs on op amp stability. This lecture will describe the Riso with dual feedback stability compensation method.

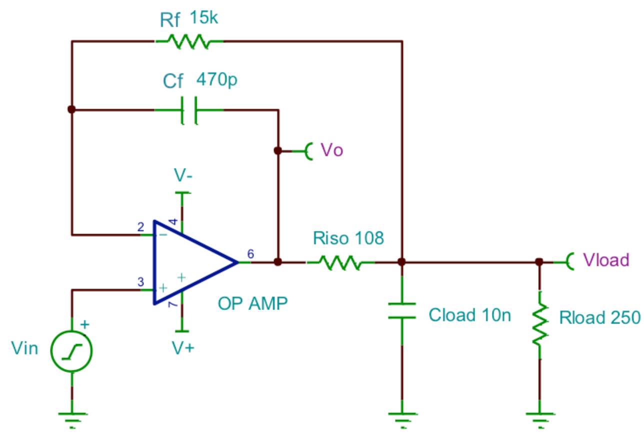
From 5:

The previous videos discussed the concepts involved in basic stability theory as well as how to test and simulate for stability issues in SPICE and on the bench. This video will discuss why capacitive loads cause stability issues as well as presenting the first capacitive load compensation technique using an isolation resistor.

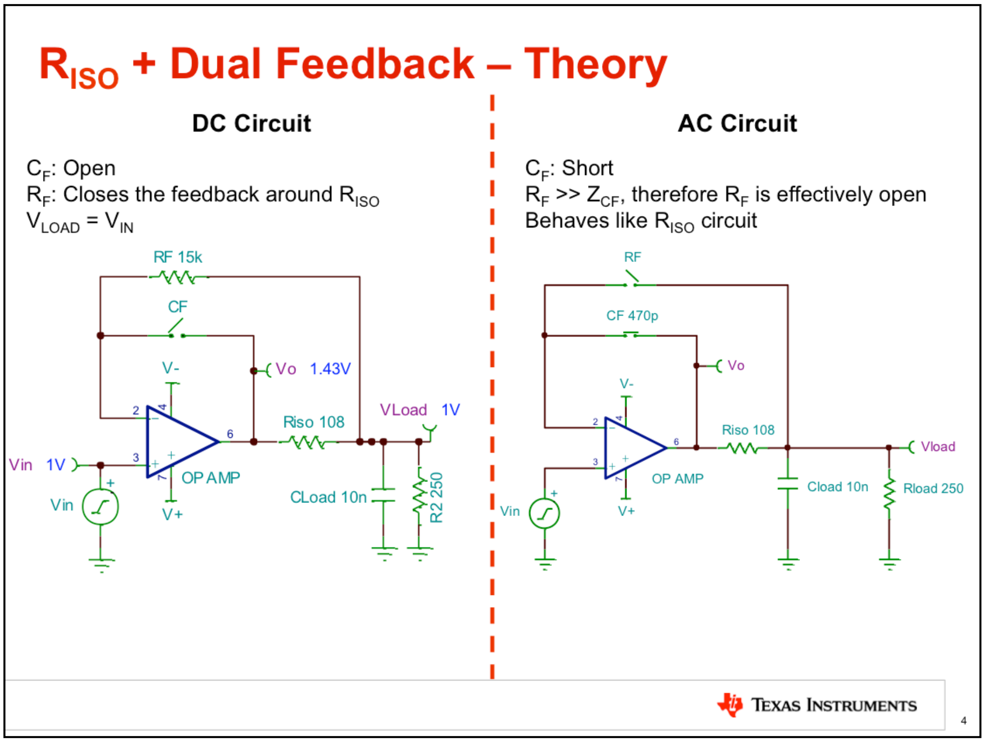


While the Riso circuit is both simple to implement and design it has a big disadvantage in precision circuits. The voltage drop from Riso is dependent on the output current or output load, and may be significant compared to the desired signal. As shown here, a 10mV signal has over 3mV (30%) of error due to a 250Ω output load.

R_{ISO} + Dual Feedback



A solution to the voltage drop problem from the Riso circuit is to implement the "Riso + Dual Feedback" circuit shown here.



The operation of the Riso + dual feedback circuit can be analyzed using the equivalent dc and ac representations of the circuit.

At dc, the feedback capacitor Cf acts as an open circuit and Rf closes the feedback loop around Riso. Since Riso is now in the op amp feedback loop, the op amp output will increase to overcome the Riso voltage drop such that the load voltage, Vload, is equal to Vin.

At ac frequencies, Cf acts as a short. When this happens, Rf can be thought of as an open-circuit because the impedance of Cf, X_{CF}, will be much smaller than the impedance of Rf. Therefore, at ac, this circuit looks effectively the same as the standard Riso circuit.

R_{ISO} + Dual Feedback - Design

Design Steps:

1) Set R_{ISO} using Method 1: R_{ISO} techniques
2) Set R_F: $R_F \ge (R_{ISO} * 100)$
3) Set C_F: $6*R_{ISO}*C_{LOAD}/R_F \le C_F \le 10*R_{ISO}*C_{LOAD}/R_F$ **lower values of C_F = faster settling, higher overshoot**

Rule 3 ensures that the two feedback paths will never create a resonance that would cause instability

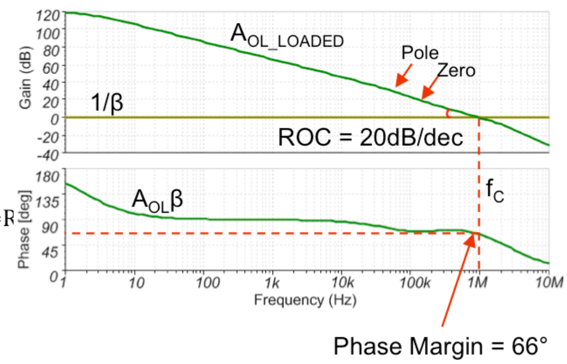
$R_{ISO} = 108\Omega$

$R_F \ge R_{ISO} * 100$

$R_F \ge 10.8k\Omega$

$6*R_{ISO}*C_{LOAD}/C_F \le C_F \le 10*R$

$\mathbf{420pF \le C_F \le 720pF}$



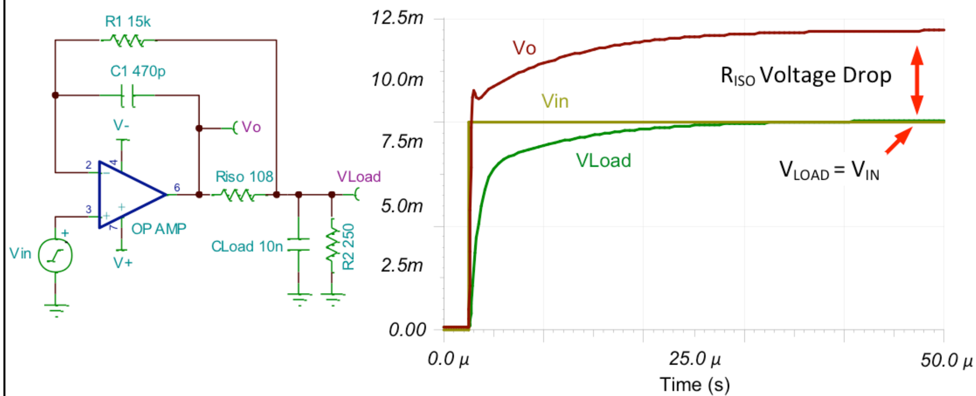
The first design step in this circuit is to select Riso. The same method that was used to select Riso in “Method 1: Riso” is used here, and Riso is selected to produce a zero in the Aol curve at f(Aol = 20dB).

Then, Rf can be selected to any value greater than 100*Riso in order to prevent interactions with Riso.

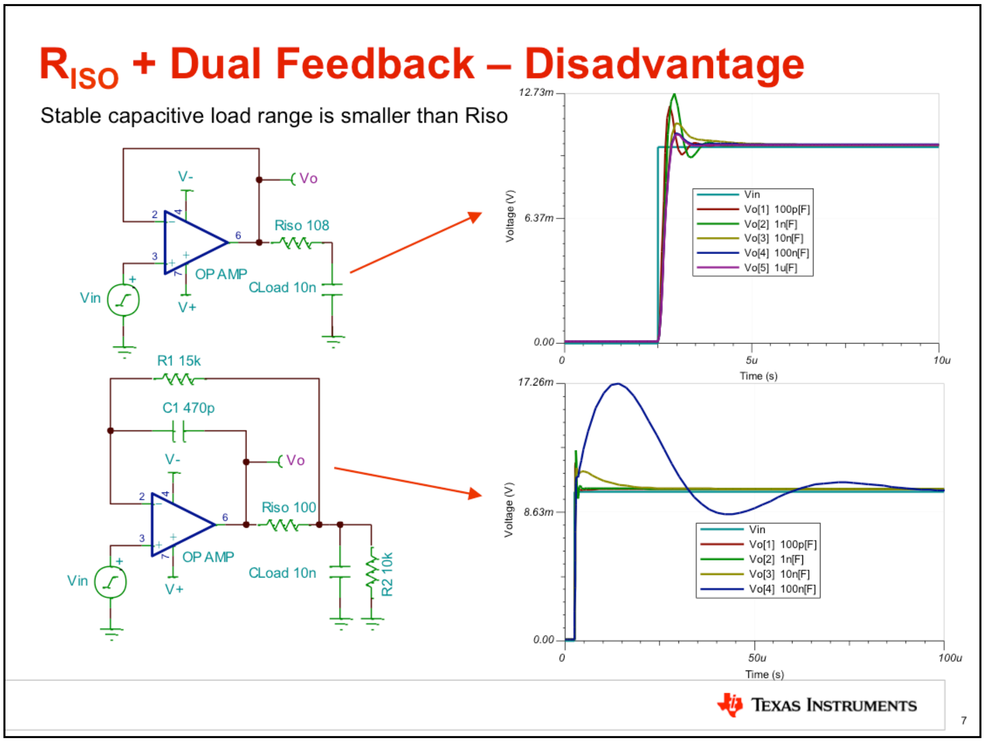
The last step is to select a value of Cf in the range shown. Using this range ensures that the two feedback paths, Rf and Cf, will never create a resonance that would cause instability. Smaller values for Cf will result in faster settling time, at the expense of overshoot for certain load ranges.

R_{ISO} + Dual Feedback - Results

- V_{LOAD} matches V_{IN} – No voltage divider error!
- This topology has some limitations on settling time and capacitive load range

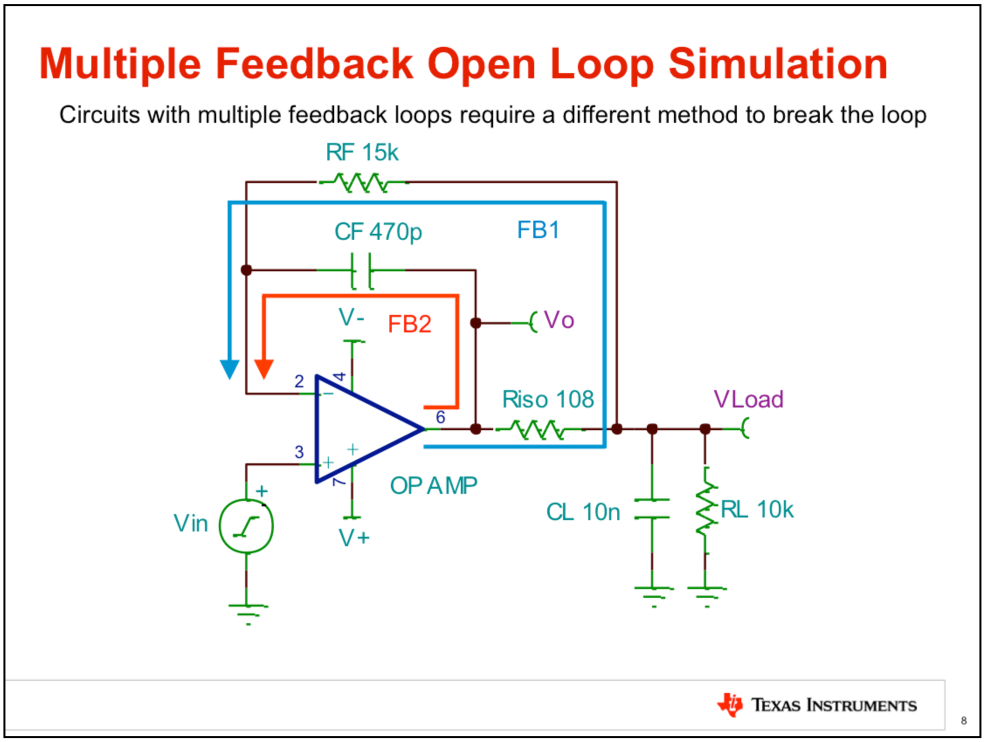


The results show that the output and load voltage arrive at the final level without excessive overshoot or ringing, indicating a stable system. The increase in Vo to overcome the voltage drop from Riso can also be clearly seen here.



While the Riso + Dual Feedback circuit solves the dc accuracy issue with the Riso circuit, it has some disadvantages as well. As shown here an Riso circuit will generally remain stable with reasonable variation in the transient response over a wide range of capacitive loads. The Riso+Dual Feedback circuit is not as tolerant to changes in the output capacitance and can quickly become unstable. Therefore, the Riso + Dual Feedback circuit is best for situations where the output capacitance is known and will not vary significantly.

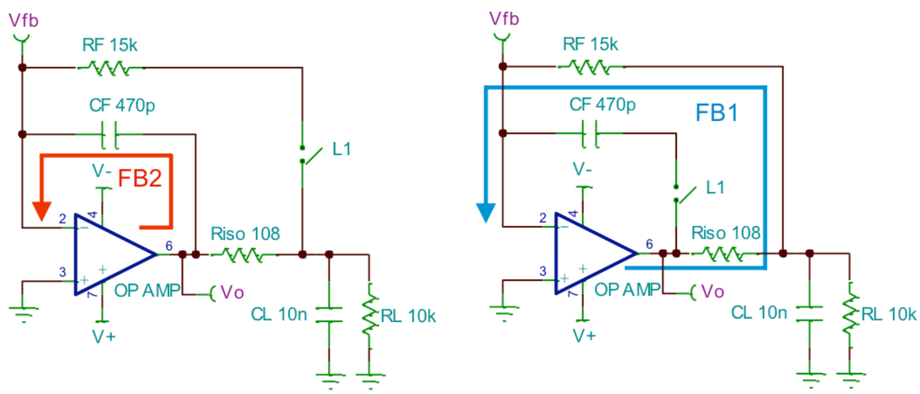
The Riso+Dual Feedback method generally results in a slower settling time than the Riso circuit as well.



Stability part 3 showed how to perform open-loop analysis on many common op amp circuits. However, those circuits all had only one feedback loop. If we want to perform a simulated open-loop analysis on multiple-feedback circuits, like the circuit with Riso + dual feedback compensation, a different method is required which we'll now discuss.

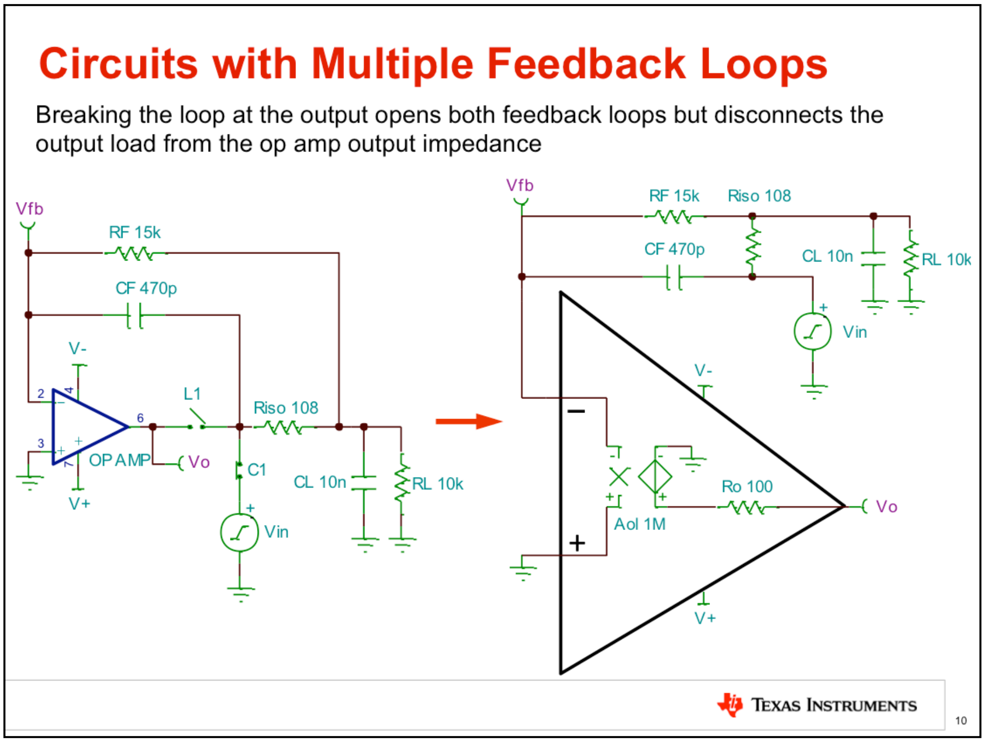
Circuits with Multiple Feedback Loops

Breaking either loop of the feedback network as shown before still results in a closed loop path through the other feedback loop



TEXAS INSTRUMENTS 9

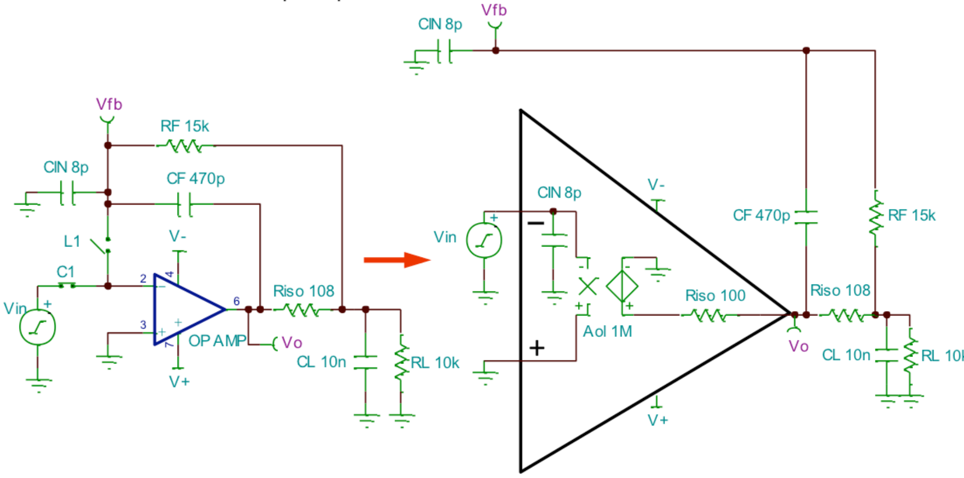
Opening either feedback path still leaves a closed-loop path around the other loop. If FB1 is opened, FB2 remains as a closed-loop feedback path. If FB2 is opened, FB1 remains as a closed-loop feedback path. The circuit will not properly report open-loop curves unless both feedback loops are open.



Breaking the loop directly at the output will remove the connections between the output and both feedback loops resulting in an open-loop circuit. However breaking the loop in this location disconnects the output capacitive load, CL from the op amp output. Therefore, CL will not interact with the open-loop output impedance, Ro, preventing the simulation from identifying possible stability issues caused by the capacitive load as discussed in the previous video.

Circuits with Multiple Feedback Loops

Breaking the loop at the input opens both feedback loops while leaving the output load connected to the op amp



TEXAS INSTRUMENTS 11

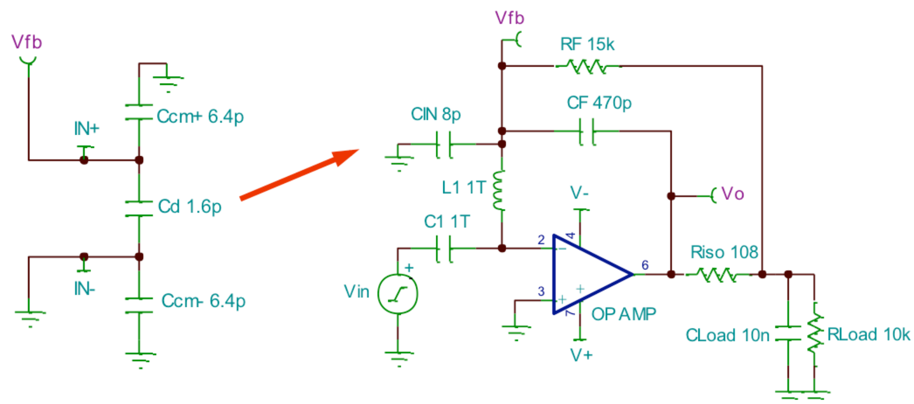
The recommended method for this circuit and other similar circuits with multiple feedback loops is to break the loop directly at the inverting input of the amplifier. Breaking the loop in this location also disconnects both feedback loops, but now the output impedance of the op amp can interact with the output loading and feedback network.

However, by breaking the loop at the input, the inherent input capacitance of the amplifier no longer interacts with the feedback network. Therefore, it is required to place a representation of the amplifier input capacitance, CIN, on the other side of the inductor to match the amplifier input capacitance.

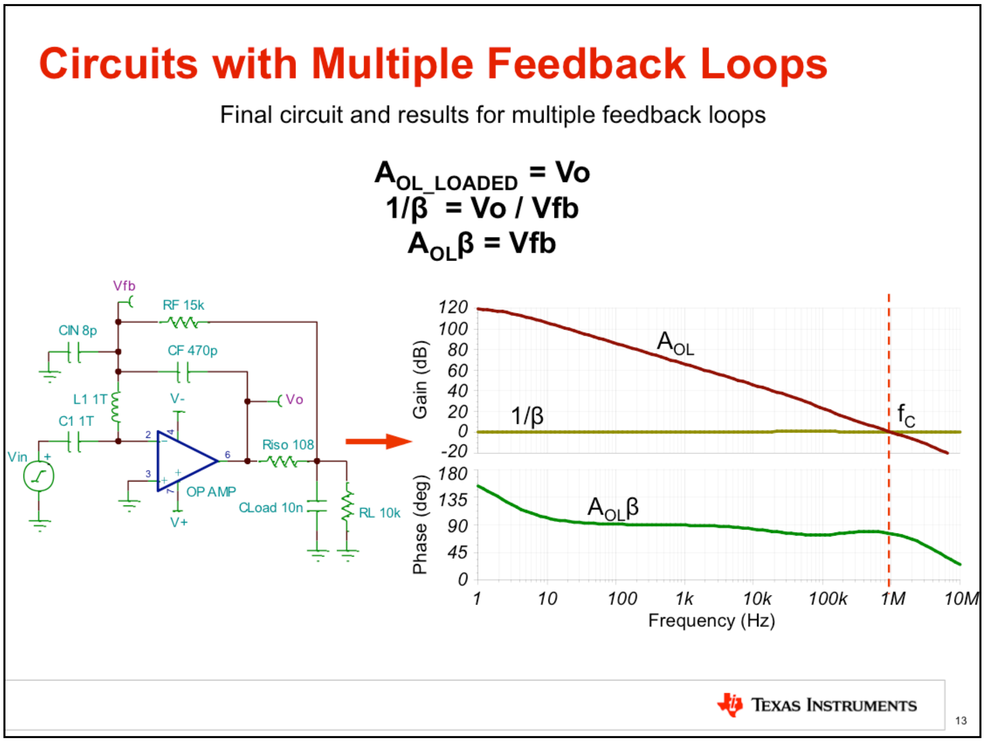
Circuits with Multiple Feedback Loops

Determining the op amp input capacitance model

INPUT IMPEDANCE			
Z_{ID}	Differential	100 || 1.6	MΩ || pF
Z_{IC}	Common-mode	1 || 6.4	10^{13}Ω || pF



The differential and common-mode input capacitances are typically specified in op amp datasheets. The information can be used to develop a simple model of the input capacitance of the amplifier as shown. In this circuit the non-inverting input is grounded so the negative common-mode capacitor is shorted out and the positive common-mode capacitor and differential input capacitor are in parallel with each other. The parallel sum of the two capacitors is 8pF and should be added to the circuit above the inductor as shown.



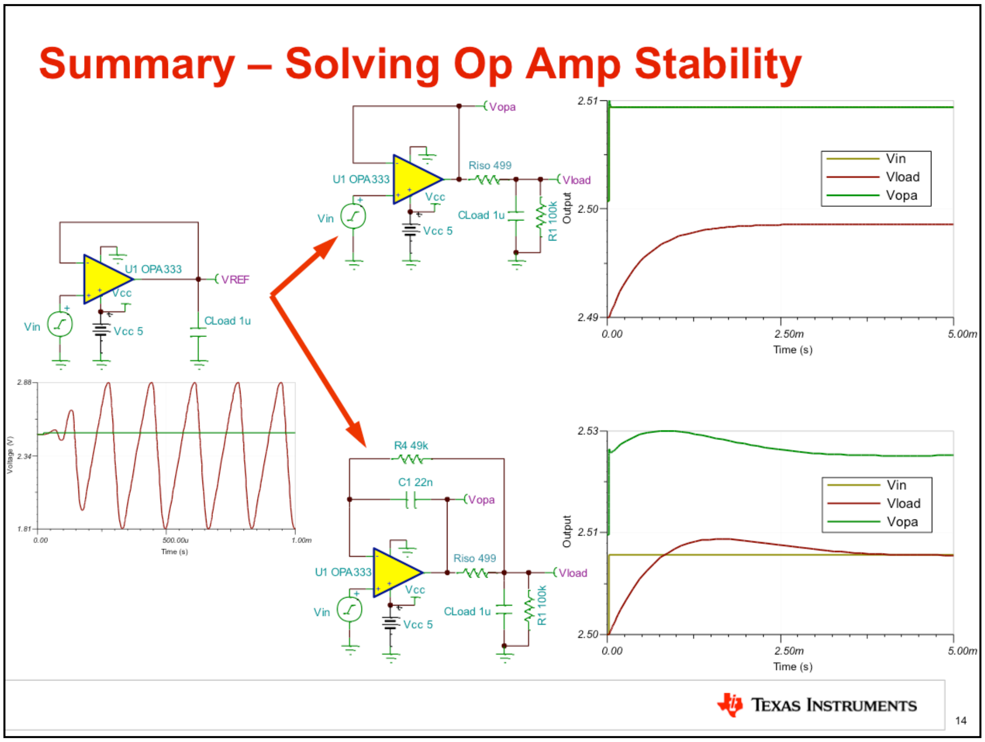
Breaking the loop at the input requires different equations to obtain the open-loop results. The equations for generating the desired curves are as follows:

Aol_loaded = Vo/Vfb

1/ß = 1/Vfb

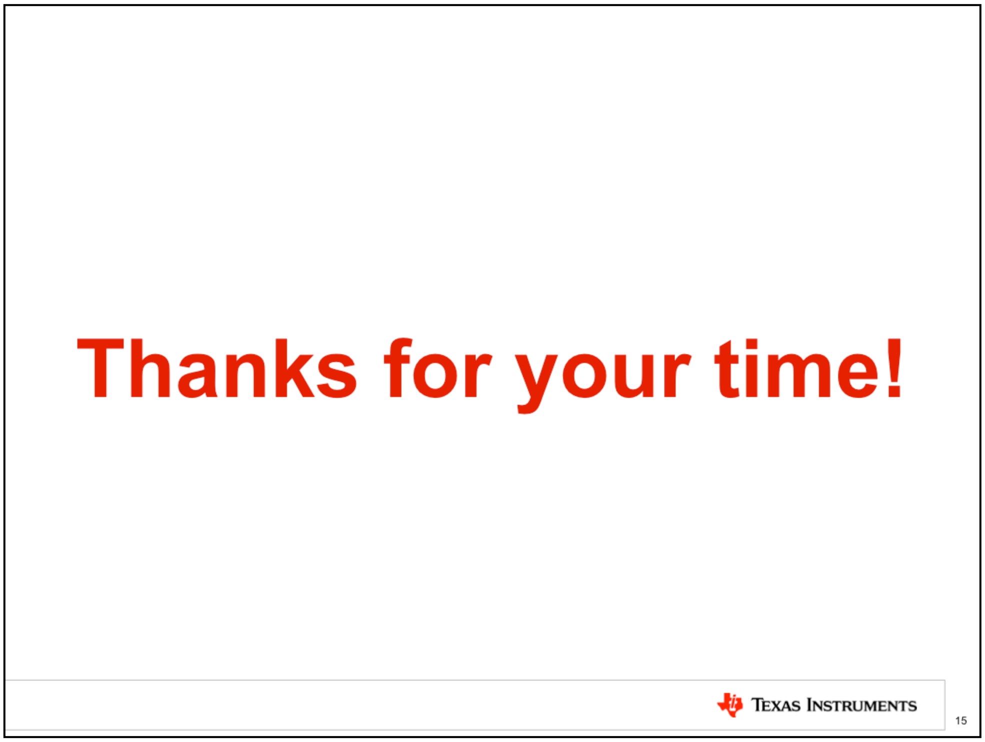
Aol*ß = Vo

The procedure for determining the rate of closure and measuring the phase margin is the same as before.



In summary, this video described the Riso + dual feedback method for stability compensation and showed its advantage of DC accuracy compared to the Riso method. A new method for performing open-loop simulation analysis on multiple feedback circuits was also shown.

While both the Riso and Riso + dual feedback compensation methods are effective there are many other methods that can also be used to compensate stability issues. Stay tuned for future videos which will detail more compensation methods that are better suited for certain applications.

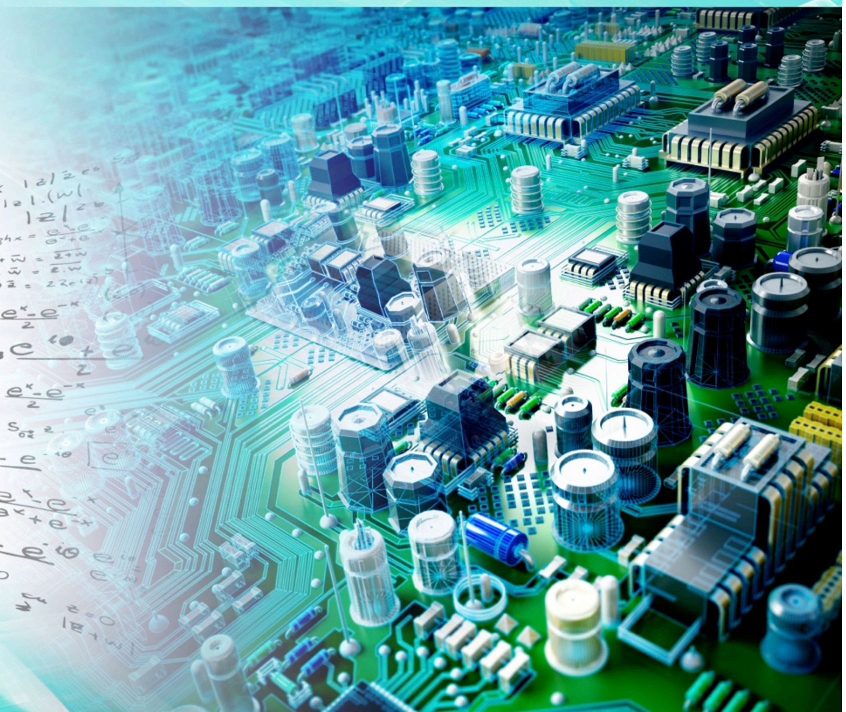


That concludes this presentation – thank you for your time! Please try the quiz to check your understanding of this video's content.

Stability 6

Multiple Choice Quiz

TI Precision Labs – Op Amps



Quiz: Stability 6

1. (T/F) The Riso + Dual Feedback stability method suffers from the same dc voltage errors at the load as the Riso circuit.

a. True
b. False

2. (T/F) When properly designed, the Riso + Dual Feedback stability behaves very similarly to the Riso circuit at ac frequencies.

a. True
b. False

3. (T/F) Stability issues can occur in the Riso + Dual Feedback circuit due to resonance in the feedback paths if the feedback capacitor is not properly selected.

a. True
b. False

4. (T/F) The Riso + Dual Feedback circuit is typically less sensitive to changes in the load capacitance than the Riso circuit.

a. True
b. False

Quiz: Stability 6

5. (T/F) The method discussed in Part 3 can be used to break the loop and measure the open-loop results on circuits with multiple feedback loops.

a. True
b. False

6. Breaking the feedback loop at the ________ of the circuit is the recommended method to test circuits with multiple feedback loops.

a. Input
b. Output

7. When breaking the loop at the input of multiple feedback circuits, the effects of the amplifier’s _________ must be externally added to the circuit.

a. Open-Loop Gain
b. Input Resistance
c. Input Capacitance
d. Output Impedance

Stability 6

Multiple Choice Quiz: Solutions

TI Precision Labs – Op Amps

Quiz: Stability 6

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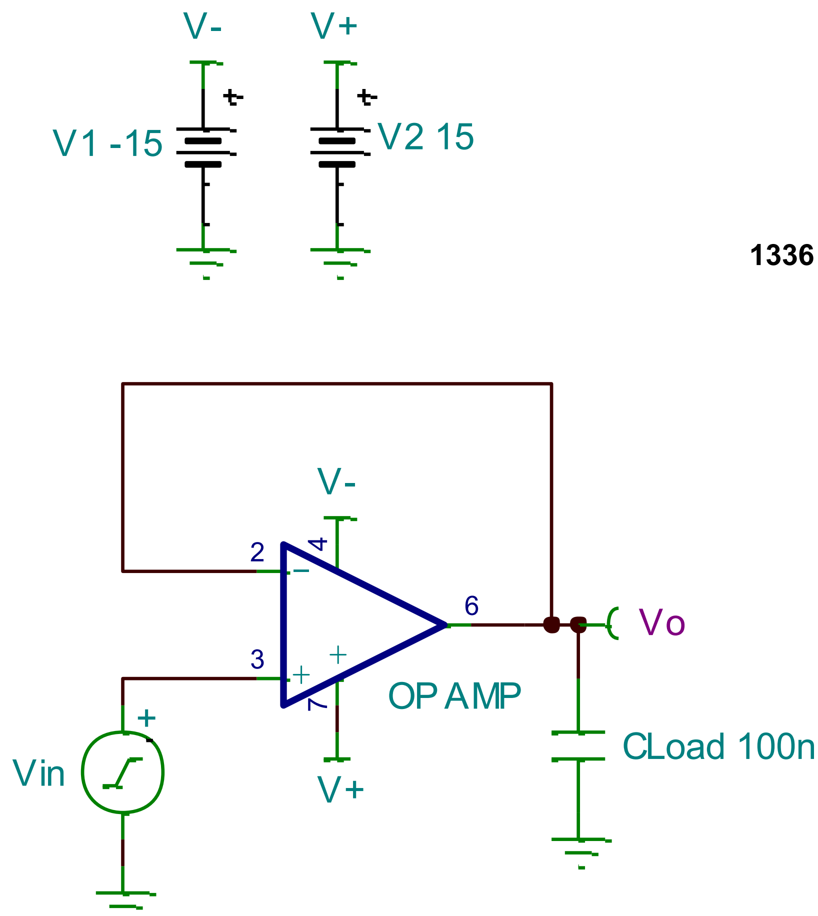
Stability 6

Exercises

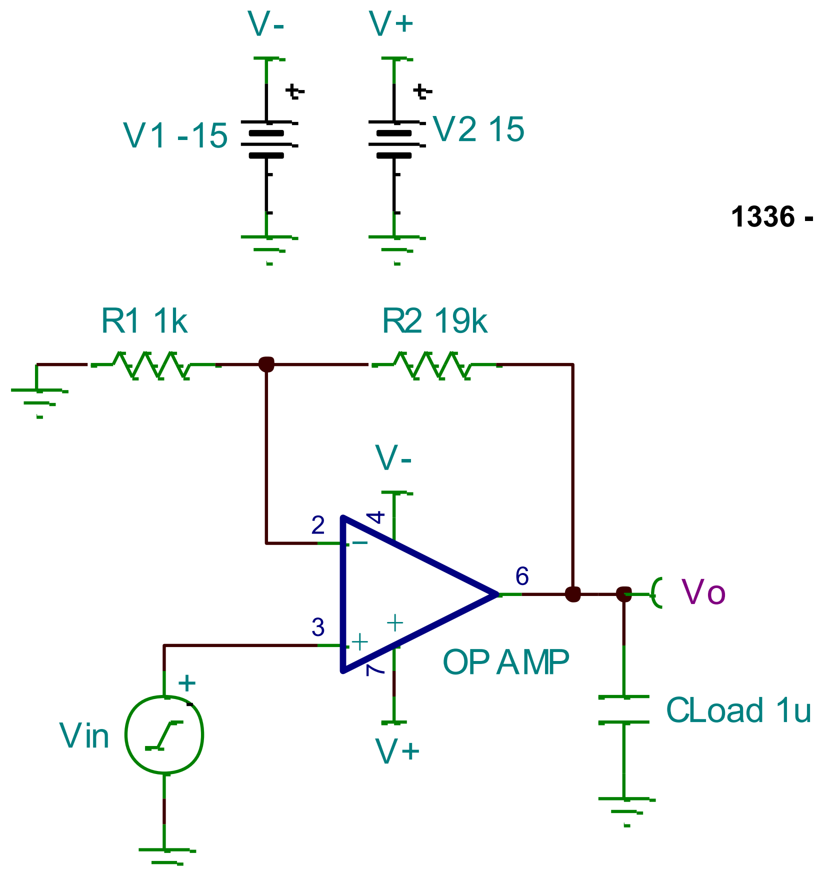
TI Precision Labs – Op Amps

1. Compensate the amplifier circuit using the R_{ISO} + Dual Feedback method so the final circuit has at least 60° of phase margin. Assume the input capacitance totals to 8 pF for this amplifier.



1336 - Stability 6 - Problem 1.TSC

2. Compensate the amplifier circuit using the R_{ISO} + Dual Feedback method so the final circuit has at least 60° of phase margin. Assume the input capacitance totals to 8 pF for this amplifier.

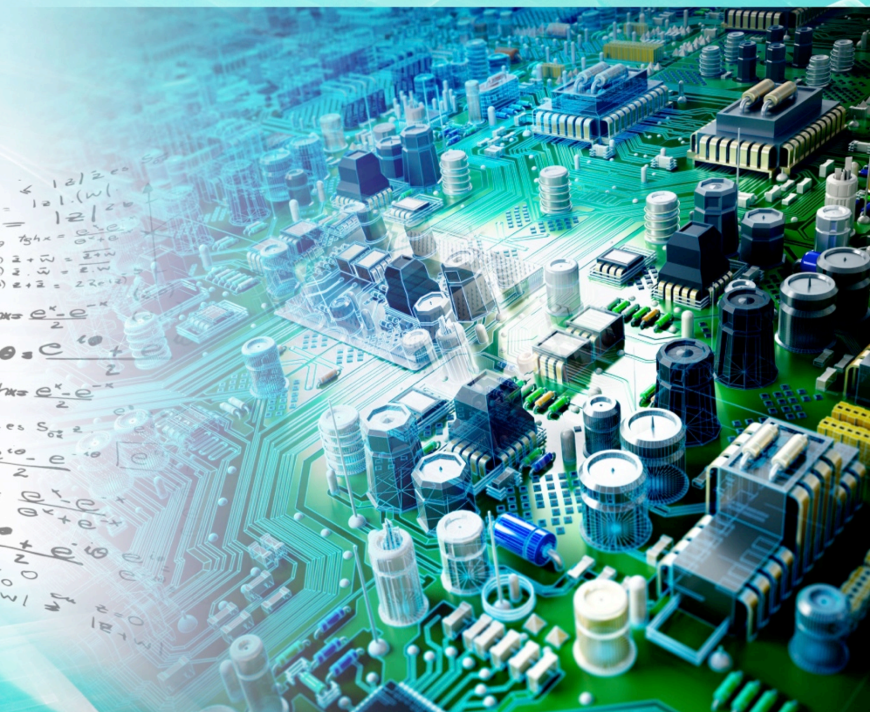


1336 - Stability 6 - Problem 2.TSC

Stability 6

Solutions

TI Precision Labs – Op Amps



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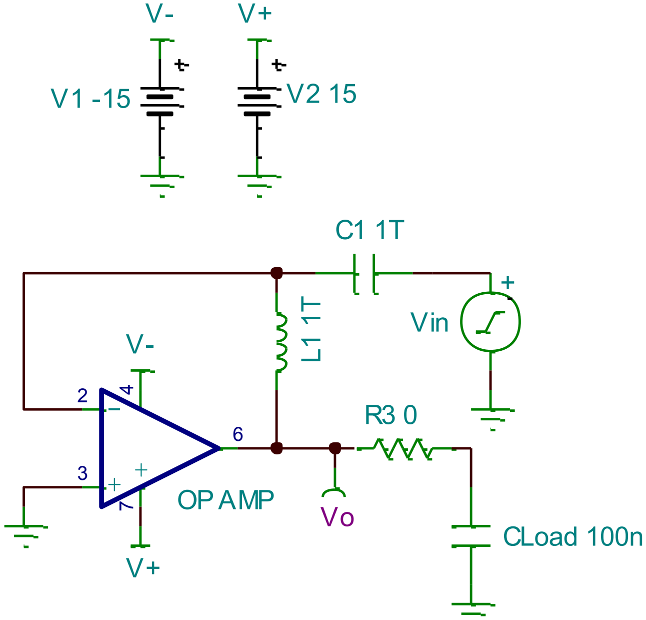

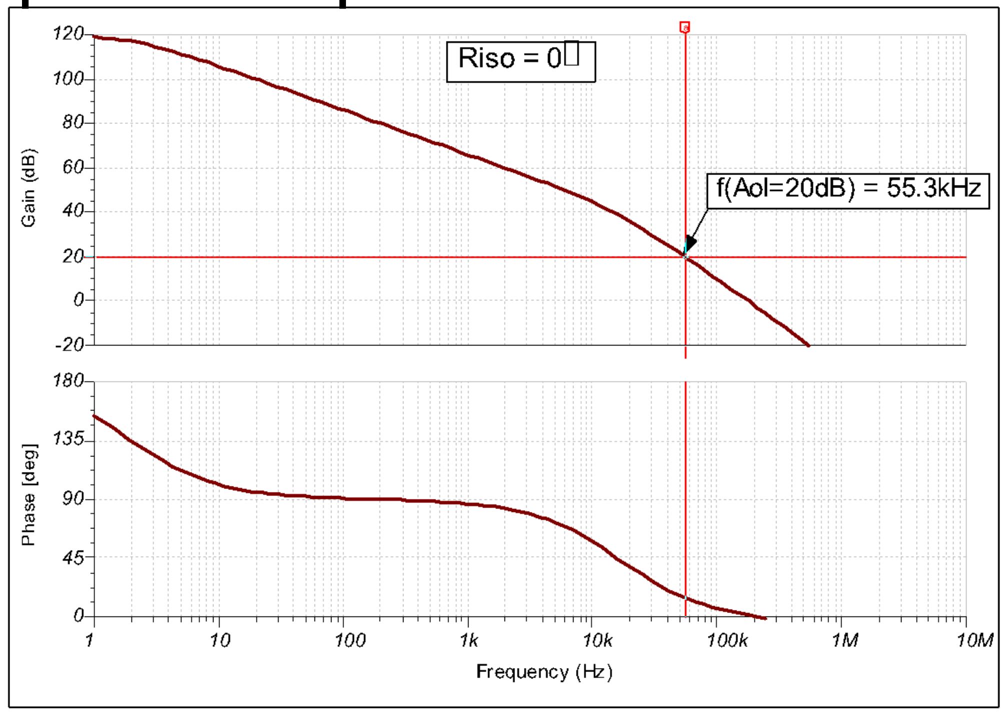

1336 - Stability 6 - Problem 1 - Solution.TSC

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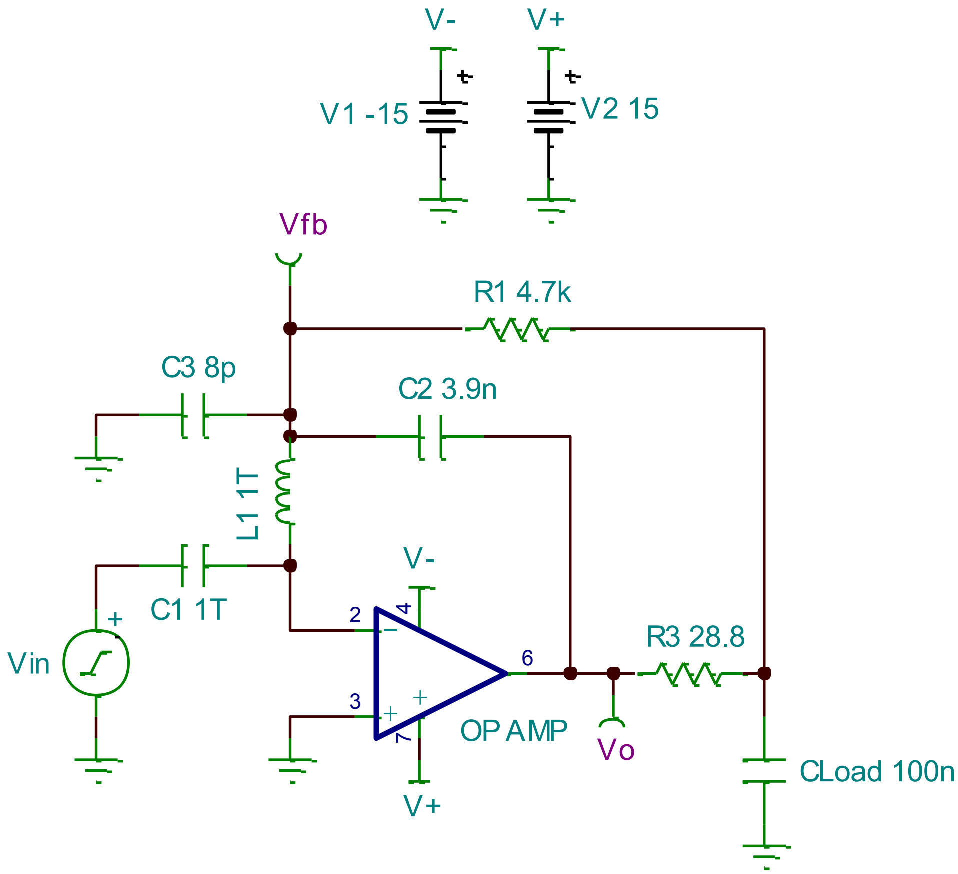

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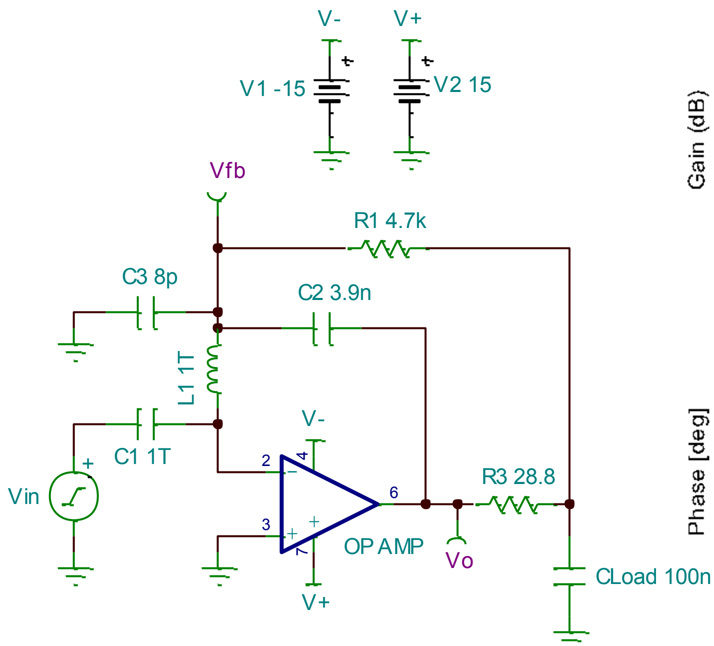

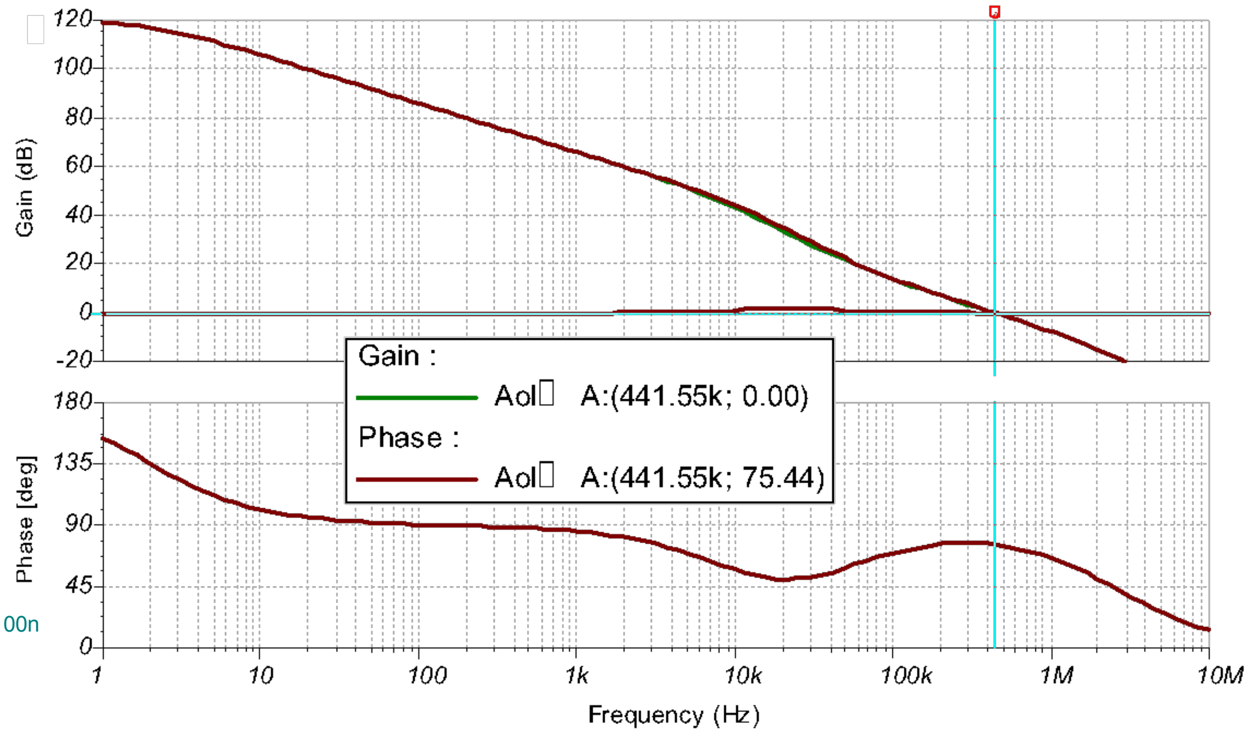

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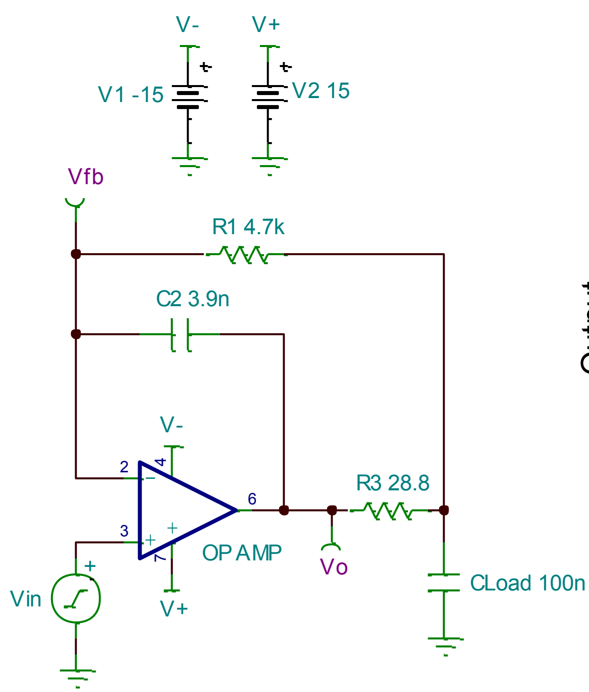

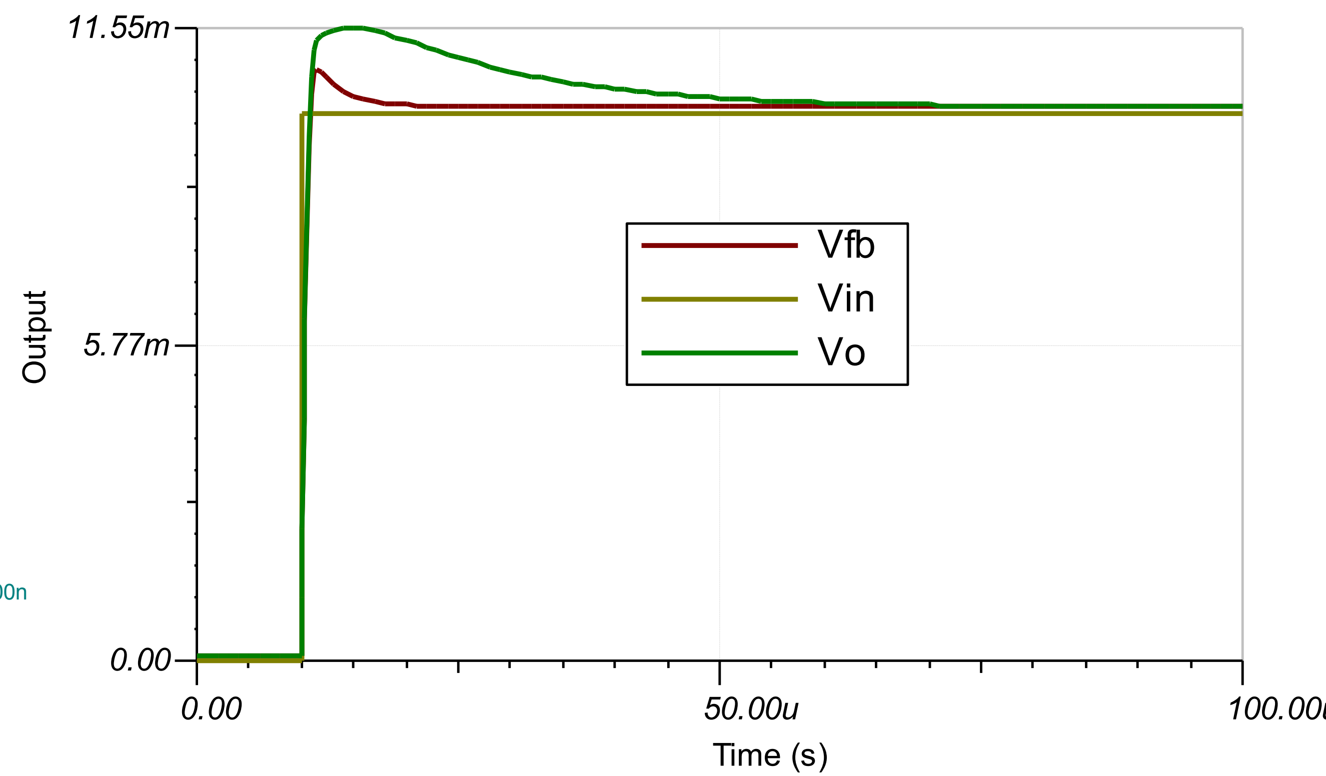

1336 - Stability 6 - Problem 1 - Solution2.TSC

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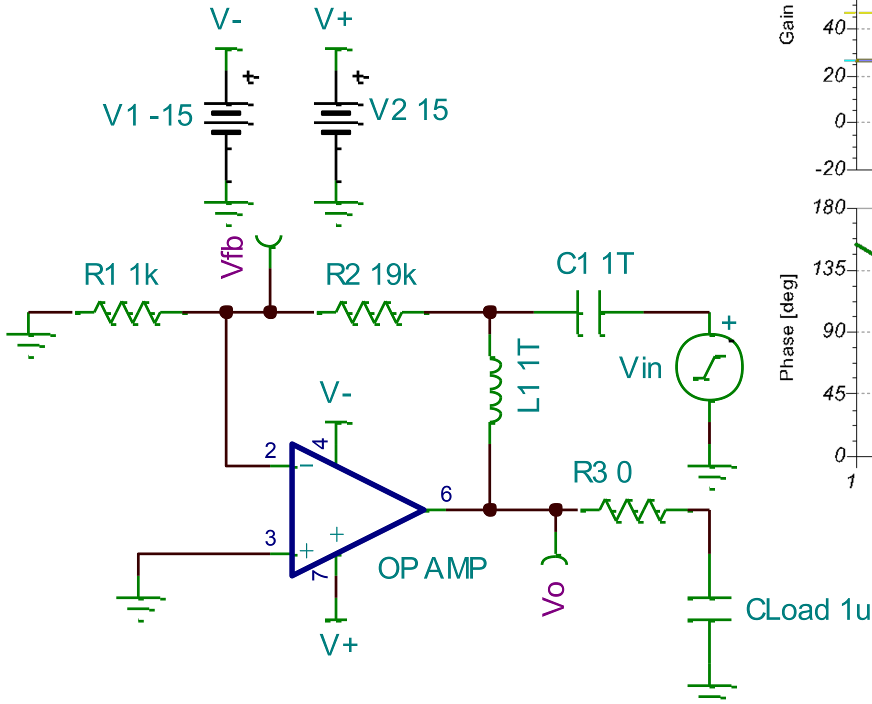
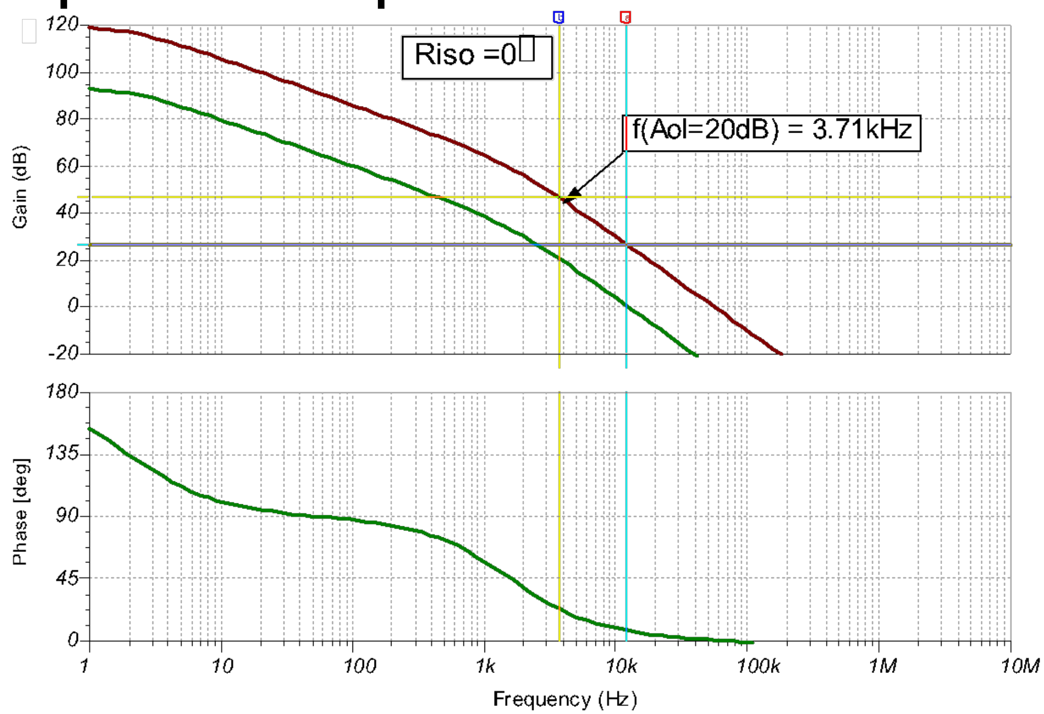
1336-STAB6-Problem_2_Solution.TSC





1336 - Stability 6 - Problem 2 - Solution.TSC

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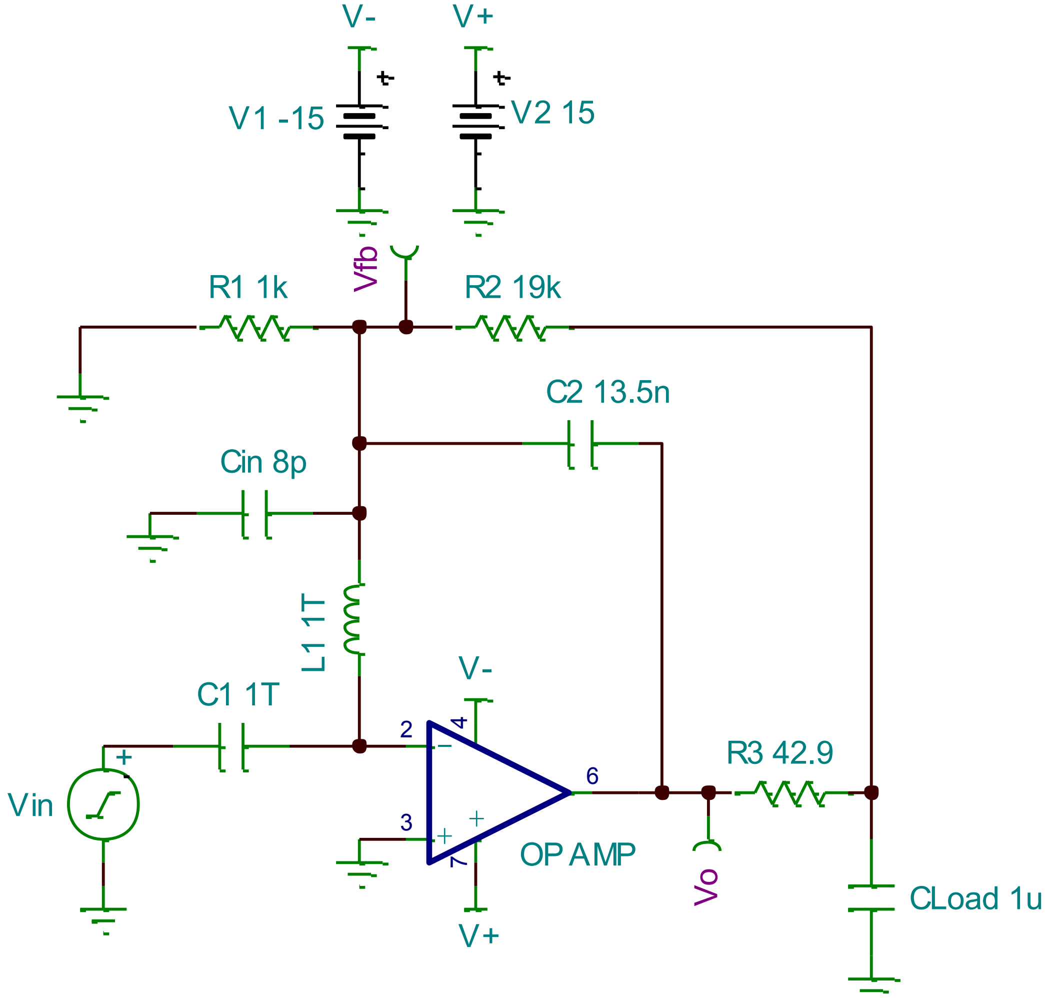

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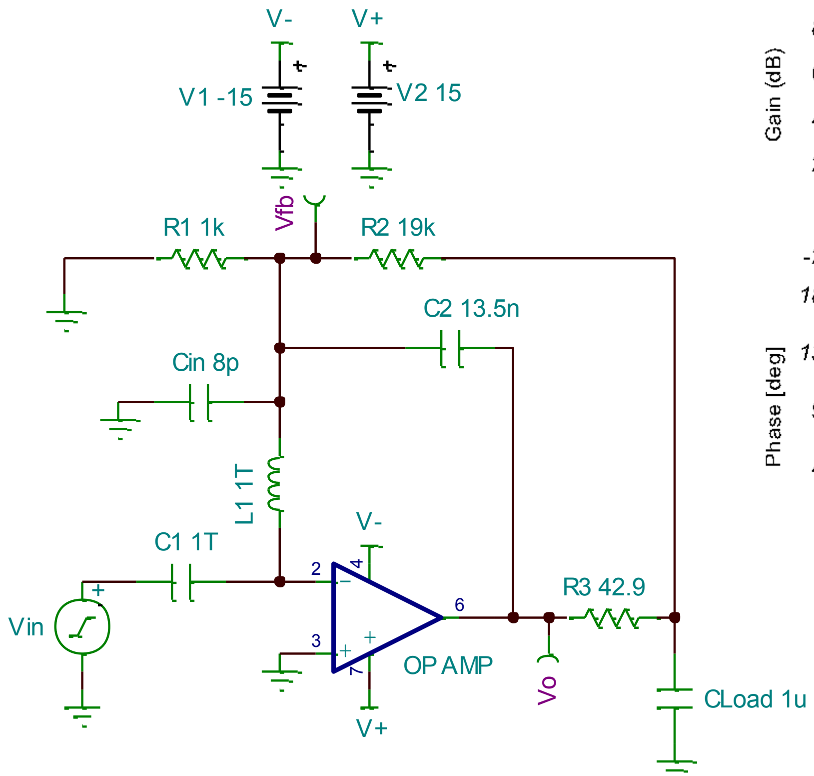

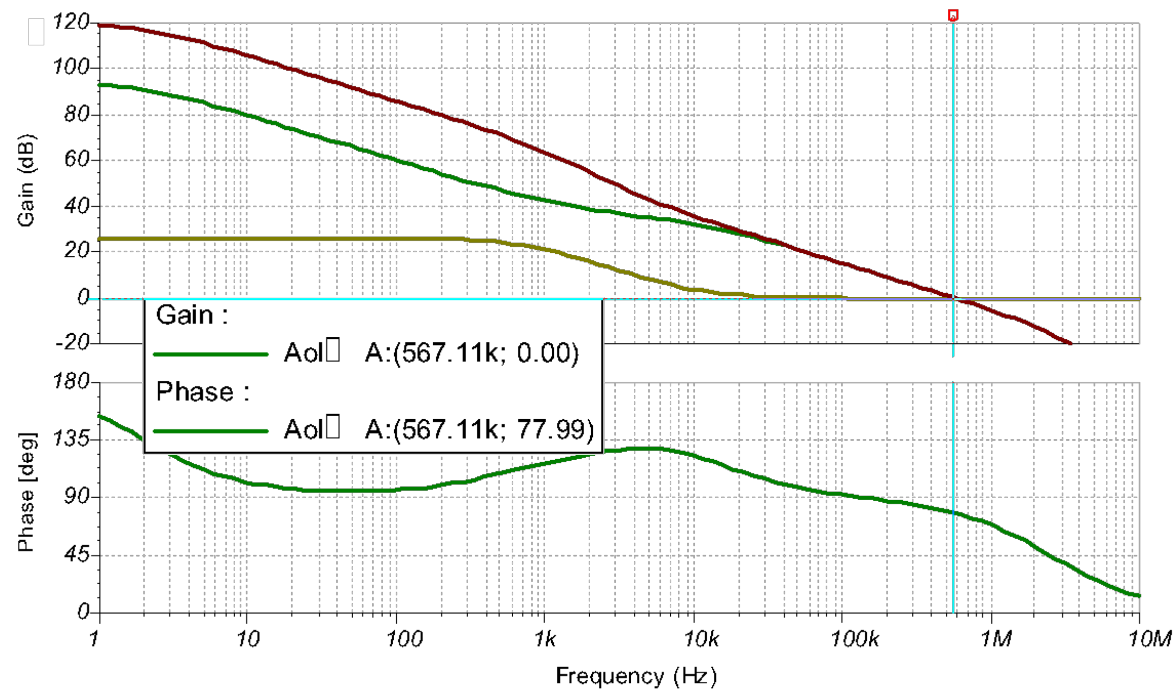

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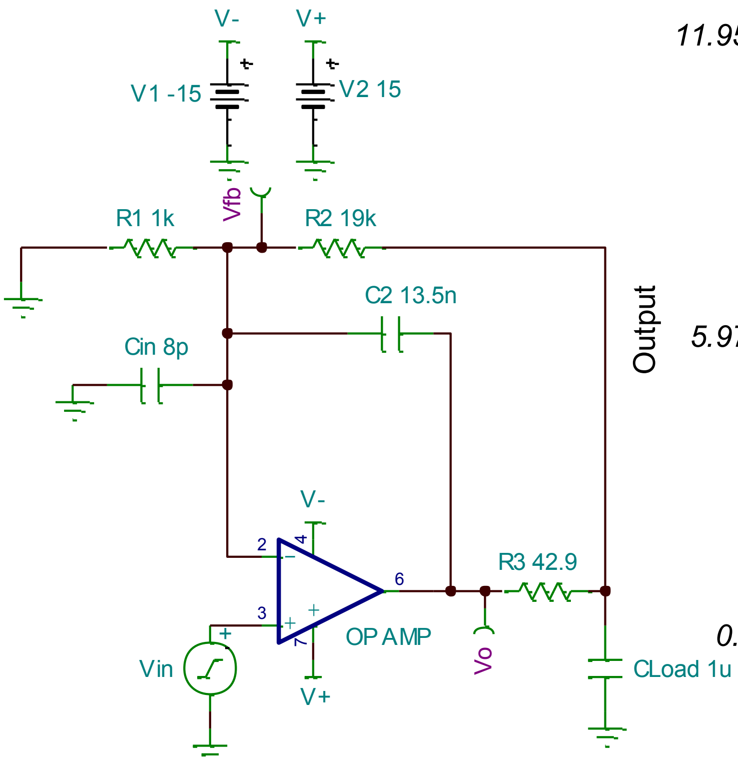

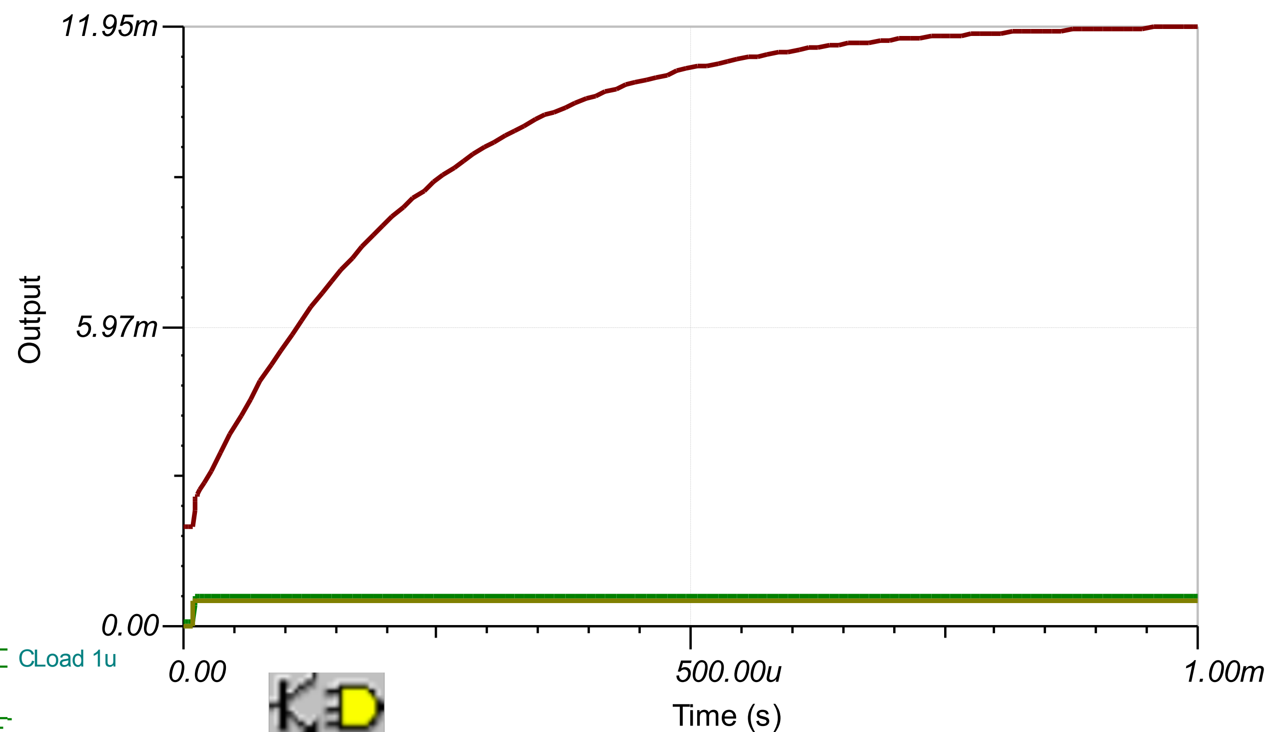

1336 - Stability 6 - Problem 2 - Solution2.TSC